IS3XCS9310

Preliminary

MCU with TK/APS, LED Driver

GENERAL DESCRIPTION

IS3XCS9310 integrates a 32-bit MCU with Touch Key Controller and LED Driver for control applications and LED lighting control.

The MCU is a 32-bit RISC-V (EMC) CPU that runs up to 32MHz and includes 256KB e-Flash and 32KB SRAM (16KB data SRAM and 16KB DMA SRAM) for processing touch key and Active Proximity Sensing (APS) signals as well as LED control.

The Touch Key controller supports both self-capacitance and (mutual-capacitance) modes as well as proximity sensing. For self-capacitance, up to 16 keys are supported. Each of these keys can configured for shielded outputs for water-resistance. (Mutual sensing is also supported allowing for key matrix scanning. Mutual sense can be configured as Proximity sense.)

The LED controller and driver supports up to 8 x 12 matrix LED consisting of 8 PMOS switches with scanning logic and 12 PWM controlled current sinks.

APPLICATIONS

- LED control and lighting control
- Industrial HMI control for White Goods and Appliance

FEATURES

CPU

- RISC-V EMC core up to 32MHz with wait state insertion
- C-JTAG debug and ISP
- CS/CRC Accelerator

Memory

- 16KB Data SRAM
- 16KB DMA SRAM
- DMA Controller for peripherals
- 256KB Flash Memory with four 1KB IFB
  - Data Flash emulation
  - Zone protection and Security key
  - 100K cycles endurance @ 85°C
  - 20 years retention @ 85°C

Clock Sources

- IOSC – 16MHz/32MHz /w spread spectrum
  - +/- 1% (0°C to 50°C)
  - +/- 1.5% (-40°C to 85°C)
  - +/- 2.0% (-40°C to 125°C)
- SOSC – 128KHz/256KHz +/- 30%
- POSC – 16MHz/32MHz /w spread spectrum LED Driver

Timers

- Watchdog Timers
  - 16-bit Windowed WDT1 (SYSCLK)
  - 16-bit Independent WDT2 (SOSC)
- 16-bit T0/T1 and 24-bit T2 Timers

Host Interface

- I²C Master
- I²C Slave
- EUART1 based on DMA for heavy data transfer
- EUART2 with LIN 2.0/2.2 Extension
- SPI Master/Slave

Digital Peripherals

- 16-bit Timer/Comparator/Capture (TCC)
- Melody generator
- 3-ch 14-bit PWM generator

Analog Peripherals

- 12-bit SAR ADC, 4 CH inputs, 1.5V/5V full scale
- 10-bit DAC,2 CH output, 1.5V/5V full scale
- 8-bit current output DAC, be used as a DC/DC converter FB reference voltage control
- 3 CH analog comparator and 8-bit DAC

Touch Key Controller

- Up to 20-bit resolutions
- Self capacitance mode
  - Up to 16 Keys
  - Configurable shield output for water resistance
- Mutual capacitance mode (Optional)
  - 8 x 8 matrix
  - Active proximity sensing up to 8 channels

Melody Controller

- 14-bit precision tone generation
- Note, duration and pause control
- Wide octave support
- Pulse or amplifier output

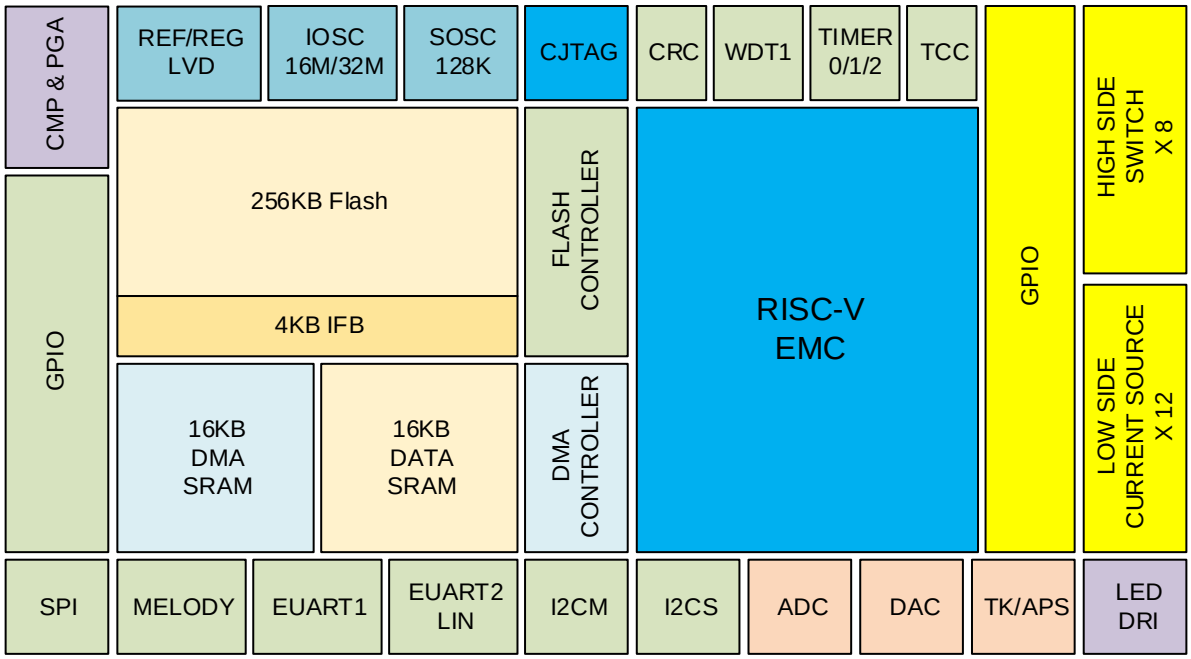
LED Control and Driver

- LED supply 3.0V – 5.5V, PVDD supply 3.0V – 5.5V
- Up to 8 x 12 LED matrix
- 12-bit PWM controlled current sink up to 80mA@-40~85°C
  - +/- 6% channel to channel
  - Left/Right alignment
  - PWM frequency > 20KHz
- Two display buffers (8 x 12 x 14 x 2 = 2688 bits)
- 8-bit global control of current sink
- Low RON (0.5Ω) high side switch
- Anti-ghost
- Spread spectrum clock
- Open-short detection/protection

Miscellaneous

- Up to 35 GPIO pins
- Power on reset (1.25V) and LVD/LVR (2.0V-5.5V)
- 3.0V to 5.5V single supply with programmable low voltage detect and reset.
- MCU low power modes
  - 20uA eep sleep mode
  - 50uA TK/CMP wakeup sleep mode
- Operating temperature
  - IS31CS9310: (TA)-40°C to 85°C (TJ)-40°C to 125°C
  - IS32CS9310: (TA)-40°C to 125°C (TJ)-40°C to 125°C
- ESD HBM±4KV, ESD CDM: ±500V
- Latch up ±200mA
- eLQFP-64 with exposed pad 7x7 mm RoHS & Halogen-Free compliant package
- TSCA compliance
- AEC-Q100 grade-1 qualification (IS32CS9310)

BLOCK DIAGRAM

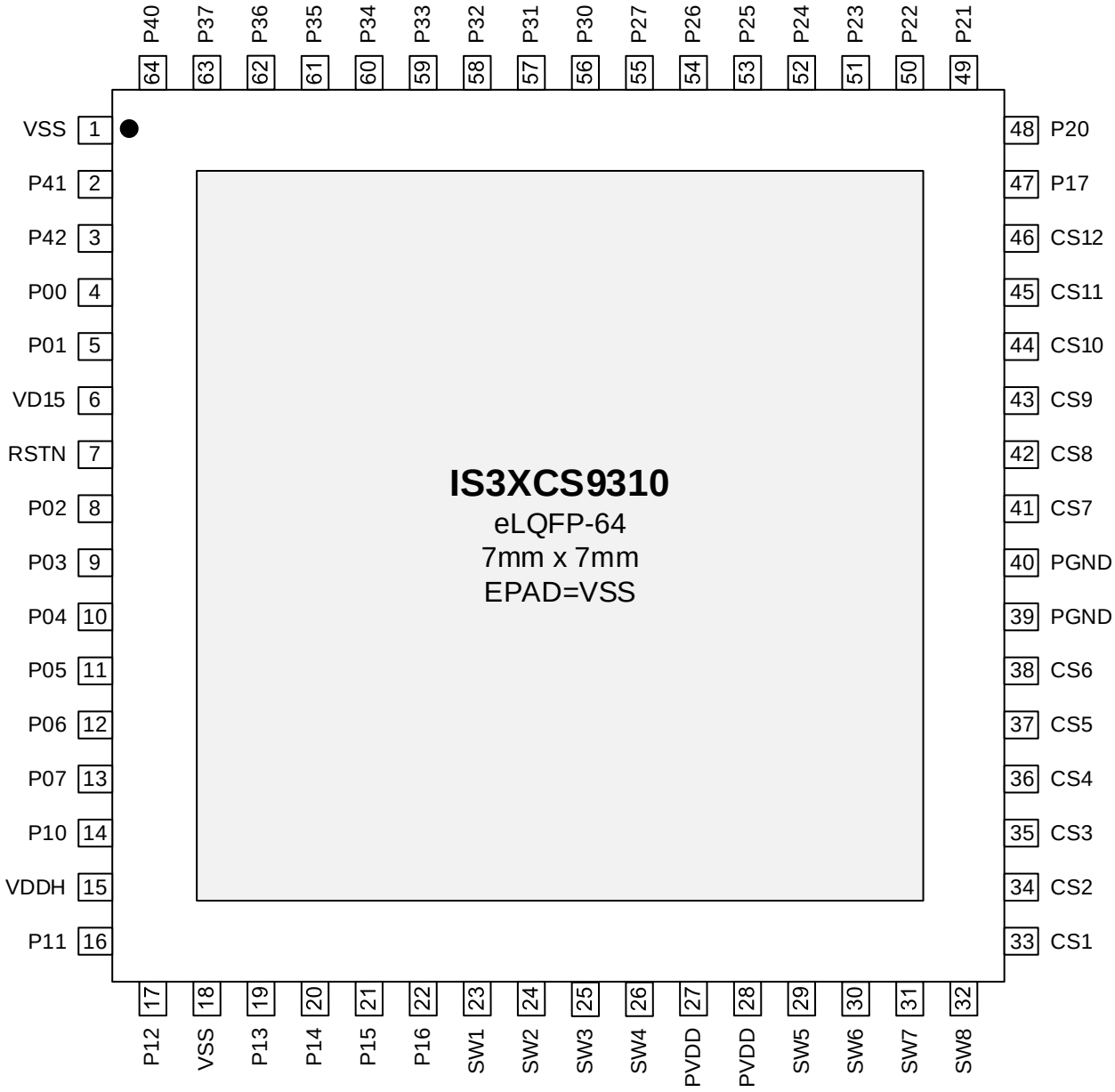


Note:

Each EUART RX pin must be always allocated as an interrupt to wakeup function from sleep. Missing the 1st packet detection event is fine.

ADC wakeup can be implemented via an analog comparator using a pre-set threshold trigger.

PIN CONNECTION



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1. PIN Descriptions

64 PIN	Name	Type	ANIO1	ANIO2	Pin Description
1	VSS	G			Ground Supply digital and IO
2	P41	IO/A	KEY	SHIELD	GPIO multi-function pin
3	P42	IO/A	KEY	SHIELD	GPIO multi-function pin
4	P00	IO/A	KEY	SHIELD	GPIO multi-function pin
5	P01	IO/A	KEY	SHIELD	GPIO multi-function pin
6	VD15	P			Internal 1.5V regulator supply, Connect to external 1.0uF/0.1uF decoupling capacitor.
7	RSTN	A			Reset input pin which includes an internal 5.5KΩ pull-up resistor. Connect to an external 0.1uF to 10uF capacitor to determine the reset time. RSTN is pulled low by POR and LVR events.
8	P02	IO/A	KEY	SHIELD	GPIO multi-function pin
9	P03	IO/A	KEY	SHIELD	GPIO multi-function pin
10	P04	IO/A	KEY	SHIELD	GPIO multi-function pin
11	P05	IO/A	KEY	SHIELD	GPIO multi-function pin
12	P06	IO/A	KEY	ADCIN	GPIO multi-function pin
13	P07	IO/A	KEY	SHIELD	GPIO multi-function pin
14	P10	IO/A	KEY	DACOUT	GPIO multi-function pin
15	VDDH	P			External Power supply 3V – 5.5V. Connect 1.0uF/0.1uF to VSS as close as to IC.
16	P11	IO/A	VFB	ADCIN	GPIO multi-function pin
17	P12	IO/A	VFB	SHIELD	GPIO multi-function pin
18	VSS	G			Ground Supply digital and IO
19	P13	IO/A	PGAINP	ADCIN	GPIO multi-function pin
20	P14	IO/A	PGAINN	ADCIN	GPIO multi-function pin
21	P15	IO/A	DACOUT	TEST	GPIO multi-function pin
22	P16	IO/A	DACOUT	ADCIN	GPIO multi-function pin
23	SW1	A			Power SW
24	SW2	A			Power SW
25	SW3	A			Power SW
26	SW4	A			Power SW
27	PVDD	P			5V Power supply for SW
28	PVDD	P			5V Power supply for SW
29	SW5	A			Power SW
30	SW6	A			Power SW
31	SW7	A			Power SW
32	SW8	A			Power SW
33	CS1	A			Current sink pin for LED matrix.
34	CS2	A	-		Current sink pin for LED matrix.
35	CS3	A			Current sink pin for LED matrix.
36	CS4	A			Current sink pin for LED matrix.

64 PIN	Name	Type	ANIO1	ANIO2	Pin Description
37	CS5	A			Current sink pin for LED matrix.
38	CS6	A			Current sink pin for LED matrix.
39	PGND	G			Ground Supply for led driver CS#
40	PGND	G			Ground Supply for led driver CS#
41	CS7	A			Current sink pin for LED matrix.
42	CS8	A			Current sink pin for LED matrix.
43	CS9	A			Current sink pin for LED matrix.
44	CS10	A			Current sink pin for LED matrix.
45	CS11	A			Current sink pin for LED matrix.
46	CS12	A			Current sink pin for LED matrix.
47	P17	IO/A	CMPINA	ADCIN	GPIO multi-function pin. This pin also serves as TMS for CJTAG & JTAG.
48	P20	IO/A	DACOUT	ADCIN	GPIO multi-function pin. This pin also serves as TCK for CJTAG & JTAG.
49	P21	IO/A	ADCREF	DACOUT	GPIO multi-function pin, This pin also serves as TDO for CJTAG & JTAG.
50	P22	IO/A	ADCREF	CMPTH	GPIO multi-function pin. This pin also serves as TDI for CJTAG & JTAG.
51	P23	IO/A	CMPINB	ADCIN	GPIO multi-function pin
52	P24	IO/A	CMPINC	ADCIN	GPIO multi-function pin
53	P25	IO/A	KEY	TEST	GPIO multi-function pin
54	P26	IO/A	KEY	SHIELD	GPIO multi-function pin
55	P27	IO/A	KEY	SHIELD	GPIO multi-function pin
56	P30	IO/A	KEY	SHIELD	Buzzer/Melody Output/GPIO multi-function pin
57	P31	IO/A	KEY	SHIELD	GPIO multi-function pin
58	P32	IO/A	KEY	SHIELD	GPIO multi-function pin
59	P33	IO/A	KEY	SHIELD	POW Output GPIO multi-function pin
60	P34	IO/A	KEY	SHIELD	GPIO multi-function pin
61	P35	IO/A	KEYR	KEYR	Both ANIO1 and ANIO2 are for external reference capacitance connection. GPIO multi-function pin
62	P36	IO/A	KEY	SHIELD	GPIO multi-function pin.
63	P37	IO/A	KEY	SHIELD	GPIO multi-function pin
64	P40	IO/A	KEY	SHIELD	GPIO multi-function pin

Table 1-1 Pin Description

2. Memory Map And Register Map

2.1 Memory Address Map

Module	Size	Start Address	End Address	Comment
e-Flash	256KB	0x0000_0000	0x0003_FFFF	Code
Data SRAM	16KB	0x2000_0000	0x2000_3FFF	Data SRAM
DMA SRAM	16KB	0x3000_0000	0x3000_3FFF	-
Peripheral Register	64KB	0x4000_0000	0x4000_FFFF	-
System Control	4KB	0x5000_0000	0x5000_0FFF	-
Timer	1KB	0x5000_1000	0x5000_1FFF	Timer
GPIO	4KB	0x5000_2000	0x5000_2FFF	-
Bus Control	4KB	0x5000_3000	0x5000_3FFF	-
SW Interrupt Control	1KB	0x5000_C000	0x5000_CFFF	-
Debug	1KB	0x5000_D000	0x5000_DFFF	-

Table 2-1 Memory Address Map

2.2 Peripheral Register Map

Module	Size	Base Address	Slave Port	Comment
DMA Controller	1KB	0x4000_0000	APBS0	-
e-Flash Controller	1KB	0x4000_1000	APBS1	-
SPF Controller	1KB	0x4000_2000	APBS2	-
SPV Controller	1KB	0x4000_3000	APBS3	-
Lumibus Controller	1KB	0x4000_4000	APBS4	-
CAN FD Controller	1KB	0x4000_5000	APBS5	-
I2CM/I2CS	1KB	0x4000_6000	APBS6	-
EUART1 EUART2/LIN	1KB	0x4000_7000	APBS7	-
SPI	1KB	0x4000_8000	APBS8	-
TCC1/TCC2/QED	1KB	0x4000_9000	APBS9	-
PWM	1KB	0x4000_A000	APBS10	-
MELODY	1KB	0x4000_B000	APBS11	-
TK Controller	1KB	0x4000_C000	APBS12	-
DAC/ACMP	1KB	0x4000_D000	APBS13	-
ADC	1KB	0x4000_E000	APBS14	-
Essential Analog	4KB	0x4000_F000	APBS15	-
LED	4KB	0x4001_0000	APBS16	-
DCFB	1KB	0x4001_1000	APBS17	Not implemented
Reserved	1KB	0x4001_2000	APBS18	Not implemented
Reserved	1KB	0x4001_3000	APBS19	Not implemented
Reserved	1KB	0x4001_4000	APBS20	Not implemented
Reserved	1KB	0x4001_5000	APBS21	Not implemented
Reserved	1KB	0x4001_6000	APBS22	Not implemented
Reserved	1KB	0x4001_7000	APBS23	Not implemented
Reserved	1KB	0x4001_8000	APBS24	Not implemented

Module	Size	Base Address	Slave Port	Comment
Reserved	1KB	0x4001_9000	APBS25	Not implemented
Reserved	1KB	0x4001_A000	APBS26	Not implemented
Reserved	1KB	0x4001_B000	APBS27	Not implemented
Reserved	1KB	0x4001_C000	APBS28	Not implemented
Reserved	1KB	0x4001_D000	APBS29	Not implemented
Reserved	1KB	0x4001_E000	APBS30	Not implemented
Reserved	1KB	0x4001_F000	APBS31	Not implemented

Table 2-2 Peripheral Register Map

3. CPU

3.1 Architecture

IS3XCS9310 includes a RISC-V CPU core with Embedded Multiplication/Division and Compressed Instruction (EMC) options. The E option features a CPU with 16 general purpose registers and only Machine mode although the user mode CSRs are preserved.

The RISC-V CPU has separate instruction and data memory accesses. For the IS3XCS9310, instructions are stored in an embedded Flash and accessed through a Flash Controller which features ECC capability. Similarly, data accesses to the data memory features ECC. ECC requires two clock cycles for write accesses.

Tightly coupled with the CPU core, are the Debug Module with JTAG debug port and C-JTAG converter to allow for 2-wire debugging interface. An interrupt controller is associated with the CPU which allows up to 16 external vectored interrupts as well as NMI and software interrupt. The interrupt is non-nested but software nesting control can be utilized. The overall block diagram of the CPU core is shown below.

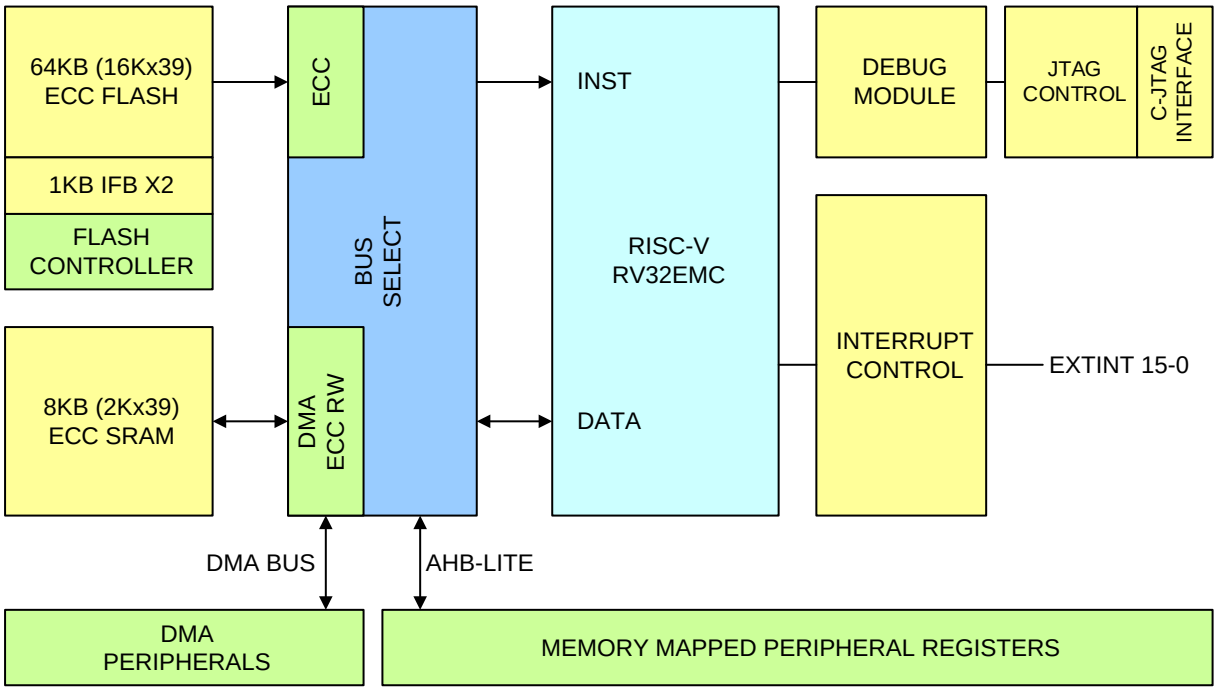


Figure 3-1 CPU Block Diagram

4. CSR (Control and Status Registers)

The RISC-V CPU core contains various CSR for control and status purposes. The following lists the CSR and corresponding address.

4.1 MSTATUS (0x300) Machine Status Register WARL

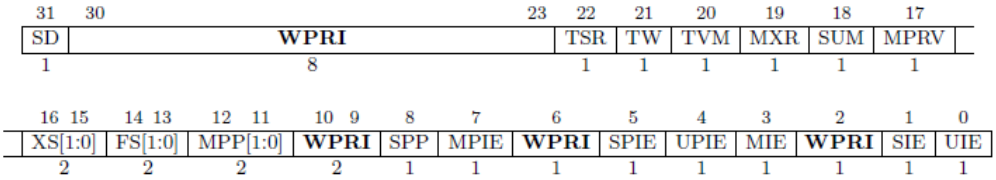


Figure 4-1 Bit Definition for MSTATUS

4.2 MISA (0x301) ISA and Extension Register WARL

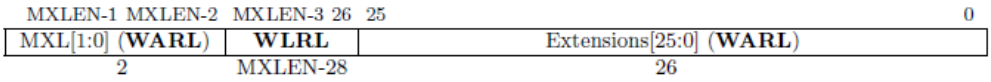


Figure 4-2 Bit Definition for MISA

The MXL (Machine XLEN) field encodes the native base integer ISA width. The MXL field are writable and supports multiple base ISA widths. The effective XLEN in M-mode, MXLEN, is given by the setting of MXL, or has a fixed value if MISA is zero. The MXL field is always set to the widest supported ISA variant at reset. The MISA CSR is MXLEN bits wide. If the value read from MISA is nonzero, field MXL of that value always denotes the current MXLEN. If a write to MISA causes MXLEN to change, the position of MXL moves to the most-significant two bits of MISA at the new width.

MXL[1-0]	Machine XLEN 00 Reserved 01 32-Bit 10 64-Bit 11128-Bit
EXTEN[25-0]	Extension Bits

Bit	Character	Description
0	A	Atomic extension
1	B	*Tentatively reserved for Bit-Manipulation extension*
2	C	Compressed extension
3	D	Double-precision floating-point extension
4	E	RV32E base ISA
5	F	Single-precision floating-point extension
6	G	Additional standard extensions present
7	H	Hypervisor extension
8	I	RV32I/64I/128I base ISA
9	J	*Tentatively reserved for Dynamically Translated Languages extension*
10	K	*Reserved*
11	L	*Tentatively reserved for Decimal Floating-Point extension*
12	M	Integer Multiply/Divide extension
13	N	User-level interrupts supported
14	O	*Reserved*
15	P	*Tentatively reserved for Packed-SIMD extension*
16	Q	Quad-precision floating-point extension
17	R	*Reserved*
18	S	Supervisor mode implemented
19	T	*Tentatively reserved for Transactional Memory extension*
20	U	User mode implemented
21	V	*Tentatively reserved for Vector extension*
22	W	*Reserved*
23	X	Non-standard extensions present
24	Y	*Reserved*
25	Z	*Reserved*

Figure 4-3 Standard Extensions for RISC-V

The following definitions and abbreviations are used to specify CSR fields.

4.3 Reserved Writes Preserve Values, Reads Ignore Values (WPRI)

Some read/write fields are reserved for future use. Software should ignore the values read from these fields and should preserve the values held in these fields when writing values to other fields of the same register. For future compatibility, implementations that do not furnish these fields must hardwired to a logic zero. These fields are labeled as WPRI in the register descriptions.

4.4 Write/Read Only Legal Values (WLRL)

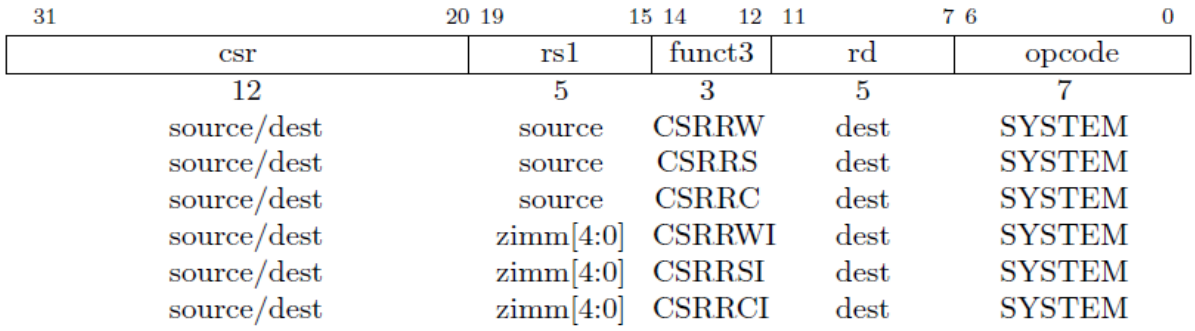
Some read/write CSR fields specify behavior for only a subset of possible bit encodings, while other bit encodings are reserved. Software should not write anything other than legal values to these fields and users should not assume a read will return a legal value unless the last write was a legal value, or the register has not been written since another operation (e.g., reset) set the register to a legal value. These fields are labeled WLRL in the register descriptions.

4.5 Write Any Values, Reads Legal Values (WARL)

Some read/write CSR fields are defined for a subset of bit encodings but allow any value to be written while guaranteeing a legal value when read. Assuming that writing the CSR has no issues, the range of supported values can be determined by attempting a write to a desired setting then read to determine if the value was retained. These fields are labeled WARL in the register description. Implementations will not raise an exception on writes of unsupported values to a WARL field. Implementations can return any legal value on the read of a WARL field when the last write was an illegal value, but the legal value returned should deterministically depend on the illegal written value and the value of the field prior to the write.

5. CSR Access Instructions

The CSRs are accessed through special CSR instruction such as CSRRW, CSRRS, CSRRC, CSRRWI, CSRRSI, and CSRRCI instructions. These special instructions allow CSR read/write operations and bit operations. The format of these instructions is as follows.



31 20	19 15	14 12	11 7	6 0
csr	rs1	funct3	rd	opcode
12	5	3	5	7
source/dest	source	CSRRW	dest	SYSTEM
source/dest	source	CSRRS	dest	SYSTEM
source/dest	source	CSRRC	dest	SYSTEM
source/dest	zimm[4:0]	CSRRWI	dest	SYSTEM
source/dest	zimm[4:0]	CSRRSI	dest	SYSTEM
source/dest	zimm[4:0]	CSRRCI	dest	SYSTEM

Figure 5-1 Instruction Decode for CSR Access

CSRRW (Atomic Read/Write CSR) instruction reads the CSR value and writes the value to the RD register. It then writes the CSR with the value from the RS1 register.

CSRRS (Atomic Read and Set Bit in CSR) instruction reads the value of the CSR and writes it to register RD. It then set the bits of CSR specified by RS1 value. Any bit with 1 value of RS1 will set the corresponding bits in CSR, provided the bits are writable. Other bits in CSR are not affected.

CSRRC (Atomic Read and Clear Bit in CSR) instruction reads the CSR value then writes the value to the RD register. It then set the CSR bits specified by the RS1 value. Any RS1 bit with a logic 1 clears the CSR corresponding bits, provided that the bits are writable. Other CSR bits are not affected. For CSRRS and CSRRC, if RS1 is x0, there is no effect for modification of CSR.

CSRRWI, CSRRSI, and CSRRCI instructions are similar to CSRRW, CSRRS, and CSRRC respectively, except that they update CSR using a 32-bit value obtained by zero-extending a 5-bit immediate value of zimm[4-0].

The assembler pseudo-instruction to read a CSR, CSRR rd, csr, is encoded as CSRRS rd, csr, x0.

The assembler pseudo-instruction to write a CSR, CSRW csr, rs1, is encoded as CSRRW x0, csr, rs1, while CSRWI csr, zimm, is encoded as CSRRWI x0, csr, zimm.

6. Exception and Interrupt

The interrupt controller of RISC-V EMC is a non-nested controller. When an interrupt occurs, the global interrupt enable is disabled by the hardware. Nested interrupt behavior can be software emulated.

INT# EX#	EX Code	Mask	Name	Description
INT14	30	Y	WDT/ECC	Watchdog/ECC error/APB Fault
INT13	29	Y	LVD	Low Voltage Detect
INT12	28	Y	DMA	DMA Move/DMA CRC
INT11	27	Y	TCC/PWM	TCC/PWM
INT10	26	Y	T012	Timer 0/1/2
INT9	25	Y	GPIO	GPIO interrupt
INT8	24	Y	ACMP	ACMP
INT7	23	Y	EUARTDMA	EUART DMA TX/RX
INT6	22	Y	DMASPI	DMA SPI Controller
INT5	21	Y	ADC	ADC
INT4	20	Y	EUART2	EUART2/LIN
INT3	19	Y	EUART1	EUART1
INT2	18	Y	I^2C	I2CM/I2CS
INT1	17	Y	TKC	TKC
INT0	16	Y	MLDY	Melody
INTEXT	11	Y	MEXT	Machine external interrupt
INTTM	7	Y	MTI	Machine timer interrupt
INTSW	3	Y	MSI	Machine software interrupt
EX0	0	N	IAMF	Instruction addresses misaligned
EX1	1	N	IAAF	Instruction access fault
EX2	2	N	ILGI	Illegal instruction
EX3	3	N	BKP	Breakpoint
EX5	5	N	LAF	Load access fault
EX7	7	N	SAF	Store/AMO access fault
EX8	8	N	ECU	Environment call from U-mode
EX11	11	N	ECM	Environment call from M-mode

Table 6-1 Interrupt list

Interrupt or exception is identified by CSR mcause[31] where mcause[30-0] identifies INT# or EX#.

How does the program counter (PC) react to exceptions or interrupts depend on the MODE setting in mtvec. If MODE is 0, then all exceptions and interrupts causes the PC to jump to BASE. If MODE is 1, exceptions still cause the PC to jump to BASE, but interrupts causes the PC to jump to BASE + 4*EXCODE.

7. System Control

7.1 Clock Control

CKSEL (0x5000_0000) System Clock Selection Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	SLPMODE		-	-	-	CKSEL[2-0]		
WR	SLPMODE		-	-	-	CKSEL[2-0]		

SLPMODE[7-6] SLEEP MODE Selection
00 Light Sleep Mode, internal regulator (1.5V) and IOSC are still enabled in sleep mode. This allows fast recovery time from sleep mode to normal mode.
01 Standby Mode, internal regulator (1.5V) is enabled and IOSC are disabled.
10 Deep Sleep Mode, internal regulator (1.5V) and IOSC are disabled in sleep mode (or deep sleep mode) to achieve minimum power consumption. When exiting deep sleep mode, delay time (defined by REGRDY) is inserted for turning on the regulator and IOSC for stable transition to normal mode.
11 = reserved

CKSEL[2-0] SYSCLK Selection
000 = IOSC
001 = SOSC
010 = POSC
011 = External Clock
1XX = IOSC

WTST (0x5000_0004) E-Flash Wait State Controlled Register R/W (0x17)

	7	6	5	4	3	2	1	0
RD	-	-	-	IBUSTM	-	WTST[2-0]		
WR	-	-	-	IBUSTM	-	WTST[2-0]		

IBUSTM Instruction Bus Timing
IBUSTM=0 uses address latch for e-Flash instruction access with no delay on address enable.
IBUSTM=1 uses add ½ SYSCLK delay to address enable signal for e-Flash instruction access.
This is default.
When WTST[2-0]=0x7, IBUSTM can be modified.

WTST[2-0] Main Flash Access Time
If IBUSTM=0, e-Flash access is (WTST+1) SYSCLK.
If IBUSTM=1, e-Flash access is (WTST+2) SYSCLK.
When WTST=0/IBUSTM=0, the effective instruction fetch from e-Flash takes two cycles. Therefore, for maximum performance, WTST=0 allows up to 32MHz SYSCLK assuming 40ns e-Flash access time.

7.2 Reset

There are several software and hardware resets. Software resets include software command reset, WDT reset and reset issued through the debug port. Hardware resets include power-on reset (low voltage detect on VD15), LVD reset (low voltage detect on VDDH), SYSCLK clock monitor reset, and external RSTN reset. Power on reset and LVD reset as well as clock monitor reset are routed to RSTN pin to allow for external RC extension. Both hardware and software reset are combined to generate e-Flash reset and system reset including CPU resets restore all registers to default values.

Power-on reset and extended RSTN reset (RSTN=0 longer than 250msec) is specially treated. This combined condition generates Special Reset (SP RST). Some of the registers are restored only by the SP reset. These include RSTCMD, BSTCMD, LVDCFG, and RTCCFGA, JTAGCFG etc. and are described in the register description. In addition, the debug port logic, and its associated state and registers are reset only by the SP reset and not by the SYSTEM reset. This behavior is shown in the following block diagram.

The last thing to note is that the total delay in system startup at power-on is approximately 3ms.

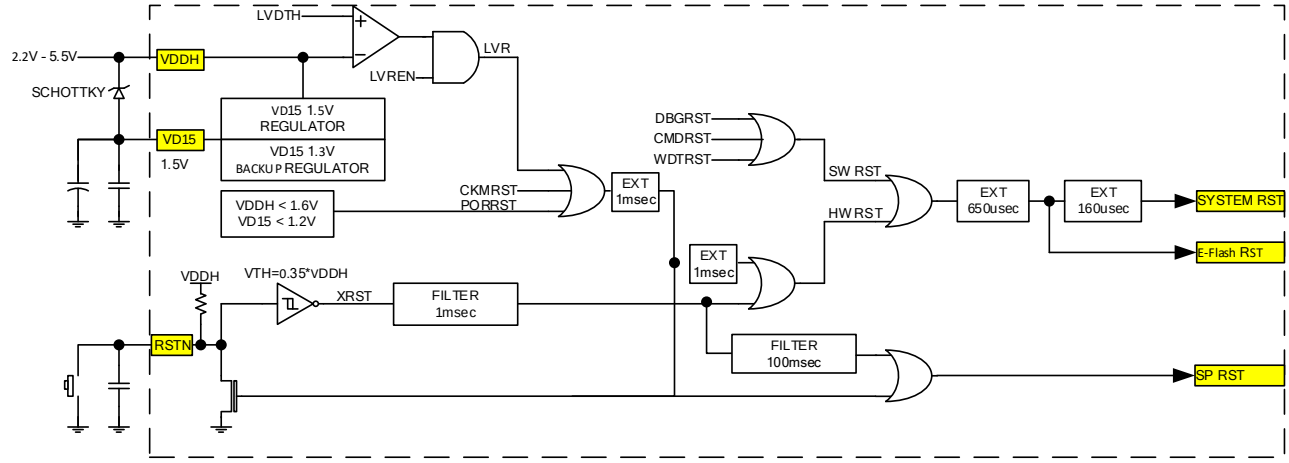


Figure 7-1 Reset Network

RSTCMD (0X5000_0008) Reset Command Register R/W (0x80)

	7	6	5	4	3	2	1	0
RD	RSTCKM	RSTNFLTEN	-	LVRF	CKMRF	WDT2RF	WDT1RF	CMDRF
WR	RSTCKM	RSTNFLTEN	CLRF	-	RSTCMD[3-0]			

RSTCKM — Reset Enable for Clock Monitor Fault
RENCKM=1 enables reset after clock fault detection. RSTCKM is cleared to 0 after any reset. Default RSTCKM is 0.

RSTNFLTEN — RSTN Analog Filter Enable
RSTNFLTEN = 1 enables a noise filter on the RSTN circuits. The filter is set at around 4usec. The signal is further filtered by digital means for less than 4msec as shown in the block diagram by the assertion filter.

CLRF — Clear Reset Flag
Writing 1 to CLRF will clear CKMRF, WDT2RF, WDT1RFand CMDRF. It is self-cleared.

LVRF — Low Voltage Detect Reset Flag
LVRF is set to 1 by hardware if a reset condition caused by LVD has occurred.

CKMRF — Clock Monitor Fault Reset Flag
CKMRF is set to 1 by hardware when a clock fault reset has occurred. CKMRF is not cleared by reset except power-on reset.

WDT2RF — WDT2 Reset Flag
WDT2RF is set to 1 by hardware when WT2 caused a reset.

WDT1RF — WDT1 Reset Flag
WDT1RF is set to 1 by hardware when WT1 caused a reset.

CMDRF — RST Command Reset Flag
CMDRF is set to 1 by hardware when reset is caused by issuing software reset command.

RSTCMD[3-0] — Software Reset Command
Writing RSTCMD[3-0] with consecutive 4b'0101, 4b'1010 sequences will cause a software reset. Any other value will clear the sequence state. These bits are write-only and self-cleared.

Please note all flags in this register are cleared by either CLRF or Power-On-Reset (or it's equivalent).

7.3 Built-in Self Test

BSTCMD (0x5000_000C) SRAM Built-In and Logic Self-Test R/W (0x00)

	7	6	5	4	3	2	1	0
RD	MODE[3-0]				BST	FAIL2	FAIL1	FINISH
WR	MODE[3-0]				BSTCMD[3-0]			

MODE[3-0] — BIST Mode Selection
0000 – Normal Mode

0001 – Reserved
0010 –SRAM MBIST
0011 – Reserved
0100 – Register LBIST
0101 – Reserved
0110 – Reserved
0111 – Reserved
1000 – Normal Mode
1001 – SRAM MBIST and monitor on pins
1010 – Reserved
1011 – Reserved
1100 – Register LBIST and monitor on pins
1101 – Reserved
1110 – Reserved
1111 – Reserved
Please note MODE[3-0] is cleared only by POR and RSTN. Software can read this setting along with the Pass/Fail status to determine which BIST was performed and its result even after a software reset.
If a “Reserved” mode command is issued, neither FINISH or FAIL will be set to 1. It is recommended that software should check BST=0 or FINISH=1 to determine if a command is finished or not.

BST — BIST Status
BST is set to 1 by hardware when BIST in ongoing.

FAIL2 — DMAMBIST Test Fail Flag
FAIL2 is set to 1 by hardware when DMAMBIST error has occurred. FAIL2 is cleared to 0 by hardware when a new BIST command is issued.

FAIL1 — MBIST Test Fail Flag
FAIL1 is set to 1 by hardware when MBIST error has occurred. FAIL1 is cleared to 0 by hardware when a new BIST command is issued.

FINISH — BIST Completion Flag
FINISH is set to 1 by hardware when BIST controller finishes the test. FINISH is cleared to 0 by hardware when a new BIST command is issued.

BSTCMD[3-0] — Memory BIST Command
Writing BSTCMD[3-0] with value 4b’0101 causes the BIST controller to perform BIST. Writing BSTCMD[3-0] with value 4b’1010 causes the BIST controller to perform BIST, and after BIST is completed, it automatically generates a software reset.
Writing BSTCMD[3-0] with value 4b’0000 causes FAIL and FINISH bits to be cleared to 0.
Any other value will either have no effect or abort any ongoing BIST.

Please note after the BSTCMD is issued, CPU is paused until BIST is completed. And any BIST operations will result the state of CPU in undefined states, and the content of the SRAM undefined. Therefore, it is highly recommended that a software reset or initiation should be performed after any BIST operation. Please also note MODE[3-0], FINISH, FAIL bits are not cleared by software resets.

7.4 Watchdog Timers

WDT1 is a 16-bit windowed watchdog timer clocked by SYSCLK. Please note WDT1 is stopped during sleep mode as SYSCLK is stopped. And WDT1 default after powered on is disabled.

WDT1CF (0x5000_0010) WDT1 Configure Registers R/W (0x8E)

	7	6	5	4	3	2	1	0
RD	-	WDT1REN	-	WDT1IEN	WDT1CS[2-0]			WDT1IF
WR	WDT1CLR	WDT1REN	-	WDT1IEN	WDT1CS[2-0]			WDT1IF

WDT1CLR — WDT1 Counter Clear
Writing “1” to WDT1CLR clears the WDT1 count to 0. It is self-cleared by hardware.

WDT1REN — WDT1 Reset Enable
WDT1REN=1 configures WDT1 to perform software reset.

WDT1IEN — WDT1 Interrupt Enable

WDT1IEN=1 enables WDT1 interrupt.

WDT1CS[2-0] WDT1 Clock Scaling

WDT1CS[2-0]	SYSCLK DIVIDER
000	1
001	2
010	4
011	8
100	16
101	32
110	64
111	128

WDT1IF WDT1 Interrupt Flag

WDT1IF is set to “1” after a WDT1 interrupt. This must be cleared by software by writing “1”.

If both WDT1IF and WDT1CLR bits need to be cleared simultaneously, it must be done with two separate instructions.

WDT1CNT (0x5000_0014) WDT1 Current Count RO (0x00000000)

	31-16	15-0
RD	-	WDT1CNT[15-0]
WR	-	-

WDT1TOV (0x5000_0018) WDT1 Time Out Value Register RW (0x0000FFFF)

	31-16	15-0
RD	-	WDT1TOV[15-0]
WR	-	WDT1TOV[15-0]

WDT1TMN (0x5000_001C) WDT1 Minimum Value Register RW (0x0000FFFF)

	31-16	15-0
RD	-	WDT1TMN[15-0]
WR	-	WDT1TMN[15-0]

WDT2 is a 16-bit independent watchdog timer clocked by 32KHz from the non-stop SOSC. Please note WDT2 is always enabled and cannot be turned off in non-debug modes.

WDT2CF (0x5000_0020) WDT2 Configure Registers R/W (0x50)

	7	6	5	4	3	2	1	0
RD	-	DBGDIS[2-0]			WDT2CS[2-0]			-
WR	WDT2CLR	DBGDIS[2-0]			WDT2CS[2-0]			-

WDT2CLR WDT2 Counter Clear

Writing “1” to WDT2CLR clears the WDT2 count to 0. It is self-cleared by hardware.

DBGDIS[2-0] Debug Mode Disable Enable

If DBGDIS[2-0] = 101, WDT2 counting is stopped in JTAG or CJTAG debug mode.

If DBGDIS[2-0] is not “101”, WDT2 function is not affected in debug mode.

Please note DBGDIS[2-0] defaults to 101. The software should take care of WDT2 counting when entering and exiting the debug mode. Also DBGDIS[2-0] does not affect WDT2 behavior in the non-debug modes, in other words, WDT2 is always enabled and continue counting during non-debug modes.

WDT2CS[2-0] WDT2 Clock Scaling

WDT2CS[2-0]	SOSC DIVIDER	Default (Max) Duration
000	1	2.1 second

WDT2CS[2-0]	SOSC DIVIDER	Default (Max) Duration
001	4	8.4 second
010	16	34 second
011	64	131 second
100	256	524 second
101	1024	2097 second
110	4096	8398 second
111	16384	33554 second

WDT2CNT (0x5000_0024) WDT2 Current Count RO (0x00000000)

	31-16	15-0
RD	-	WDT2CNT[15-0]
WR	-	-

WDT2TOV (0x5000_0028) WDT2 Time Out Value Register RW (0x0000FFFF)

	31-16	15-0
RD	-	WDT2TOV[15-0]
WR	-	WDT2TOV[15-0]

7.5 Test Monitor

TSTMON (0x5000_0060) Test Flag Monitor R/W (0x00)

	7	6	5	4	3	2	1	0
RD	TSTMON[7-0]							
WR	TSTMON[7-0]							

TSTMON[7-0] Test Flag Monitor
TSTMON[7-0] stores temporary test status and is initialized by power-on reset only. This is used for internal test by manufacturer.

7.5.1 System Clock Fault

SYSCLK in normal running mode is monitored by SOSC (128KHz). If SYSCLK is not present in normal mode for four SOSC cycles, a hardware reset is triggered.

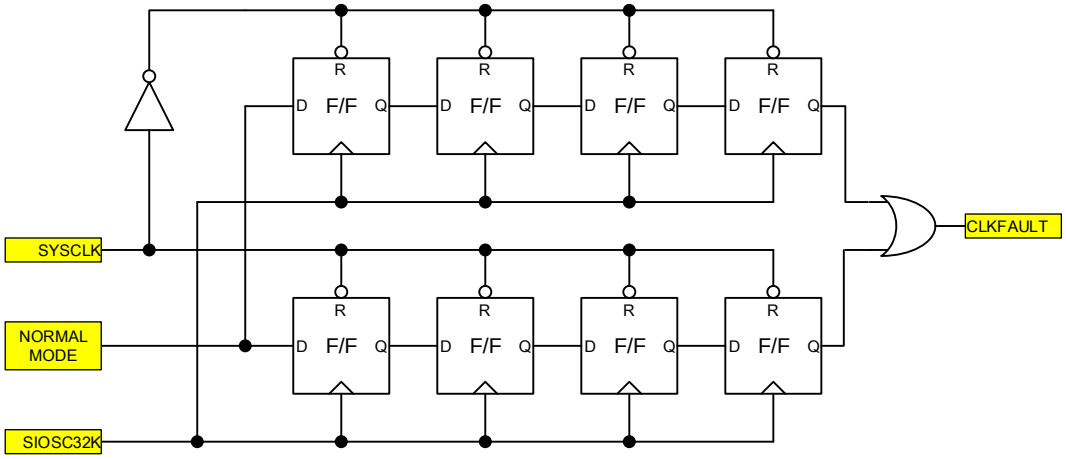


Figure 7-2 Clock Fault Monitor diagram

The clock monitoring is always on during normal mode. When a fault occurs, it generates a reset and the RSTCKM flag bit in RSTCMD register is set as a result

7.5.2 Peripheral Clock and Command Fault

There are up to 32 APB peripheral partitions as shown in the peripheral register map as shown in Section 2.6. Only portions are used in the IS3XCS9310. Each clock can be enabled or disabled to conserve power. If there are clock or bus command faults, the bus transaction may still be completed, however the transaction result is erroneous. In this case, a fault interrupt (NMI EX Code = 31) can be generated for software corrections.

APBCKEN (0x5000_3008) APB Clock Enable Register RW (0x0007FFFF)

	31-19	18-0
RD	-	APBCKEN[18-0]
WR	-	APBCKEN[18-0]

APBCKEN[18-0] APBS Peripheral Clock Enable
APBCKEN[i]=0 disables corresponding APB peripheral clock.
APBCKEN[i]=1 enables corresponding APB peripheral clock.
Individual APB peripheral can be clock disabled to save power.
Default all APB clock is turned on.

APBIEN (0x5000_3300) APB Fault Interrupt Enable Register RW（0x000000000）

	31-19	18-0
RD	-	APBIEN[18-0]
WR	-	APBIEN[18-0]

APBIEN[18-0] APB Fault Interrupt Enable
APBIEN[i] controls the APB fault interrupt enable for the corresponding APB partition. When APB command fault occurs, it generates an interrupt/exception (NMI EX Code = 31).
For example, APBIEN[10]=1 will enable APBS10 (PWM Controller) fault interrupt. APBIEN[10]=0 will turns off the interrupt.

APBINTF (0x5000_3304) APB Fault Interrupt Flag Register RW（0x000000000）

	31-19	18-0
RD	-	APBINTF[18-0]
WR	-	APBINTF[18-0]

APBINTF[18-0] APB Fault Interrupt Flag
APBINTF[i] is set to 1 when a corresponding APB partition has fault and its APBIEN is enabled. APBINTF[i] is cleared by writing “1”.
For example, if APBIEN[10]=1, and APBS10 has APB command or bus fault, APBINTF[10] is set to 1 by hardware. To clear APBINTF[10], write 1 into APBINTF[10].

8. ECC Controller

There are several memory macros including data SRAM, DMA SRAM, e-Flash on chip as well as external SPI flash. These memories have their own ECC checking due to different width, access path and speed. The handling of ECC errors can be different depending on the applications. For this reason, ECC checking logic can be configured to generate an interrupt when it detects an ECC error. The ECC interrupt flags are grouped in ECCFLAG register, when the ECC interrupt occurs, software can check this register to determine which memory has ECC error and if it is correctable or un-correctable. And software can take appropriate actions.

ECCFLAGA (0x5000_0100) ECC FLAG Register A RO (0x00)

	7	6	5	4	3	2	1	0
RD	FERRF1	FERRF0	SERRF1	SERRF0	MERRF1	MERRF0	DERRF1	DERRF0
WR	-	-	-	-	-	-	-	-

FERRF[1-0] e-Flash ECC Error Flags
SERRF[1-0] SPI Flash ECC Error Flags
MERRF[1-0] DMA SRAM ECC Error Flags
DERRF[1-0] Data SRAM ECC Error Flags

ECCBYTE (0x5000_0104) ECC Byte (8-bit) Calculation Register RW (0x00000000)

	31-24	23-16	15-8	7-0
RD	ECCCODE[31-24]	ECCCODE[23-16]	ECCCODE[15-8]	ECCCODE[7-0]
WR	ECCBYTE[31-24]	ECCBYTE[23-16]	ECCBYTE[15-8]	ECCBYTE[7-0]

Writing into ECCBYTE will yield the ECC data when read out. The ECC data is nibble based. In other words, the ECC is based on 4-bit data with ECC code of 4-bit being 1-bit parity plus length of 3-bit Hamming code. This operation takes about 6-cycles to complete with hardware ready control.

ECCWORDL (0x5000_0108) ECC Word (32-bit) Calculation Register L RW (0x00000000)

	31-24	23-16	15-8	7-0
RD	-	-	-	ECCCODE[7-0]
WR	ECCWORD[31-24]	ECCWORD[23-16]	ECCWORD[15-8]	ECCWORD[7-0]

ECCWORDH (0x5000_010C) ECC Word (32-bit) Calculation Register H RW (0x00000000)

	31-24	23-16	15-8	7-0
RD	-	-	-	-
WR	ECCWORD[63-56]	ECCWORD[55-48]	ECCWORD[47-40]	ECCWORD[39-32]

Writing into ECCWORD will yield the ECC code data when read out. The ECCCODE[7] is always parity bit plus variable length of Hamming code bits. The result format is summarized in the following table where P is parity, 0 is dummy bits and H is hamming code.

Data Width	ECCCODE[7-0]	Descriptions
11-8	P + 000 + H[3-0]	One-bit parity, three-bit zero and four-bit Hamming code
26-12	P + 00 + H[4-0]	One-bit parity, two-bit zero and five-bit Hamming code
57-27	P + 0 + H[5-0]	One-bit parity, one-bit zero and six-bit Hamming code
64-58	P + H[6-0]	One-bit parity and seven-bit Hamming code

ECCSRAMX (0x5000_0110) SRAM ECC Fault Injection Register X RW (0x00000000)

	31-24	23-16	15-8	7-0
RD	ECCSRAMX[31-24]	ECCSRAMX[23-16]	ECCSRAMX[15-8]	ECCSRAMX[7-0]
WR	ECCSRAMX[31-24]	ECCSRAMX[23-16]	ECCSRAMX[15-8]	ECCSRAMX[7-0]

ECCSRAMX[31-0] SRAM ECC Fault Injection
Each bit inverses the polarity of SRAM output to ECC decoder logic. By setting this register, it can inject fault to ECC decoder logic for testing purpose. ECC encoder is not of concern because encoder can be verified by decoder.

ECCSRAMY (0x5000_0114) SRAM ECC Fault Injection Register Y RW (0x00000000)

	31-24	23-16	15-7	6-0
RD	-	-	-	ECCSRAMY[6-0]
WR				ECCSRAMY[6-0]

ECCSRAMY[6-0] SRAM ECC Fault Injection
Each bit inverses the polarity of SRAM output for ECC code to ECC decoder logic. By setting this register, it can inject fault to ECC decoder logic for testing purpose. ECC encoder is not of concern because encoder can be verified by decoder.

ECCSRAMS (0x5000_0118) SRAM ECC Fault Injection Select Register RW (0x00000000)

	7	6	5	4	3	2	1	0
RD	-	-	-	-	-	-	ECCSRAMS[1-0]	
WR	-	-	-	-	-	-	ECCSRAMS[1-0]	

ECCSRAMS[1-0] SRAM ECC Fault Injection Select
00=disable
01=data SRAM
10=DMA SRAM
11=disable

8.1 Software Interrupt

Software can trigger a local machine interrupt vectored as Machine Software Interrupt. Software interrupts are typically used for system calls.

SINTC (0x5000_C000) Software Interrupt Configure Registers R/W (0x00)

	7	6	5	4	3	2	1	0
RD	-	-	-	-	-	-	-	SINT
WR	-	-	-	-	-	-	-	SINT

SINT Software Interrupt
Writing SINT=1 triggers software interrupt. SINT must be cleared by software by writing 0.

9. Timer T0/T1/T2

There are three general-purpose counters. T0 and T1 are 16-bit with clock source of SYSCLK. T2 is 24-bit with selectable clock source of SYSCLK or SOSC. T2 can also be used as wake-up purpose.

TMR0CFG (0x5000_1000) Timer 0 Configure Registers R/W (0x00)

	7	6	5	4	3	2	1	0
RD	T0IF	-	-	TM0	TR0	-	-	T0IEN
WR	CLRT0IF	-	-	TM0	TR0	-	-	T0IEN

T0IF	Timer 0 Overflow Interrupt Flag bit. T0IF is set by hardware when overflow condition occurs. This bit needs to be cleared by writing 1.
CLRT0IF	Clear Timer0 Interrupt Flag.
TM0	Timer 0 Mode Control bit. TM0=1 set timer 0 as auto reload, and TM0=0 set timer 0 as free-run.
TR0	Timer 0 Run Control bit. Set to enable Timer0, and clear to stop Timer0.
T0IEN	Timer 0 Interrupt Enable bit. T0IEN=0 disable the Timer 0 overflow interrupt T0IEN=1 enable the Timer 0 overflow interrupt

TMR0CNT (0x5000_1004) Timer 0 Counter R/W (0x00000000)

	31-24	23-16	15-8	7-0
RD	-	-	TMR0CNT[15-8]	TMR0CNT[7-0]
WR	-	-	TMR0VAL[15-8]	TMR0VAL[7-0]

TMR0CNT functions differently when it has been read or written. When written, the reload value register is written, and is in free-run mode, the counter value is written immediately. When it has been read, the return value is always the present counter value. There is no snapshot buffer in the read operation, so the software is recommended to read with word or half-word operations.

TMR1CFG (0x5000_1008) Timer 1 Configure Registers R/W (0x00)

	7	6	5	4	3	2	1	0
RD	T1IF	-	-	TM1	TR1	-	-	T1IEN
WR	CLRT1IF	-	-	TM1	TR1	-	-	T1IEN

T1IF	Timer 1 Overflow Interrupt Flag bit. T1IF is set by hardware when overflow condition occurs. This bit needs to be cleared by writing 1.
CLRT1IF	Clear Timer1 Interrupt Flag.
TM1	Timer 1 Mode Control bit. TM1=1 set timer 1 as auto reload, and TM1=0 set timer 1 as free-run.
TR1	Timer 1 Run Control bit. Set to enable Timer1, and clear to stop Timer1.
T1IEN	Timer 1 Interrupt Enable bit. T1IEN=0 disable the Timer 1 overflow interrupt T1IEN=1 enable the Timer 1 overflow interrupt

TMR1CNT (0x5000_100C) Timer 1 Counter R/W (0x00000000)

	31-24	23-16	15-8	7-0
RD	-	-	TMR1CNT[15-8]	TMR1CNT[7-0]
WR	-	-	TMR1VAL[15-8]	TMR1VAL[7-0]

TMR1CNT functions differently when it has been read or written. When written the reload value register is written, and in free-run mode, the counter value is written immediately. When it has been read, the return value is always the present counter value. There is no snapshot buffer in the read operation, so software is recommended to read with word or half-word operation.

TMR2CFG (0x5000_1020) Timer 2 Configure Registers R/W (0x00)

	7	6	5	4	3	2	1	0
RD	T2IF	-	T2SEL	TM2	TR2	-	-	T2IEN
WR	CLRT2IF	-	T2SEL	TM2	TR2	-	-	T2IEN

T2IF	Timer2 Overflow Interrupt Flag bit. T2IF is set by hardware when overflow condition occurs. This bit needs to be cleared by writing 1.
CLRT2IF	Clear Timer2 Interrupt Flag.
T2SEL	Timer 2 Clock Selection bits. 0: SYSCLK 1: SOSC
TM2	Timer 2 Mode Control bit. TM2=1 set timer 2 as auto reload, and TM2=0 set timer 2 as free-running mode.
TR2	Timer2 Run Control bit. Set to enable Timer2, and clear to stop Timer2.
T2IEN	Timer 2 Interrupt Enable bit. T2IEN=0 disable the Timer 2 overflow interrupt T2IEN=1 enable the Timer 2 overflow interrupt

TMR2CNT (0x5000_1024) Timer 2 Counter R/W (0x00000000)

	31-24	23-16	15-8	7-0
RD	-	TMR2CNT[23-16]	TMR2CNT[15-8]	TMR2CNT[7-0]
WR	-	TMR2VAL[23-16]	TMR2VAL [15-8]	TMR2VAL [7-0]

TMR2CNT functions differently when it has been read or written. When written the reload value register is written, and in free-run mode, the counter value is written (word mode) immediately. When it has been read, the return value is always the present counter value. There is no snapshot buffer in the read operation, so software is recommended to read with word-mode.

10. SRAM and DMA Controller

The SRAM is implemented in 4096 x 39 with 7-bits for ECC. The CPU can access the SRAM with 8/16/32 bit width. When writing into SRAM, a read-modify-write operation is inserted for maintaining ECC consistency. The DMA controller is responsible for controlling the SRAM from peripherals. The DMA paths only allow for 32-bit access. DMA controller also integrated two memory related functions, memory move and CRC/CS accelerators.

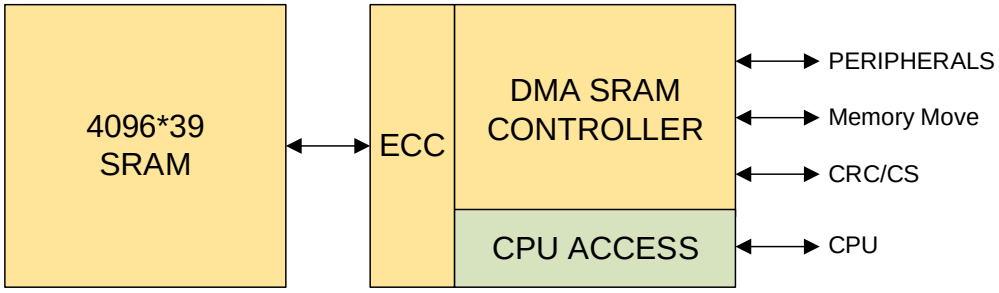


Figure 10-1 ECC for SRAM and DMA SRAM

The access is based on 16-slot round-robin arbitration. The even slots are always assigned to CPU access, and the odd slots are allocated for peripheral accesses. Each odd slot can be configured to be assigned to CPU or one of the DMA peripherals such as, CRC accelerator, SPI and LMC etc. This guarantees that the CPU has at least 50% of memory access. Note that it is not recommended to assign two adjacent odd slots to the same peripheral, as the second slot will not be serviced and be wasted.

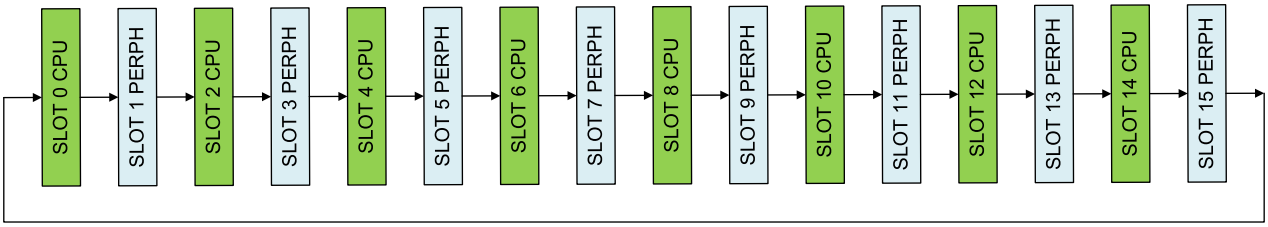


Figure 10-2 DMA Slot Assignment

The ECC is performed when the data is written as well as reading. When reading, if a 1-bit correctable error is detected, then output data is automatically corrected without modifying stored data. If an uncorrectable error is detected, the stored data (possibly corrupted) is still outputted. ECC error (both 1-bit and 2-bit) triggers ECC interrupt. It is necessary the data should be initialized before usage to prevent unintended ECC error.

DATARAMECC (0x4000_0000) DATA Memory ECC Error Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	-	-	-	-	IEN1	IEN0	ERRF1	ERRF0
WR	-	-	-	-	IEN1	IEN0	ERRF1	ERRF0

IEN1 — Interrupt Enable for Un-correctable Error
If IEN1=1, an un-correctable error will generate an ECC interrupt.

IEN0 — Interrupt Enable for Correctable Error
If IEN0=1, a correctable error will generate an ECC interrupt.

ERRF1 — Un-correctable Error Flag
ERRF1 is set to 1 when un-correctable error occurs for IEN1=1. This error flag is also mapped to ECCFLAG register as read only. This bit needs to be cleared by software by writing 1.

ERRF0 — Correctable Error Flag
ERRF0 is set to 1 when correctable error occurs for IEN0=1. This error flag is also mapped to ECCFLAG register as read only. This bit needs to be cleared by software by writing 1.

DATAECCA (0x4000_0004) DATA Memory ECC Most Address Register R/W (0x00000000)

	31-24	23-16	15-8	7-0
RD	-	-	ECCADR[15-0]	
WR	-	-	-	

ECCADR[15-0] ECC Error Address
The DMA SRAM address where ECC error occurs. This is read only.
This is in byte address format. Since the size of the SRAM is 2K x 39, only ECCADR[12-2] are meaningful, ECCADR[1-0] and ECCADR[15-13] should be ignored.

10.1 Slot Assignment

DMACFGA (0x4000_0100) DMA Configuration Register A R/W (0x00)

	7	6	5	4	3	2	1	0
RD	SLOT3[3-0]				SLOT1[3-0]			
WR	SLOT3[3-0]				SLOT1[3-0]			

SLOT3[3-0] Slot 3 Assignment
Same definition as SLOT1[3-0]
SLOT1[3-0] Slot 1 Assignment
0000 = CPU
0001 = CRC/CS
0010 = SPI RCV
0011 = SPI XMT
0100 = EUART
0101 = CANFD
0110 = Memory Move
Other = Reserved

DMACFGB (0x4000_0104) DMA Configuration Register B R/W (0x00)

	7	6	5	4	3	2	1	0
RD	SLOT7[3-0]				SLOT5[3-0]			
WR	SLOT7[3-0]				SLOT5[3-0]			

SLOT7[3-0] Slot 7 Assignment
Same definition as SLOT1[3-0]
SLOT5[3-0] Slot 5 Assignment
Same definition as SLOT1[3-0]

DMACFGC (0x4000_0108) DMA Configuration Register C R/W (0x00)

	7	6	5	4	3	2	1	0
RD	SLOT11[3-0]				SLOT9[3-0]			
WR	SLOT11[3-0]				SLOT9[3-0]			

SLOT11[3-0] Slot 11 Assignment
Same definition as SLOT1[3-0]
SLOT9[3-0] Slot 9 Assignment
Same definition as SLOT1[3-0]

DMACFGD (0x4000_010C) DMA Configuration Register D R/W (0x00)

	7	6	5	4	3	2	1	0
RD	SLOT15[3-0]				SLOT13[3-0]			
WR	SLOT15[3-0]				SLOT13[3-0]			

SLOT15[3-0] Slot 15 Assignment
Same definition as SLOT1[3-0]
SLOT13[3-0] Slot 13 Assignment
Same definition as SLOT1[3-0]

DMAECC (0x4000_0110) DMA Memory ECC Error Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	-	-	-	-	IEN1	IEN0	ERRF1	ERRF0
WR	-	-	-	-	IEN1	IEN0	ERRF1	ERRF0

IEN1 Interrupt Enable for Un-correctable Error
If IEN1=1, an un-correctable error will generate an ECC interrupt.

IEN0 Interrupt Enable for Correctable Error
If IEN0=1, a correctable error will generate an ECC interrupt.

ERRF1 Un-correctable Error Flag
ERRF1 is set to 1 when un-correctable error occurs for IEN1=1. This error flag is also mapped to ECCFLAG register as read only. This bit needs to be cleared by software by writing 1.

ERRF0 Correctable Error Flag
ERRF0 is set to 1 when correctable error occurs for IEN0=1. This error flag is also mapped to ECCFLAG register as read only. This bit needs to be cleared by software by writing 1.

DMAECCA (0x4000_0120) DMA Memory ECC Address Register R/W (0x00000000)

	31-24	23-16	15-8	7-0
RD	-	-	ECCADR[15-0]	
WR	-	-	-	

ECCADR[15-0] ECC Error Address
The DMA SRAM address where ECC error occurs. This is read only.
This is in byte address format. Since the size of the SRAM is 2K x 39, only ECCADR[12-2] are meaningful, ECCADR[1-0] and ECCADR[15-13] should be ignored.

10.2 DMA SRAM Move

Within DMA controller, it has built-in memory move function. When enabled, it moves a portion of the memory contents to another locations. The move is in 32-bit alignment and up to 256 x 32.

DMAMOVC (0x4000_0200) DMA Memory MOVE Command Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	INTE	INTF	ASQREV	ENDREV	BYTREV	-	-	BUSY
WR	INTE	INTF	ADDSEQ	ENDREV	BYTREV	-	-	START

INTE Interrupt Enable

INTF Completion Interrupt Flag
This bit is set to 1 by hardware after completion of the move operation. It must be cleared by software by writing 1.

ASQREV Move Address Sequencing Reverse
ASQREV=0, the move action is performed by incrementing both source and destination addresses.
ASQREV =1, the move action is performed by incrementing source address and decrementing destination address.

ENDREV Endian Reverse
ENDREV=0, the move preserves the word endian.
ENDREV=1, the move reverses the word endian.

BYTREV Byte Revers
BYTREV=0, the move does not perform byte endian reversion.
BYTREV=1, the move reverses the endian on byte (8-bit) base.

ENDREV	BYTREV	Result
0	0	DATA[31-24] : DATA[23-16] : DATA[15-8] : DATA[7-0]
0	1	DATA[24-31] : DATA[16-23] : DATA[8-15] : DATA[0-7]
1	0	DATA[0-7] : DATA[8-15] : DATA[16-23] : DATA[24-31]

ENDREV	BYTREV	Result
1	1	DATA[7-0] : DATA[15-8] : DATA[23-16] : DATA[31-24]

BUSY — Busy Status
Busy=1 indicates the move operation is ongoing.

START — Start Move Operation
This bit is auto cleared when operation is completed.
START=0 No operation
START=1 Start the move

DMAMOVL (0x4000_0201) DMA Memory MOVE Length Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	LENGTH[7-0]							
WR	LENGTH[7-0]							

LENGTH[7-0] — Move Data Length
LENGTH[7-0] defines the number of word (32-bit) to be moved.

DMAMOVA (0x4000_0204) DMA Memory MOVE Address Register R/W (0x00000000)

	31-16	15-0
RD	DADDR[15-0]	SADDR[15-0]
WR	DADDR[15-0]	SADDR[15-0]

10.3 CS/CRC Accelerator

To enhance the performance, a hardware Checksum/CRC Accelerator is included and closely coupled with CPU and DMA. It provides most commonly used checksum and CRC operation for 8/16/32-bit data width. The input data stream is obtained from DMA SRAM through DMA access. The calculation is started by issuing START command. Alternatively, CPU can also perform CRC calculation by writing data into the CCDATA register if REGMODE is set.

CCCFGA (0x4000_0300) Checksum/CRC Accelerator Configuration Register A R/W (0x00)

	7	6	5	4	3	2	1	0
RD	DWIDTH[1-0]		REVERSE	NOCARRY	SEED	CRCMODE[2-0]		
WR	DWIDTH[1-0]		REVERSE	NOCARRY	SEED	CRCMODE[2-0]		

DWIDTH[1-0] — Data Width
00 – set input as 8-bit wide
01 – set input as 16-bit wide
10 – set the input as 24-bit wide
11 – set the input as 32-bit wide

REVERSE — Reverse Input MSB/LSB Sequence
REVERSE=0 is for LSB first operations.
REVERSE=1 is for MSB first operation.
The reverse order is based on the data width. The CS/CRC encoding hardware is done in LSB width.

NOCARRY — Carry Setting for Checksum
NOCARRY=0 uses previous carry result for new result
NOCARRY=1 discard previous carry result.

SEED — Seed Entry
SEED=1 results writing into CRCDATA to become SEED value
SEED=0 for normal data inputs.

CRCMODE[2-0] — Defines CRC/Checksum Mode
000 – Accelerator is disabled and clock gated off
001 – 8-bit Checksum
010 – 32-bit Checksum
011 – CRC-16 0x8005
X16+X15+X2+1
100 – CRC-16 0x102 CCITT

X16+X12+X5+1 1
101 – CRC-32 0x04C11DB7
X32+X26+C23+X22+X16+X12+X11+X10+X8+X7+X5+X4+X2+X1+1
110 – Reserved.
111 – CRC and Checksum Clear
Writing “111” to CRCMODE[1-0] reset the CS/CRC states and restore default seed value (for checksum, seed value=0x00 or 0x0000, for CRC seed value = 0xFFFF). Writing “111” does not affect the previously set mode selection.

CCCFGB (0x4000_0301) Checksum/CRC Accelerator Configuration Register B R/W (0x00)

	7	6	5	4	3	2	1	0
RD	REGMODE	-	OBYTESWP	OBITREV	-	-	-	BUSY
WR	REGMODE	-	OBYTESWP	OBITREV	-	-	-	START

REGMODE — Register Mode
REGMODE=0, CRC data is obtained automatically through DMA.
REGMODE=1, CRC data is input through writing of the CCDATA register.

OBYTESWP — Output Byte Swap
OBYTESWP=0, CCDATA is arranged as MSB byte, …, LSB byte.
OBYTESWP=1, CCDATA is arranged as LSB byte, …, MSB byte.

OBITREV — Output Bit Reverse
OBREV=0, CCDTAT is arrange as MSB, …., LSB
OBERV=1, CCDTAT is arrange as LSB, …., MSB
Please note, OBITREV is performed first then OBYTESWP.

BUSY — CRC Status
BUSY=1 indicates the results is not yet completed. Since only up to two cycles are used to calculate the Checksum or CRC, there is no need to check BUSY status before next data entry and reading the results.

START — CRC Start
Setting START=1 will start the CRC calculation with DMA access to the data. It is self-cleared to 0.

CCCFGC (0x4000_0302) Checksum/CRC Accelerator Configuration Register C R/W (0x00)

	7	6	5	4	3	2	1	0
RD	INTEN	-	-	-	-	-	-	INTF
WR	INTEN	-	-	-	-	-	-	INTF

INTEN — Interrupt Enable
INTEN=1 enables interrupt when DMA CRC calculation is completed.

INTF — Interrupt Flag
INTF is set to 1 by hardware when DMA CRC calculation is completed. INTF must be cleared by software by writing 1.

CCADDR (0x4000_0304) CS/CRC DMA Address Register R/W (0x00000000)

	31	30-16	15-8	7-0
RD	DESC	BC[14-0]	CCADDR[15-8]	CCADDR[7-0]
WR	DESC	BC[14-0]	CCADDR[15-8]	CCADDR[7-0]

DESC — Address Descending/Ascending
DESC=0 the new data is fetched with incrementing address when performing calculation.
DESC=1 the new data is fetched with decrementing address when performing calculation.

BC[14-0] — Byte Count
The number of bytes to be calculated. This must match with the DWIDTH setting.

CCADDR[15-0] — DMA Start Address
DMA memory start address. This can be byte, word, or double word address.

CCDATA (0x4000_0308) CS/CRC Data Register R/W (0x00000000)

	31-24	23-16	15-8	7-0
RD	CCDATA[31-24]	CCDATA[23-16]	CCDATA[15-8]	CCDATA[7-0]
WR	CCDATA[31-24]	CCDATA[23-16]	CCDATA[15-8]	CCDATA[7-0]

CCDATA registers are the data port for Checksum/CRC Accelerator. For 8-bit data width only CCDATA[7-0] should be used. When SEED=1, the data been written goes to CS or CRC seed value. The result of accelerator can be directly read out from CCDATA registers.

11. E-Flash Memory Controller

The embedded Flash memory contains two blocks. Main Memory and Information Block (IFB). The Main Memory is 12KX39 with uniform 256x39 page (1KB sector) size. There are four Information Blocks (IFB), each is also 256X39 in separate page. IFB0 (also referred to as IFBM) contains manufacture device information and calibration data. This block$_T$ should not be altered. IFB1 (referred to as IFBU) contains user data and can be accessed by the user.

The 39-bit access width of e-Flash consist of 32-bit data and 7-bit ECC. ECC is hardware encoded and decoded. When the e-Flash is erased, all contents is read as “1”. When e-Flash is programmed, the content is read as “0”. Reading e-Flashs' content enables ECC automatic checked. As a result, if a read operation is performed after erase, since all 39 bits are 1, ECC error will occur (DATA=FFFFFFFF ECC=0011000, DATA=00000000 ECC=0000000). After a write operation, the correct ECC content will be written by the hardware automatically. Then further reading operations should yield no ECC error.

The CPU access of the FLASH through AHB-Lite bus does not require any special attention. Due to limited FLASH access time (<40nsec), CPU running higher than 16MHz will need to set FLASH access wait state through WTST register. In the instruction fetch path, ECC is checked automatically. If ECC error is encounter, the ECC fault handling can be enabled to generate interrupt.

Software and including SWI can also access the FLASH through Flash Controller. The commands performed by a Flash Controller are defined in FLSHCMD registers. The defined operations allow the user program to use on-chip flash as a program memory, and a non-volatile data memory in In-System-Programming as well as In-Application-Programming.

There are two locking mechanisms for data and code security. UKEY is stored in IFB1’s top 8-byte location, and MKEY is stored in IFB0’s top 8-byte location. MKEY governs IFB0 data, and UKEY governs IFB1, IFB2, IFB3 and main memory data. Regardless of access means, the corresponding KEY information must be provided and Key Verify command completed successfully to unlock the data protection. Under locked state, only limited command can be issued and recognized. For command Locked State Erase commands are only accepted from SWI or CJTAG interface.

FLSHCMD0 (0x4000_1008) Flash Controller Command Register 0 R/W (0x90)

	7	6	5	4	3	2	1	0
RD	UKOPEN	MKOPEN	TBIT	ECCST	FAIL[2-0]			BUSY
WR	CMD[7-0]							

UKOPEN — UKEY Lock Status
UKOPEN is set to 1 after a successful UKEY verify command is finished with matching key value. Any further unsuccessful UKEY verify command will reset UKOPEN to 0. UKOPEN is also cleared to 0 after any reset condition.

MKOPEN — MKEY Lock Status
MKOPEN is set to 1 after a successful MKEY verify command is finished with matching key value. Any further unsuccessful MKEY verify command will reset MKOPEN to 0. MKOPEN is also cleared to 0 after any reset condition.

TBIT — An e-Flash Internal signal.

ECCST — ECC status
ECCST is updated by hardware after a read command is finished. The corresponding ECC checking result is shown by ECCST. If ECC passed, ECCST=0, if ECC failed, ECCST=1. This ECC does not cause the command to fail or cause any interrupt.

FAIL[2-0] — Command execution result.
FAIL[2-0] is set and cleared by hardware after a command is finished.
000 Command Successful
001 Fail due to locked state
010 Fail due to time out
011 Fail due to protection zone
100 Invalid address range
101 Invalid commands

BUSY — Flash Controller Status
BUSY is set to 1 by hardware indicating current command is still under execution.

FLSHCMD1 (0x4000_1009) Flash Controller Command Register 1 R/W (0x01)

	7	6	5	4	3	2	1	0
RD	SLEEPEN	-	1's comp of DMODE[1-0]		-	-	DMODE[1-0]	
WR	SLEEPEN	-	1's comp of DMODE[1-0]		-		DMODE[1-0]	

SLEEPEN — When set, enable the embedded flash sleep mode when the CPU entering the sleep mode.

DMODE[1-0] — Command Data Mode
00 = ECC decoded data
01 = ECC decoded data
10 = Raw data
11 = Raw data

FLSHCMD2 (0x4000_100A) Flash Controller Command Register 2 R/W (0x80)

	7	6	5	4	3	2	1	0
RD	RDALL1	-	-	-	-	-	-	MMERASED
WR	2's Complement of CMD[7-0]							

RDALL1 — This bit is set for a read command and all 39 bits of read data are one. This status helps to speed up for verify erase results.

MMERASED — This bit is set by hardware after MM erase command is completed successfully. This bit is cleared by any reset condition.

FLSHCMD3 (0x4000_100B) Flash Controller Command Register 3 R/W (0x00)

	7	6	5	4	3	2	1	0
RD	-	-	-	-	-	-	-	-
WR	1's Complement of CMD[7-0]							

CMD[7-0] — Command Definition is listed in the following table.

CMD7	CMD6	CMD5	CMD4	CMD3	CMD2	CMD1	CMD0	LOCK	Command
0	0	0	0	0	0	0	0	Y	Verify MKEY[1-0]. Key0 data is in FLSHDAT[31-0], Key1 data is in FLSHADDR[31-0]
0	0	0	0	0	0	0	1	Y	Verify UKEY[1-0]. Key0 data is in FLSHDAT[31-0], Key1 data is in FLSHADDR[31-0]
0	0	0	0	0	0	1	0	Y	Main Memory Erase
0	0	0	0	0	0	1	1	Y	Whole Chip Erase Only if MKOPEN=1. Use with caution. This erases manufacturing data and void any warranty.
0	0	0	0	0	1	0	0	Y	Lock State IFB 1 Erase. Executable only Main Memory Erase Command has just been completed and passed.
0	0	0	0	0	1	0	1	N	Main Memory Sector Erase
0	0	0	0	0	1	1	0	N	IFB 0 Erase Only if MKOPEN=1. Use with caution. This erases manufacturing data and voids warranty.
0	0	0	0	0	1	1	1	N	IFB 1 Erase
0	0	0	0	1	0	0	0	N	Main Memory Read
0	0	0	0	1	0	0	1	N	Main Memory Read, Auto Increment.

CMD7	CMD6	CMD5	CMD4	CMD3	CMD2	CMD1	CMD0	LOCK	Command
0	0	0	0	1	1	0	0	N/Y	IFB 0 Word Read Locked state limit access to 0x000-0x3F7.
0	0	0	0	1	1	0	1	N/Y	IFB 0 Word Read, Auto Increment. Locked state limit access to 0x000-0x3F7.
0	0	0	0	1	1	1	0	N	IFB 1 Word Read
0	0	0	0	1	1	1	1	N	IFB 1 Word Read, Auto Increment.
0	0	0	1	0	0	0	0	N	Main Memory Write
0	0	0	1	0	0	0	1	N	Main Memory Write Auto Increment.
0	0	0	1	0	1	0	0	N	IFB 0 Word Write
0	0	0	1	0	1	0	1	N	IFB 0 Word Write, Auto Increment.
0	0	0	1	0	1	1	0	N	IFB 1 Word Write
0	0	0	1	0	1	1	1	N	IFB 1 Word Write, Auto Increment.
0	0	0	1	1	0	0	0	N	IFB2 Erase
0	0	0	1	1	0	0	1	N	IFB2 Word Read
0	0	0	1	1	0	1	0	N	IFB2 Word Write
0	0	0	1	1	0	1	1	N	IFB3 Erase
0	0	0	1	1	1	0	0	N	IFB3 Word Read
0	0	0	1	1	1	0	1	N	IFB3 Word Write

The command definition is listed in the above table. Commands not listed are invalid and will cause a FAIL to be set. Please note to provide command integrity, FLSHCMD[15-8] must have the 1's complement value of CMD[7-0].

FLSHDAT (0x4000_1004) Flash Controller Data Register R/W (0x00000000)

	31 - 0
RD	Flash Read Data Register [31-0]
WR	Flash Write Data Register [31-0]

FLSHECC (0x4000_100C) Flash Controller Data Register R/W (0x7F)

	31 - 7	6-0
RD	-	ECC[6-0]
WR	-	ECC[6-0]

FLASHECC[6-0] contains raw data bits for the ECC code of the e-Flash. It is addressed by the FLASHARD and used when FLSHCMD's DMODE is set for raw data accesses.

FLSHADR (0x4000_1000) Flash Controller Address Register R/W (0xFF)

	31 - 0
RD	Flash Address Register ADDR[31-0]
WR	Flash Address Register ADDR[31-0]

Please note the least significant two bits of the address register are ignored as the flash interface is organized as 32-bit wide.

FLSHCFG0 (0x4000_1010) Flash Configuration Register 0 R/W (0x40)

	7	6	5	4	3	2	1	0
RD	ISPCLKF[7-0]							
WR	ISPCLKF[7-0]							

ISPCLKF[7-0] configures the clock time base for generation of Flash erase and write timing. ISPCLK = SYSCLK * (ISPCLKF[7-0]+1)/256. For correct timing, ISPCLK should be set to approximately at 4MHz.

FLSHCFG1 (0x4000_1011) Flash Configuration Register 1 R/W (0x04)

	7	6	5	4	3	2	1	0
RD	-	-	-	-	-	CYC[2-0]		
WR	-	-	-	-	-	CYC[2-0]		

CYC[2-0] Flash Command Time Out Setting

CYC[2-0] defines command time out cycle count. Cycle period is defined by ISPCLK. The number of ISPCLK cycles for time out is tabulated as following.

CYC[2-0]			WRITE	ERASE
0	0	0	100	10000
0	0	1	110	11000
0	1	0	120	12000
0	1	1	130	13000
1	0	0	140	14000
1	0	1	150	15000
1	1	0	160	16000
1	1	1	170	17000

Default is 100. For 4MHz ISPCLK, time out for write and erase is 35usec and 3.5msec respectively.

EFMECC (0x4000_1014) Embedded Flash Memory ECC Error Register R/W(0x00)

	7	6	5	4	3	2	1	0
RD	ECCOFF	-	-	-	IEN1	IEN0	ERRF1	ERRF0
WR	ECCOFF	-	-	-	IEN1	IEN0	ERRF1	ERRF0

ECCOFF ECC Enable
ECCOFF=0 enables ECC
ECCOFF=1 disable ECC

IEN1 Interrupt Enable for Un-correctable Error.
If IEN1=1, an un-correctable error will generate an ECC interrupt.

IEN0 Interrupt Enable for Correctable Error
If IEN0=1, a correctable error will generate an ECC interrupt.

ERRF1 Un-correctable Error Flag
ERRF1 is set to 1 when un-correctable error occurs for IEN1=1. This error flag is also mapped to ECCFLAG register as read only. This bit needs to be cleared by software by writing 1.

ERRF0 Correctable Error Flag
ERRF0 is set to 1 when correctable error occurs for IEN0=1. This error flag is also mapped to ECCFLAG register as read only. This bit needs to be cleared by software by writing 1.

EFMECCA (0x4000_1018) Embedded Flash Memory ECC Address Register R/W (0x80)

	31-24	23-18	17-8	7-0
RD	-	-	ECCADR[17-0]	
WR	-	-	-	

ECCADR[15-0] ECC Error Address

The e-Flash word address where ECC error occurs. This is read only. And it is cleared when ERRF1 and ERRF0 are cleared to 0.
Since the e-Flash size is 64K x 39, only ECCADR[17-0] are meaningful, and the LSB two bits are 0.

FLSHCFG2 (0x4000_101C) Flash Configuration Register 2 R/W (0x00)

	7	6	5	4	3	2	1	0
RD	-	-	-	PRTDLYST	PRTDLY[1-0]		-	
WR	-	-	-	-	PRTDLY[1-0]		-	

PRTDLYST — Protection Delay Status
PRTDLYST=1 indicates protection delay is still on.
PRTDLYST=0 indicates protection delay is off or no-effect.

PRTDLY[1-0] — Protection Off Delay Setting
This setting inserts a delay for turning off protection (setting FLSHPRT[31-0] or PRTIFB1, PRTIFB0, bit to 1) to prevent transient interference. Default is 100msec.

After power-on reset, all zones are protected for 100ms regardless of protection zone settings. After this period, any modification of the protection bits to turn off protection needs to elapse for a protection period defined by PRTDLY[1-0]. Please note, in order to erase or modify the content of the Flash, the corresponding MKEY and UKEY has to be first unlocked. In addition, PRTDLY setting insert an additional delay when turning off the protection. To regain total protection, the user program can issue an invalid KEY verify command ant restore lock state.

The e-Flash has segment size of 256 x 39 in 1KB size. For IS3XCS9310, the e-Flash is 64KB, each of the main memory 64 segments and two IFBs has its own protection setting bits. The protection is controlled by two protection bits, PRT and PPT. PRT default after reset to a logic 0, and PPT is a logic 1 where logic 0 means protected, and logic 1 means unprotected. PPT (permanent) can be written a logic 0 only and once written a logic 0, it stays a logic 0.

FLSHPIFB (0x4000_101D) Flash IFB Protection Register R/W (0xF0)

	7	6	5	4	3	2	1	0
RD	PPTIFB3	PPTIFB2	PPTIFB1	PPTIFB0	PRTIFB3	PRTIFB2	PRTIFB1	PRTIFB0
WR	PPTIFB3	PPTIFB2	PPTIFB1	PPTIFB0	PRTIFB3	PRTIFB2	PRTIFB1	PRTIFB0

PPTIFB3 — IFB3 Permanent Protection
PPTIFB2 — IFB2 Permanent Protection
PPTIFB1 — IFB1 Permanent Protection
PPTIFB0 — IFB0 Permanent Protection
PRTIFB3 — IFB3 Protection
PRTIFB2 — IFB2 Protection
PRTIFB1 — IFB1 Protection
PRTIFB0 — IFB0 Protection

FLSHPRT0 (0x4000_1100) MM Protection Register R/W (0x00000000)

	31-0
RD	FLSHPRT[31-0]
WR	FLSHPRT[31-0]

FLSHPRT1 (0x4000_1104) MM Protection Register R/W (0x00000000)

	31-0
RD	FLSHPRT[63-32]
WR	FLSHPRT[63-32]

FLSHPRT2 (0x4000_1108) MM Protection Register R/W (0x00000000)

	31-0
RD	FLSHPRT[95-64]
WR	FLSHPRT[95-32]

FLSHPRT3 (0x4000_110C) MM Protection Register R/W (0x00000000)

	31-0
RD	FLSHPRT[127-96]
WR	FLSHPRT[127-96]

FLSHPRT4 (0x4000_1110) MM Protection Register R/W (0x00000000)

	31-0
RD	FLSHPRT[159-128]
WR	FLSHPRT[159-128]

FLSHPRT5 (0x4000_1114) MM Protection Register R/W (0x00000000)

	31-0
RD	FLSHPRT[191-160]
WR	FLSHPRT[191-160]

FLSHPRT6 (0x4000_1118) MM Protection Register R/W (0x00000000)

	31-0
RD	FLSHPRT[223-192]
WR	FLSHPRT[223-192]

FLSHPRT7 (0x4000_111C) MM Protection Register R/W (0x00000000)

	31-0
RD	FLSHPRT[255-224]
WR	FLSHPRT[1255-224]

FLSHPPT0 (0x4000_1180) MM Permanent Protection Register R/W (0xFFFFFFFF)

	31-0
RD	FLSHPPT[31-0]
WR	FLSHPPT[31-0]

FLSHPPT1 (0x4000_1184) MM Permanent Protection Register R/W (0xFFFFFFFF)

	31-0
RD	FLSHPPT[63-32]
WR	FLSHPPT[63-32]

FLSHPPT2 (0x4000_1188) MM Permanent Protection Register R/W (0xFFFFFFFF)

	31-0
RD	FLSHPPT[95-64]
WR	FLSHPPT[95-64]

FLSHPPT3 (0x4000_118C) MM Permanent Protection Register R/W (0xFFFFFFFF)

	31-0
RD	FLSHPPT[127-96]
WR	FLSHPPT[127-96]

FLSHPPT4 (0x4000_1190) MM Permanent Protection Register R/W (0xFFFFFFFF)

	31-0
RD	FLSHPPT[159-128]
WR	FLSHPPT[159-128]

FLSHPPT5 (0x4000_1194) MM Permanent Protection Register R/W (0xFFFFFFFF)

	31-0
RD	FLSHPPT[191-160]
WR	FLSHPPT[191-160]

FLSHPPT6 (0x4000_1198) MM Permanent Protection Register R/W (0xFFFFFFFF)

	31-0
RD	FLSHPPT[223-192]
WR	FLSHPPT[223-192]

FLSHPPT7 (0x4000_119C) MM Permanent Protection Register R/W (0xFFFFFFFF)

	31-0
RD	FLSHPPT[255-224]
WR	FLSHPPT[1255-224]

12. LED

STATUS (0x4001_0000) General Status Register R/W (0x80)

	7	6	5	4	3	2	1	0
RD	-	THST	-		-		LEDF	
WR	-	-	-	-	-		LEDF	

THST — Thermal Status
THST=0 for die temperature lower preset temperature
THST=1 for die temperature higher than preset temperature

LEDF — LED Controller Interrupt Flag

CONTROL (0x4001_0001) General Control Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	RESET						IENLED	
WR	RESET						IENLED	

RESET — 0110: reset the LED controller state machine.
1001: reset the LED controller registers

IENLED — Interrupt Enable for LED Controller

DEGHOST (0x4001_0002) General Control Register R/W (0x0F)

	7	6	5	4	3	2	1	0
RD				SWNOP				
WR				SWNOP				

SWNOP[4-0] — SW non-overlap setting (n+1)*PWMCLK

SWOCP (0x4001_0003) SW OCP State Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	SWOCP[7-0]							
WR	SWOCP[7-0]							

This register show 8 SW OCP state.

SWOCP[n] — SW OCP state.
1: OCP

LEDCFGA (0x4001_0004) LED Configuration Register A R/W (0x00)

	7	6	5	4	3	2	1	0
RD	LEDEN	LEDCS[2-0]			PWMMD[3-0]			
WR	LEDEN	LEDCS[2-0]			PWMMD[3-0]			

LEDEN — LED Controller Enable
LEDEN=0 disable the LED control. No Clock, and analog is shut down.
LEDEN=1 enables the LED control. Clock and analog is enabled.

LEDCS[2-0] — LED Clock Scaler
LED clock is LEDCLK/(LEDCS[2-0]+1)

PWMMD[3-0] — CS PWM Mode
0000/0100/1000 = 8-bit
0001/0101/1001 = 6+2 bit
XX10 = 8+4 bit
XX11 = 12 bit
1100 = 7+5 bit
1101 = 7+6 bi

LEDCFGB (0x0x4001_0005) LED Configuration Register B R/W (0x00)

	7	6	5	4	3	2	1	0
RD	RND	SCM	DISPOFF[1-0]		SWMD[3-0]			
WR	RND	SCM	DISPOFF[1-0]		SWMD[3-0]			

RND — Random Scan Mode
RND=0 Disable
RND=1 Enable

SCM — Small Current Mode
SCM=0 Disable
SCM=1 Enable

DISPOFF[1-0] — LED Display Control
DISPOFF = 00 for normal LED display, CS switches are controlled by PWM
DISPOFF = 01 turns off all CS switch for no display.
DISPOFF = 10 turns on all CS switch for maximum display intensity.
DISPOFF = 11 Reserved and is the same as 00 setting.
DISPOFF is synchronized by frame timing.

SWMD[2-0] — Switch Scan Mode
0000 = 1/8 duty, SW8 – SW1 are all enabled.
0001 = 1/7 duty, SW7 – SW1 are enabled. SW8 is disabled.
0010 = 1/6 duty, SW6 – SW1 are enabled. SW8 – SW7 are disabled.
0011 = 1/5 duty, SW5 – SW1 are enabled. SW8 – SW6 are disabled.
0100 = 1/4 duty, SW4 – SW1 are enabled. SW8 – SW5 are disable.
0101 = 1/3 duty, SW3 – SW1 are enabled. SW8 – SW4 are disabled.
0110 = 1/2 duty, SW2 – SW1 are enabled. SW8 – SW3 are disabled.
0111 = 1/1 duty, SW1 is enabled. SW8 – SW2 are disabled.
1000 = 1/4 duty, SW1=SW2, SW3=SW4, SW5=SW6, SW7=SW8.
1001 = 1/2 duty, SW1=SW2=SW3=SW4, SW5=SW6=SW7=SW8.

LEDCFGC (0x4001_0006) LED Configuration Register C R/W (0x80)

	7	6	5	4	3	2	1	0
RD	THSDEN	THST	-					
WR	THSDEN	-	-					

THSDEN — Thermal Shutdown Enable
THSDEN=0 disable thermal shutdown LED
THSDEN=1 enable thermal shutdown LED
Thermal shutdown condition is asserted if THST=1.

THST — Thermal Status
THST=0 for die temperature lower preset temperature
THST=1 for die temperature higher than preset temperature

LEDCFGD (0x4001_0007) LED Configuration Register D R/W (0x00)

	7	6	5	4	3	2	1	0
RD	-	SWPD[2-0]			-	CSPU[2-0]		
WR	-	SWPD[2-0]			-	CSPU[2-0]		

SWPD[2-0] — SWx Pull Down Select
SWPD[2-0] = 000 No pull down
SWPD[2-0] = 001 3.2V
SWPD[2-0] = 010 2.8V
SWPD[2-0] = 011 2.4V
SWPD[2-0] = 100 2.0V
SWPD[2-0] = 101 1.6V
SWPD[2-0] = 110 1.2V
SWPD[2-0] = 111 0V

CSPU[2-0] — CSx Pull Up Select
CSPU [2-0] = 000 No pull up

CSPU [2-0] = 001 PVDD – 3.2V
CSPU [2-0] = 010 PVDD – 2.8V
CSPU [2-0] = 011 PVDD – 2.4V
CSPU [2-0] = 100 PVDD – 2.0V
CSPU [2-0] = 101 PVDD – 1.6V
CSPU [2-0] = 110 PVDD – 1.2V
CSPU [2-0] = 111 PVDD

LEDPWMA (0x4001_0008) LED CS PWM Alignment Register A R/W (0x00)

	7	6	5	4	3	2	1	0
RD	CSPWM[8-1]							
WR	CSPWM[8-1]							

CSPWM[8-1] CS[i] PWM Alignment Selection
CSPWM[i] = 0 uses left alignment
CSPWM[i] = 1 uses right alignment

LEDPWMB (0x4001_0009) LED CS PWM Alignment Register B R/W (0x00)

	7	6	5	4	3	2	1	0
RD	-				CSPWM[12-9]			
WR	-				CSPWM[12-9]			

CSPWM[12-9] CS[i] PWM Alignment Selection
CSPWM[i] = 0 uses left alignment
CSPWM[i] = 1 uses right alignment

LEDOSA (0x4001_000B) LED Open Short Detect Register A R/W (0x00)

	7	6	5	4	3	2	1	0
RD	OS[1-0]		SWOC	OSSPD		SWSEL[2-0]		
WR	OS[1-0]		SWOC	OSSPD		SWSEL[2-0]		

OS[1-0] Select Open or Short
0x Disable
10 Open Detect
11 Short Detect
SWOC Switch Short Detection
OSSPD OPEN/SHORT sample point delay
00 POSC clock *16
01 POSC clock *24
10 POSC clock *32
11 POSC clock *40
SWSEL[2-0] Switch Select for Open/Short Detect
000 SW1
001 SW2
010 SW3
011 SW4
100 SW5
101 SW6
110 SW7
111 SW8.

LEDOSB (0x4001_000C) LED CS Open Short Detect Register B RO (0x00)

	7	6	5	4	3	2	1	0
RD	CSOS[8-1]							
WR	-							

CSOS[8-1] CS Open/Short Status
CSOS[i] is 0 if OS[1-0] is 0x.
CSOS[i] status is refreshed as frame rate.

LEDOSC (0x4001_000D) LED Open Short Detect Register C RW (0x00)

	7	6	5	4	3	2	1	0
RD	-	-	-	-	CSOS[12-9]			
WR	-	-	-	-	-			

CSOS[12-9] CS Open/Short Status

LEDGCC (0x4001_000E) LED CS Global Current Control R/W (0x00)

	7	6	5	4	3	2	1	0
RD	LEDGCC[7-0]							
WR	LEDGCC[7-0]							

LEDGCC[7-0] LED Global Current Control

LEDCS1 (0x4001_0010) LED CS1 Current Scale R/W (0x00)

	7	6	5	4	3	2	1	0
RD	LEDCS1[7-0]							
WR	LEDCS1[7-0]							

LEDCS1[7-0] CS1 Current Scale

LEDCS2 (0x4001_0011) LED CS2 Current Scale R/W (0x00)

	7	6	5	4	3	2	1	0
RD	LEDCS2[7-0]							
WR	LEDCS2[7-0]							

LEDCS2[7-0] CS2 Current Scale

LEDCS3 (0x4001_0012) LED CS3 Current Scale R/W (0x00)

	7	6	5	4	3	2	1	0
RD	LEDCS3[7-0]							
WR	LEDCS3[7-0]							

LEDCS3[7-0] CS3 Current Scale

LEDCS4 (0x4001_0013) LED CS4 Current Scale R/W (0x00)

	7	6	5	4	3	2	1	0
RD	LEDCS4[7-0]							
WR	LEDCS4[7-0]							

LEDCS4[7-0] CS4 Current Scale

LEDCS5 (0x4001_0014) LED CS5 Current Scale R/W (0x00)

	7	6	5	4	3	2	1	0
RD	LEDCS5[7-0]							
WR	LEDCS5[7-0]							

LEDCS5[7-0] CS5 Current Scale

LEDCS6 (0x4001_0015) LED CS6 Current Scale R/W (0x00)

	7	6	5	4	3	2	1	0
RD	LEDCS6[7-0]							
WR	LEDCS6[7-0]							

LEDCS6[7-0] CS6 Current Scale

LEDCS7 (0x4001_0016) LED CS7 Current Scale R/W (0x00)

	7	6	5	4	3	2	1	0
RD	LEDCS7[7-0]							
WR	LEDCS7[7-0]							

LEDCS7[7-0] CS7 Current Scale

LEDCS8 (0x4001_0017) LED CS8 Current Scale R/W (0x00)

	7	6	5	4	3	2	1	0
RD	LEDCS8[7-0]							
WR	LEDCS8[7-0]							

LEDCS8[7-0] CS8 Current Scale

LEDCS9 (0x4001_0018) LED CS9 Current Scale R/W (0x00)

	7	6	5	4	3	2	1	0
RD	LEDCS9[7-0]							
WR	LEDCS9[7-0]							

LEDCS9[7-0] CS9 Current Scale

LEDCS10 (0x4001_0019) LED CS10 Current Scale R/W (0x00)

	7	6	5	4	3	2	1	0
RD	LEDCS10[7-0]							
WR	LEDCS10[7-0]							

LEDCS10[7-0] CS10 Current Scale

LEDCS11 (0x4001_001A) LED CS11 Current Scale R/W (0x00)

	7	6	5	4	3	2	1	0
RD	LEDCS11[7-0]							
WR	LEDCS11[7-0]							

LEDCS11 [7-0] CS11 Current Scale

LEDCS12 (0x4001_001B) LED CS12 Current Scale R/W (0x00)

	7	6	5	4	3	2	1	0
RD	LEDCS12[7-0]							
WR	LEDCS12[7-0]							

LEDCS12[7-0] C1S2 Current Scale

There are total 8x12 LED pixels. Each pixel has 12-bit PWM data and thus occupies two bytes. These are organized as frame buffer and should be implemented using latches. There are two frame buffers one is for active display and one is for data buffering. When UPD command is issued, the content of the data buffer is loaded into the active display frame buffer. The frame buffer is accessed in the following address organization.

SW8	SW8CS1 PWM	SW8CS2 PWM	SW8CS3 PWM	SW8CS4 PWM	SW8CS5 PWM	SW8CS6 PWM	SW8CS7 PWM	SW8CS8 PWM	SW8CS9 PWM	SW8CS10 PWM	SW8CS11 PWM	SW8CS12 PWM
SW7	SW7CS1 PWM	SW7CS2 PWM	SW7CS3 PWM	SW7CS4 PWM	SW7CS5 PWM	SW7CS6 PWM	SW7CS7 PWM	SW7CS8 PWM	SW7CS9 PWM	SW7CS10 PWM	SW7CS11 PWM	SW7CS12 PWM
SW6	SW6CS1 PWM	SW6CS2 PWM	SW6CS3 PWM	SW6CS4 PWM	SW6CS5 PWM	SW6CS6 PWM	SW6CS7 PWM	SW6CS8 PWM	SW6CS9 PWM	SW6CS10 PWM	SW6CS11 PWM	SW6CS12 PWM
SW5	SW5CS1 PWM	SW5CS2 PWM	SW5CS3 PWM	SW5CS4 PWM	SW5CS5 PWM	SW5CS6 PWM	SW5CS7 PWM	SW5CS8 PWM	SW5CS9 PWM	SW5CS10 PWM	SW5CS11 PWM	SW5CS12 PWM
SW4	SW4CS1 PWM	SW4CS2 PWM	SW4CS3 PWM	SW4CS4 PWM	SW4CS5 PWM	SW4CS6 PWM	SW4CS7 PWM	SW4CS8 PWM	SW4CS9 PWM	SW4CS10 PWM	SW4CS11 PWM	SW4CS12 PWM
SW3	SW3CS1 PWM	SW3CS2 PWM	SW3CS3 PWM	SW3CS4 PWM	SW3CS5 PWM	SW3CS6 PWM	SW3CS7 PWM	SW3CS8 PWM	SW3CS9 PWM	SW3CS10 PWM	SW3CS11 PWM	SW3CS12 PWM
SW2	SW2CS1 PWM	SW2CS2 PWM	SW2CS3 PWM	SW2CS4 PWM	SW2CS5 PWM	SW2CS6 PWM	SW2CS7 PWM	SW2CS8 PWM	SW2CS9 PWM	SW2CS10 PWM	SW2CS11 PWM	SW2CS12 PWM
SW1	SW1CS1 PWM	SW1CS2 PWM	SW1CS3 PWM	SW1CS4 PWM	SW1CS5 PWM	SW1CS6 PWM	SW1CS7 PWM	SW1CS8 PWM	SW1CS9 PWM	SW1CS10 PWM	SW1CS11 PWM	SW1CS12 PWM
	CS1	CS2	CS3	CS4	CS5	CS6	CS7	CS8	CS9	CS10	CS11	CS12

Figure 12-1 PWM configuration register address matrix

PWM configuration register address list

Name	Address	Name	Address	Name	Address	Name	Address
SW1CS1PWM	0x4001_0020 0x4001_0021	SW2CS1PWM	0x4001_0038 0x4001_0039	SW3CS1PWM	0x4001_0050 0x4001_0051	SW4CS1PWM	0x4001_0068 0x4001_0069
SW1CS2PWM	0x4001_0022 0x4001_0023	SW2CS2PWM	0x4001_003A 0x4001_003B	SW3CS2PWM	0x4001_0052 0x4001_0053	SW4CS2PWM	0x4001_006A 0x4001_006B
SW1CS3PWM	0x4001_0024 0x4001_0025	SW2CS3PWM	0x4001_003C 0x4001_003D	SW3CS3PWM	0x4001_0054 0x4001_0055	SW4CS3PWM	0x4001_006C 0x4001_006D
SW1CS4PWM	0x4001_0026 0x4001_0027	SW2CS4PWM	0x4001_003E 0x4001_003F	SW3CS4PWM	0x4001_0056 0x4001_0057	SW4CS4PWM	0x4001_006E 0x4001_006F
SW1CS5PWM	0x4001_0028 0x4001_0029	SW2CS5PWM	0x4001_0040 0x4001_0041	SW3CS5PWM	0x4001_0058 0x4001_0059	SW4CS5PWM	0x4001_0070 0x4001_0071
SW1CS6PWM	0x4001_002A 0x4001_002B	SW2CS6PWM	0x4001_0042 0x4001_0043	SW3CS6PWM	0x4001_005A 0x4001_005B	SW4CS6PWM	0x4001_0072 0x4001_0073
SW1CS7PWM	0x4001_002C 0x4001_002D	SW2CS7PWM	0x4001_0044 0x4001_0045	SW3CS7PWM	0x4001_005C 0x4001_005D	SW4CS7PWM	0x4001_0074 0x4001_0075
SW1CS8PWM	0x4001_002E 0x4001_002F	SW2CS8PWM	0x4001_0046 0x4001_0047	SW3CS8PWM	0x4001_005E 0x4001_005F	SW4CS8PWM	0x4001_0076 0x4001_0077

Name	Address	Name	Address	Name	Address	Name	Address
SW1CS9PWM	0x4001_0030 0x4001_0031	SW2CS9PWM	0x4001_0048 0x4001_0049	SW3CS9PWM	0x4001_0060 0x4001_0061	SW4CS9PWM	0x4001_0078 0x4001_0079
SW1CS10PWM	0x4001_0032 0x4001_0033	SW2CS10PWM	0x4001_004A 0x4001_004B	SW3CS10PWM	0x4001_0062 0x4001_0063	SW4CS10PWM	0x4001_007A 0x4001_007B
SW1CS11PWM	0x4001_0034 0x4001_0035	SW2CS11PWM	0x4001_004C 0x4001_004D	SW3CS11PWM	0x4001_0064 0x4001_0065	SW4CS11PWM	0x4001_007C 0x4001_007D
SW1CS12PWM	0x4001_0036 0x4001_0037	SW2CS12PWM	0x4001_004E 0x4001_004F	SW3CS12PWM	0x4001_0066 0x4001_0067	SW4CS12PWM	0x4001_007E 0x4001_007F
SW5CS1PWM	0x4001_0080 0x4001_0081	SW6CS1PWM	0x4001_0098 0x4001_0099	SW7CS1PWM	0x4001_00B0 0x4001_00B1	SW8CS1PWM	0x4001_00C8 0x4001_00C9
SW5CS2PWM	0x4001_0082 0x4001_0083	SW6CS2PWM	0x4001_009A 0x4001_009B	SW7CS2PWM	0x4001_00B2 0x4001_00B3	SW8CS2PWM	0x4001_00CA 0x4001_00CB
SW5CS3PWM	0x4001_0084 0x4001_0085	SW6CS3PWM	0x4001_009C 0x4001_009D	SW7CS3PWM	0x4001_00B4 0x4001_00B5	SW8CS3PWM	0x4001_00CC 0x4001_00CD
SW5CS4PWM	0x4001_0086 0x4001_0087	SW6CS4PWM	0x4001_009E 0x4001_009F	SW7CS4PWM	0x4001_00B6 0x4001_00B7	SW8CS4PWM	0x4001_00CE 0x4001_00CF
SW5CS5PWM	0x4001_0088 0x4001_0089	SW6CS5PWM	0x4001_00A0 0x4001_00A1	SW7CS5PWM	0x4001_00B8 0x4001_00B9	SW8CS5PWM	0x4001_00D0 0x4001_00D1
SW5CS6PWM	0x4001_008A 0x4001_008B	SW6CS6PWM	0x4001_00A2 0x4001_00A3	SW7CS6PWM	0x4001_00BA 0x4001_00BB	SW8CS6PWM	0x4001_00D2 0x4001_00D3
SW5CS7PWM	0x4001_008C 0x4001_008D	SW6CS7PWM	0x4001_00A4 0x4001_00A5	SW7CS7PWM	0x4001_00BC 0x4001_00BD	SW8CS7PWM	0x4001_00D4 0x4001_00D5
SW5CS8PWM	0x4001_008E 0x4001_008F	SW6CS8PWM	0x4001_00A6 0x4001_00A7	SW7CS8PWM	0x4001_00BE 0x4001_00BF	SW8CS8PWM	0x4001_00D6 0x4001_00D7
SW5CS9PWM	0x4001_0090 0x4001_0091	SW6CS9PWM	0x4001_00A8 0x4001_00A9	SW7CS9PWM	0x4001_00C0 0x4001_00C1	SW8CS9PWM	0x4001_00D8 0x4001_00D9
SW5CS10PWM	0x4001_0092 0x4001_0093	SW6CS10PWM	0x4001_00AA 0x4001_00AB	SW7CS10PWM	0x4001_00C2 0x4001_00C3	SW8CS10PWM	0x4001_00DA 0x4001_00DB

Name	Address	Name	Address	Name	Address	Name	Address
SW5CS11PWM	0x4001_0094 0x4001_0095	SW6CS11PWM	0x4001_00AC 0x4001_00AD	SW7CS11PWM	0x4001_00C4 0x4001_00C5	SW8CS11PWM	0x4001_00DC 0x4001_00DD
SW5CS12PWM	0x4001_0096 0x4001_0097	SW6CS12PWM	0x4001_00AE 0x4001_00AF	SW7CS12PWM	0x4001_00C6 0x4001_00C7	SW8CS12PWM	0x4001_00DE 0x4001_00DF

Table 12-1 PWM configuration register address list

LEDFRM (0x4001_00E0) LED Display Frame Update Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	FRMIEN	UPDIEN	OSIEN	FSYNC	FRMIF	UPDIF	OSEIF	FUPD
WR	FRMIEN	UPDIEN	OSIEN	FSYNC	FRMIF	UPDIF	OSEIF	FUPD

FRMIEN Frame Interrupt Enable
UPDIEN Update Complete Interrupt Enable
OSIEN Open/Short Interrupt Enable
FSYNC Frame Sync
Write FSYNC=1 cause a frame restart synchronization. It is self-cleared.
FRMIF Frame Interrupt Flag
UPDIF Update Interrupt Flag
OSIF Open/Short Interrupt Flag
FUPD Frame Update
Write FUPD=1 causes the frame date update. The update occurs when the current frame is completed. FUPD is self-cleared.
Reading FUPD=1 indicate the update is still pending and reading FUPD=0 indicate the update is completed. Software should check FUPD=0 before writing new data into the frame buffer.

Each LED pixel can be individually turned on and off by using LEDDISPx register. This can be used by host to implement flicker function. The on/off action is frame synchronized. Dabc corresponds to SWa and CSbc pixel. For example, D105 means pixel located by SW1 and CS05, and D105 = 1 turns off the pixel's CS switch.

LEDOVP1 (0x4001_00E1) LED PVDD Overvoltage Protection (0x00)

	7	6	5	4	3	2	1	0
RD	OVP_VREF[5-0]						OVPINTEN	OVP_EN
WR	OVP_VREF[5-0]						OVPINTEN	OVP_EN

OVP_VREF[5-0] overvoltage threshold value trim, the higher the value of OVP_VREF<5-0>, the lower the threshold is.
When OVP_VREF[5-0] is changed， the program needs to wait at least 2us allowing OVP_EN=1 ,in order to make OVP_VREF fully established
OVPINTEN OVP interrupt enable
OVP_EN LED PVDD overvoltage protection enable
OVP_EN = 0 LED PVDD overvoltage protection disable
when in sleep mode, LED PVDD overvoltage protection should be disable
OVP_EN = 1 PVDD LED PVDD overvoltage protection enable

LEDOVP2 (0x4001_00E2) State Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD								OVST
WR								

OVST LED PVDD Overvoltage Status
OVST=0 for PVDD voltage lower preset voltage
OVST=1 for PVDD voltage higher than preset voltage

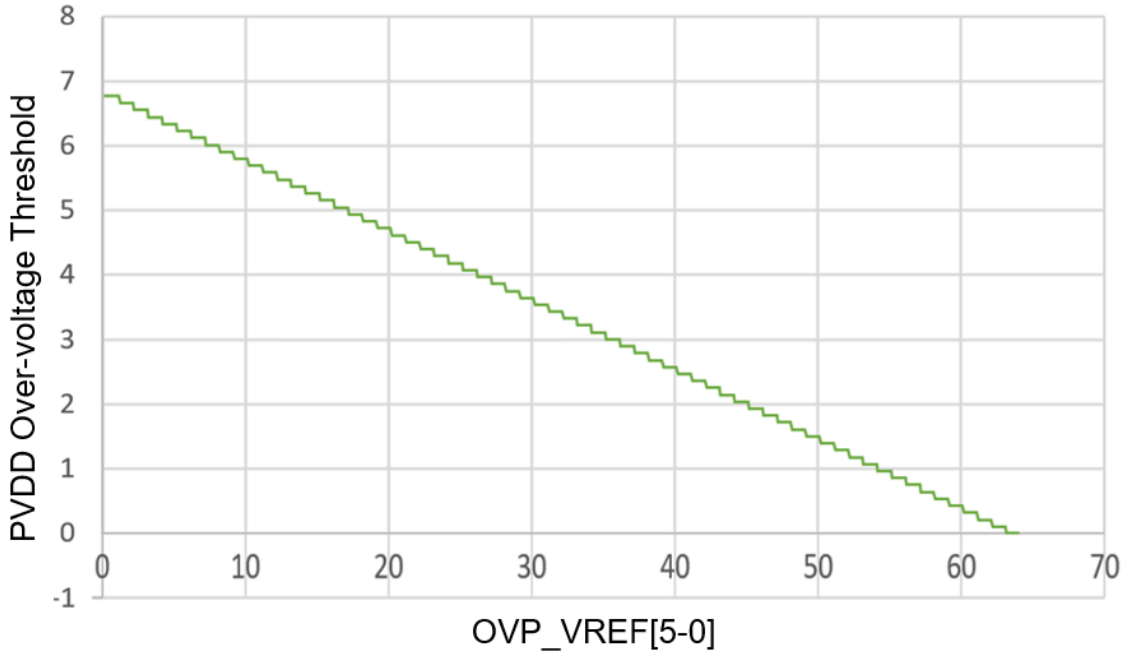


Figure 12-2 OVP Threshold

The supply overvoltage detection (OVD) circuit detects for when PVDD > VTH and can be used to generates an Overvoltage Status. The OVP_VREF [5-0] sets the compare threshold according to the following equation when OVPTHV is the detected voltage. Do not set the overvoltage threshold too high or below 3V.

OVPTHV = VD15 * 55 * (64-OVP_VREF[5-0])/768

TESTDEGHOST (0x4001_00E3) TEST DEGHOST OPTION State Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	TESTDE[7-4]				TESTDE[3-0]			
WR	TESTDE[7-4]				TESTDE[3-0]			

This register show SW PULLDN and CS PULLUP Options.

TESTDE[7-4] CS PULLUP Options state.
TESTDE[3-0] SW PULLDN Options state.

LEDDISPA (0x4001_00E4) LED Display On/Off Register A R/W (0x00)

	7	6	5	4	3	2	1	0
RD	D108	D107	D106	D105	D104	D103	D102	D101
WR	D108	D107	D106	D105	D104	D103	D102	D101

LEDDISPB (0x4001_00E5) LED Display On/Off Register B R/W (0x00)

	7	6	5	4	3	2	1	0
RD	D204	D203	D202	D201	D112	D111	D110	D109
WR	D204	D203	D202	D201	D112	D111	D110	D109

LEDDISPC (0x4001_00E6) LED Display On/Off Register C R/W (0x00)

	7	6	5	4	3	2	1	0
RD	D212	D211	D210	D209	D208	D207	D206	D205
WR	D212	D211	D210	D209	D208	D207	D206	D205

LEDDISPD (0x4001_00E7) LED Display On/Off Register D R/W (0x00)

	7	6	5	4	3	2	1	0
RD	D308	D307	D306	D305	D304	D303	D302	D301
WR	D308	D307	D306	D305	D304	D303	D302	D301

LEDDISPE (0x4001_00E8) LED Display On/Off Register E R/W (0x00)

	7	6	5	4	3	2	1	0
RD	D404	D403	D402	D401	D312	D311	D310	D309
WR	D404	D403	D402	D401	D312	D311	D310	D309

LEDDISPF (0x4001_00E9) LED Display On/Off Register F R/W (0x00)

	7	6	5	4	3	2	1	0
RD	D412	D411	D410	D409	D408	D407	D406	D405
WR	D412	D411	D410	D409	D408	D407	D406	D405

LEDDISPG (0x4001_00EA) LED Display On/Off Register G R/W (0x00)

	7	6	5	4	3	2	1	0
RD	D508	D507	D506	D505	D504	D503	D502	D501
WR	D508	D507	D506	D505	D504	D503	D502	D501

LEDDISPH (0x4001_00EB) LED Display On/Off Register H R/W (0x00)

	7	6	5	4	3	2	1	0
RD	D604	D603	D602	D601	D512	D511	D510	D509
WR	D604	D603	D602	D601	D512	D511	D510	D509

LEDDISPI (0x4001_00EC) LED Display On/Off Register I R/W (0x00)

	7	6	5	4	3	2	1	0
RD	D612	D611	D610	D609	D608	D607	D606	D605
WR	D612	D611	D610	D609	D608	D607	D606	D605

LEDDISPJ (0x4001_00ED) LED Display On/Off Register I R/W (0x00)

	7	6	5	4	3	2	1	0
RD	D708	D707	D706	D705	D704	D703	D702	D701
WR	D708	D707	D706	D705	D704	D703	D702	D701

LEDDISPK (0x4001_00EE) LED Display On/Off Register I R/W (0x00)

	7	6	5	4	3	2	1	0
RD	D804	D803	D802	D801	D712	D711	D710	D709
WR	D804	D803	D802	D801	D712	D711	D710	D709

LEDDISPL (0x4001_00EF) LED Display On/Off Register I R/W (0x00)

	7	6	5	4	3	2	1	0
RD	D812	D811	D810	D809	D808	D807	D806	D805
WR	D812	D811	D810	D809	D808	D807	D806	D805

PROTECT (0x4001_00F0) Protection Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	PR[7-0]							
WR	PR[7-0]							

PR[7-0] Protection Content for TP protected registers

PR[7-0] = 0xC5 to unlock protected registers. Any other value protects those registers value to be changed.
PR[7-0] is cleared to 0x00 after 10msec.

TSTMD (0x4001_00F1) Test Mode Control R/W (0x00) TP Protect

	7	6	5	4	3	2	1	0
RD	TSTEN[3-0]				TSTMD[3-0]			
WR	TSTEN[3-0]				TSTMD[3-0]			

TSTEN[3-0] Test Mode Enable
TSTEN[3-0]=1001 put device in test mode. The test mode is determined by TSTMD[3-0].
TSTMD[3-0] Test Mode Select

TRMREG1 (0x4001_00F2) Trim Register 1 R/W (0x00) TP Protect

	7	6	5	4	3	2	1	0
RD	BGTESTEN	TISETSM[2-0]			TBG[3-0]			
WR	BGTESTEN	TISETSM[2-0]			TBG[3-0]			

BGTESTEN BG Test Enable
BG output is brought out to PIN?
TISETSM[2-0] ISET Small Current Trim
TBG[3-0] BG Trim
+128mV -- -148mV. Each LSB is 20mV.

TRMREG2 (0x4001_00F3) Trim Register 2 R/W (0x00) TP Protect

	7	6	5	4	3	2	1	0
RD		-	TISET[5-0]					
WR		-	TISET[5-0]					

TISET[5-0] ISET Trim

TRMREG3 (0x4001_00F4) Trim Register 3 R/W (0x00) TP Protect

	7	6	5	4	3	2	1	0
RD	OSRANK[1-0]		-					
WR	OSRANK[1-0]		-					

OSRANK[1-0] CS Offset Global Trim

TRMREG4 (0x4001_00F5) Trim Register 4 R/W (0x00) TP Protect

	7	6	5	4	3	2	1	0
RD	CSOFFSET[7-0]							
WR	CSOFFSET[7-0]							

TRMREG5(0x4001_00F6) Trim Register 4 R/W (0x00) TP Protect

	7	6	5	4	3	2	1	0
RD	CSOFFSET[15-8]							
WR	CSOFFSET[15-8]							

TRMREG6 (0x4001_00F7) Trim Register 6 R/W (0x00) TP Protect

	7	6	5	4	3	2	1	0
RD	CSOFFSET[23-16]							
WR	CSOFFSET[23-16]							

CSOFFSET[23-0] 2bit CS OFFSET TRIM for 12 CS

TRMREG7 (0x4001_00F8) Trim Register 7 R/W (0x00) TP Protect

	7	6	5	4	3	2	1	0
RD	CSEN	SWEN						
WR	CSEN	SWEN						

CSEN — CS Headroom Test Enable
SWEN — SW Headroom Test Enable

TRMREG8 (0x4001_00F9) Trim Register 8 R/W (0x00) TP Protect

	7	6	5	4	3	2	1	0
RD	TESTSW[7-0]							
WR	TESTSW[7-0]							

TESTSW[7-0] — SWx Test Enable

LEDTESTA (0x4001_00FA) LED Test Register A R/W (0x00) TP Protect

	7	6	5	4	3	2	1	0
RD					OT_DIS		OT	
WR					OT_DIS		OT	

OT_DIS — 1: Over-Temperature Disable
OT[1-0] — Over-Temperature Range Trim
00: Default

LEDTESTB (0x4001_00FB) LED Test Register B R/W (0x00) TP Protect

	7	6	5	4	3	2	1	0
RD	BK[7-0]							
WR	BK[7-0]							

BK[7] — Test CS Pull up Enable
BK[6] — Test SW Pull Down Enable
BK[5-4] — SW_OC current Trim
BK[3-0] — Reserved

PRTIME (0x4001_00FC) I2CS Watchdog Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	-	-	PROTWIN		-	-		
WR	-	-	PROTWIN		-	-		

PROTWIN[1-0]
00: PR[7-0] is cleared to 0x00 after 10msec.
01: PR[7-0] is cleared to 0x00 after 20msec.
10: PR[7-0] is cleared to 0x00 after 50msec.
11: PR[7-0] is cleared to 0x00 after 100msec.

POSCITRM (0x4001_00FD) POSC Coarse Trim Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	SSC[3-0]				SSA[1-0]			
WR	SSC[3-0]				SSA[1-0]			

SSC[3-0] — SSC[3-0] defines the spread spectrum sweep rate. If SSC[3-0] = 0000, then the spread spectrum is disabled.

SSA[1-0] — SSA[1-0] defines the amplitude of spread spectrum frequency change. The frequency is changed by adding SSA[1-0] range to actual POSCVTRM[7-0].
SSA[1-0] = 11, +/- 125
SSA[1-0] = 10, +/- 64
SSA[1-0] = 01, +/- 32
SSA[1-0] = 00, +/- 16

POSCVTRM (0x4001_00FE) POSC Fine Trim Register R/W (0x80)

	7	6	5	4	3	2	1	0
RD	POSCVTRM[7-0]							
WR	POSCVTRM[7-0]							

This register provides fine trimming of the POSC frequency. The higher the value of POSCVTRM, the lower the frequency is.

POSCPDIV (0x4001_00FF) POSC Post Divider Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	-		ITRM[2-0]					
WR	-		ITRM[2-0]					

ITRM[2-0] ITRM[2-0] is the coarse trimming of the POSC.

The manufacturer trim value is stored in IFB and is trimmed to 16MHz/32MHz. The user program provides the freedom to set the POSC at a preferred frequency as long as the program is able to calibrate the frequency. Once set, the POSC frequency has accuracy deviation within +/- 2% over the operation conditions. The following lists the range of the POSC frequency for each trimming setting.

ITRM[2-0] = 2'b111 , POSCCLK =36.7---48.53MHz

ITRM[2-0] = 2'b110 , POSCCLK =31.86---42.08MHz

ITRM[2-0] = 2'b101 , POSCCLK =26.8---35.51MHz

ITRM[2-0] = 2'b100 , POSCCLK =21.57---28.71MHz

ITRM[2-0] = 2'b011 , POSCCLK =25.05---33.22MHz

ITRM[2-0] = 2'b010 , POSCCLK =19.76---26.35MHz

ITRM[2-0] = 2'b001 , POSCCLK =14.24---19.1MHz

ITRM[2-0] = 2'b000 , POSCCLK =8.43---11.38MHz

13. I²C Master (I2CM)

The I²C master controller provides the interface to an I²C slave. It can be programmed to operate with arbitration and clock synchronization to allow for multi-master configurations. The master uses SCL and SDA pins. The controller contains a built-in 8-bit timer to allow for various I²C bus speeds. The maximum I²C bus speed is limited to SYSCLK/12.

I2CMTP (0x4000_6000) I²C Master Time Period R/W (0x01)

	7	6	5	4	3	2	1	0
RD	I2CMTP[7-0]							
WR	I2CMTP[7-0]							

I2CMTP — I²C Clock Speed Setting.
This register set the period time of I²C bus clock – SCL. The SCL period time is set according to
SCLPERIOD = 8 * (1 + I2*CMTP) * CPUCLK_PERIORD

I2CMSA (0x4000_6004) I²C Master Slave Address R/W (0x00)

	7	6	5	4	3	2	1	0
RD	SA[6-0]							RS
WR	SA[6-0]							RS

SA[6-0] — Slave Address.
SA[6-0] defines the slave address the I²C master uses to communicate.

RS — Receive/Send Bit.
RS determines if the following operation is to RECEIVE (RS=1) or SEND (RS=0).

I2CMBUF (0x4000_6008) I²C Master Data Buffer Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	RD[7-0]							
WR	TD[7-0]							

I2CMBUF functions as a transmit-data register when written and as a receive data register when read. When written, TD is sent to the bus by the next SEND or BURST SEND operations. TD[7] is sent first. When read, RD contains the 8-bit data received from the bus upon the last RECEIVE or BURST RECEIVE operation.

I2CMCR (0x4000_600C) I²C Master Control and Status Register R/W (0x20)

	7	6	5	4	3	2	1	0
RD	-	BUSBUSY	IDLE	ARBLOST	DACKERR	AACKERR	ERROR	BUSY
WR	CLEAR	INFILEN	-	-	ACK	STOP	START	RUN

The I2CMCR register is used for setting control when it is written, and as a status signal when read.

CLEAR — Clear I2CM state machine.
Writing 1 to CLEAR, clears the state machine and also clears I2CMINT flags.

BUSBUSY — This bit indicates that the external I²C bus is busy and access to the bus is not possible. This bit is set/reset by START and STOP conditions.

INFILEN — Input Noise Filter Enable. When IFILEN is set, pulses shorter than 50 nsec on inputs of SDA and SCL are filtered out.

IDLE — This bit indicates that I²C master is in the IDLE mode.

ARBLOST — This bit is automatically set when the last operation I²C master controller loses the bus arbitration.

DACKERR — This bit is automatically set when the last operation transmitted data is not acknowledged.

AACKERR — This bit is automatically set when the last operation slave address transmitted is not acknowledged.

ERROR — This bit indicates that an error occurs in the last operation. The errors include slave address was not acknowledged, or transmitted data is not acknowledged, or the master controller loses arbitration.

BUSY — This bit indicates that I²C master is receiving or transmitting data, and other status bits are not valid.

START, STOP, RUN and HS, RS, ACK bits are used to drive the I²C Master to initiate and terminate a transaction. The Start bit generates a START, or REPEAT START protocol. The Stop bit determines if the cycle stops at the end of the data cycle or continues to burst. To generate a single read cycle, the designated address is written in the SA register, RS is set to 1, ACK=0, STOP=1, START=1, RUN=1 are set in the I2CMCR register to perform the operation then STOP. When the operation is completed (or aborted due to errors), the I²C master generates an interrupt. The ACK bit must be set to a logic 1. This causes the controller to send an ACK automatically after each byte transaction. The ACK bit must be reset to a logic 0 when the master operates in receive mode and can not receive further data from the slaves. The following table lists the permitted control bits combinations in master IDLE mode.

RS	ACK	STOP	START	RUN	Operations
0	-	0	1	1	START condition followed by SEND. Master remains in TRANSMITTER mode
0	-	1	1	1	START condition followed by SEND and STOP
1	0	0	1	1	START condition followed by RECEIVE operation with negative ACK. Master remains in RECEIVER mode
1	0	1	1	1	START condition followed by RECEIVE and STOP
1	1	0	1	1	START condition followed by RECEIVE. Master remains in RECEIVER mode
1	1	1	1	1	Illegal command
0	0	0	0	1	Master Code sending and switching to HS mode

The following table lists the permitted control bits combinations in master TRANSMITTER mode.

RS	ACK	STOP	START	RUN	Operations
-	-	0	0	1	SEND operation. Master remains in TRANSMITTER mode
-	-	1	0	0	STOP condition
-	-	1	0	1	SEND followed by STOP condition
0	-	0	1	1	REPEAT START condition followed by SEND. Master remains in TRANSMITTER mode
1	-	1	1	1	REPEAT START condition followed by SEND and STOP condition
1	0	0	1	1	REPEAT START condition followed by RECEIVE operation with negative ACK. Master remains in TRANSMITTER mode
1	0	1	1	1	REPEAT START condition followed by SEND and STOP condition.
1	1	0	1	1	REPEAT START condition followed by RECEIVE. Master remains in RECEIVER mode.
1	1	1	1	1	Illegal command

The following table lists the permitted control bits combinations in master RECEIVER mode.

RS	ACK	STOP	START	RUN	Operations
-	0	0	0	1	RECEIVE operation with negative ACK. Master remains in RECEIVE mode
-	-	1	0	0	STOP condition
-	0	1	0	1	RECEIVE followed by STOP condition
-	1	0	0	1	RECEIVE operation. Master remains in RECEIVER mode
-	1	1	0	1	Illegal command
1	0	0	1	1	REPEAT START condition followed by RECEIVE operation with negative ACK. Master remains in RECEIVER mode
1	0	1	1	1	REPEAT START condition followed by RECEIVE and STOP conditions
1	0	1	1	1	REPEAT START condition followed by RECEIVE. Master remains in RECEIVER mode

RS	ACK	STOP	START	RUN	Operations
0	-	0	1	1	REPEAT START condition followed by SEND. Master remains in TRANSMITTER mode.
0	-	1	1	1	REPEAT START condition followed by SEND and STOP conditions.

All other control-bit combinations not included in the three tables above are NOP. In Master RECEIVER mode, STOP should be generated only after data negative ACK is executed by the Master or the address negative ACK executed by the slave. Negative ACK means that SDA is pulled low when the acknowledge clock pulse is generated.

I2CMTO0 (0x4000_6010) I²C Time Out Control Register 0 R/W (0x00)

	7	6	5	4	3	2	1	0
RD	I2CMTO[7-0]							
WR	I2CMTO[7-0]							

I2CMTO[7-0] I2CM Time Out Setting

I2CMTO1 (0x4000_6011) I²C Time Out Control Register 1 R/W (0x00)

	7	6	5	4	3	2	1	0
RD	I2CMTOEN	I2CMTO[14-8]						
WR	I2CMTOEN	I2CMTO[14-8]						

I2CMTOEN I2CM Time Out Enable

I2CMTO[14-8] I2CM Time Out Setting
The TO time is set to (I2CMTO[14-0]+1)*2*SCLPERIOD. When time out occurs, an I2CM interrupt will be generated.

I2CMINT (0x4000_6014) I²C Master Interrupt Control R/W (0x00)

	7	6	5	4	3	2	1	0
RD	-						I2CMTOF	I2CMINTF
WR	-						-	I2CMINTF

I2CMTOF I2CM Time Out Flag
This bit is set when a time out occurs. It is cleared when I2MINTF is cleared, or I2CMCR(CLEAR) command is issued.

I2CMINTF I2CM Interrupt Flag
This bit is set by hardware when I2CM interrupt occurs. This bit is cleared by software writing 1 or I2CMCR(CLEAR) command is issued.

14. I²C Slave Controller (I2CS1)

The I²C Slave Controller 1 features enhanced functions such as clock-stretching and a programmable hold time. These enhancements provided improvements. I2CS1 can be configured to respond to two I²C addresses, – I2CADR1 and I2CADR2. These ~~two~~ addresses can be enabled separately. In addition, I2CS1 can be configured as a wakeup source in sleep mode when an address match occurs.

In receive mode, the controller detects a valid matched address and issues an ADDRMI interrupt. Simultaneously, the data bit on the SDA line is shifted into the receive buffer. The RCBI interrupt is generated when a byte is received and is ready to be read from I2CSDAT. If the software does not respond to the RCBI interrupt in time (i.e. RCBI is not cleared), and a new byte is received, and the controller either forces an NACK response on I²C (if CLKSTREN bit is not set) or by pulling and holding SDA low (if CLKSTREN bit is set) to stretch the SCL low duration to force the master into a wait state. In clock stretching mode, SCL is released when the software responds to RCBI interrupt and cleared RCBI flag.

In transmit mode, the controller detects a valid matched address and issues an ADDRMI interrupt. At the same time, the data is preloaded into the transmit data register through I2CSDAT is transferred to the transmit shift register and is serially shifted out onto the SDA line. When this occurs, the controller generates a TXBI interrupt to inform the software that a new byte can be written into I2CSDAT. When the shift register is empty and ready for the next transmit, the slave controller checks if the new byte is written to I2CSDAT. If TXBI is not cleared, it indicates no new data, and the slave controller holds the SCL line to a logic 0 to stretch the current clock cycle if CLKSTREN is set. If the clock stretching is not enabled, the slave controller takes the old byte into the shift register and replies with NACK, thus causing a data corruption. On the other hand, if the master returns the NACK after the byte transfer, this indicates the end of data to the I²C slave. In this case, the I²C slave releases the data line to allow for the master to generate a STOP or REPEAT START.

I2CS1CONA (0x4000_6100) I2CS1 Configuration Register A R/W (0x00)

	7	6	5	4	3	2	1	0
RD	EADRWK	EADDRMI	ESTOPI	ERPSTARTI	ETXBI	ERCBI	CLKSTREN	EACKWK
WR	EADRWK	EADDRMI	ESTOPI	ERPSTARTI	ETXBI	ERCBI	CLKSTREN	EACKWK

EADRWK — Enable Address matched wakeup from sleep mode.

EADDRMI — ADDRMI Interrupt Enable bit.
Set this bit to set ADDRMI interrupt as the I²C slave interrupt. This interrupt is generated when I²C slave received a matching address.

ESTOPI — STOPI Interrupt Enable bit.
Set this bit to set STOPI interrupt as the I²C slave interrupt.

ERPSTARTI — RPTSTARTI Interrupt Enable Bit.
Set this bit to set RPTSTARTI interrupt as the I²C slave interrupt.

ETXBI — TXBI Interrupt Enable bit.
Set this bit to allow TXBI interrupt as the I²C slave interrupt.

ERCBI — RCBI Interrupt Enable bit.
Set this bit to allow RCBI interrupt as the I²C slave interrupt.

CLKSTREN — Clock Stretching Enable bit.
Set to enable the clock stretching function of the slave controller. Clock stretching is an optional feature defined in I²C specification.
If the clock stretching option is enabled (for slave I²C), the data written into transmit buffer is shifted out only after the occurrence of clock stretching, and the data cannot be loaded to transmit shift register. The programmer must write the same data again to the transmit buffer.

EACKWK — 1: Enable clock stretching during system wakeup from sleep and wait until system wakeup completed and asks controller send ACK to master.
0: controller send NACK when address matched

I2CS1CONB (0x4000_6104) I2CS1 Configuration Register B R/W (0x00)

	7	6	5	4	3	2	1	0
RD	STRTOF	SADR2M	XMT	START	SDAFLT[1-0]		GDFLT[1-0]	
WR	I2CSRST	-	-	-	SDAFLT[1-0]		GDFLT[1-0]	

STRTOF — Clock Stretch Time Out Flag
STRTOF is set to 1 by hardware when clock stretch exceeds STRTO setting.
STRTOF can be cleared only by I2CRST.

I2CSRST	I²C Slave Reset bit. Set this bit causes the Slave Controller to reset all internal state machine. Auto clear by controller.
SARD2M	Slave Address Match Flag bit. This bit is meaningful only when SDDRMI is set. SARD2M=0 indicates the received I²C address matches with I2CSADR1. SARD2M=1 indicates the received I²C address matches with I2CSADR2. This bit is cleared when ADDRMI is cleared.
XMT	This bit is set by the controller when the I²C slave is in transmit operation. This bit is cleared when the I²C slave controller is in receive operation.
START	Start Condition. This bit is set when the slave controller detects a START condition on the SCL and SDA lines. This bit is not very useful as the start of transaction can be indicated by address match interrupt. This read-only bit is cleared when STOP condition is detected.
SDAFLT[1-0]	Delay filter for SDA input 0: 10ns RC filter delay 1: 20ns RC filter delay 2: 20ns RC filter delay 3: 30ns RC filter delay
GDFLT[1-0]	Global delay filter for SCL and SDA input 0: 10ns RC filter delay 1: 20ns RC filter delay 2: 20ns RC filter delay 3: 30ns RC filter delay

I2CS1ST (0x4000_6108) I2CS1 Status Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	ADRWKF	ADDRMI	STOPI	RPSTARTI	TXBI	RCBI	FIRSTBT	NACK
WR	CLRWKF	CLRADMI	CLRSTOPI	CLRRPSTI	-	-	-	CLRNACK

ADRWKF	Address Matched Wakeup Flag This bit is set by hardware when wakeup by address match during sleep mode or address match in normal mode.
CLRWKF	Clear Address Matched Wakeup Flag (ADRWKF)
ADDRMI	Slave Address Match Interrupt Flag bit. This bit is set when the received address matches the address defined in I2CSADR1. If EADDMI is set, this generates an interrupt. This bit must be cleared by software.
STOPI	Stop Condition Interrupt Flag bit. This bit is set when the slave controller detects a STOP condition on the SCL and SDA lines. This bit must be cleared by software.
RPTSARTI	Repeat Start Condition Interrupt Flag bit. This bit is set when the slave controller detects a REPEAT START condition on the SCL and SDA lines. This bit must be cleared by software.
TXBI	Transmit Buffer Interrupt Flag. This bit is set when the slave controller is ready to accept a new byte for transmission. This bit is cleared when new data is written into I2CSDAT register.
RCBI	Receiver Buffer Interrupt Flag bit. This bit is set when the slave controller puts new data in the I2CSDAT and ready for software reading. This bit is cleared after the software reads I2CSDAT.
FIRSTBT	This bit is set to indicate the data in the data register as the first byte received after address match. This bit is cleared after the second byte received. The bit is read only and generated by the slave controller.
NACK	NACK Condition bit. This bit is set when the host responds with NACK in the byte transaction. This bit is only meaningful for slave-transmit operation. Please note if the master returns with NACK on the byte transaction, the slave will release bus for following continuing transaction until STOP or RESTART condition is detected. This bit is cleared when a new ACK is detected or it can be cleared by software.

I2CS1ADR1 (0x4000_610C) I2CS1 1st Slave Address Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	I2CSEN1	RXADDR[6-0]						
WR	I2CSEN1	ADDRA1[6-0]						

I2CSEN1 Set this bit to enable the I²C slave controller and ADDRA1[6-0] for address matching.
Please note either I2CSEN1 or I2CEN2 is 1 will enable I2CS.

RXADDR Received slaved address

ADDRA1[6-0] 7-bit slave address.

I2CS1DAT (0x4000_6110) I2CS1 Data Register R/W (0xFF)

	7	6	5	4	3	2	1	0
RD	I²C Slave Receive Data Register							
WR	I²C Slave Transmit Data Register							

I2CS1ADR2 (0x4000_6114) I2CS1 2nd Slave Address Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	I2CSEN2	ADDRA2[6-0]						
WR	I2CSEN2	ADDRA2[6-0]						

I2CSEN2 Set this bit to enable the I²C slave controller and ADDRA2[6-0] for address matching
Please note either I2CSEN1 or I2CEN2 is 1 will enable I2CS.

ADDRA2[6-0] 7-bit slave address.

I2CS1STO (0x4000_6118) Stretch Time Out Register R/W (0xFF)

	7	6	5	4	3	2	1	0
RD	STRTO[7-0]							
WR	STRTO[7-0]							

STRTO[7-0] Clock Stretch Time Out Setting
To prevent extended clock stretching duration interferes with normal I²C bus operation, a time out mechanism is implemented. When time out occurs, an interrupt is generated and STRTOF bit is set. Since this is an adverse and dire situation, I2CRST must be done to resume I2CS operation. The time out setting is SOSC32K/4 * STRTO[7-0].
Please note STRTO should be set longer than REGRDY delay to prevent error when address matching wakeup is used.

14.1 Clock Stretch

Clock stretching is used to allow a slow I²C slave to hold the transaction from the master by driving SCL low after ACK bit and before the start of 1st bit of next byte. In another word, the SCL is driven low by the slave after it sees SCL is driven low by the host at ACK field. The maximum delay the slave can stretch does not have a limit but should be limited to 35ms if SMBus conformance is required. Clock stretching has an impact on the slave response and behaves differently for host read or host write. The diagram below illustrates clock stretching disable and enable.

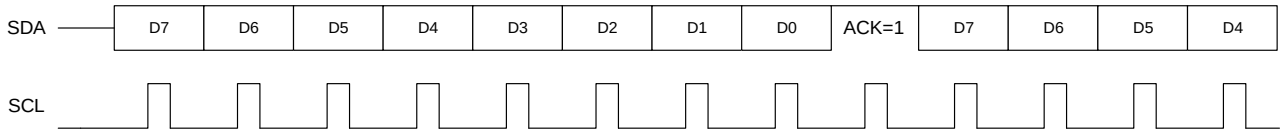


Figure 14-1 I²C without lock stretch

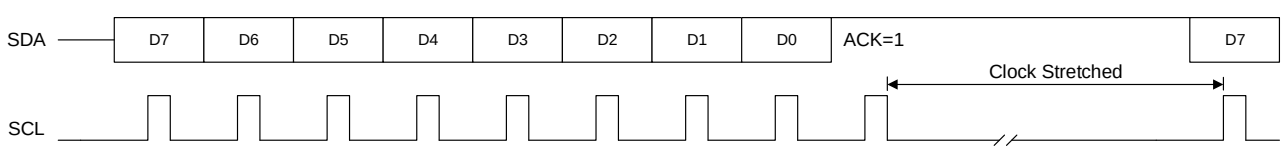


Figure 14-2 I²C with clock stretch

For a host write, the address byte is always responded with ACK=1. The data byte will respond with ACK=1 if the data buffer is empty. If the data buffer is not empty, I2CS1 will respond with ACK=0 (NACK), if clock stretching is disabled. If clock stretching is enabled, after responds with ACK=1, I2CS1 will pull SCL low to facilitate clock stretching. The software needs to read out the data buffer, and I2CS1 then releases SCL for the host to continue.

For a host read, the address byte is responded with ACK=1 if the data buffer is ready. If however the data buffer is not ready and clock stretching is not enabled, then ACK=0 is responded. If clock stretching is enabled, ACK=1 is responded but clock stretching is commenced by I2CS1 until the data buffer is written to by the software. Similar action is taken for the data transaction that ACD=1 is first responded with clock stretching.

15. EUART1

EUART1 is an enhanced UART controller (EUART) with separate transmit and receive FIFO. Both transmit and receive FIFO are 15-bytes deep and can be parameterized for interrupt triggers. The addition of FIFO significantly reduces CPU load which allows for high-speed serial interface. Transmit FIFO and receive FIFO have respective interrupt trigger levels that can be set based on optimal CPU performance adjustment. EUART also has a dedicated 16-bit Baud Rate generator and provides accurate baud rates allowing for a wide range of system clock frequencies. The following registers are used for the configurations EUART1.

SCON1A (0x4000_7100) EUART1 Configuration Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	EUARTEN	SB	WLS[1-0]		BREAK	OP	PERR	SP
WR	EUARTEN	SB	WLS[1-0]		BREAK	OP	PE	SP

EUARTEN — Transmit and Receive Enable bit
Set to enable EUART1 transmit and receive functions: To transmit messages in the TX FIFO and to store received messages in the RX FIFO.

SB — Stop Bit Control
Set to enable 2 Stop bits, and clear to enable 1 Stop bit.

WLS[1-0] — The number of bits of a data byte. This does not include the parity bit when parity is enabled.
00 - 9 bits
01 - 6 bits
10 - 7 bits
11 - 8 bits

BREAK — Start Sending BREAK and followed by SYNC byte.
Set to initiate a break condition on the EUART interface by holding EUART output at low for duration of BRKLEN, and then followed by a SYNC byte (if BRKSYNC=1).
When read, 1 indicates it is still ongoing. It is self-cleared by hardware when completed.
At completion, it also generates an EUART1 interrupt.
Software can start putting data into TX FIFO. The data will start transmission after SYNC byte is transmitted.

OP — Odd/Even Parity Control Bit

PE/PERR — Parity Enable / Parity Error status.
Set to enable parity and clear to disable parity checking functions. If read, PERR=1 indicates a parity error in the current data of RX FIFO.

SP — Parity Set Control Bit.
When SP is set, the parity bit is always transmitted as 1.

SCON1B (0x4000_7101) EUART1 Configuration Register B R/W (0x00)

	7	6	5	4	3	2	1	0
RD	RXST	BITERR	BECLRX	BECLRR	LBKEN	BERIE	-	TXPOL
WR	-	BITERR	BECLRX	BECLRR	LBKEN	BERIE	CLRFIFO	TXPOL

RXST — Receive Status
RXST controlled by hardware. RXST is set by hardware when a START bit is detected. It is cleared when STOP condition is detected.

BITERR — Bit Error Flag
BITERR is set by hardware when received bit does not match with transmit bit, if BERIE=1, then this error generates an interrupt. BITERR must be cleared by software. Write 1 to clear.

BECLRX — Bit Error Force Clear Transmit Enable
If BECLRX=1, when BITERR is set by hardware, hardware also immediately disables current transmission and clears TX state machines and FIFO.

BECLRR — Bit Error Force Clear RECEIVE Enable
If BECLRX=1, when BITERR is set by hardware, hardware also immediately disables current reception and clears RX state machines and FIFO.

LBKEN — Enable EUART Loopback Test,

When LBKEN=1, EUART1 enters loopback mode, with its TX output connected to RX input. When in loopback mode, to prevent the TX output to pin, corresponding MFCFG bit must be cleared.

BERIE — Bit Error Interrupt Enable (1:Enable / 0:Disable)

CLRFIFO — Set to clear transmit/received FIFO pointer and state machine. CLRFIFO bit is auto clear by hardware.

TXPOL — EUART output polarity

SCON1C (0x4000_7102) EUART1 Configuration Register C R/W (0x00)

	7	6	5	4	3	2	1	0
RD	DMATXEN	DMARXEN	-	-			RCVSPL[1-0]	
WR	DMATXEN	DMARXEN	CLRRX	CLRTX			RCVSPL[1-0]	

DMATXEN — Enable DMA function in EUART TX direction

DMARXEN — Enable DMA function in EUART RX direction

CLRRX — Clear RX FIFO pointer and RX bit-error

CLRTX — Clear TX FIFO pointer and TX bit-error

RCVSPL[1-0] — Adjust Receive Sampling Point
00 = 50%
01 = 62.5%
10 = 69%
11 = 75%

SCON1D (0x4000_7103) EUART1 Configuration Register DR/W (0x01)

	7	6	5	4	3	2	1	0
RD	BRKIEN	BRKBR[2-0]			BRKF	BRKSYNC	BRKLEN[1-0]	
WR	BRKIEN	BRKBR[2-0]			BRKF	BRKSYNC	BRKLEN[1-0]	

BRKIEN — BREAK Completion Interrupt Enable
BRKIEN=1 enables EUART1 interrupt when BRK/SYNC transmission is completed

BRKBR[2-0] — Break Field Baud Rate
Break Baud rate is based on BR.
000 = BR
001 = BR/2
010 = BR/4
011 = BR/8
100 = BR/16
101 = BR/64
110 = BR/128
111 = BR/256

BRKF — BREAK Completion Flag
BRKF is set by hardware when BRK/SYNC transmission completes. It must be cleared by software.

BRKSYNC — Send SYNC after Break
If BRKSYNC=0, then only the Break field is sent.
If BRKSYNC=1, then after Break field, a SYNC byte is also sent.

BRKLEN[1-0] — BREAK Length Setting
00 = 13 BT
01 = 14 BT
10 = 15 BT
11 = 16 BT

SBAUD1 (0x4000_7104) EUART1 Baud Rate Register RW (0x00XX0000)

	31-24	23-16	15-0
RD	BRCS[7-0]	-	BR[15-0]
WR	BRCS[7-0]	-	BR[15-0]

BRCS[7-0] — Baud Rate Pre-Scaler

BR[15-0] — The Baud Rate Setting of EUART.

BUAD RATE = SYSCLK/(BRCS[7-0]+1)/(BR[15-0]+1).

SFIFO1 (0x4000_7108) EUART1 FIFO Status/Control Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	RFL[3-0]				TFL[3-0]			
WR	RFLT[3-0]				TFLT[3-0]			

RFL[3-0] Current Receive FIFO level. This is read only and indicate the current receive FIFO byte count.

RFLT[3-0] Receive FIFO trigger threshold. This is write-only. RDA interrupt will be generated when RFL[3-0] is greater than RFLT[3-0].

RFLT[3-0]	Description
0000	RX FIFO trigger level = 0
0001	RX FIFO trigger level = 1
0010	RX FIFO trigger level = 2
0011	RX FIFO trigger level = 3
0100	RX FIFO trigger level = 4
0101	RX FIFO trigger level = 5
0110	RX FIFO trigger level = 6
0111	RX FIFO trigger level = 7
1000	RX FIFO trigger level = 8
1001	RX FIFO trigger level = 9
1010	RX FIFO trigger level = 10
1011	RX FIFO trigger level = 11
1100	RX FIFO trigger level = 12
1101	RX FIFO trigger level = 13
1110	RX FIFO trigger level = 14
1111	NA

TFL[3-0] Current Transmit FIFO level. This is read only and indicate the current transmit FIFO byte count.

TFLT[3-0] Transmit FIFO trigger threshold. This is write-only. TRA interrupt will be generated when TFL[3-0] is less than TFLT[3-0].

TFLT[3-0]	Description
0000	NA
0001	TX FIFO trigger level = 1
0010	TX FIFO trigger level = 2
0011	TX FIFO trigger level = 3
0100	TX FIFO trigger level = 4
0101	TX FIFO trigger level = 5
0110	TX FIFO trigger level = 6
0111	TX FIFO trigger level = 7
1000	TX FIFO trigger level = 8
1001	TX FIFO trigger level = 9
1010	TX FIFO trigger level = 10
1011	TX FIFO trigger level = 11
1100	TX FIFO trigger level = 12

TFLT[3-0]	Description
1101	TX FIFO trigger level = 13
1110	TX FIFO trigger level = 14
1111	TX FIFO trigger level = 15

Receive and transmit FIFO pointers can be reset by clear TX/RX FIFO operation.

SINT1L (0x4000_710C) EUART1 Interrupt Enable Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	INTEN	TRAEN	RDAEN	RFOEN	RFUEN	TFOEN	FERREN	TIEN
WR	INTEN	TRAEN	RDAEN	RFOEN	RFUEN	TFOEN	FERREN	TIEN

INTEN — Interrupt Enable
Set to enable EUART1 interrupt. Clear to disable interrupt. Default is 0.

TRAEN — Transmit FIFO Ready Interrupt Enable.

RDAEN — Receive FIFO Ready Interrupt Enable.

RFOEN — Receive FIFO Overflow interrupt Enable.

RFUEN — Receive FIFO Underflow Interrupt Enable

TFOEN — Transmit FIFO Overflow Interrupt Enable

FERREN — Framing Error Interrupt Enable

TIEN — Transmit Message Completion Interrupt Enable

SINT1H (0x4000_710D) EUART1 Interrupt Status Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	-	TRA	RDA	RFO	RFU	TFO	FERR	TI
WR	-	TRA	RDA	RFO	RFU	TFO	FERR	TI

TRA — Transmit FIFO Ready Flag
This bit is set when transmit FIFO has been emptied below FIFO threshold.
The flag is cleared by software writing “1”.

RDA — Receive FIFO Ready Flag.
This bit is set by hardware when receive FIFO exceeds the FIFO threshold. RDA will also be set when RFL < RFLT for bus idle duration longer than RFLT * 16 * Baud Rate. This is to inform software that there are remaining unread received bytes in the FIFO.
The flag is cleared by software writing “1”.

RFO — Receive FIFO Overflow Flag
This bit is set when overflow condition of receive FIFO occurs.
The flag is cleared by software writing “1” or by FIFO reset action.

RFU — Receive FIFO Underflow Flag
This bit is set when underflow condition of receive FIFO occurs.
The flag is cleared by software writing “1” or by FIFO reset action.

TFO — Transmit FIFO Overflow Flag
This bit is set when overflow condition of transmit FIFO occurs.
The flag is cleared by software writing “1” or by FIFO reset action.

FERR — Framing Error Flag.
This bit is set when framing error occurs as the byte is received.
The flag is cleared by software writing “1”.

TI — Transmit Message Completion Flag
This bit is set when all messages in the TX FIFO are transmitted and thus the TX FIFO becomes empty.
The flag is cleared by software writing “1”

SBUF1L (0x4000_7110) EUART1 Data Buffer Low Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	EUART1 Receive Data Register RXDATA[7-0]							
WR	EUART1 Transmit Data Register TXDATA[7-0]							

SBUF1H (0x4000_7111) EUART1 Data Buffer High Register R/W (0x00)

	15	14	13	12	11	10	9	8
RD	-	-	-	-	-	-	-	RXDATA[8]
WR	-	-	-	-	-	-	-	TXDATA[8]

This register is the virtual data buffer register for both receive and transmit FIFO. When being read, it reads out the top byte of the RX FIFO; when being written, it writes into the top byte of the TX FIFO. Write TXDATA[7-0] cause FIFO write-point +1 and any read on SBUF cause read-point +1, so word or half-word read for 9bit mode only.

DMACFGA (0x4000_7120) EUART1 DMA Configuration Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	DMATX0BY	DMATX1BY	DMARX0BY	DMARX1BY	-	-	-	-
WR	DMATX0UP	DMATX1UP	DMARX0UP	DMARX1UP	-	-	DMATXRST	DMARXRST

DMATX0BY	Busy status for DMA TX0 channel
DMATX0UP	Update the DMA counter and address configuration for TX0 channel.
DMATX1BY	Busy status for DMA TX1 channel
DMATX1UP	Update the DMA counter and address configuration for TX1 channel.
DMARX0BY	Busy status for DMA RX0 channel
DMARX0UP	Update the DMA counter and address configuration for RX0 channel.
DMARX1BY	Busy status for DMA RX1 channel
DMARX1UP	Update the DMA counter and address configuration for RX1 channel.
DMATXRST	Reset the DMA TX address pointer to DMATXADR0
DMARXRST	Reset the DMA RX address pointer to DMARXADR0

DMACFGB (0x4000_7121) EUART1 DMA Configuration Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD					TX0INTEN	TX1INTEN	RX0INTEN	RX1INTEN
WR					TX0INTEN	TX1INTEN	RX0INTEN	RX1INTEN

TX0INTEN	Enable DMA interrupt for DMA TX0 channel.
TX1INTEN	Enable DMA interrupt for DMA TX1 channel.
RX0INTEN	Enable DMA interrupt for DMA RX0 channel.
RX1INTEN	Enable DMA interrupt for DMA RX1 channel.

DMASTAT (0x4000_7122) EUART1 DMA Status Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD					TX0INTST	TX1INTST	RX0INTST	RX1INTST
WR					TX0INTCL	TX1INTCL	RX0INTCL	RX1INTCL

TX0INTST	Status of DMA TX0 channel interrupt
TX0INTCL	Clear the DMA TX0 channel interrupt status.
TX1INTST	Status of DMA TX1 channel interrupt
TX1INTCL	Clear the DMA TX1 channel interrupt status.
RX0INTST	Status of DMA RX0 channel interrupt
RX0INTCL	Clear the DMA RX0 channel interrupt status.
RX1INTST	Status of DMA RX1 channel interrupt
RX1INTCL	Clear the DMA RX1 channel interrupt status.

DMATXADR0 (0x4000_7124) EUART1 DMA TX Address 0 Register R/W (0x00)

	15-0
RD	DMATXADR0
WR	DMATXADR0

DMATXADR1 (0x4000_7128) EUART1 DMA TX Address 1 Register R/W (0x0000)

	15-0
RD	DMATXADR1
WR	DMATXADR1

DMARXADR0 (0x4000_712C) EUART1 DMA RX Address 0 Register R/W (0x0000)

	15-0
RD	DMARXADR0
WR	DMARXADR0

DMARXADR1 (0x4000_7130) EUART1 DMA RX Address 1 Register R/W (0x0000)

	15-0
RD	DMARXADR1
WR	DMARXADR1

DMATXCNT (0x4000_7134) EUART1 DMA TX Counter Register R/W (0x00000000)

	31-16	15-0
RD	TXCNTR1	TXCNTR0
WR	TXCNTW1	TXCNTW0

DMARXCNT (0x4000_7138) EUART1 DMA RX Counter Register R/W (0x00000000)

	31-16	15-0
RD	RXCNTR1	RXCNTR0
WR	RXCNTW1	RXCNTW0

16. EUART2 with LIN Controller (EUART2)

The IS3XC9310 features a LIN-capable 16550-like EUART2 as an enhanced UART controller (EUART) featuring separate transmit and receive FIFOs. Both the transmit and receive FIFOs are 15-bytes deep and can be parameterized for interrupt triggering. The addition of FIFOs significantly reduces CPU load allowing the a high-speed serial interface. The Transmit and receive FIFOs have respective interrupt trigger levels that can be set based on CPU utilizations. The EUART also has a dedicated 16-bit Baud Rate generator and that provides accurate baud rate under wide range of system clock frequencies. The EUART2 also provides LIN extensions that incorporate message handling and baud-rate synchronization. The block diagram of EUART2 is shown in the following.

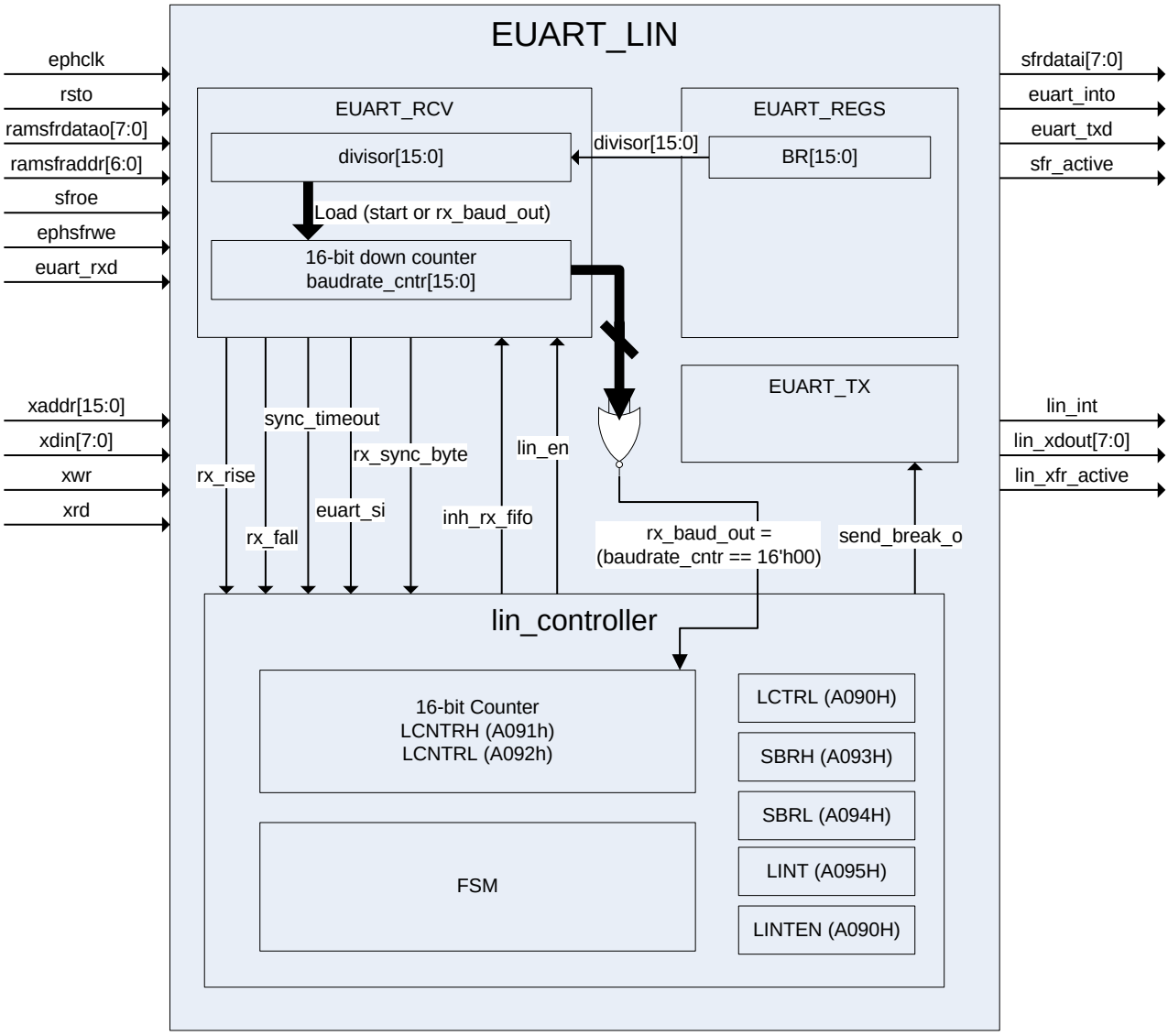


Figure 16-1 EUART2 Block Diagram

SCON2A (0x4000_7200) EUART2 Configuration Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	EUARTEN	SB	WLS[1-0]		BREAK	OP	PERR	SP
WR	EUARTEN	SB	WLS[1-0]		BREAK	OP	PE	SP

EUARTEN — Transmit and Receive Enable bit
Set to enable EUART2 transmit and receive functions: To transmit messages in the TX FIFO and to store received messages in the RX FIFO.

SB — Stop Bit Control
Set to enable 2 Stop bits, and clear to enable 1 Stop bit.

WLS[1-0] — The number of bits of a data byte. This does not include the parity bit when parity is enabled.

00 - 9 bits
01 - 6 bits
10 - 7 bits
11 - 8 bits

BREAK — BREAK Condition Control Bit.
Set to initiate a break condition on the UART interface by holding UART output at low until BREAK bit is cleared.

OP — Odd/Even Parity Control Bit

PE/PERR — Parity Enable / Parity Error status.
Set to enable parity and clear to disable parity checking functions. If read, PERR=1 indicates a parity error in the current data of RX FIFO.

SP — Parity Set Control Bit
When SP is set, the parity bit is always transmitted as 1.

SCON2C (0x4000_7202) EUART2 Interrupt Status/Enable Register R/W (0x000000)

	15	14	13	12	11	10	9	8
RD	-	-	-	-	-	-	RCVSPL[1-0]	
WR	-	-	-	-	-	-	RCVSPL[1-0]	

RCVSPL[1-0] — Adjust Receive Sampling Point
00 = 50%
01 = 62.5%
10 = 69%
11 = 75%

SBAUD2 (0x4000_7204) EUART2 Baud Rate Register RW (0x00000000)

	31-24	23-16	15-0
RD	BRCS[7-0]	-	SBR[15-0]
WR	BRCS[7-0]	-	BR[15-0]

BRCS[7-0] — Baud Rate Pre-Scaler.

SBR[15-0] — The acquired Baud Rate under LIN protocol. This is read-only.
SBR[15-0] is the acquired baud rate from last received valid sync byte. SBR is meaningful only in LIN-Slave mode. The actual baud rate acquired is SYSCLK/(SRB[15=0]+1). If not in LIN-Slave mode, SBR[15-0] is valid only in LIN-Slave mode.

BR[15-0] — The Baud Rate Setting of EUART.
BUAD RATE = SYSCLK/(BR[15-0]+1).
When a slave receives a BREAK followed by a valid SYNC field, an RSI interrupt is generated and the acquired baud rate from SYNC field is stored in SBR[15-0]. The acquired baud rate is BAUD RATE = SYSCLK/(SBR[15-0]+1). The software can just update this acquired value SBR[15-0] into BR[15-0] to achieve synchronization with the master. If Auto-Sync Update (ASU) register bit is enabled under LIN slave mode, LIN controller will automatically perform the update of BR[15-0] with SBR[15-0] and issue another ASUI interrupt when received a valid SYNC field.

SFIFO2 (0x4000_7208) EUART2 FIFO Status/Control Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	RFL[3-0]				TFL[3-0]			
WR	RFLT[3-0]				TFLT[3-0]			

RFL[3-0] — Current Receive FIFO level. This is read only and indicate the current receive FIFO byte count.

RFLT[3-0] — Receive FIFO trigger threshold. This is write-only. RDA interrupt will be generated when RFL[3-0] is greater than RFLT[3-0].

RFLT[3-0]	Description
0000	RX FIFO trigger level = 0
0001	RX FIFO trigger level = 1

RFLT[3-0]	Description
0010	RX FIFO trigger level = 2
0011	RX FIFO trigger level = 3
0100	RX FIFO trigger level = 4
0101	RX FIFO trigger level = 5
0110	RX FIFO trigger level = 6
0111	RX FIFO trigger level = 7
1000	RX FIFO trigger level = 8
1001	RX FIFO trigger level = 9
1010	RX FIFO trigger level = 10
1011	RX FIFO trigger level = 11
1100	RX FIFO trigger level = 12
1101	RX FIFO trigger level = 13
1110	RX FIFO trigger level = 14
1111	NA

TFL[3-0] Current Transmit FIFO level. This is read only and indicate the current transmit FIFO byte count.

TFLT[3-0] Transmit FIFO trigger threshold. This is write-only. TRA interrupt will be generated when TFL[3-0] is less than TFLT[3-0].

TFLT[3-0]	Description
0000	NA
0001	TX FIFO trigger level = 1
0010	TX FIFO trigger level = 2
0011	TX FIFO trigger level = 3
0100	TX FIFO trigger level = 4
0101	TX FIFO trigger level = 5
0110	TX FIFO trigger level = 6
0111	TX FIFO trigger level = 7
1000	TX FIFO trigger level = 8
1001	TX FIFO trigger level = 9
1010	TX FIFO trigger level = 10
1011	TX FIFO trigger level = 11
1100	TX FIFO trigger level = 12
1101	TX FIFO trigger level = 13
1110	TX FIFO trigger level = 14
1111	TX FIFO trigger level = 15

Receive and transmit FIFO pointers can be reset by clear TX/RX FIFO operation.

SINT2L (0x4000_720C) EUART2 Interrupt Enable Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	INTEN	TRAEN	RDAEN	RFOEN	RFUEN	TFOEN	FERREN	TIEN
WR	INTEN	TRAEN	RDAEN	RFOEN	RFUEN	TFOEN	FERREN	TIEN

INTEN Interrupt Enable
Set to enable UART2 interrupt. Clear to disable interrupt. Default is 0.

TRAEN	Transmit FIFO Ready Interrupt Enable.
RDAEN	Receive FIFO Ready Interrupt Enable.
RFOEN	Receive FIFO Overflow interrupt Enable.
RFUEN	Receive FIFO Underflow Interrupt Enable
TFOEN	Transmit FIFO Overflow Interrupt Enable
FERREN	Framing Error Interrupt Enable
TIEN	Transmit Message Completion Interrupt Enable

SINT1H (0x4000_720D) EUART2 Interrupt Status Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	-	TRA	RDA	RFO	RFU	TFO	FERR	TI
WR	-	TRA	RDA	RFO	RFU	TFO	FERR	TI

TRA	Transmit FIFO Ready Flag. This bit is set when transmit FIFO has been emptied below FIFO threshold. The flag is cleared by software writing “1”.
RDA	Receive FIFO Ready Flag. This bit is set by hardware when receive FIFO exceeds the FIFO threshold. RDA will also be set when RFL < RFLT for bus idle duration longer than RFLT * 16 * Baud Rate. This is to inform software that there are still remaining unread received bytes in the FIFO. The flag is cleared by software writing “1”.
RFO	Receive FIFO Overflow Flag. This bit is set when overflow condition of receive FIFO occurs. The flag is cleared by software writing “1” or by FIFO reset action.
RFU	Receive FIFO Underflow Flag. This bit is set when underflow condition of receive FIFO occurs. The flag is cleared by software writing “1” or by FIFO reset action.
TFO	Transmit FIFO Overflow Flag. This bit is set when overflow condition of transmit FIFO occurs. The flag is cleared by software writing “1” or by FIFO reset action.
FERR	Framing Error Flag. This bit is set when framing error occurs as the byte is received. The flag is cleared by software writing “1”.
TI	Transmit Message Completion Flag. This bit is set when all messages in the TX FIFO are transmitted and thus the TX FIFO becomes empty. The flag is cleared by software writing “1”.

SBUF2L (0x4000_7210) EUART2 Data Buffer Low Register (0x00) R/W

	7	6	5	4	3	2	1	0
RD	EUART2 Receive Data Register RXDATA[7-0]							
WR	EUART2 Transmit Data Register TXDATA[7-0]							

SBUF2H (0x4000_7211) EUART2 Data Buffer High Register (0x00) R/W

	15	14	13	12	11	10	9	8
RD	-	-	-	-	-	-	-	RXDATA[8]
WR	-	-	-	-	-	-	-	TXDATA[8]

This register is the virtual data buffer register for both receive and transmit FIFO. When being read, it reads out the top byte of the RX FIFO; when written, it writes into the top byte of the TX FIFO.

Writing TXDATA[7-0] causes FIFO write-pointer +1 and any reading on SBUF cause read-pointer +1, so word or half-word read for 9bit mode only.

EUART2 can be configured to add LIN capability. The major enhancement of LIN includes master/slave configurations, auto baud-rate synchronization, and frame-based protocol with header. Under LIN extension mode, all EUART2 registers and functions are still effective and operational. LIN is a single-wire bus and it requires external components to combine RX and TX signals externally. LIN is frame based and consists of message protocols with master/slave configurations. The following diagram shows the basic composition of a header

message sent by the master. It starts with BREAK, the SYNC byte, ID bytes, DATA bytes, and CRC bytes.

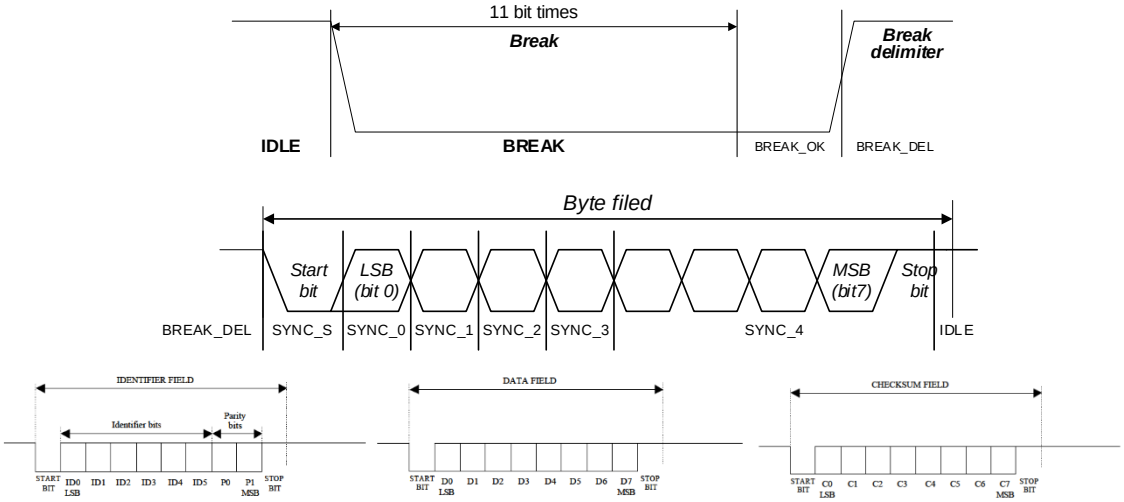


Figure 16-2 LIN Frame Structure

A LIN frame structure is shown and the frame time matches the number of bits sent and has a fixed timing.

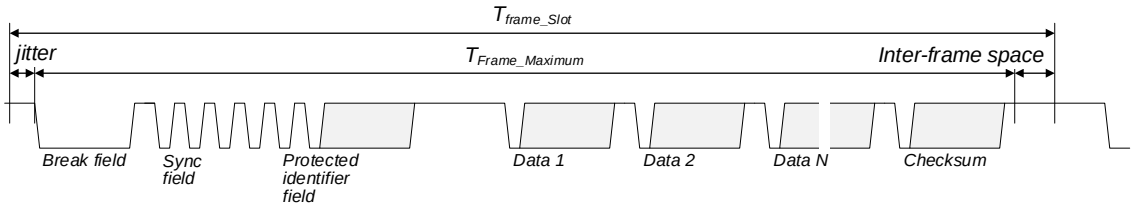


Figure 16-3 LIN Bus Protocol

LIN bus protocol is based on a frame structure. Each frame is partitioned into several parts as shown . For the master to initiate a frame, the software should follow the following procedure.

Initiate a SBK command. (SW needs to check if the bus is in idle state, and there is no pending transmit data).

Write “55” into TFIFO.

Write “PID” into TFIFO.

Wait for SBK to complete its interrupts then write the transmit data if applicable. The following diagram shows a Finite State Machine (FSM) of the LIN extension and is followed by registers within EUART2.

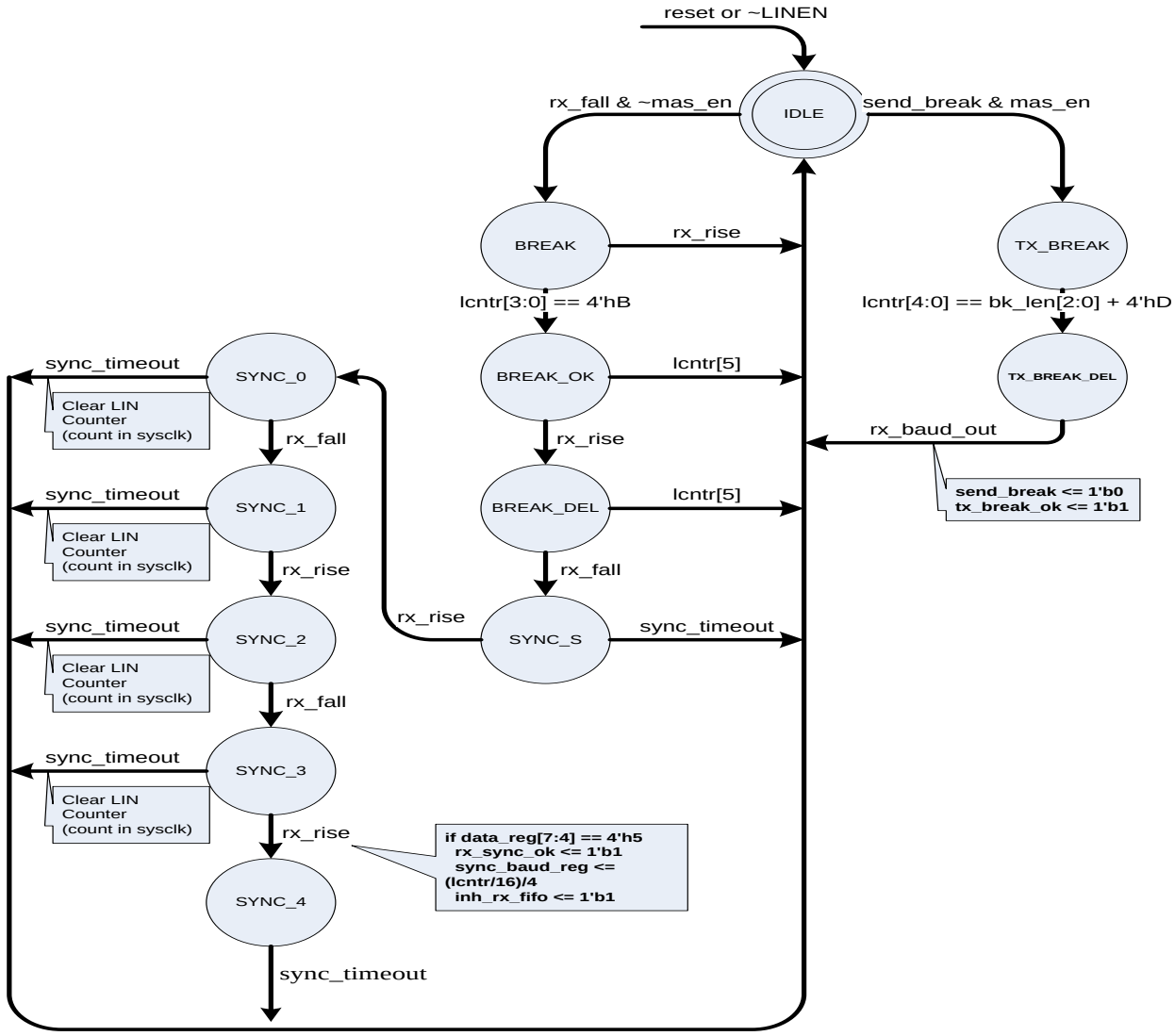


Figure 16-4 FSM For LIN SBK

LCTRL2 (0x4000_7214) EUART2 LIN Status/Control Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	LINEN	MASEN	ASU	MASU	SBK	BL[2-0]		
WR	LINEN	MASEN	ASU	MASU	SBK	BL[2-0]		

LINEN — LIN Enable (1: Enable / 0: Disable).
LIN header detection / transmission is functional when LINEN = 1

※ Before enabling LIN functions, the EUART2 registers must be set correctly：0xB0 is recommended for SCON2.

MASEN — Master Enable bit (1: Master / 0: Slave) LIN operating mode selection. This bit is changeable only when LINEN = 0 (must clear LINEN before changing MASEN).

ASU — Auto-Sync Update Enable (1: Enable / 0: Disable), Write Only
If ASU is 1, the LIN controller will automatically overwrite BR[15-0] with SBR[15-0] and issue an ASUI interrupt when received a valid SYNC field.
If ASU is 0, the LIN controller will only notice the synchronized baud rate in SBR[15-0] by issuing an RSI interrupt.
Please note, ASU should not be set under UART mode. ASU capability is based on the message containing BREAK and SYNC field in the beginning.
When ASU=1, the auto sync update is performed on every receiving frame and is updated frame by frame.

MASU — Message Auto Sync Update Enable.

MASU is meaningful only if ASU=0. MASU=1 will enable the auto sync update on the next received frame only. It is self-cleared when the sync update is completed. The software must set MASU again if another auto sync operation is desired.

SBK — Send Break (1: Send / 0: No send request)
LINEN and MASEN should be set before setting SBK. When LINEN and MASEN are both 1, set SBK to send a bit sequence of 13+BL[2-0] consecutive dominant bits and 1 recessive bit (Break Delimiter). Once SBK is set, this bit represents the "Send Break" status and CANNOT be cleared by writing to "0"; instead, clearing LINEN cancels the "Send Break" action. In normal cases, SBK is cleared automatically when the transmission of Break Delimiter is completed.

BL[2-0] — Break Length Setting
Break Length = 13 + BL[2-0]. Default BL[2-0] is 3'b000.

LINCFG2 (0x4000_7215) EUART2 LIN Configure Register R/W (0x00)

	15	14	13	12	11	10	9	8
RD	-	-	-	-	-	-	-	SYNCLRX
WR	-	-	-	-	-	-	-	SYNCLRX

SYNCLRX — Sync Auto Clear RX FIFO
If SYNCLRX is set, the RX FIFO will be cleared automatically while LIN Slave controller receives a valid Sync byte following a Break (RSI=1). This function is valid only when SYNCMD is set under LIN Slave operating mode.

LINTMR2 (0x4000_7218) LIN Timer Register High R/W (0x3FFFF)

	31-18	17-0
RD	-	LCNTR[17-0]
WR	-	LINTMR[17-0]

LCNTR[17-0] is read only and is an internal 16-bit counter clocked by the baud rate clock. LINTMR[17-0] is write only and is the timer limit for LCNTR[17-0]. If MASEN=1 as LIN master mode, this timer is used to generate Frame time base. The internal counter LCNTR[17-0] is cleared whenever a "SEND BREAK" command is executed, and when the counter reaches LINTMR [17-0] (LCNTR[17-0] >= LINTMR[17-0]), a LCNTRO interrupt is generated. Thus the software can write a Frame Time value into LINTMR and use interrupts to initiate frames. If MASEN=0 as LIN slave mode, this timer is used for determining the accumulated bus idle time. The internal counter is cleared whenever a RX transition occurs. When the internal counter reaches LINTMR[17-0], an LCNTRO interrupt is generated. The software can use this interrupt to enter sleep mode by writing the required bus idling time into LINTMR[17-0].

LININTF2 (0x4000_721C) EUART2 LIN Interrupt Flag Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	RXSTAT	BITERR	LSTAT	LIDLE	ASUI	SBKI	RSI	LCNTRO
WR	-	BITERR			ASUI	SBKI	RSI	LCNTRO

RXSTAT — Receive status
RXSTAT = 1 indicates that the LIN controller is in receive state.

BITERR — Bit Error
BITERR is set by hardware when received bit does not match with transmit bit, If BERIE=1, then this error generates an interrupt. BITERR must be cleared by software with write "1".

LSTAT — LIN Bus Status bit (1: Recessive / 0: Dominant), Read only.
LSTAT = 1 indicates that the LIN bus (RX pin) is in recessive state.
LSTAT = 0 indicates that the LIN bus (RX pin) is in dominant state.

LIDLE — LIDLE is 1 when LIN bus is idle and not transmitting/receiving LIN header or data bytes. This bit read only. It is 1 when LINEN = 0.

ASUI — Receive Sync Completion Interrupt bit (1: Set / 0: Clear)
This flag is set when a valid Sync byte is received following a Break. It must be cleared by writing "1" in the bit.

SBKI — If MASEN=1, SBKI is Send Break Completion Interrupt bit (1: Set / 0: Clear)
This flag is set when Send Break completes. It must be cleared by writing "1" in the bit.

If MASEN=0, SBKI is Receive Break Completion Interrupt bit
This flag is set when a Break condition is detected and completed by a rising edge of bus signal. It must be cleared by writing “1” in the bit.

RSI — RSI Receive 4bit Sync Interrupt bit (1: Set / 0: Clear)
This flag is set when a valid Sync byte is received following a Break. It must be cleared by writing “1” in the bit.

LCNTRO — LIN Counter Overflow Interrupt bit (1: Set / 0: Clear).
This flag is set when the LIN counter reaches 0xFFFF. It must be cleared by writing “1” in the bit.

LININTE2 (0x4000_7220) EUART2 LIN Interrupt Enable Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	LINTEN	BERIE	SYNCMD	SYNCVALID	ASUIE	SBKIE	RSIE	LCNTRIE
WR	LINTEN	BERIE	SYNCMD	-	ASUIE	SBKIE	RSIE	LCNTRIE

LINTEN — LIN Interrupt Enable (1: Enable / 0: Disable)
Set to enable all LIN interrupts. LINT flags should be checked before setting or modifying.

BERIE — Bit Error Interrupt Enable (1: Enable / 0: Disable)

SYNCMD — SYNCMD=0 will only allow automatic synchronization of baud rate within +/- 6% deviations from current baud rate setting. Larger than +/- 6% deviation may cause error of reception.
SYNCMD=1 will automatically synchronize and update the baud rate register with newly acquired baud rate. SYNCMD should be set to 1 when either ASU or MASU is 1. Although under this setting, the tolerant range of deviation can be up to +/- 50%, it is recommended to set the LINBR[15-0] as close as target baud rate.
The new baud rate can be successfully synchronized and frame received correctly must meet the following conditions at the same time.
1. Within +/- 50% of the current baud rate setting.
2. The incoming Break Length satisfies following two conditions at the same time
A. Break length is less than 32 current baud rate bit times
B. Break length is less than 253952 system clocks
3. For the application with multi-baud rates, software should set the LINBR[15-0] using the lowest value. Since after each LIN transaction, LINBR[15-0] is automatically updated with newly synchronized value, software needs to reset LINBR[15-0] to the lowest baud rate again if new baud rate is used.

SYNCVALID — Valid SYNC Waveform
This bit is set to 1 by hardware when valid SYNC waveform is received. SYNCVALID is valid when SYNCMD=1.

ASUIE — Auto-Sync Update Interrupt Enable (1: Enable / 0: Disable)

SBKIE — If MASEN=1, SBKIE is Send Break Completion Interrupt Enable (1: Enable / 0: Disable)
If MASEN=0, SBKIE is Receive Break Completion Interrupt Enable (1: Enable / 0: Disable)

RSIE — Receive Sync Completion Interrupt Enable (1: Enable / 0: Disable)

LCNTRIE — LIN Counter Overflow Interrupt Enable (1: Enable / 0: Disable)

LININTE2B (0x4000_7221) EUART2 LIN Interrupt Enable Register R/W (0x00)

	15	14	13	12	11	10	9	8
RD	TLOOPEN	BETXCLR	BERXCLR	-	-	-	RXPOL	TXPOL
WR	TLOOPEN	BETXCLR	BERXCLR	CLRTX	CLRRX	CLRFIFO	RXPOL	TXPOL

TLOOPEN — TX loop back to RX for test only

BETXCLR — clear TX bit-error

BERXCLR — clear RX bit-error

CLRTX — Clear TX FIFO pointer and TX bit-error

CLRRX — Clear RX FIFO pointer and RX bit-error

CLRFIFO — Clear FIFO pointer and clears flags and LIN state machine
Set to clear transmit/received FIFO buffer and CLRFIFO is auto clear by hardware. In addition, this will also reset the LIN state machine, i.e., also clears RFO, RFU and

TFO interrupt flags without writing the interrupt register. The LIN counter LCNTR is also cleared.

RXPOL EUART/LIN input polarity

TXPOL EUART/LIN output polarity

LINTCON2 (0x4000_7224) EUART2 LIN Time Out Configuration R/W (0x00)

	7	6	5	4	3	2	1	0
RD	-	LRXDFEN	-	-	RXDD_F	TXDD_F	RXDDEN	TXDDEN
WR	-	LRXDFEN	-	-	RXDD_F	TXDD_F	RXDDEN	TXDDEN

LRXDFEN Set to enable LIN break check condition added received dominant fault

RXDD_F RXD Dominant Fault Interrupt Flag
RXDD_F is set to 1 by hardware and must be cleared by software with write “1”

TXDD_F TXD Dominant Fault Interrupt Flag
TXDD_F is set to 1 by hardware and must be cleared by software with write “1”

RXDDEN RXD Dominant Fault Interrupt Enable

TXDDEN TXD Dominant Fault Interrupt Enable

TXDTO2 (0x4000_7228) EUART2 LIN TXD Dominant Time Out Registers R/W (0x0000)

	31-16	15-0
RD	-	TXDTO[15-0]
WR	-	TXDTO[15-0]

TXDTO TXD Dominant Time Out (TXDTO +1) * SYSCLK*(BRCS[7-0]+1). The value of TXDTO[15-0] shall be greater than zero.

RXDTO2 (0x4000_722C) EUART2 LIN RXD Dominant Time Out Registers R/W (0x0000)

	31-16	15-0
RD	-	RXDTO[15-0]
WR	-	RXDTO[15-0]

RXDTO RXD Dominant Time Out (2*RXDTO[15-0] + 1) * IOSCCLK

BSDCLR2 (0x4000_7230) EUART2 Bus Stuck Dominant Clear Width Registers R/W (0x0000)

	31-8	7-0
RD	-	BSDCLR[7-0]
WR	-	BSDCLR[7-0]

BSDCLR Bus Stuck Dominant Clear Time
0: 1 SOSC128K to 2 SOSC128K
1: 1 SOSC128K to 2 SOSC128K
2: 2 SOSC128K to 3 SOSC128K
N: N SOSC128K to N+1 SOSC128K, N=3 to 255.
BSDCLR detects the recessive state duration after a dominant to recessive transition. BSDCLR is used in conjunction with BSDACT setting.

BSDACT2 (0x4000_7234) EUART2 Bus Stuck Dominant Active Width Registers R/W (0x0000)

	31-8	7-0
RD	-	BSDACT[7-0]
WR	-	BSDACT[7-0]

BSDACT Bus Stuck Dominant Active Time
0: 1 SOSC128K to 2 SOSC128K
1: 1 SOSC128K to 2 SOSC128K
2: 2 SOSC128K to 3 SOSC128K
N: N SOSC128K to N+1 SOSC128K, N=3 to 255.
BSDACT detects the dominant state duration after a recessive state meeting BSDCLR transition to dominant state.
If BSDCLR and BSDCLR timings are both met, a BSDWEN interrupt is generated.

Purpose of BSDCLR and BSDACT is to prevent false wakeup if sleep mode entry occurs during system fault with bus stuck in dominant state where transceiver is integrated with LIN controller to control the supply voltage. In typically application, it should not be used and BSDWEN interrupt turned off.

WKFLT2 (0x4000_7235) EUART2 Wakeup Time Registers R/W (0x0000)

	31-8	7-0
RD	-	WKFLT[7-0]
WR	-	WKFLT[7-0]

WKFLT — LIN Wakeup Time
0: 1 SOSC128K to 2 SOSC128K
1: 1 SOSC128K to 2 SOSC128K
2: 2 SOSC128K to 3 SOSC128K
N: N SOSC128K to N+1 SOSC128K, N=3 to 255.

BSDWKC2 (0x4000_7238) EUART2 Bus Stuck Wakeup Configuration R/W (0x00)

	7	6	5	4	3	2	1	0
RD	BSDW_F	BFW_F	BSDWEN	BFWEN	-			
WR	BSDW_F	BFW_F	BSDWEN	BFWEN	-			

BSDW_F — LIN Bus Stuck Wake Up Interrupt Flag
BSDW_F is set to 1 by hardware and must be cleared by software with write “1”

BFW_F — LIN Wake Up Interrupt Flag
BFW_F is set to 1 by hardware and must be cleared by software with write “1”

BSDWEN — LIN Bus Stuck Wake Up/ Interrupt Enable
BSDWEN controls the BSDCLR/BSDACT interrupt. In typical applications, it should be turned off.

BFWEN — LIN Wake Up/Interrupt Enable

Note for auto synchronization of the baud rate in slave configuration, ASU and SYNCMD should be set to a logic 1. In addition, SBR[15-0] should be initialized to 0xFFFF (as the slowest baud rate). If SBR[15-0] is not initialized properly, the incoming break field may cause LNTRO to timeout and interrupt the baud rate detection logic state, or lead to extra data bytes being received.

17. DMA Serial Peripheral Interface (SPI) Controller DSPI

The Serial Peripheral Interface (SPI) is an enhanced synchronous serial hardware which is compatible with most SPI specifications. The SPI Interface uses a Master-Out-Slave-In (MOSI), Master-In-Slave-Out (MISO), Serial Clock (SCK) and Slave Select (SSN) interface. SSN is low active, and SSN can also be configured as latch output in master mode to serve in video bus applications. The maximum SPI clock rate is SYSCLK/4 as the master and SYSCLK/8 as the slave.

SPI Controller uses a DMA transmit and receive. The maximum number of bytes for a transaction is 256 bytes. SPI interface is bidirectional as both input and output data stream can occur simultaneously. The transaction is denoted by SSN. In other words, when SSN is low, this indicates the start of a transaction, and SSN high indicates the transaction end.

When configured as SPI master, the software initiates a transaction through the SPI command register. The transaction byte count register (SPIXBC) determines the number of bytes for a transaction. The SPI controller accesses both the transmitted data and the received data through DMA. When the transaction is completed, an interrupt is generated.

When configured as a SPI slave, the transaction starts when a low on SSN is detected and ends when SSN is high. The SPI controller also accesses the transmitted data and the received data through DMA. The first transmitted byte is 0x00. When a transaction is completed, an interrupt is generated, and the number of bytes for the transaction is recorded in SPIXBC. Note if a transaction does not complete in an 8-bit boundary, extra dribble bits are ignored.

SPICRA (0x4000_8000) SPI Configuration Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	SPEN	SPIEN	MSTR	CPOL	CPHA	SCKE	SSNLAT	-
WR	SPEN	SPIEN	MSTR	CPOL	CPHA	SCKE	SSNLAT	-

SPEN — SPI interface Enable bit.

SPIEN — SPI Interrupt Enable

MSTR — SPI Master/Slave Switch.
MSTR=1: Master.
MSTR=0: Slave.

CPOL — SPI interface Polarity bit: Set to configure the SCK to stay HIGH while the SPI interface is idling and clear to keep it LOW.

CPHA — Clock Phase Control bit: If CPOL=0, set to shift output data at rising edge of SCK, and clear to shift output data at falling edge of SCK. If CPOL=1, set to shift output data at falling edge of SCK and clear to shift output data at rising edge of SCK.

SCKE — Clock Selection bit in Master Mode
Set to delay 0.5 period of SCK to sample the input data.
Clear to use normal edge of SCK to sample the input data.
The sampling phase is determined by the combinations of CPOL and CPHA setting shown in the following table.

CPOL	CPHA	DATAIN Edge			DATAOUT Edge
		Slave	Master, SCKE=0	Master, SCKE=1	
0	0	Rising edge	Rising edge	Falling edge	Falling edge
0	1	Falling edge	Falling edge	Rising edge	Rising edge
1	0	Falling edge	Falling edge	Rising edge	Rising edge
1	1	Rising edge	Rising edge	Falling edge	Falling edge

SSNLAT — Use SSN as LATCH Signal.
SSNLAT=0, configure SSN as normal SPI interface.
SSNLAT=1, configure SSN as LATCH signal. The LATCH start position and width are defined in SLTCHSP and SLTCHWD registers.

SPICRB (0x4000_8001) SPI Configuration Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	FCLR	SIFLTEN	CSFLTEN	CKFLTEN	SPR[2]	SPR[1]	SPR[0]	DIR
WR	FCLR	SIFLTEN	CSFLTEN	CKFLTEN	SPR[2]	SPR[1]	SPR[0]	DIR

FCLR — Force Clear/Reset
Set this bit to terminate all on-going transactions and reset all status flags. This bit is auto cleared by hardware.

SIFLTEN — Enable SDI digital filter

CSFLTEN — Enable CS digital filter

CKFLTEN — Enable SCK digital filter

SPR[2-0] — Slave SPI Clock Rate up to SYSCLK/8,
Master SPI Clock Rate Setting.
000 – SCK = SYSCLK/4;
001 – SCK = SYSCLK/6;
010 – SCK = SYSCLK/8;
011 – SCK = SYSCLK/16;
100 – SCK = SYSCLK/32;
101 – SCK = SYSCLK/64;
110 – SCK = SYSCLK/128;
111 – SCK = SYSCLK/256.

DIR — Transfer Format
DIR=1 uses MSB-first format.
DIR=0 uses LSB-first format.

SPICMD (0x4000_8004) SPI Command Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	XMTF	-	-	-	-	-	-	BUSY
WR	XMTF	-	-	-	-	-	-	XSTART

XMTF — Transaction Complete Interrupt Flag
XMTF is set by hardware when transmission completes. Write “1” to clear.

BUSY — SPI Busy Status

XSTART — SPI Transaction Start
For Master only, CPU write 1 to this bit to start transaction.

SPIXBC (0x4000_8006) SPI Transaction Byte Count R/W (0x00)

	7	6	5	4	3	2	1	0
RD	XBC[7-0]							
WR	XBC[7-0]							

XBC[7-0] — Transaction Byte Count
XBC[7-0]+1 is the transmit byte count.

SPIDMATL (0x4000_8008) SPI DMA Transmit Address Low Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	DMATAD[7-0]							
WR	DMATAD[7-0]							

SPIDMATH (0x4000_8009) SPI DMA Transmit Address High Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	DMATAD[15-8]							
WR	DMATAD[15-8]							

DMATAD[15-0] — Transmit Frame DMA Start Address
DMATAD[15-0] indicates the SPI transmit start address in DMA memory.
DMATAD[1-0] shall be cleared to 0.

SPIDMARL (0x4000_800C) SPI DMA Receive Address Low Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	DMARAD[7-0]							
WR	DMARAD[7-0]							

SPIDMARH (0x4000_800D) SPI DMA Receive Address High Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	DMARAD[15-8]							
WR	DMARAD[15-8]							

DMARAD[15-0] Receive Frame DMA Start Address
DMARAD[15-0] indicates the SPI receive start address in DMA memory.
DMARAD[1-0] shall be cleared to 0.

SLTCHSPL (0x4000_8010) SSN Latch Start Position Low Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	SLTCHSP[7-0]							
WR	SLTCHSP[7-0]							

SLTCHSPH (0x4000_8011) SSN Latch Start Position High Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	SLTCHSP[15-8]							
WR	SLTCHSP[15-8]							

SLTCHSP[15-0] SSN Latch Signal Start Position. This defines the start location in SPI bit time.

SLTCHWD (0x4000_8012) SSN Latch Width Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	SLTCHWD[7-0]							
WR	SLTCHWD[7-0]							

SLTCHWD[7-0] SSN Latch Signal Width. This defines the Latch width in SPI bit time.

17.1 SPI Master Timing Illustration

17.1.1 CPOL=0 CPHA=0

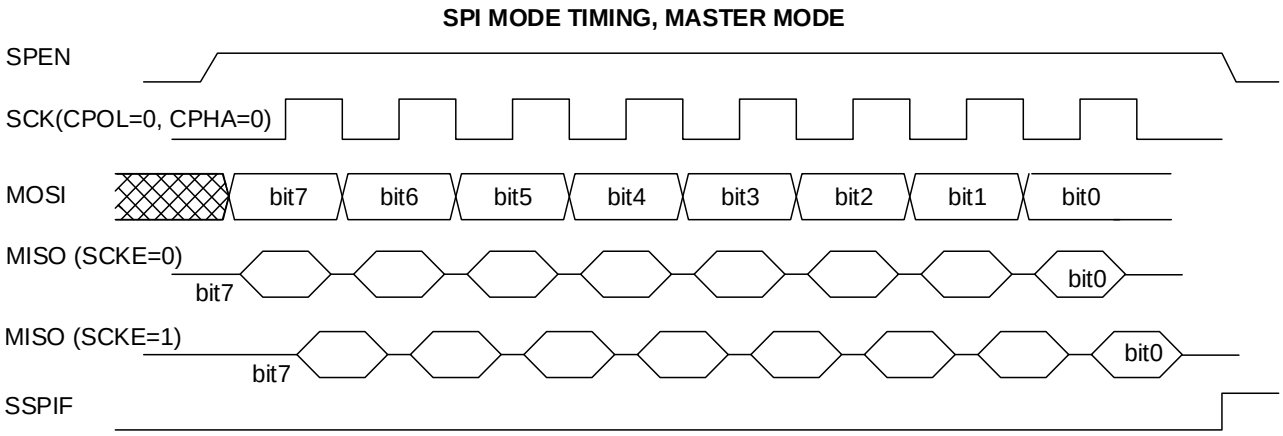


Figure 17-1 SPI Master Timing with CPOL=0, CPHA=0

17.1.2 CPOL=0 CPHA=1

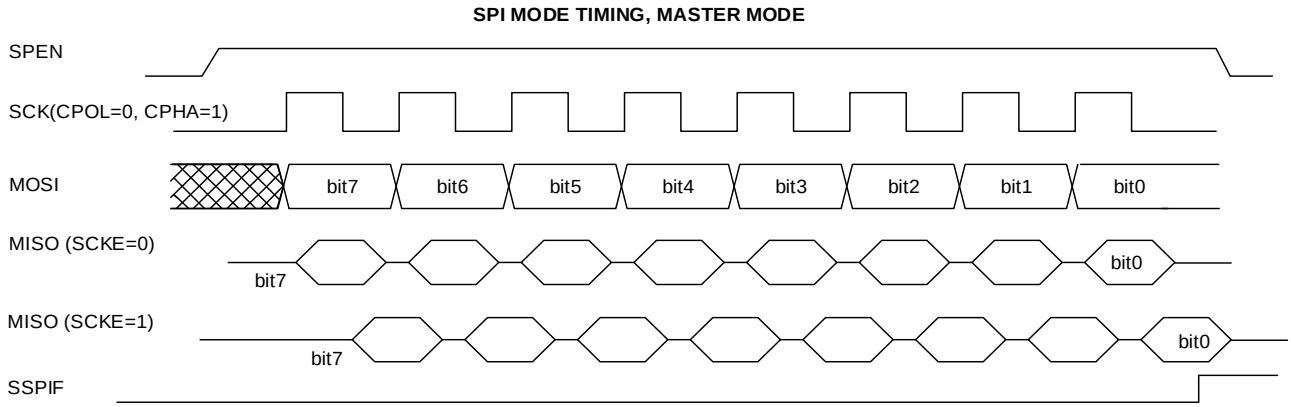


Figure 17-2 SPI Master Timing with CPOL=0, CPHA=1

17.1.3 CPOL=1 CPHA=0

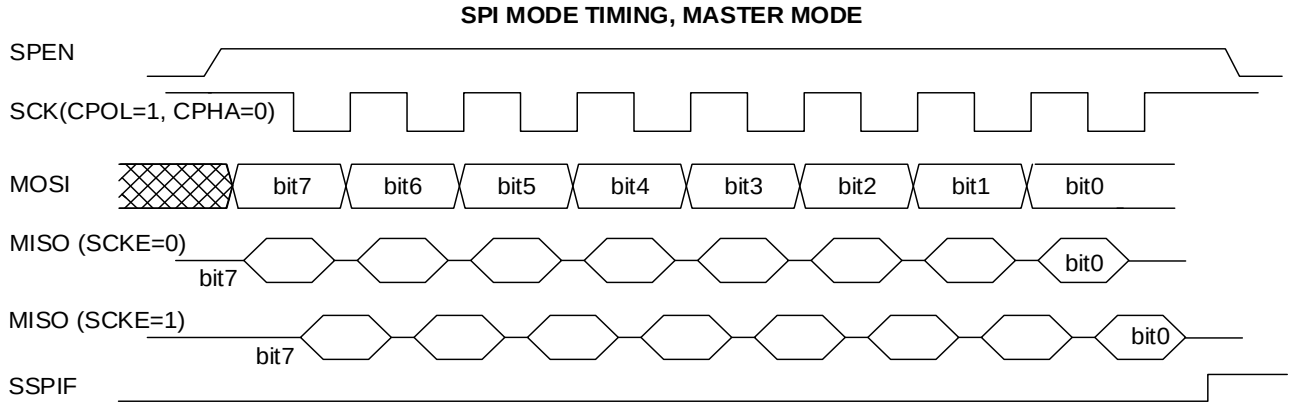


Figure 17-3 SPI Master Timing with CPOL=1, CPHA=0

17.1.4 CPOL=1 CPHA=1

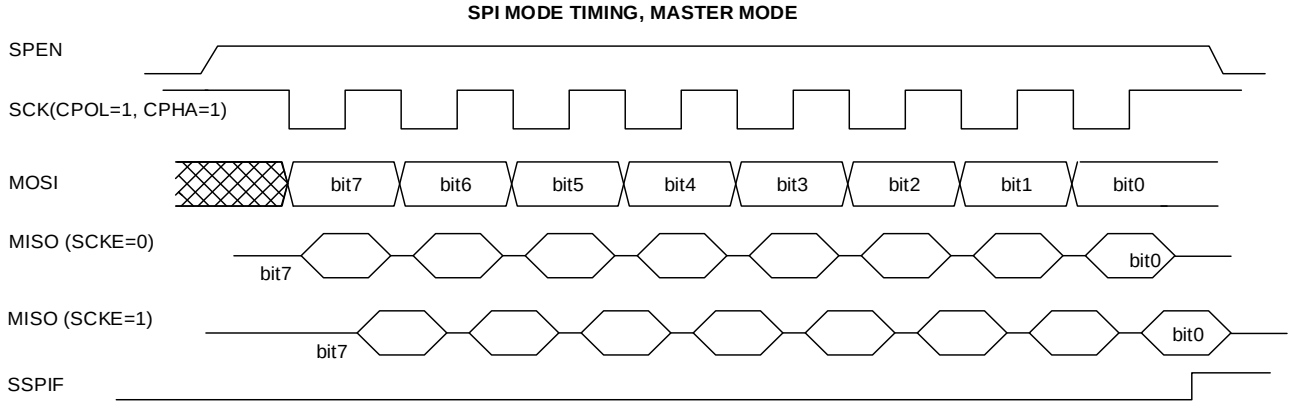


Figure 17-4 SPI Master Timing with CPOL=1, CPHA=1

17.2 SPI Slave Timing Illustration

17.2.1 CPOL=0 CPHA=0

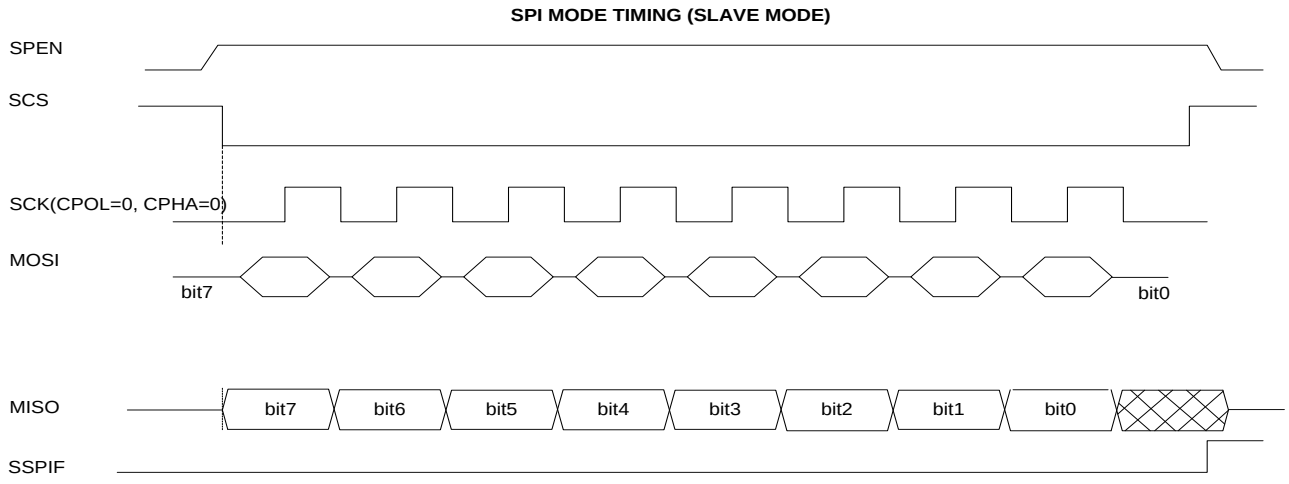


Figure 17-5 SPI Slave Timing with CPOL=0, CPHA=0

17.2.2 CPOL=0 CPHA=1

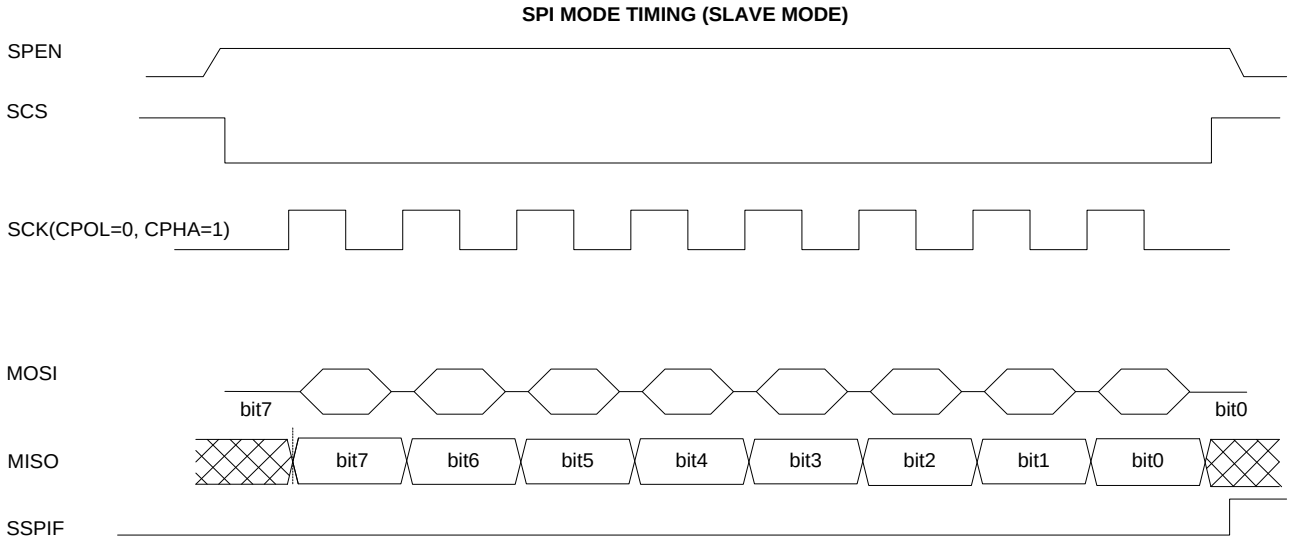


Figure 17-6 SPI Slave Timing with CPOL=0, CPHA=1

17.2.3 CPOL=1 CPHA=0

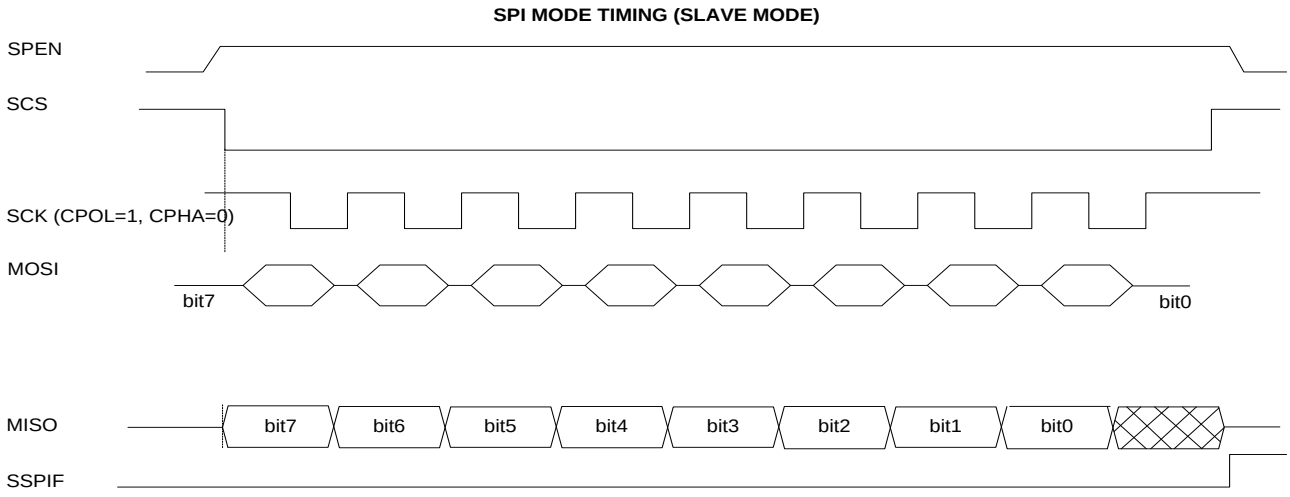


Figure 17-7 SPI Slave Timing with CPOL=1, CPHA=0

17.2.4 CPOL=1 CPHA=1

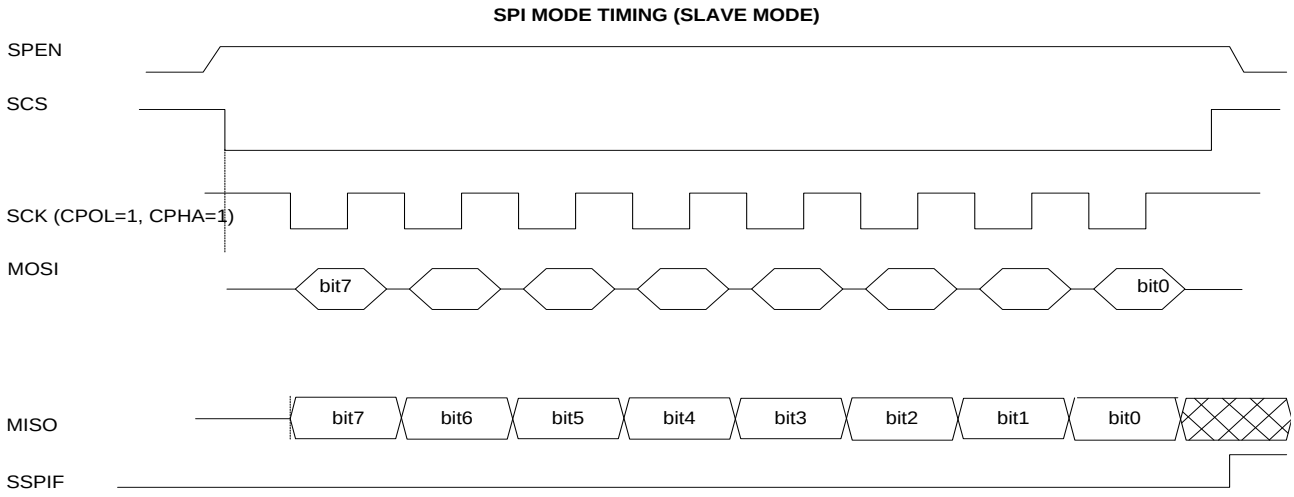


Figure 17-8 SPI Slave Timing with CPOL=1, CPHA=1

17.2.5 SSN as LATCH

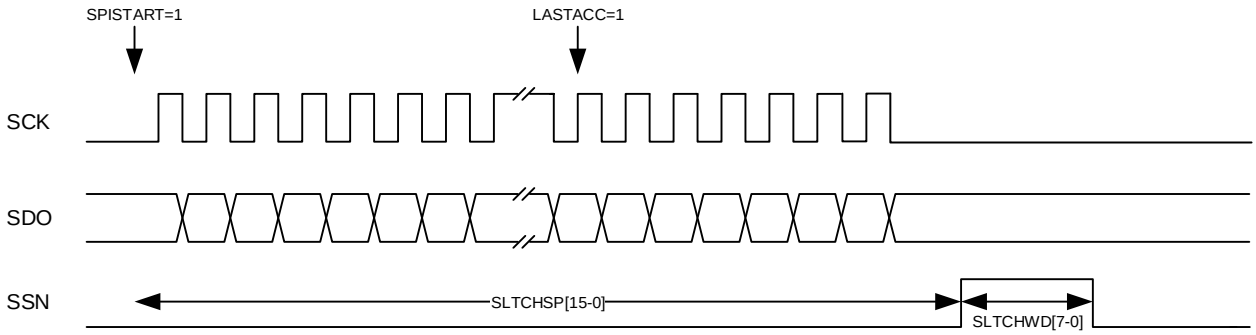


Figure 17-9 SSN as Latch signal

18. Timer with Compare/Capture TCC1/TCC2

The Timer/Capture unit is based on a 16-bit counter with pre-scalable SYSCLK clock. The count starts from 0 and re-loads when the terminal count (TC) is reached. TC is met when the count equals the period value. During the count, the count value is compared with COMP and when there is a match, a CC condition is met. Note that both PERIOD and COMP register are double buffered, therefore new values are updated after the period ends. TC and CC can be used for triggering interrupts and can be routed to the GPIO pins. The output pulse width of TC and CC are programmable. For CC, it can be configured as a PWM output. There are two data registers for captured events. The captured event can be from an external GPIO with an edge selection option, or from the QE block, or triggered by the software. The software can also be selected if is used to reset the counter, this option allows for simpler calculation of consecutive capture without an offset. The following block diagram shows the TCC implementations.

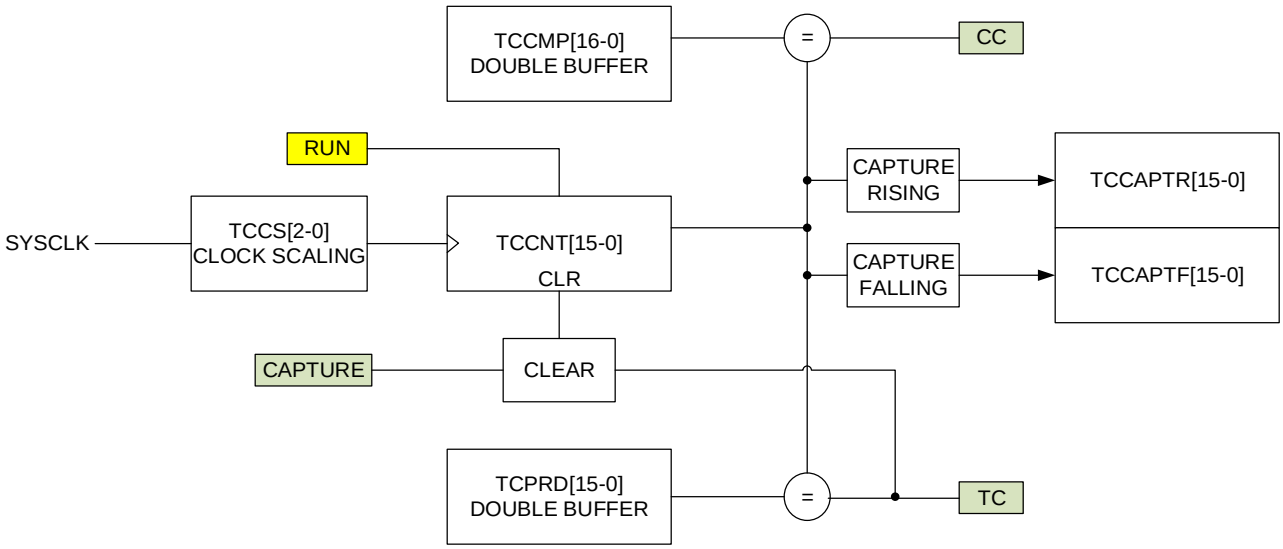


Figure 18-1 TCC Block Diagram

TC1CFG1A (0x4000_9000) TC1 Configuration Register 1A R/W (0x00)

	7	6	5	4	3	2	1	0
RD	TCEN	TCCS[2-0]			CCSEL[1-0]		TCSEL	RUNST
WR	TCEN	TCCS[2-0]			CCSEL[1-0]		TCSEL	RUN

TCEN — TC Enable
TC = 0 disables TC. In disabled state, TCCNT, and TCCPTR/TCCPTF are cleared to 0. TC and CC are also set to low.
TC = 1 enable TC. RUN bit also needs to set to 1 to start the counter, otherwise if RUN=0 then counter is in pause mode.

TCCS[2-0] — TC Clock Scaling
000 SYSCLK
001 SYSCLK/2
010 SYSCLK/4
011 SYSCLK/8
100 SYSCLK/16
101 SYSCLK/32
110 SYSCLK/64
111 SYSCLK/128

CCSEL[1-0] — CC Output Pulse Select
00 PW = 16 TCCLK
01 PW = 64 TCCLK
10 PWM Waveform (CC = low when TCCNT < CMP, CC = high when TCCNT >= CMP).
11 PWM Toggle waveform (CC toggles when TCCNT = CMP).

TCSEL — TC Output Pulse Select
0 PW = 16 TCCLK
1 PW = 64 TCCLK

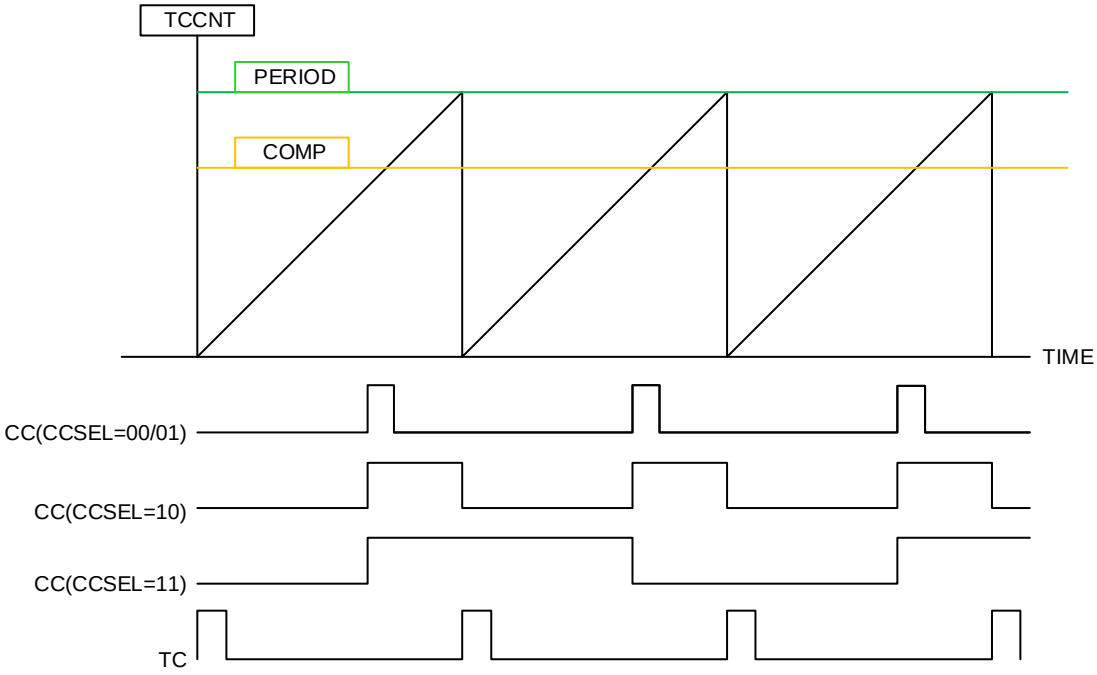


Figure 18-2 TCC timing diagram

RUNST Run Status
Set by hardware to indicate running TC counter. RUNST=1 indicates running.

RUN Run or Pause TC Counter
Writing “0” to RUN will pause the TC counting.
Writing “1” to RUN will resume the TC counting.

TC1CFG2A (0x4000_9004) TC1 Configuration Register 2A R/W (0x00)

	7	6	5	4	3	2	1	0
RD	-	-	-	-	XCRF	XCFF	TCF	CCF
WR	RSTTC	-	-	-	XCRF	XCFF	TCF	CCF

RSTTC Reset TC
Writing RSTTC “1” will reset the TC counter and capture registers. Once counter is cleared, TC counter is put in STOP mode. To resume counting, RUN bit must be set by software.

XRCF External Rising Edge Capture Flag
XRCF is set to “1” by hardware when an external rising edge capture event has occurred. XRCF must be cleared by software by writing “1”. The captured value is stored in CPTR register.

TCF Terminal Count Interrupt Flag
TCF is set to “1” by hardware when terminal count occurs. TCF must be cleared by software by writing “1”.

CCF Compare Match Interrupt Flag
CCF is set to “1” by hardware when compare match occurs. CCF must be cleared by software by writing “1”.

TC1CFG2B (0x4000_9005) TC1 Configuration Register 2B R/W (0x00)

	7	6	5	4	3	2	1	0
RD	SYNCTC2	SYNCPWM	-	-	-	-	-	-
WR	SYNCTC2	SYNCPWM	-	-	-	-	SWCPTR	SWCPTF

SYNCTC2 Synchronize with TC2
Synchronize the counter start with TC2 counter.
This bit is set by software and cleared by hardware. Once this bit is set, the counter restart counting when TC2 count reaches restart point.

To maintain synchronization, TC1 and TC2's clock scaling and period setting must be the same.

SYNCPWM — Synchronize with PWM
Synchronize the counter start with PWM counter.
This bit is set by software and cleared by hardware. Once this bit is set, the counter restart counting when PWM count reaches restart point.
To maintain synchronization, TC1 and PWM clock scaling must be the same. Due to PWM counting is center aligned, the period setting of TC1 must be 2X of PWM period setting.

SWCPTR — Software Capture R
Writing "1" to SWCPTR will generate a capture event and capture the count value into CAPTR register. This bit is cleared by hardware.

SWCPTF — Software Capture F
Writing "1" to SWCPTF will generate a capture event and capture the count value into CAPTF register. This bit is cleared by hardware.

TC1CFG3A (0x4000_9008) TC1 Configuration Register 3A R/W (0x00)

	7	6	5	4	3	2	1	0
RD	IENTC1	IENCC	-	CPTCLR	XRCEN	XFCEN	TCPOL	CCPOL
WR	IENTC1	IENCC	-	CPTCLR	XRCEN	XFCEN	TCPOL	CCPOL

IENCC — CC Interrupt Enable

CPTCLR — Enable Clear Counter after Capture
If CPTCLR=1, the TCCNT is cleared to 0 after each capture event. This allows continuous capture value with identical initial value.
If CPTCLR=0, the capture event does not affect the TCCNT counting.

XRCEN — External Rising Edge Capture Enable
XRCEN=1 use external input rising edge as capture event.

XFCEN — External Falling Edge Capture Enable
XFCEN=1 use external input falling edge as capture event.

TCPOL — TC output polarity

CCPOL — CC output polarity

Please note all capture sources are not mutually exclusive, i.e. allow several capture sources can coexist.

TC1CFG3B (0x4000_9009) TC1 Configuration Register 3B R/W (0x00)

	7	6	5	4	3	2	1	0
RD	-	-	-	-	-	-	IENXRC	IENXFC
WR	-	-	-	-	-	-	IENXRC	IENXFC

IENXRC — XC Rising Edge Interrupt Enable
IENXRC=1 enables interrupt when XRC event occurs.

IENXFC — XC Falling Edge Interrupt Enable
IENXFC=1 enables interrupt when XFC event occurs.

TC1PRDL (0x4000_900C) TC1 Period and Count Register R/W (0x00)

	15 - 0
RD	TCCNT[15-0]
WR	TCPRD[15-0]

TC1CMP (0x4000_9010) TC1 Compare Register R/W (0x00)

	15 - 0
RD	TCCMP[15-0]
WR	TCCMP[15-0]

TC1CPTRL (0x4000_9014) TC1 Capture Register R Low R/W (0x00)

	7	6	5	4	3	2	1	0
RD	TCCPTR[7-0]							
WR	-							

TC1CPTRH (0x4000_9015) TC1 Capture Register R High R/W (0x00)

	7	6	5	4	3	2	1	0
RD	TCCPTR[15-8]							
WR	-							

TC1CPTFL (0x4000_9018) TC1 Capture Register F Low R/W (0x00)

	7	6	5	4	3	2	1	0
RD	TCCPTF[7-0]							
WR	-							

TC1CPTFH (0x4000_9019) TC1 Capture Register F High R/W (0x00)

	7	6	5	4	3	2	1	0
RD	TCCPTF[15-8]							
WR	-							

TC2 is the same as TC1. Its control registers start with 0x4000_8020.

TC2CFG1A (0x4000_9020) TC2 Configuration Register 1A R/W (0x00)

	7	6	5	4	3	2	1	0
RD	TCEN	TCCS[2-0]			CCSEL[1-0]		TCSEL	RUNST
WR	TCEN	TCCS[2-0]			CCSEL[1-0]		TCSEL	RUN

TCEN — TC Enable
TC = 0 disables TC. In disabled state, TCCNT, and TCCPTR/TCCPTF are cleared to 0. TC and CC are also set to low.
TC = 1 enable TC. RUN bit also needs to set to 1 to start the counter, otherwise if RUN=0 then counter is in pause mode.

TCCS[2-0] — TC Clock Scaling
000 SYSCLK
001 SYSCLK/2
010 SYSCLK/4
011 SYSCLK/8
100 SYSCLK/16
101 SYSCLK/32
110 SYSCLK/64
111 SYSCLK/128

CCSEL[1-0] — CC Output Pulse Select
00 PW = 16 TCCLK
01 PW = 64 TCCLK
10 PWM Waveform (CC = low when TCCNT < CMP, CC = high when TCCNT >= CMP).
11 PWM Toggle waveform (CC toggles when TCCNT = CMP).

TCSEL — TC Output Pulse Select
0 PW = 16 TCCLK
1 PW = 64 TCCLK

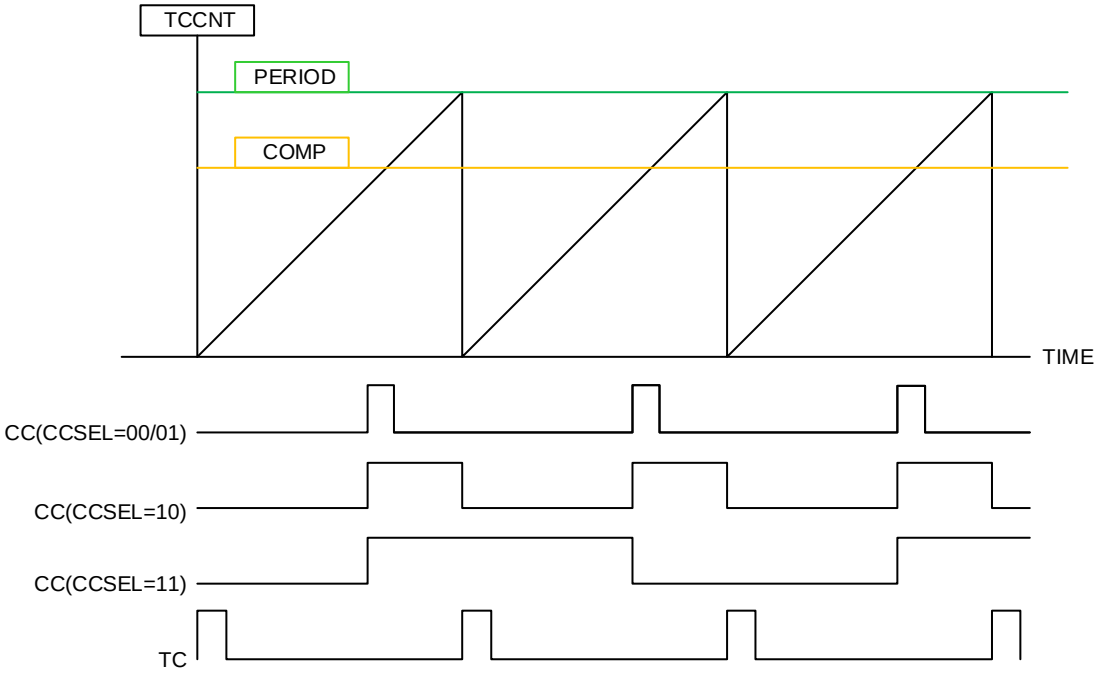


Figure 18-3 TCC timing diagram

RUNST — Run Status
Set by hardware to indicate running TC counter. RUNST=1 indicates running.

RUN — Run or Pause TC Counter
Writing “0” to RUN will pause the TC counting.
Writing “1” to RUN will resume the TC counting.

TC2CFG2A (0x4000_9024) TC2 Configuration Register 2A R/W (0x00)

	7	6	5	4	3	2	1	0
RD	-	-	-	-	XRCF	XFCF	TCF	CCF
WR	RSTTC	-	-	-	XRCF	XFCF	TCF	CCF

RSTTC — Reset TC
Writing RSTTC “1” will reset the TC counter and capture registers. Once counter is cleared, TC counter is put in STOP mode. To resume counting, RUN bit must be set by software.

XRCF — External Rising Edge Capture Flag
XRCF is set to “1” by hardware when an external rising edge capture event has occurred. XRCF must be cleared by software by writing “1”. The captured value is stored in CPTR register.

XFCF — External Falling Edge Capture Flag
XFCF is set to “1” by hardware when an external falling edge capture event has occurred. XFCF must be cleared by software by writing “1”. The captured value is stored in CPTF register.

TCF — Terminal Count Interrupt Flag
TCF is set to “1” by hardware when terminal count occurs. TCF must be cleared by software by writing “1”.

CCF — Compare Match Interrupt Flag
CCF is set to “1” by hardware when compare match occurs. CCF must be cleared by software by writing “1”.

TC2CFG2B (0x4000_9025) TC2 Configuration Register 2B R/W (0x00)

	7	6	5	4	3	2	1	0
RD	SYNCTC1	SYNCPWM	-	-	-	-	-	-
WR	SYNCTC1	SYNCPWM	-	-	-	-	SWCPTR	SWCPTF

SYNCTC1 — Synchronize with TC1

Synchronize the counter start with TC1 counter.
This bit is set by software and cleared by hardware. Once this bit is set, the counter restart counting when TC1 count reaches restart point.
To maintain synchronization, TC1 and TC2's clock scaling and period setting must be the same.

SYNCPWM — Synchronize with PWM
Synchronize the counter start with PWM counter.
This bit is set by software and cleared by hardware. Once this bit is set, the counter restart counting when PWM count reaches restart point.
To maintain synchronization, TC2and PWM clock scaling must be the same. Due to PWM counting is center-aligned, the period setting of TC1 must be 2X of PWM period setting.

SWCPTR — Software Capture R
Writing "1" to SWCPTR will generate a capture event and capture the count value into CPTR register. This bit is cleared by hardware.

SWCPTF — Software Capture F
Writing "1" to SWCPTF will generate a capture event and capture the count value into CPTF register. This bit is cleared by hardware

TC2CFG3A (0x4000_9028) TC2 Configuration Register 3A R/W (0x00)

	7	6	5	4	3	2	1	0
RD	IENTC2	IENCC	-	CPTCLR	XRCEN	XFCEN	TCPOL	CCPOL
WR	IENTC2	IENCC	-	CPTCLR	XRCEN	XFCEN	TCPOL	CCPOL

IENTC2 — TCC2 Interrupt Enable

IENCC — CC Interrupt Enable

CPTCLR — Enable Clear Counter after Capture
If CPTCLR=1, the TCCNT is cleared to 0 after each capture event. This allows continuous capture value with identical initial value.
If CPTCLR=0, the capture event does not affect the TCCNT counting.

XRCEN — External Rising Edge Capture Enable
XRCEN=1 use external input rising edge as capture event.

XFCEN — External Falling Edge Capture Enable
XFCEN=1 use external input falling edge as capture event.

TCPOL — TC output polarity

CCPOL — CC output polarity

Please note all capture sources are not mutually exclusive, i.e. allow several capture sources can coexist.

TC2CFG3B (0x4000_9029) TC2 Configuration Register 3B R/W (0x00)

	7	6	5	4	3	2	1	0
RD	-	-	-	-	-	-	IENXRC	IENXFC
WR	-	-	-	-	-	-	IENXRC	IENXFC

IENXRC — XC Rising Edge Interrupt Enable
IENXRC=1 enables interrupt when XRC event occurs.

IENXFC — XC Falling Edge Interrupt Enable
IENXFC=1 enables interrupt when XFC event occurs.

TC2PRD (0x4000_902C) TC2 Period and Count Register R/W (0x00)

	15 - 0
RD	TC2CNT[15-0]
WR	TC2PRD[15-0]

TC2CMP (0x4000_9030) TC2 Compare Register R/W (0x00)

	15 - 0
RD	TC2CMP[15-0]
WR	TC2CMP[15-0]

TC2CPTRL (0x4000_9034) TC2 Capture Register R Low R/W (0x00)

	7	6	5	4	3	2	1	0
RD	TC2CPTR[7-0]							
WR	-							

TC2CPTRH (0x4000_9035) TC2 Capture Register R High R/W (0x00)

	7	6	5	4	3	2	1	0
RD	TC2CPTR15-8]							
WR	-							

TC2CPTFL (0x4000_9038) TC2 Capture Register F Low R/W (0x00)

	7	6	5	4	3	2	1	0
RD	TC2CPTF[7-0]							
WR	-							

TC2CPTFH (0x4000_9039) TC2 Capture Register F High R/W (0x00)

	7	6	5	4	3	2	1	0
RD	TC2CPTF[15-8]							

19. PWM Controller

The PWM controller provides programmability of 8 channels with14/12/10/8-bit PWM center-aligned duty cycle outputs. The duty cycle setting is double buffered and PWM outputs are GPIO multiplexed.

PWMCFG1A (0x4000_A080) PWM Clock Scaling Setting Register A R/W (0x00)

	7	6	5	4	3	2	1	0
RD	PWMEN	-	-	-	PRSEN	SYNCEN	MODE[1-0]	
WR	PWMEN	-	-	-	PRSEN	SYNCEN	MODE[1-0]	

PWMEN — PWM Controller Enable
PWMEN=0 clears the counter, reset the PWM state and all channel outputs are forced to 0.
PWMEN=1 allows normal running operation of PWM controller.

PRSEN — Pseudo-Random Sequence Enable
PRSEN=1 will enable a pseudo random sequence to the PWM output width. This can be an effective way to reduce EMI for output. When PRSEN=1, the instantaneous duty cycle will be affected cycle by cycle, but the average duty cycle remains the same.

SYNCEN — SYNC double update enable
SYNCEN=1, allow using SYNC to synchronize all channel duty value update.
SYNCEN=0, duty double buffer update immediately at next PWM start.

MODE[1-0] — PWM Mode
00 = 8-bit
01 = 10-bit
10 = 12-bit
11 = 14-bit

PWMCFG1B (0x4000_A081) PWM Clock Scaling Setting Register B R/W (0x00)

	7	6	5	4	3	2	1	0
RD	CS[7-0]							
WR	CS[7-0]							

CS[7-0] — PWM Counting Clock Scaling
The counting clock is SYSCLK/[CS[7-0]+1]
14-bit PWM clock = SYSCLK / [CS[7-0] + 1] / 32768
12-bit PWM clock = SYSCLK / [CS[7-0] + 1] / 8192
10-bit PWM clock = SYSCLK / [CS[7-0] + 1] / 2048

8-bit PWM clock = SYSCLK / [CS[7-0] + 1] / 512. There are 8 independent PWMDTY registers that defines the duty cycle. If PWMDTY = 0, the output is 0. If PWMDTY > then the maximum for the specific mode setting the output duty cycle is full. For example, in 12-bit mode, if PWMDTY is set higher than 0x10000, the output is in full duty cycle. PWMDTY is always double buffered and loaded to the duty cycle comparator when the current count cycle is completed.

PWMCFG2 (0x4000_A084) PWM Interrupt Enable and Flag Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	SYNC	-	-	-	-	TINTF	ZINTF	CINTF
WR	SYNC	-	-	-	-	TINTF	ZINTF	CINTF

SYNC — Channel DTY Synchronize Control
If SYNCEN=1, SYNC is used to synchronize all channels DTY value update timing. When SYNC is written 1, the DTY values of all channels are updated together at next PWM cycle start. SYNC is cleared by hardware after the update occurs.

TINTF — Trigger Interrupt Flag
TINTF is set to 1 by hardware to indicate a trigger interrupt has occurred. TINTF must be cleared by software.

ZINTF — Zero Interrupt Flag
ZINTF is set to 1 by hardware to indicate a Zero interrupt has occurred. ZINTF must be cleared by software.

CINTF — Center Interrupt Flag

CINTF is set to 1 by hardware to indicate a center interrupt has occurred. CINTF must be cleared by software.

PWMCFG3 (0x4000_A088) PWM Configuration 3 Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	-	TTRGEN	ZTRGEN	CTRGEN	-	TINTEN	ZINTEN	CINTEN
WR	-	TTRGEN	ZTRGEN	CTRGEN	-	TINTEN	ZINTEN	CINTEN

TTRGEN	Trigger ADC Trigger Enable
ZTRGEN	Zero ADC Trigger Enable
CTRGEN	Center ADC Trigger Enable
TINTEN	Trigger Interrupt Enable TINTEN=1 allows PWM Controller to generate interrupt when count reach PWMTRG.
ZINTEN	Zero Interrupt Enable ZINTEN=1 allows PWM Controller to generate interrupt at start of the PWM cycle.
CINTEN	Center Interrupt Enable CINTEN=1 allows PWM Controller to generate interrupt at center of the PWM cycle.

PWM0DTY (0x4000_A090) PWM0 Duty Register R/W (0x00)

	31-14	13-0
RD	-	PWM0DTY[13-0]
WR	-	PWM0DTY[13-0]

PWM1DTY (0x4000_A094) PWM1 Duty Register R/W (0x00)

	31-14	13-0
RD	-	PWM1DTY[13-0]
WR	-	PWM1DTY[13-0]

PWM2DTY (0x4000_A098) PWM2 Duty Register R/W (0x00)

	31-14	13-0
RD	-	PWM2DTY[13-0]
WR	-	PWM2DTY[13-0]

PWM3DTY (0x4000_A09C) PWM3 Duty Register R/W (0x00)

	31-14	13-0
RD	-	PWM3DTY[13-0]
WR	-	PWM3DTY[13-0]

PWM4DTY (0x4000_A0A0) PWM4 Duty Register R/W (0x00)

	31-14	13-0
RD	-	PWM4DTY[13-0]
WR	-	PWM4DTY[13-0]

PWM5DTY (0x4000_A0A4) PWM5 Duty Register R/W (0x00)

	31-14	13-0
RD	-	PWM5DTY[13-0]
WR	-	PWM5DTY[13-0]

PWM6DTY (0x4000_A0A8) PWM6 Duty Register R/W (0x00)

	31-14	13-0
RD	-	PWM6DTY[13-0]
WR	-	PWM6DTY[13-0]

PWM7DTY (0x4000_A0AC) PWM7 Duty Register R/W (0x00)

	31-14	13-0
RD	-	PWM7DTY[13-0]
WR	-	PWM7DTY[13-0]

It is also possible to set interrupt trigger and ADC trigger through register setting.

PWMTRG (0x4000_A0D0) PWM Trigger Setting Register R/W (0x00)

	31-15	14	13-0
RD	-	UD	PWMTRG[13-0]
WR	-	UD	PWMTRG[13-0]

UD	Up/Down Setting RF=0 indicates up counting aligned RF=1 indicates down counting aligned
PWMTRG[13-0]	Trigger Point setting

20. Melody Controller

The melody controller is used to generate melody. The tone frequency is derived from SYSCLK divided by either 32 or 64, and the tone frequency is generated with resolution of 14-bit to support precision tone generation with wide octave span. The duration/pause timers are programmed in 1, 2, 4 or 8ms steps.

The Melody Controller has two outputs, BZ and POW. BZ is used to drive a speaker or a buzzer. POW is used to enable the driver which allows gradual diminishing tonal effects. BZ and POW can be multiplexed to GPIO pins using a GPIO multifunction select.

For each melody note, the frequency, duration, and pause time, and driver on window (POW time) are note parameters. There are two double buffered parameters so a new note can be written when a note is being played. As these are double buffered, the write sequence is FRQL, DUR, PAU, POW. (These can be written by byte, word, or double word), then last FRQH. When FRQH is written, it completes the setting. The timing waveform of a note is shown below.

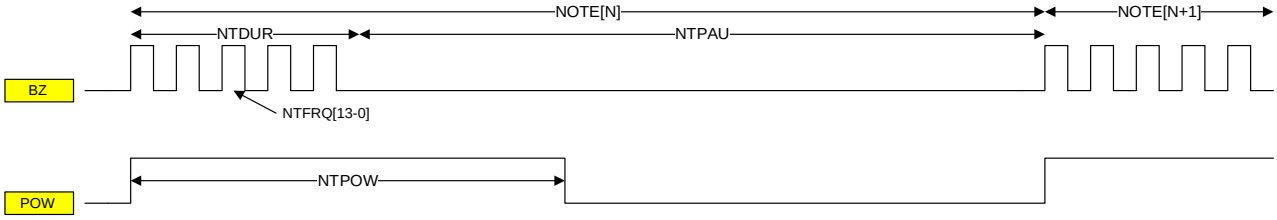


Figure 20-1 Melody Controller Output Waveform

NTFRQL (0x4000_B000) Note Frequency Register L RW DB (0x00)

	7	6	5	4	3	2	1	0
RD	NTFRQ[7-0]							
WR	NTFRQ[7-0]							

NTFRQ[7-0] Note Frequency

NTFRQH (0x4000_B001) Note Frequency Register H DB R/W (0x00)

	7	6	5	4	3	2	1	0
RD	PLAYQUE	MBZINTF	NTFRQ[13-8]					
WR	PLAYQUE	MBZINTF	NTFRQ[13-8]					

PLAYQUE Play Queue
Writing this bit “1” will put the parameters of the note (frequency, duration, pause, and POW) into the play queue.
This bit is self-cleared by hardware when the queue is ready to update.

MBZINTF Melody Buzzer Controller Interrupt Flag
MBZINTF is set to 1 if MBZIE=1 and play queue is ready to be updated. In other words, the flag is set by self-clearing action of PLAYQUE bit. MBZINTF must be cleared by software by writing “1”.

NTFRQ[13-0] Note Frequency
Tone frequency is Tone Base Clock/(NTFRQ[13-0]+1).
Please note due to timing restriction, NTFRQ[13-0] must be >= 2.

NTDUR (0x4000_B004) Note Duration Register WR DB (0x00)

	7	6	5	4	3	2	1	0
RD	NTDUR[7-0]							
WR	NTDUR[7-0]							

NTDUR[7-0] Note Duration
Note duration is TU * NTDUR[7-0]

NTPAU (0x4000_B005) Note Pause Register RW DB (0x00)

	7	6	5	4	3	2	1	0
RD	NTPAU[7-0]							
WR	NTPAU[7-0]							

NTPAU[7-0] Note Pause
Note pause is TU * NTPAU[7-0]

NTPOW (0x4000_B006) Note Power-On Window Register RW DB (0x00)

	7	6	5	4	3	2	1	0
RD	NTPOW [7-0]							
WR	NTPOW [7-0]							

NTPOW[7-0] Note POW Time
POW time is TU * NTPOW[7-0]

BZCFG (0x4000_B008) Buzzer Configure Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	MBZEN	MBZIE	BUSY	POWPOL	BZPOL	TBASE	TU[1-0]	
WR	MBZEN	MBZIE	-	POWPOL	BZPOL	TBASE	TU[1-0]	

MBZEN Melody Buzzer Controller Enable
MBZEN=1 enables the buzzer controller
MBZEN=0 disables the buzzer controller

MBZIE Melody Buzzer Controller Interrupt Enable
IE = 0 disables interrupt.
IE = 1 enables interrupt.
There is only one interrupt for Melody controller. It is generated when the play queue is ready for input after a note was written previously. The interrupt flag is MBZIF in NTFRQH register.

BUSY Melody/Buzzer Status
BUSY is set to 1 by hardware if Melody controller is playing.

POWPOL POW Polarity Setting
POWPOL=1, POW output logic is inverted, i.e., POW is low at the start of the note.
POWPOL=0, normal POW polarity as shown in the timing diagram.

BZPOL BZOUT Polarity Setting
BZPOL=1, BZOUT is inverted
BZPOL=0, normal polarity

TBASE Tone Base Frequency Select
TBASE=0 uses (SYSCLK or APB Clock)/32 as tone base clock
TBASE=1 uses (SYSCLK or APB Clock)/64 as tone base clock

TU[1-0] Time Unit
TU[1-0] defines the time unit for duration and pause, and POW timer
00 = 1msec
01 = 2msec
10 = 4msec
11 = 8msec

21. Essential Analog Blocks

21.1 On-Chip 1.5V Regulator

An on-chip regulator is used for the core logic and internal E-Flash memory (VD15). The regulator is partitioned a back-up and a main regulator. The main regulator is enabled in normal, and STOP modes, and disabled in DEEP SLEEP mode when the backup regulator is disabled. The main regulator consumes 300uA, while the back-up regulator consumes 1uA. The back-up regulator supplies up to 500uA therefore it is important that all peripheral circuits are disabled during DEEP SLEEP mode. In addition, the e-Flash power is turned off during the DEEP SLEEP mode to reduce power. After reset, the main regulator defaults on. The regulator requires an external capacitor, which should be connected to the VD15 pin. A 1uF an a 0.1uF in parallel is required for stability. The main regulator outputs can be adjusted by the REGTRM (with default at its maximum) and the back-up regulator outputs 1.5V. A manufacturing calibrated value of REGTRM for 1.5V is stored in IFB.

REGTRM (0x4000_F100) Regulator Trim Register RW (0xFF)

	7	6	5	4	3	2	1	0
RD	REGTRM[7-0]							
WR	REGTRM[7-0]							

REGTRM[7-0] Trim Register for main 1.5V regulator.
REGTRM[7-0]=FF corresponds to maximum output level. REGTRM[7-0]=00 corresponds to minimum output level. The in-between value in general is linear to the output level. Typically the maximum is around 1.65V while the minimum is around 1.35V.

REGRDY (0x4000_F104) Regulator Ready Delay Register RW (0x06)

	7	6	5	4	3	2	1	0
RD	-					REGRDY[2-0]		
WR	-					REGRDY[2-0]		

REGRDY[2-0] Regulator Ready Delay Setting
REGRDY[2-0] defines the number of SOSC32K cycle for allowing regulator stabilize at exit of sleep mode.
000 N=0
001 N=1
010 N=4
011 N=16
100 N=64
101 N=128
110 N=256
111 N=510

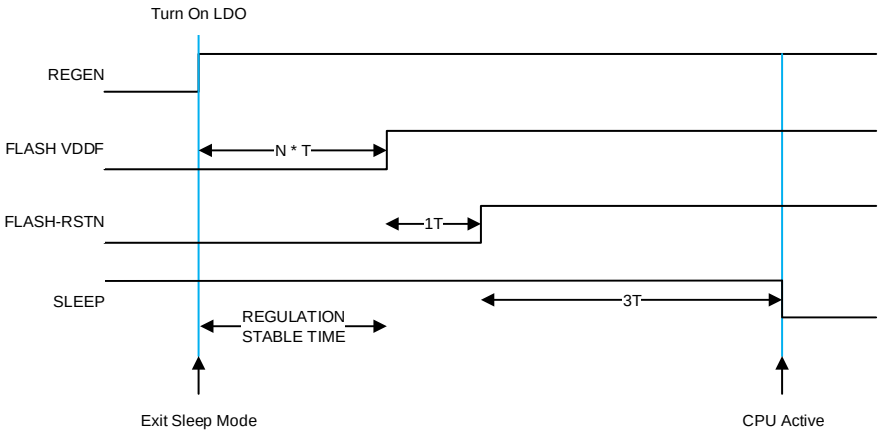


Figure 21-1 Regulator Control Timing

21.2 Precision Internal Oscillator (IOSC)

The internal oscillator provides the default clock after reset. The internal oscillator has the salient feature that allows for functionality during the enable and disable transient phase. No clock glitches or extra clock edge is generated during the on/off transition, and the oscillator can reach to a stable oscillation state within 10 cycles. The IOSC consumes around 300uA when enabled. IOSC is always enabled except when it enters into STOP/SLEEP mode. In STOP/SLEEP mode it is disabled, IOSC consumes less than 0.1uA of standby current.

Similar to the on-chip regulator, IOSC exhibits chip-to-chip variations. A calibrated value that sets IOSC at 16MHz/32MHz +/- 1% is stored in IFB. The user program can set this value to IOSC trimming register, IOSCITRM (A001h) and IOSCVTRM (A002h). The IOSC frequency has very little variations over the operation range (-40°C– 85°C and VDDH = 2.5V – 5.5V). The variation is typically less than +/-1.5% over the operation conditions (-40°C– 85°C), less than +/-1.0% over the temperature range (0°C– 50°C). It is possible that user program to set a different frequency as long as the user program provide a calibration method to set the IOSC frequency, and it will be stable and accurate over the entire operating range. Please note that the trimming register will be set to a default value after reset, therefore, the trimming register must reinitialize to its calibrated value.

The IOSC features Spread Spectrum. Spread Spectrum (SS) attenuates unwanted EMI emissions enabling the IS3X310 to pass EMI compliance testing. The SS is programmable to various ranges. However, once SS is enabled, IOSC accuracy cannot be maintained.

IOSCITRM (0x4000_F200) IOSC Coarse Trim Register R/W (0x01)

	7	6	5	4	3	2	1	0
RD	SSC[3-0]				SSA[1-0]		-	
WR	SSC[3-0]				SSA[1-0]		-	

SSC[3-0] SSC[3-0] defines the spread spectrum sweep rate. If SSC[3-0] = 0000, then the spread spectrum is disabled.

SSA[1-0] SSA[1-0] defines the amplitude of spread spectrum frequency change. The frequency is changed by adding SSA[1-0] range to actual IOSCVTRM[7-0].
SSA[1-0] = 11, +/- 32
SSA[1-0] = 10, +/- 16
SSA[1-0] = 01, +/- 8
SSA[1-0] = 00, +/- 4

IOSCVTRM (0x4000_F201) IOSC Fine Trim Register R/W (0x80)

	7	6	5	4	3	2	1	0
RD	IOSCVTRM[7-0]							
WR	IOSCVTRM[7-0]							

This register provides fine trimming of the IOSC frequency. The higher the value of IOSCVTRM, the lower the frequency is.

IOSCPDIV (0x4000_F204) IOSC Post Divider Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	-		ITRM[2-0]			IOSCPDIV[2-0]		
WR	-		ITRM[2-0]			IOSCPDIV[2-0]		

ITRM[2-0] ITRM[2-0] is the coarse trimming of the IOSC.

IOSCDIV[2-0] IOSC Post Divider

IOSCPDIV[2-0]	IOSC Output
0	IOSC
1	IOSC/2
2	IOSC/4
3	IOSC/6
4	IOSC/8
5	IOSC/10
6	IOSC/12

IOSCPDIV[2-0]	IOSC Output
7	IOSC/16

The manufacturer trim value is stored in IFB and is trimmed to 16MHz/32MHz. The user program provides the freedom to set the IOSC at a preferred frequency as long as the program is able to calibrate the frequency. Once set, the IOSC frequency has accuracy deviation within +/- 2% over the operation conditions. The following lists the range of the typical IOSC frequency for each trimming setting.

ITRM[2-0] = 2'b111 , IOSCCLK =36.7---48.53MHz

ITRM[2-0] = 2'b110 , IOSCCLK =31.86---42.08MHz

ITRM[2-0] = 2'b101 , IOSCCLK =26.8---35.51MHz

ITRM[2-0] = 2'b100 , IOSCCLK =21.57---28.71MHz

ITRM[2-0] = 2'b011 , IOSCCLK =25.05---33.22MHz

ITRM[2-0] = 2'b010 , IOSCCLK =19.76---26.35MHz

ITRM[2-0] = 2'b001 , IOSCCLK =14.24---19.1MHz

ITRM[2-0] = 2'b000 , IOSCCLK =8.43---11.38MHz

A hardware Spread Spectrum can be enabled for the IOSC. This is controlled by SSC[3-0]. When SSC[3-0] = 0, the spread spectrum is disabled, and IOSC functions normally as a fixed frequency oscillator. If SSC[3-0] is not 0, then Spread Spectrum is enabled and IOSC frequency is swept according to the setting of SSC[3-0] and SSA[1-0]. The spread is achieved by varying the actual VTRM output to the oscillator circuit thus effectively changes the oscillation frequency. The effect of SSC[3-0] and SSA[1-0] is shown in the following graph.

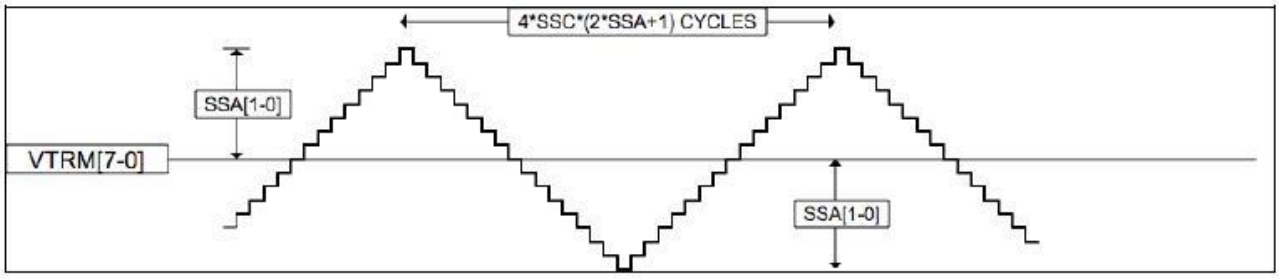


Figure 21-2 Spread Spcetrum Curve

When Spread Spectrum is enabled, the actual controlling output to IOSC is VTRM[7-0] +/- SSA. This is shown in the graph above as the bold curve. The above example shows SSA[1-0] = 01, and the deviation is +/- 8. SSC[3-0] defines the update time in IOSC cycles. Then we can calculate the period of a complete sweep is 4*SSC*(2SSA+1) IOSC cycles, and we can obtain the sweep frequency from this period. When SS is enabled, the frequency of IOSC varies according to time and setting, therefore, the accuracy of IOSC frequency cannot be guaranteed. Please also note that VTRMOUT is VTRM[7-0] +/- SSA but is bounded by 0 and 255. Therefore for a linear non-clipped sweep, VTRM[7-0] needs to be within the range of SSA – 256-SSA, for example, SSA[10] = 01, then SSA is 8. VTRM[7-0] should be in the range from 8 to 248 to prevent the sweep from being clipped. As Spread Spectrum suggests, the total EMI energy is not reduced, but the energy is spread over wider frequency. It is recommended that SS usage should be carefully evaluated and the setting of spread amplitude and the sweep frequency should be chosen carefully for reducing EMI effect.

21.3 SOSC

An ultralow power 128KHz is featured for use as a wake-up or a sleep mode system clock. SOSC is always enabled and consumes 1uA. The SOSC frequency is temperature dependent and varies by +/- 30% over the operating range. It can be trimmed using the SOSCTRM register.

SOSCTRM (0x4000_F300) SOSC Trim Register R/W (0x08)

	7	6	5	4	3	2	1	0
RD	-			SOSCTRM[4]	SOSCTRM[3-0]			
WR	-			SOSCTRM[4]	SOSCTRM[3-0]			

SOSCTRM[4] 256KHz Select
If SOSCTRM[4]=1, SOSC oscillator centers at 256KHz.
If SOSCTRM[4]=0, SOSC oscillator centers at 128KHz.

SOSCTRM[3-0] SOSC Trim Setting
SOOSCTRM[3-0] is used to fine tune the oscillation frequency.

SOSC32KHz is 32KHz to ensure consistent timing based on SOSC. The implementation is shown as the following block diagram.

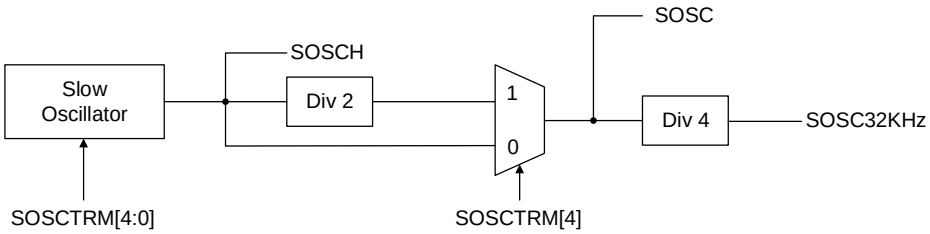


Figure 21-3 SOSC VS. SOCK32K

21.4 Supply Low Voltage Detection (LVD)

The supply Low Voltage Detection (LVD) circuit detects for when VDDH < VTH and can be used to generate an interrupt or reset. LVD defaults to a disabled state to save power. An enabled LVD circuit consumes100uA to 200uA. The LVDTHD[6-0] sets the compare threshold according to the following equation when LVDTHV is the detection voltage.

LVDTHV = VD15 * (1 + 2 * (1 – LVDTHD[6-0]/128)

= 1.5 + 3 * (1 – LVDTHD[6-0]/128), if VD15 is calibrated to 1.5V.

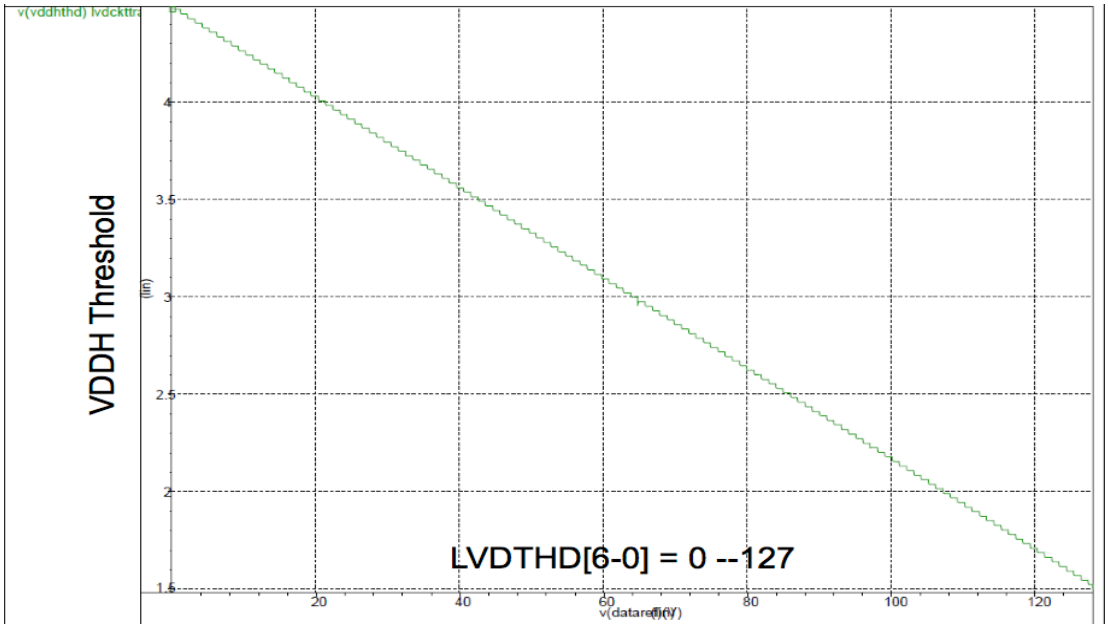


Figure 21-4 LVD Threshold

LVDCFG (0x4000_F700) Low Voltage Detection Configuration Register RW (0xA0)

	7	6	5	4	3	2	1	0
RD	LVDEN	LVREN	LVTEN	LVDFLTEN	-	-	-	LVTIF
WR	LVDEN	LVREN	LVTEN	LVDFLTEN	-	-	-	LVTIF

LVDEN LVD Enable bit. Set to turn on supply voltage detection circuits.
LVREN LVR Enable bit. LVREN = 1 allows low voltage detect condition to cause a system reset.
LVTEN LVT Enable bit. LVTEN = 1 allows low voltage detect condition to generate an interrupt.
LVDFLTEN LVD Filter Enable
LVDFLTEN = 1 enables a noise filter on the supply detection circuits. The filter is set at around 30usec.
LVTIF Low Voltage Detect Interrupt Flag

LVTIF is set by hardware when LVD detection occurs and must be cleared by software writing 1.

LVDTHD (0x4000_F704) LVD Threshold Register R/W (0x7F)

	7	6	5	4	3	2	1	0
RD	-	LVDTHD6	LVDTHD5	LVDTHD4	LVDTHD3	LVDTHD2	LVDTHD1	LVDTHD0
WR	-	LVDTHD6	LVDTHD5	LVDTHD4	LVDTHD3	LVDTHD2	LVDTHD1	LVDTHD0

LVDTHD = 00 will set the detection threshold at its maximum (approximately 4.5V), and LVDTHD = 7F will set the detection threshold at its minimum.

LVDHYS (0x4000_F708) LVD Threshold Hysteresis Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	LVDHYEN	LVDHYS6	LVDHYS5	LVDHYS4	LVDHYS3	LVDHYS2	LVDHYS1	LVDHYS0
WR	LVDHYEN	LVDHYS6	LVDHYS5	LVDHYS4	LVDHYS3	LVDHYS2	LVDHYS1	LVDHYS0

To ensure a solid Low Voltage detect, a digital controlled hysteresis is used. If LVDHYEN=1, when LVD is asserted a new threshold defined by LVDHYS[6-0] replaces LVDTHD[6-0]. In typical applications, LVDHYS[6-0] should be set to be smaller than LVDTHD[6-0] such that the recovery voltage is higher than detection voltage.

Please note LVDCFG, LVDTHD, and LVDHYS are set to their default values only with power-on-reset or its equivalent. Other reset condition does not restore these to their default values.

22. 12-Bit SAR ADC

The on-chip 12-bit SAR ADC has a maximum clock frequency of 4MHz and is typically 1MHz. The ADC has two full-scale reference selections, where the internal VD15 (1.5V typical) used as a reference, or external reference, ADCREF though pin input. The external reference level should be higher than 2.0V, and VDDH must be higher than ADCREF by 1.0V.

When enabled, the ADC consumes 1mA. ADC accuracy is 9.5 to 10 bits. Accuracy degrades to 8.5-bit to 9-bit if the input is between 0 to 0.25V.

There are seven intrinsic input channels of ADC, CHA is further connected to GPIO's analog I/O switches to expand multiplexed inputs. The PVDDS, is PVDD sample voltage. The TEMPOUT, is connected to external temperature sensors and can be further selected using a positive temperature coefficient source of a diode-connected NPN, or a negative temperature coefficient source derived from band-gap reference. The PGAOUT, is connected to PGA module. The DACTOADC, is connected to 10 bit DAC module. The VPS, is connected to 1/5th of VDDH for measuring the supply voltage. The VCS, is connected to Current Sink of led driver measuring the Current sink drop voltage. There is a T/H front-end of ADC input and can be set to enable or bypass.

ADC conversion can be software or hardware triggered. Hardware trigger sources include TC1 and TC2 CC events, and PWM Center and Zero events. The conversion takes 14 to 16 ADCCLK cycles. The conversion results can go through hardware 1 to 8 conversion cycles.

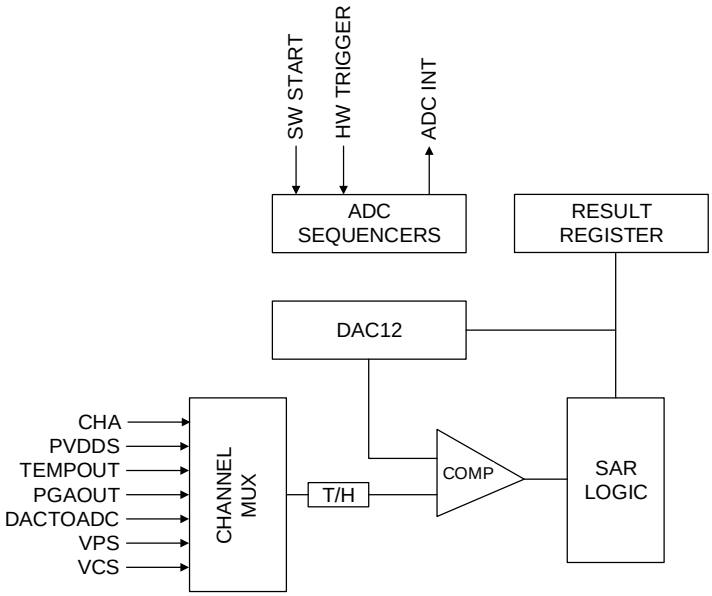


Figure 22-1 ADC Block Diagram

ADCCFG0 (0x4000_E000) ADC Configuration Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	ADCEN	ADCCS[2-0]			TRGTC2	TRGTC1	TRGPT	TRGPZ
WR	ADCEN	ADCCS[2-0]			TRGTC2	TRGTC1	TRGPT	TRGPZ

ADCEN — ADC Enable bit
ADCEN=1 enables ADC.
ADCEN=0 puts ADC into power down mode.
When ADCEN is set from 0 to 1, the program needs to wait at least 20us to allow analog bias to stabilize to ensure ADC's proper functionality.

ADCCS[2-0] — ADC Clock Divider

ADCCS[2-0]	ADC CLOCK
0	SYSCLK/2
1	SYSCLK/4
2	SYSCLK/8
3	SYSCLK/16
4	SYSCLK/32

ADCCS[2-0]	ADC CLOCK
5	SYSCLK/64
6	SYSCLK/128
7	SYSCLK/256

TRGTC2 TC2 CC Event Trigger Enable
TRGTC1 TC1 CC Event Trigger Enable
TRGPT PWM Trigger Event Trigger Enable
TRGPZ PWM Zero Event Trigger Enable

ADCCFG1 (0x4000_E001) ADC Configuration Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	REFSEL	-	-	-	-	-	INATTEN	TRGPC
WR	REFSEL	-	-	-	-	-	INATTEN	TRGPC

REFSEL ADC Reference Select
REFSEL=0 ADC uses internal VD15 1.5V as reference
REFSEL=1 ADC uses external ADCREF as reference
INATTEN INATTEN=0 ADC uses normal input
INATTEN=1 ADC input will attenuate to half value
TRGPC PWM Center Event Trigger Enable

ADCCTLA (0x4000_E004) ADC Control Register A R/W (0x00)

	7	6	5	4	3	2	1	0
RD	AVG[1-0]		CHSEL[2-0]			SHEN	ADCINTE	BUSY
WR	AVG[1-0]		CHSEL[2-0]			SHEN	ADCINTE	CSTART

AVG[1-0] AVG[2-0] controls the hardware averaging logic of ADC readout. It is recommended the setting is changed only when ADC is stopped. If multiple channels are enabled, then each channel is averaged in sequence. The default is 00.

AVG1	AVG0	ADC Result
0	0	1 Times Average
0	1	2 Times Average
1	0	4 Times Average
1	1	8 Times Average

CHSEL[2-0] ADC Channel Select

CHSEL[2]	CHSEL[1]	CHSEL[0]	ADC Channel
0	0	0	CHA
0	0	1	PVDDS
0	1	0	TEMPOUT
0	1	1	PGAOUT
1	0	0	DACTOADC
1	0	1	VPS
1	1	0	VCS
1	1	1	NC.

SHEN Sample and Hold Enable
SHEN=0 Pass Through
SHEN=1 2 ADCCLK
ADCINTE ADC Interrupt Enable
BUSY ADC Status
BUSY is set to 1 by hardware when ADC is in conversion.
CSTART Software Start Conversion bit

Set this CSTART=1 to trigger an ADC conversion on selected channels. This bit is self-cleared when the conversion is done.

ADCCTLB (0x4000_E005) ADC Control Register B R/W (0x00)

	7	6	5	4	3	2	1	0
RD	ADCT2F	ADCT1F	ADCPTF	ADCPZF	ADCPCF	-	-	ADCIF
WR	-	-	-	-	-	-	-	ADCIF

ADCT2F — TC2 Trigger Completion Flag
ADCT2F is set by hardware if the completed conversion is triggered by TC2.

ADCT1F — TC1 Trigger Completion Flag
ADCT1F is set by hardware if the completed conversion is triggered by TC1.

ADCPTF — PWM Trigger Completion Flag
ADCPTF is set by hardware if the completed conversion is triggered by PWM trigger setting.

ADCPZF — PWM Zero Trigger Completion Flag
ADCPZF is set by hardware if the completed conversion is triggered by PWM zero.

ADCPCF — PWM Center Trigger Completion Flag
ADCPCF is set by hardware if the completed conversion is triggered by PWM Center.

ADCIF — ADC Conversion Completion Interrupt Flag bit
ADCIF is set by hardware when conversion complete. If ADC interrupt is enabled, this also generates an interrupt. This bit must be cleared by software writing 1. Clearing ADCIF also clears all flags.

ADCDAT (0x4000_E008) ADC Result Register RO (0x00)

	31-12	11-0
RD	-	ADCDATA[11-0]
WR	-	

Note 1. If ADC is in conversion and another start or trigger is initiated, the result is undefined. Typically, the new start and trigger are ignored.

23. 12-Bit CR SAR ADC

The on-chip CR SAR ADC is a 12-bit ADC with ADC clock rate of 16MHz. The ADC has two full-scale reference selections, where the internal VD15 (1.5V typical) is used a as an internal reference. An external reference uses ADCREF though an input pin. VDDH must be equal or higher than ADCREF.

When enabled, the ADC consumes 1.1mA. ADC accuracy is 10.5 bits. Accuracy degrades to 8.5-bits to 9-bits if the input is between 0 to 0.25V. There are seven intrinsic input channels of ADC, CHA is further connected to GPIO's analog I/O switches to expand multiplexed inputs. PVDD is a sampled voltage. TEMPOUT is connected to an external temperature sensor and can be further selected using a positive temperature coefficient source. A diode-connected NPN, or a negative temperature coefficient source derived from band-gap reference can be utilized. The PGAOUT, is connected to PGA module. VD15 is used for measuring the supply voltage. VPS, is connected to 1/5th of VDDH for measuring the supply voltage. VCS, is connected to a LED driver c and can be used to measure the current sink and voltage drop. There is a T/H front-end of ADC input and can be set to enable or bypass.

ADC conversion can be software or by hardware triggered. Hardware trigger sources include TC1 and TC2 CC events, and PWM Center and Zero events. The conversion takes 15 to 22 ADCCLK cycles. The conversion result can go through hardware averaging of 1 to 8 conversions.

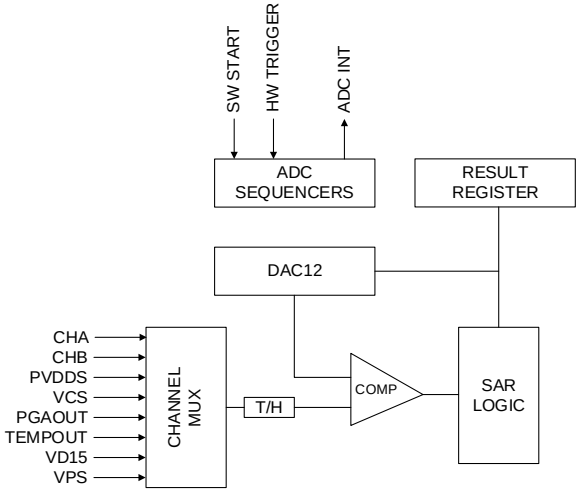


Figure 23-1 CR ADC Block Diagram

CRADCCFG0 (0x4000_E300) ADC Configuration Register 0 R/W (0x30)

	7	6	5	4	3	2	1	0
RD	ADCEN	ADCCS[2-0]			OFS[1-0]		TCSEL	ADCINTE
WR	ADCEN	ADCCS[2-0]			OFS[1-0]		TCSEL	ADCINTE

ADCEN — ADC Enable bit

ADCEN=1 enables ADC.

ADCEN=0 puts ADC into power down mode.

When ADCEN is set from 0 to 1, the program needs to wait at least 20us to allow analog bias to stabilize to ensure ADC's proper functionality.

ADCCS[2-0] — ADC Clock Divider

ADCCS[2-0]	ADC CLOCK
000	SYSCLK/2
001	SYSCLK/4
010	SYSCLK/6
011	SYSCLK/8(Default)
100	SYSCLK/10
101	SYSCLK/12
110	SYSCLK/14
111	SYSCLK/16

OFS[1-0] ADC Offset Adjust
This adjusts ADC S/H offset error.
TCSEL Temperature Sensor Select
ADCINTE ADC Interrupt Enable

CRADCCFG1 (0x4000_E301) ADC Configuration Register 1 R/W (0x07)

	7	6	5	4	3	2	1	0
RD	REFSEL[1-0]		-	-	-	SHTM[2-0]		
WR	REFSEL[1-0]		-	-	-	SHTM[2-0]		

REFSEL[1-0] ADC Reference Select
REFSEL=00 Internal VD15 1.5V as reference
REFSEL=01 External ADCREF as reference
REFSEL=10 Use VDDH as reference
REFSEL=11 Reserved

SHTM[2-0] Sample Time Setting
SHTM[2-0]=000 1 ADCCLK
SHTM[2-0]=001 2 ADCCLK
SHTM[2-0]=010 3 ADCCLK
SHTM[2-0]=011 4 ADCCLK
SHTM[2-0]=100 5 ADCCLK
SHTM[2-0]=101 6 ADCCLK
SHTM[2-0]=110 7 ADCCLK
SHTM[2-0]=111 8 ADCCLK(Default)
Sample time needs to longer than 250nsec for CHA/CHB, and for other channels longer than 500nsec is preferred.

CRADCCFG2 (0x4000_E302) ADC Configuration Register 2 R/W (0x00)

	7	6	5	4	3	2	1	0
RD	-	-	TRGTC2	TRGTC1	-	TRGPT	TRGPC	TRGPZ
WR	-	-	TRGTC2	TRGTC1	-	TRGPT	TRGPC	TRGPZ

TRGTC2 TC2 CC Event Trigger Enable
TRGTC1 TC1 CC Event Trigger Enable
TRGPT PWM Trigger Event Trigger Enable
TRGPC PWM Center Event Trigger Enable
TRGPZ PWM Zero Event Trigger Enable

CRADCCTLA (0x4000_E304) ADC Control Register A R/W (0x00)

	7	6	5	4	3	2	1	0
RD	AVG[1-0]		CHSEL[2-0]			-	BUSY	CSTART
WR	AVG[1-0]		CHSEL[2-0]			-	-	CSTART

AVG[1-0] AVG[2-0] controls the hardware averaging logic of ADC readout. It is recommended the setting is changed only when ADC is stopped. If multiple channels are enabled, then each channel is averaged in sequence. The default is 00.

AVG1	AVG0	ADC Result
0	0	1 Times Average
0	1	2 Times Average
1	0	4 Times Average
1	1	8 Times Average

CHSEL[2-0] ADC Channel Select

CHSEL[2]	CHSEL[1]	CHSEL[0]	ADC Channel	Comments	Typical
0	0	0	CH0	0 – 5V	CHA
0	0	1	CH1	0 – 5V	CHB(NC)

CHSEL[2]	CHSEL[1]	CHSEL[0]	ADC Channel	Comments	Typical
0	1	0	CH2	0 – 1.5V	PVDDS
0	1	1	CH3	0 – 1.5V	VCS
1	0	0	CH4	0 – 1.5V	PGAOUT
1	0	1	CH5	0 – 1.5V	TEMPOUT
1	1	0	VD15 internal	0 – 1.5V	VD15
1	1	1	1/5 VDDH internal	0 – 1.5V	-

CHSEL should not be changed during conversion.

BUSY — ADC Status
BUSY is set to 1 by hardware when ADC is in conversion.

CSTART — Software Start Conversion bit
Set this CSTART=1 to trigger an ADC conversion on selected channels. This bit is self-cleared when the conversion is done.

CRADCCTLB (0x4000_E305) ADC Control Register B R/W (0x00)

	7	6	5	4	3	2	1	0
RD	ADCT2F	ADCT1F	ADCPTF	ADCPZF	ADCPCF	-	BUSYTO	ADCIF
WR	-	-	-	-	-	-	-	ADCIF

ADCT2F — TC2 Trigger Completion Flag
ADCT2F is set by hardware if the completed conversion is triggered by TC2.

ADCT1F — TC1 Trigger Completion Flag
ADCT1F is set by hardware if the completed conversion is triggered by TC1.

ADCPTF — PWM Trigger Completion Flag
ADCPTF is set by hardware if the completed conversion is triggered by PWM trigger setting.

ADCPZF — PWM Zero Trigger Completion Flag
ADCPZF is set by hardware if the completed conversion is triggered by PWM zero.

ADCPCF — PWM Center Trigger Completion Flag
ADCPCF is set by hardware if the completed conversion is triggered by PWM Center.

BUSYTO — Busy Time Out
If BUSY is high longer than 32 ADCCLK, an interrupt is generated (if ADCINTE=1). This is a fail-safe mechanism in case the state machine in ADC runs wild.
To reset the ADC, ADCEN should be cleared to 0 and then set to 1.

ADCIF — ADC Conversion Completion Interrupt Flag bit
ADCIF is set by hardware when conversion complete. If ADC interrupt is enabled, this also generates an interrupt. This bit must be cleared by software writing 1. Clearing ADCIF also clears all flags.

CRADCDAT (0x4000_E308) ADC Result Register RO (0x0000)

	31-12	11-0
RD	-	ADCDATA[11-0]
WR	-	

Please note, if ADC is in conversion and another start or trigger is initiated, the result is undefined. Typically, the new start and trigger is ignored.

24. Programmable Gain Amplifier

The programmable gain amplifier provides two gain settings of 5 or 10. It can serve as a differential to single-ended signal conversion and used for high-side voltage measurements. A R2R DAC is used to adjust the PGA output offset. PGAINN is connected to ADCINA bus, and PGAINP is connected to ADCINB bus. The output of the PGA is fed into ADC's input. The OP Amp used in PGA has PMOS differential input. Therefore, the common-mode input of PGAINN and PGAINP is limited to (VDDH – 1.2V) to 0V.

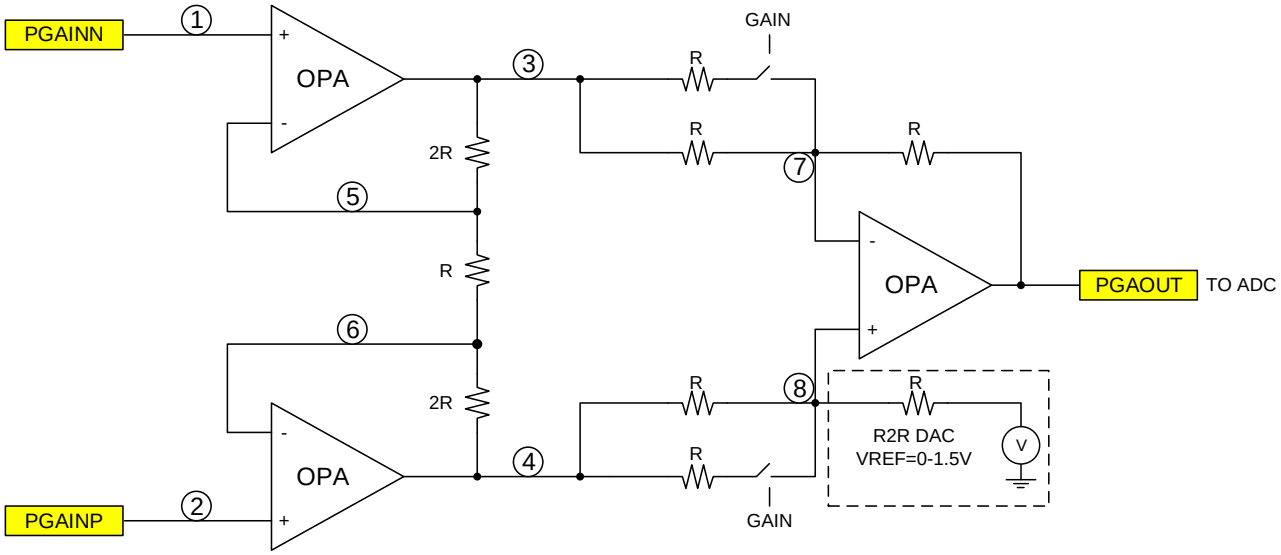


Figure 24-1 PGA Block Diagram

PGACFGA (0x4000_E220) PGA Configuration Register A R/W (0x00)

	7	6	5	4	3	2	1	0
RD	PGAEN	GAIN	-	-	INNSEL[1-0]		INPSEL[1-0]	
WR	PGAEN	GAIN	-	-	INNSEL[1-0]		INPSEL[1-0]	

PGAEN PGA Enable bit
GAIN Gain setting
GAIN=1 sets PGA gain to 10
GAIN=0 sets PGA gain to 5
INNSEL[1-0] PGA input select
00 = PGAINN
01 = force to 0V
10 = force to VD15 (1.5V)
11 is not allowed.
INPSEL[1-0] PGA input select
00 = PGAINP
01 = force to 0V
10 = force to VD15 (1.5V)
11 is not allowed.

PGACFGB (0x4000_E224) PGA Configuration Register B R/W (0x00)

	7	6	5	4	3	2	1	0
RD	VRDAC[7-0]							
WR	VRDAC[7-0]							

VRDAC[7-0] VREF for offset adjustment

25. Analog Comparator and DAC10, DAC8 for DCDC Output Control

There are three analog comparators. When enabled, each comparator consumes 250uA. The input signal range is from 0 to VDDH. There are one 8-bit R-2R DAC(DAC0) associated with the comparators to generate the compare threshold. There is another 10-bit R-2R DAC(DAC1) whose output range is adjustable. VTH1 is also sent to a gain adjustable buffer for use an DAC output. The buffer can supply or sink up to 150uA. Individual comparator when enabled consumes about 80uA/each, and the unity gain buffer consumes about 600uA/1.5mA under 5V supply conditions.

There is an 8-bit R-2R current DAC(DAC2) to control DCDC output. The output of this DAC connects to FB node through an output PIN.

The CPU can read the real-time outputs of the comparator directly through register access. The output is also sent to an edge-detector, and any edge transition can be used to trigger an interrupt. The stabilization time from off state to enabled state of the comparator block is 20us. The block diagram of the analog comparator is shown in the following diagram.

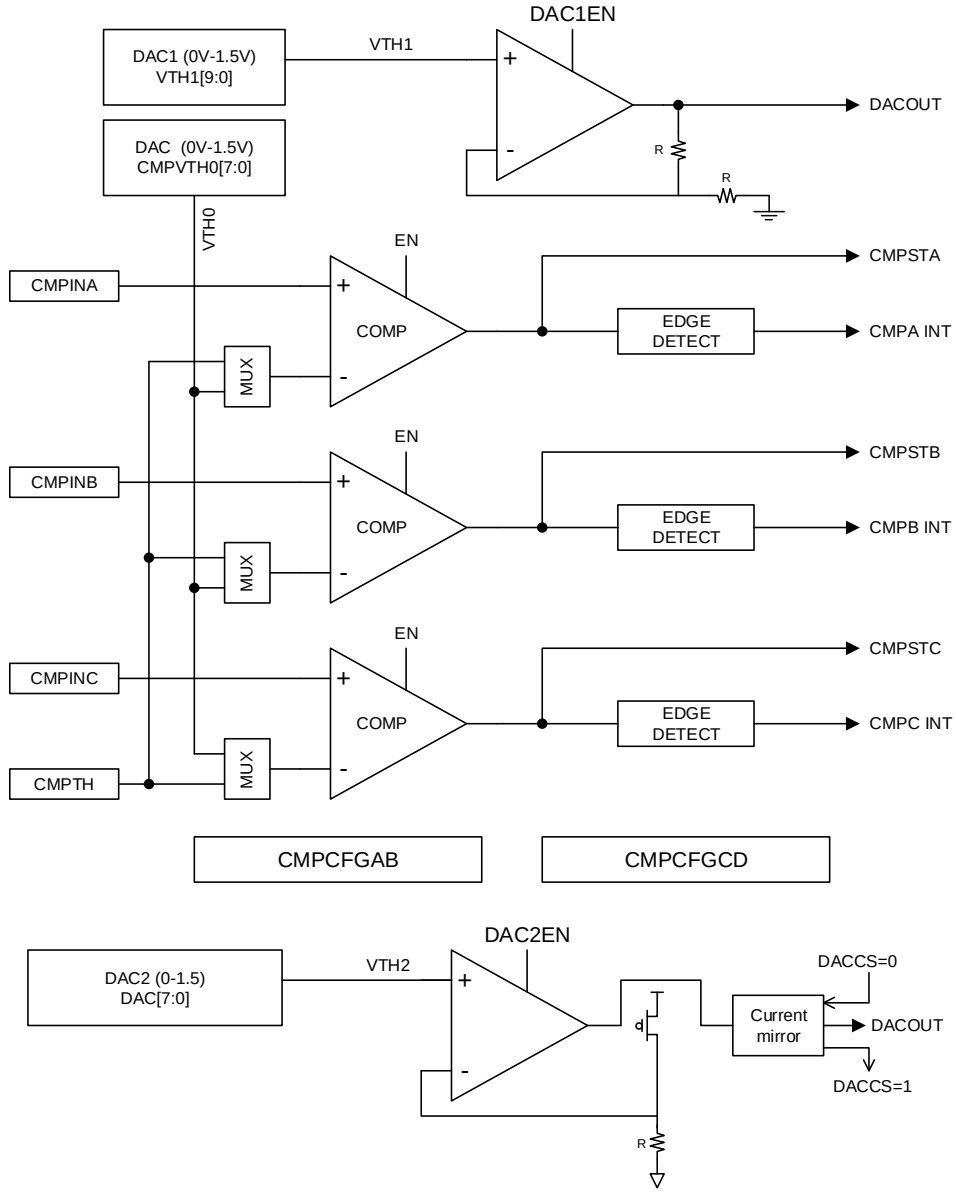


Figure 25-1 DAC and Comparator Block Diagram

CMPCFGAB (0x4000_D000) Analog Comparator A/B Configuration Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	CMPENA	THSELA	INTENA	-	CMPENB	THSELB	INTENB	-
WR	CMPENA	THSELA	INTENA	-	CMPENB	THSELB	INTENB	-

CMPENA — Comparator A Enable bit. Set to enable the comparator.
When CMPENA is set from 0 to 1, the program needs to wait at least 20us allowing analog bias to stabilize to ensure comparator A's proper functionality.

THSELA — Comparator A Threshold Select bit. THSELA = 0, the comparator A uses VTH0 as the threshold. THSELA = 1, the comparator A uses external threshold.

INTENA — Set to enable the comparator A's interrupt.

CMPENB — Comparator B Enable bit. Set to enable the comparator.
When CMPENB is set from 0 to 1, the program needs to wait at least 20us allowing analog bias to stabilize to ensure comparator B's proper functionality.

THSELB — Comparator B Threshold Select Bit. THSELB = 0, the comparator B uses VTH0 as the threshold. THSELB = 1, the comparator B uses external threshold.

INTENB — Set to enable the comparator B's interrupt.

CMPCFGCD (0x4000_D001) Analog Comparator C Configuration Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	CMPENC	THSELC	INTENC	-	-	-	-	TEMPCMPSEL
WR	CMPENC	THSELC	INTENC	-	-	-	-	TEMPCMPSEL

CMPENC — Comparator C Enable Bit. Set to enable the comparator.
When CMPENC is set from 0 to 1, the program needs to wait at least 20us to allow analog bias to stabilize to ensure comparator C's proper functionality.

THSELC — Comparator C Threshold Select Bit. THSELC = 0, the comparator C uses VTH0 as the threshold. THSELC = 1, the comparator C uses external threshold.

INTENC — Set to enable the comparator C interrupt.

TEMPCMPSEL — Comparator C input selection Bit. TEMPCMPSEL=1 Comparator C input will select temperature sensor output. TEMPCMPSEL=0 Comparator C input will select external input from GPIO.

DAC1L (0x4000_D004) Analog Comparator Threshold Control Register R/W (0xFF)

	7	6	5	4	3	2	1	0
RD	VTH1[7-0]							
WR	VTH1[7-0]							

DAC1H (0x4000_D005) Analog Comparator Threshold Control Register R/W (0x03)

	7	6	5	4	3	2	1	0
RD	-	-	DACCMPTEST[2-0]			SMEN	VTH1[9-8]	
WR	-	-	DACCMPTEST[2-0]			SMEN	VTH1[9-8]	

DAC1L and DAC1H register controls the comparator threshold VTH1 through 10-bit DAC

VTH1[7-0] =0x00h, VTH1 [9-8] =0x00h the threshold is 0V.

VTH1[7-0] =0xFFh, VTH1 [9-8] =0x03h the threshold is 1.5V.

When not used, VTH1 [7-0] =0x00h, VTH1 [9-8] =0x00h, to save power consumption.

DACCMPTEST — DACCMP's test mode.it can send the analog signal to ADC for testing.
DACCMPTEST[2-0]=000 When not used, it should be set to 000 to prevent it from interfering whit ADC.
DACCMPTEST[2-0]=001 select DACOUT connect to ADC's CH input internally. This needs software to perform DAC output and ADC conversion.
DACCMPTEST[2-0]=010 select DAC1TEST connect to ADC's CH input internally. This needs software to perform DAC output and ADC conversion.
DACCMPTEST[2-0]=100 select DAC0TEST connect to ADC's CH input internally. This needs software to perform DAC output and ADC conversion.

SMEN — Control switch for comparator in low-power mode
SMENA=0, turn off low-power mode.
SMENA=1, turn on low-power mode.

DAC0 (0x4000_D006) Analog Comparator Threshold Control Register R/W (0xFF)

	7	6	5	4	3	2	1	0
RD	VTH0 [7-0]							
WR	VTH0 [7-0]							

DAC0 register controls the comparator threshold VTH0 through 8-bit DAC

VTH0 [7-0] =0x00h, the threshold is 0V.

VTH0 [7-0] =0xFFh, the threshold is at 1.5V.

When not used, it should be set to 0x00h to save power consumption.

CMPST (0x4000_D008) Analog Comparator Status Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	-	CMPIFC	CMPIFB	CMPIFA	-	CMPSTC	CMPSTB	CMPSTA
WR	-	CMPIFC	CMPIFB	CMPIFA	-	FILENC	FILENB	FILENA

CMPIFC — Comparator C Interrupt Flag bit. This bit is set when CMPSTC is toggled and the comparator C setting is enabled. This bit must be cleared by software writing 1.
CMPIFB — Comparator B Interrupt Flag bit. This bit is set when CMPSTB is toggled and the comparator B setting is enabled. This bit must be cleared by software writing 1.
CMPIFA — Comparator A Interrupt Flag bit. This bit is set when CMPSTA is toggled and the comparator A setting is enabled. This bit must be cleared by software writing 1.
CMPSTC — Comparator C Real-time Output. If the comparator is disabled, this bit is forced low.
FILENC — Comparator C Digital Filter Enable. Filter is 16 SYSCLK.
CMPSTB — Comparator B Real-time Output. If the comparator is disabled, this bit is forced low.
FILENB — Comparator B Digital Filter Enable. Filter is 16 SYSCLK.
CMPSTA — Comparator A Real-time Output. If the comparator is disabled, this bit is forced low.
FILENA — Comparator A Digital Filter Enable. Filter is 16 SYSCLK.

DAC2 (0x4000_D009) DAC2 input Register R/W (0xFF)

	7	6	5	4	3	2	1	0
RD	VTH2[7-0]							
WR	VTH2[7-0]							

DAC2 — controls the output voltage of DAC2
When set to 0x00h, the VTH2 is 0V.
When set to 0xFFh, the VTH2 is at 1.5V.

When not used, it should be set to 0x00h to save power consumption.

DACTRIM (0x4000_D00A) DAC1 voltage (DACOUT) TRIM Register and DAC2 current (DACIOUT) TRIM Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	DACOUTTRIM[3-0]				-	-	DACIOUTTRIM[1-0]	
WR	DACOUTTRIM[3-0]				-	-	DACIOUTTRIM[1-0]	

DACOUTTRIM — controls the output voltage of DACOUT
0001 DACOUT=0-1.5V
0010 DACOUT=0-3V
0100 DACOUT=0-5V
1000 DACOUT=0-VDDH

DACIOUTTRIM — controls the feedback resistance value of DAC2
10 adjustment range(0-15uA)
01 adjustment range(0-7.5uA)

DACCFG (0x4000_D00C) Analog Comparator Status Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	DAC1EN	VDDCCMPA	-	DAC2EN	DACCS	HYSENC	HYSENB	HYSENA
WR	DAC1EN	VDDCCMPA	-	DAC2EN	DACCS	HYSENC	HYSENB	HYSENA

DAC1EN	DAC1 Enable DAC1EN=1 turns on the DAC1 output buffer. DAC1EN=0 turns off the output buffer
VDDCCMPA	Force CMPINA as VD15. VDDCCMPA = 1, connect CMPINA to VD15. This is for testing purpose only. By connecting VD15 to CMPINA and GPIO ANIO switch, VD15 is exposed on GPIO pin so testing and trimming of VD15 can be done.
DAC2EN	DAC2 Enable DAC2EN=1 turns on the current output DAC2. DAC2EN=0 turns off the current output DAC2.
DACCS	control whether the DACIOUT(DAC2) pull (drop) current to (from) DACIOUT DACCS=1 source current to output DACCS=0 sink current from output
HYSENC	Comparator C Hysteresis Disable HYSENC = 1 disables the hysteresis of Comparator C HYSENC = 0 enables the hysteresis (typical 10mV) of Comparator C.
HYSENB	Comparator B Hysteresis Disable HYSENB = 1 disables the hysteresis of Comparator B HYSENB = 0 enables the hysteresis (typical 10mV) of Comparator B.
HYSENA	Comparator A Hysteresis Disable HYSENA = 1 disables the hysteresis of Comparator A HYSENA = 0 enables the hysteresis (typical 10mV) of Comparator A.

26. DCFB

LED PVDD voltage can be self-adaptive by different VF of LED. This function needs IS3XCS9310 cooperate with DCDC chip. The DCFB function diagram is below:

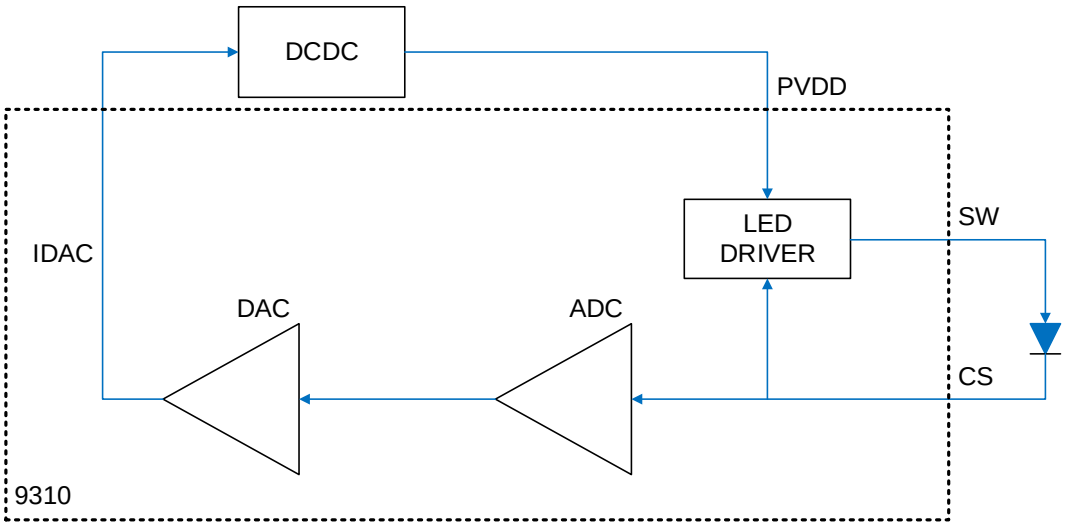


Figure 26-1 DCFB Function diagram

In this diagram, DCFB functionality includes a LED driver, 12-bit SAR ADC and 8-bit IDAC. The 12-bit ADC quantifies the CS voltage, then the internal MCU handles the 12-bit ADC quantized value. If the quantized value is within the scope of CS changing from 0.5V to 0.8V, the output of DCDC does not change. If the quantized value is outside the scope of CS, the MCU controlling the 8-bit IDAC output current to changes the FB of DCDC, so the PVDD output of DCDC changes to maintain the CS voltage to within the scope of 0.5V to 0.8V. When the quantized value is under the minimum set value of the CS voltage or over the maximum set value of CS voltage, the MCU does not respond.

When DCFB initiales, these registers should be set, as CRADCCFG0 (0x4000_E100) =1011,0000, CRADCCFG1 (0x4000_E101) =01xx,x111, CRADCCTLA (0x4000_E104) =0001,1001, ADCDAT (0x4000_E108) =0000,0000,0000, ADCMINDATL(0x4001_1000) =0000,0000,0000, CSADCTHL(0x4001_1004) = 0111,0000, CSADCHYS(0x4001_1008) =0001,0100, CSADCMAX(0x4001_1010) =1100,0000,0000, CSADCMIN(0x4001_1012) =0001,0001,0000. The 12-bit ADC starts to work by delaying to 1us to positive of PWM of SWx; The 12bit ADC quantifies the voltage of CS, then the internal MCU 12bit ADC quantizes the value to ADCDAT.

ADCMINDATL (0x4001_1000) CS 12bit ADC MIN DATA Low 8bit Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	ADCMINDAT[7-0]							
WR	ADCMINDAT[7-0]							

ADCMINDAT[7-0] Low 8bit VCS Minimum DATA from 12bit ADC

ADCMINDATH (0x4001_1001) CS 12bit ADC MIN DATA High 4bit Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	-	-	-	-	ADCMINDAT[11-8]			
WR	-	-	-	-	ADCMINDAT[11-8]			

ADCMINDAT[11-8] High 4bit VCS Minimum DATA from 12bit ADC

CSADCTHL (0x4001_1004) CS 12bit ADC THRESHOLD DATA Low 8bit Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	CSADCTH[7-0]							
WR	CSADCTH[7-0]							

CSADCTH[7-0] 8bit Threshold Value to Compare for CS

CSADCHYS (0x4001_1008) CS 12bit ADC HYSTERESIS DATA Low 8bit Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	CSADCHYS[7-0]							
WR	CSADCHYS[7-0]							

CSADCHYS[7-0] 8bit Hysteresis Value to Compare for CS

CSADCMAXL (0x4001_1010) CS 12bit ADC MAX DATA Low 8bit Register R/W (0xFF)

	7	6	5	4	3	2	1	0
RD	CSADCMAX[7-0]							
WR	CSADCMAX[7-0]							

CSADCMAX[7-0] Low 8bit VCS Minimum SET Value to Compare for CS

CSADCMAXH (0x4001_1011) CS 12bit ADC MAX DATA High 4bit Register R/W (0x0F)

	7	6	5	4	3	2	1	0
RD	-	-	-	-	CSADCMAX [11-8]			
WR	-	-	-	-	CSADCMAX [11-8]			

CSADCMAX[11-8] High 4bit VCS Minimum SET Value to Compare for CS

CSADCMINL (0x4001_1012) CS 12bit ADC MIN DATA Low 8bit Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	CSADCMIN[7-0]							
WR	CSADCMIN[7-0]							

CSADCMIN[7-0] Low 8bit VCS Maximum SET Value to Compare for CS

CSADCMINH (0x4001_1013) CS 12bit ADC MIN DATA High 4bit Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	-	-	-	-	CSADCMIN[11-8]			
WR	-	-	-	-	CSADCMIN[11-8]			

CSADCMIN[11-8] High 4bit VCS Maximum SET Value to Compare for CS

CSADCCFGA (0x4001_1014) CS 12bit ADC Configuration Register A R/W (0x00)

	7	6	5	4	3	2	1	0
RD	DACSOFT				ADCSEL	DCFBINTEN	LPEN	DACEN
WR	DACSOFT				ADCSEL	DCFBINTEN	LPEN	DACEN

DACSOFT Software can trigger the calculation of DAC data processing.
ADCSEL 0: 12-bit SAR ADC to sample the VCS. 1: 12-bit CRADC to sample the VCS
DCFBINTEN Enable the interrupt when the ADC complete one scan loop
LPEN ADC sampling mode. 0: one time scan. 1: continuous scan mode
DACEN Enable the calculation of DAC data processing

CSADCCFGB (0x4001_1015) CS 12bit ADC Configuration Register B R/W (0x00)

	7	6	5	4	3	2	1	0
RD	LPDLY							
WR	LPDLY							

LPDLY The ADC scan and measure the VCS for all LEDs, then get the Vmin and start DAC process. The delay time before next ADC scan can be set by this register.

CSADCCFGC (0x4001_1016) CS 12bit ADC Configuration Register C R/W (0x30)

	7	6	5	4	3	2	1	0
RD	PWMWAIT				ADCCYC			
WR	PWMWAIT				ADCCYC			

PWMWAIT The delay for ADC sample and hold point after the PWM rising edge. Delay=(n+1)X4

ADCCYC ADC cycle sample period

CSADCCFGD (0x4001_1017) CS 12bit ADC Configuration Register D R/W (0x00)

	7	6	5	4	3	2	1	0
RD							ADCMINF	ADCDONEF
WR							ADCMINC	ADCDONEC

ADCMINF ADC has get the minimum VCS in one scan loop
ADCMINC write 1 clear the ADCMINF flag
ADCDONEF The flag is set after ADC has scanned all VCS
ADCDONEC write 1 clear the ADCDONEF flag

CSSCANA (0x4001_101C) ADC Scan channel select Register A R/W (0xFF)

	7	6	5	4	3	2	1	0
RD	CSSEL[7-0]							
WR	CSSEL[7-0]							

CSSEL[7-0] Low 8bit SET Value to Choose channel for CS
1: Enable the selected one CS channel to ADC measure

Note: Only one bit can be set to 1 in CSSEL[11-0].

CSSCANB (0x4001_101D) ADC Scan channel select Register B R/W (0x0F)

	7	6	5	4	3	2	1	0
RD					CSSEL[11-8]			
WR					CSSEL[11-8]			

CSSEL[11-8] High 4bit SET Value to Choose channel for CS
1: Enable the selected one CS channel to ADC measure

CSSCANC (0x4001_101E) ADC Scan channel select Register C R/W (0xFF)

	7	6	5	4	3	2	1	0
RD	SWSEL[7-0]							
WR	SWSEL[7-0]							

SWSEL[7-0] 1: Enable the selected SW channel to ADC measure

27. Touch Key Control

The Gen 3 touch key (TK3) is an enhancement over TK2 featuring a differential dual slope operation. The capacitance to time conversion goes through two phase of charge transfer, phase one is used to charge and phase two is used to discharge the capacitors using two thresholds equally spaced at ½ VD15. Each charge transfer is obtained by subtracting charge on the internal reference capacitor and key capacitor. The difference of charge/discharge count is used to determine the key capacitance change ratio of the internal capacitance. Improved noise immunity from power and ground noise and common-mode noise is achieved by a dual slope operation. Better signal to noise ratio (S/N) can also be achieved because only differential charge is used for transfer, and the internal capacitance exhibits improved temperature and environmental stability making the conversion less sensitive to change.

CREF, the integration capacitor of the charge transfer, is connected to P10 through ANIO multiplexer and CKEY is connected to another GPIO pin through a multiplexer. A replica signal of CKEY is provided through a buffer and routed out as SHIELD through GPIO pins. The shield signal can be used to cancel mutual capacitance effect from neighboring signal trace of the detected key and provides better noise immunity against moisture or water.

To detect a key press, the duty count value TKLDT[15-0] or TKHDT[15-0] can be processed by software and compared with an average non-press duty count. The hardware can also be configured to auto repeat accumulation of the duty cycle count to filter sporadic noise. Since the comparator output is random duty with averages equal to the capacitance ratio, low frequency noise is rejected. For high frequency noise rejection, the hardware includes a pseudo-random sequence that randomizes the charge and discharge timing sequences. A slow-moving average duty count value is stored within TKBASE[15-0] and the software can use this for baseline calculation to auto compensate for environment change.

Issuing a START command in the TK3CFGD register starts a conversion sequence that accumulates the comparator output into a count value. The count value and the total number of the cycle of the sequence can then be calculated to obtain the key capacitance. The TK3 timing diagram in normal operation is shown in the following diagram. CREF is first equalized to VREFX that is VREF. When a START command is issued, the first few edges of the comparator output are ignored to avoid any noise caused by the VREFX switching. Then the compactor output accumulates into DTYL and DTYH registers. A sequence can consist of several conversion cycles depending on the RPT setting, and DTYL and DTYH maintain accumulation to obtain higher resolutions. After the sequence is completed, CREF is connected to VREFX for the next sequence to start.

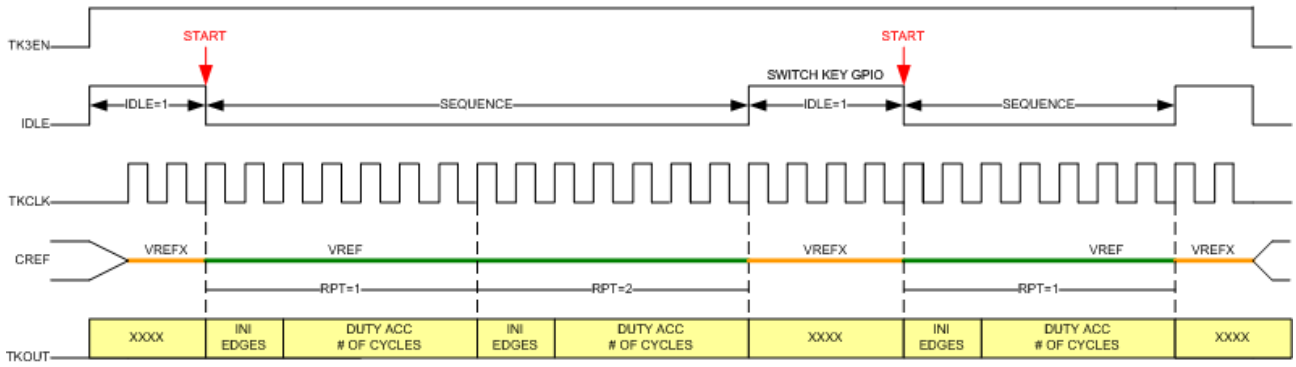


Figure 27-1 Touch Key Control Timing

TK3 can be set into low power auto detect mode by setting the AUTO bit in TK3CFGA. In this mode, an ultra-low power comparator is used and the TK3 clock should be set to SOSC (128KHz). This mode can be used for touch key wakeup during sleep mode. The total TK3 power consumption in this mode is less than 5uA. A threshold register can be set to determine the auto detect threshold either as an absolute value or relative value versus the slow-moving baseline value. When the duty count value exceeds the threshold value, a wakeup and interrupt is generated to the CPU. The timing diagram for auto mode detection and entering into SLEEP mode is shown in the following diagram. Note the actual start of the sequence is delayed by AUTO START DELAY setting. This allows the internal VD15 to stabilize from switching normal mode to sleep mode supply regulators.

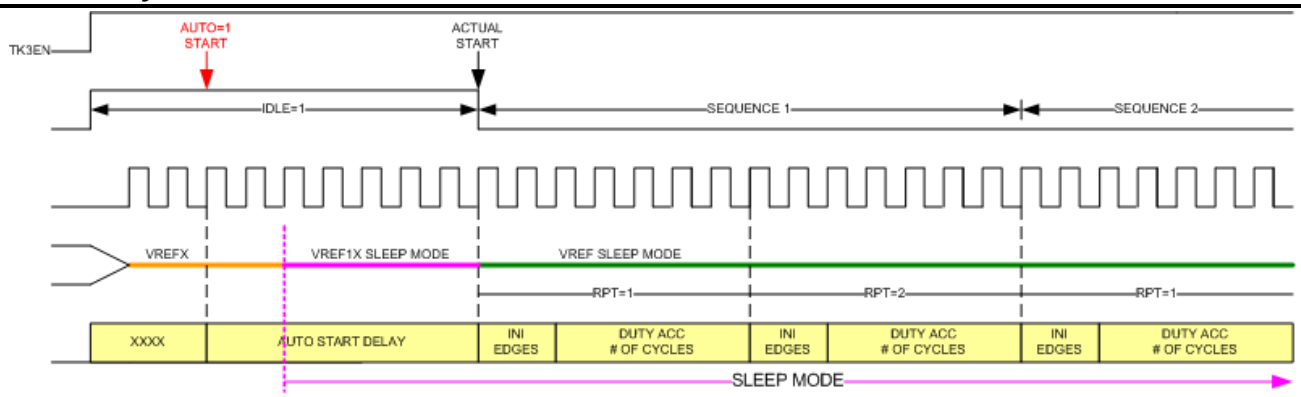


Figure 27-2 Touch Key Control Timing In Sleep Mode

TK3CFGA (0x4000_C000) TK3 Configuration Register A R/W (0x00)

	7	6	5	4	3	2	1	0
RD	TK3EN	CHOPEN	CMPHYS	REFSEL	SHIELDEN	TKIEN	TKLPM	AUTO
WR	TK3EN	CHOPEN	CMPHYS	REFSEL	SHIELDEN	TKIEN	TKLPM	AUTO

TK3EN — TK3 Enable
TK3EN=0 Disables the TK3 circuits and clear all states
TK3EN=1 for TK3 normal operations.

CHOPEN — Comparator chop Enable.
CHOPEN=0 Disables the chop of comparator input and output.
CHOPEN=1 for comparator chop normal operation.

CMPHYS — Comparator Hysteresis
CMPHYS=0 disables the comparator hysteresis.
CMPHYS=1 enables the comparator hysteresis.
Hysteresis helps immunity to external EMI disturbance, but it also increases the noise under normal condition.

REFSEL — Comparator Reference Select
REFSEL=0 uses ½ VD15 as the reference.
REFSEL=1 uses 2/3VD15 as the reference.
2/3 VD15 has higher EMI immunity but with less dynamic range.

SHIELDEN — Shield Output Buffer Enable
SHIELDEN=1 enables the shield signal buffer. The buffer consumes about 200uA when enabled.

TKIEN — TK3 Interrupt Enable
TKIEN=1 enables the TK3 interrupt. TK3 interrupt is generated when a counting sequence is completed (including the repeat count if RPT[1-0] is not 00). Interrupt and wakeup are also generated when TKIEN=1 and AUTO=1 after auto detection threshold is met.
When TK3 interrupt is generated, TKIF is also set to 1 by hardware.

TKLPM — TK3 Low Power Mode
TKLPM=0 for normal mode operations.
TKLPM=1 put the comparator into ultra-low power mode and should be used in auto wakeup power saving mode. In this mode, TKCLK should use SOSC/2 slow clock.

AUTO — Auto Wake Up Mode
AUTO=1 enables auto detect mode. Writing START with “1” initiate continuous automatic key detect. In auto mode, the current duty count register value is compared with baseline plus threshold (either absolute or relative). If duty count value is higher, an interrupt and wakeup is generated.
AUTO=0 enable normal detect mode. In normal mode, writing START with “1” initiates a conversion sequence, and when the duty count is obtained, an interrupt is generated.

TK3CFGB (0x4000_C001) TK3 Configuration Register B R/W (0x00)

	7	6	5	4	3	2	1	0
RD	RPT[1-0]		INI[1-0]		ASTDLY[1-0]		LFNF[1-0]	
WR	RPT[1-0]		INI[1-0]		ASTDLY[1-0]		LFNF[1-0]	

RPT[1-0] Repeat Sequence Count
00 = No Repeat
01 = 4 times
10 = 8 times
11 = 16 times

INI[1-0] Discard Starting Comparator Edges
The number of initial comparator output edges is ignored when each sequence starts for better stable response. The number is (INI[1-0] + 1) *4. These edges are not included in the DTY count and the cycle count.

ASTDLY[1-0] Auto Mode Start Delay
STDLY[1-0] inserts an inter-sequence idle time of (ASTDLY[1-0]+1) * 256 TKCLK at each sequence start. This delay allows the stabilization time of VREFX from normal mode to sleep mode.

LFNF[1-0] Low Frequency Noise Filter Setting
00 = disables LFNF
Comparator output after staying continuous either “0” or “1” longer than LFNF[1-0]*8 is ignored in duty counter.

TK3CFGC (0x4000_C002) TK3 Configuration Registers C R/W (0x00)

	7	6	5	4	3	2	1	0
RD	SLOW[1-0]		CYCLE[2-0]			BASEINI	THDSEL	AUTOLFEN
WR	SLOW[1-0]		CYCLE[2-0]			BASEINI	THDSEL	AUTOLFEN

SLOW[1-0] Baseline Slow Moving Average setting
00 = 32 average
01 = 64 average
10 = 128 average
11 = 256 average
The duty value is averaged by SLOW[1-0] conversion and updated to BASELINE register through moving average.

CYCLE[2-0] Cycle Count of each conversion sequence
000 = 1024
001 = 2048
010 = 4096
011 = 8192
100 = 12288
101 = 16384
110 = 32768
111 = 65536
The cycle count is each sequence cycle count. And it is repeated if RPT is not 0.

BASEINI Baseline Initial Value
If BASEINI=1, then the first DTYL count after entering auto mode is loaded to BASELINE register as its initial value to start moving average.
If BASEINI=0, then the value written in BASELINE before entering auto mode is used as the initial value to start moving average.

THDSEL Threshold Value Setting
THDSEL=0 uses TKTHD[15-0] as the threshold to compare with DTYL to generate the interrupt and wakeup
THDSEL=1 uses TKTHD[15-0] + TKBASE[15-0] as the threshold.

AUTOLFEN Low Frequency Noise Filtering in Auto mode
If AUTOLFEN=0, then low frequency noise filtering in Auto mode is disabled.
If AUTOLFEN=1, then low frequency noise filtering in auto mode is enabled.

The low noise filtering status flag is still valid regardless of AUTOLFEN setting. Software can determine if to discard the current conversion result by checking LFNF flag.

TK3CFGD (0x4000_C003) TK3 Configuration Register D R/W (0x00)

	7	6	5	4	3	2	1	0
RD	-	CHOPDIV2	CHOPSEL	ASEN	TKCS[3-0]			
WR	-	CHOPDIV2	CHOPSEL	ASEN	TKCS[3-0]			

CHOPDIV2 CHOP flip frequency selection when CHOPEN=1
CHOPDIV2=1 TKCLK/2
CHOPDIV2=0 TKCLK/4

CHOPSEL CHOP value select when CHOPEN=0
CHOPSEL=1 CHOP=1
CHOPSEL=0 CHOP=0

ASEN Asymmetric Clock Enable
ASEN=1 uses asymmetric clock for charge sharing
ASEN=0 uses symmetric clock for charge sharing
ASEN is only meaningful when SYSCLK is the clock source.

TKCS[3-0] TK3 Clock Select
TKCS[3-0]=0000 SYSCLK/4, ASEN controlled
TKCS[3-0]=0001 SYSCLK/8, ASEN controlled
TKCS[3-0]=0010 SYSCLK/16, ASEN controlled
TKCS[3-0]=0011 SYSCLK/20, ASEN controlled
TKCS[3-0]=0100 SYSCLK/24, ASEN controlled
TKCS[3-0]=0101 SYSCLK/32, ASEN controlled
TKCS[3-0]=0110 SYSCLK/64, ASEN controlled
TKCS[3-0]=0111 SYSCLK/128, ASEN controlled
TKCS[3-0]=Other Reserved
TKCS[3-0]=1110 SOSC/2 (64KHz)
TKCS[3-0]=1111 SOSC/4 (32KHz)
SOSC/2 should be used for sleep mode auto wakeup. Typical SOSC/2 is 64KHz.

TK3CRA (0x4000_C004) TK3 Control Registers A R/W (0x00)

	7	6	5	4	3	2	1	0
RD	CCHG[2-0]			ASTDLYEN	PSRDEN	LFNF	TKIF	BUSY
WR	CCHG[2-0]			ASTDLYEN	PSRDEN	LFNF	TKIF	START

CCHG[2-0] Charge Capacitance Setting
CCHG[0] = 10pf
CCHG[1] = 20pF
CCHG[2] = 40pF
Charge capacitance is used to compensate the parasitic capacitance of the key. The setting can be key specific and should be set along with DC pull-up and CSEN[1-0] (Sensing Capacitance) to obtain a reasonable duty count in 25% to 80% of full count.

ASTDLYEN Auto Start Delay Enable
ASTDLYEN=1 enables ASTDLY[1-0] delay start for auto mode.
ASTDLYEN=0 disables ASTDLY[1-0] delay.

PSRDEN Pseudo Random Sequence Enable
PSRDEN=1 enables the random sequence in conversion
PSRDEN=0 disables

LFNF Low Frequency Noise Detection Flag
LFNF is set by hardware if in the present conversion a Low Frequency Noise is detected. Software needs to write LFNF “1” to clear.

TKIF TK3 Interrupt Flag
TKIF is set by hardware when a TK3 interrupt occurred by either conversion sequence completed or a valid detection in auto mode. Software needs to write TKIF “1” to clear.

BUSY	Conversion Status BUSY is set to 1 by hardware indicating the conversion sequences are still running.
START	Start Conversion Writing “1” into START initiates the conversion sequence. It is cleared by hardware when conversion is complete. Please note writing AUTO “1” starts the conversion in auto mode.

A DC pull-up can compensate for the high equivalent pull-down current induced by large parasitic capacitance associated with sensing key due to long signal trace or size of the key. There are two means for providing DC pullup either through resistor or through current source. Typically, resistor option is used for normal mode because switch frequency is high and the pulldown current is large. Current source can be used in auto detection because the switching frequency is low. Pullups along with CCHG[2-0] should be used together to obtain a duty count in a reasonable range.

TK3CRB (0x4000_C005) TK3 Pull-Up Control Register H R/W (0x00)

	7	6	5	4	3	2	1	0
RD	PUIEN	PUREN	CSEN[1-0]		PU[3-0]			
WR	PUIEN	PUREN	CSEN[1-0]		PU[3-0]			

PUIEN	Pull-up DC Current Enable
PUREN	Pull-up DC Resistor Enable
CSEN[1-0]	Sensing Capacitance Setting ΔC_{KEY}/CSEN is represented in the change of duty count. Therefore, the smaller CSEN is the higher the sensitivity of the touch key detection. An intrinsic CSEN of 5pF is always there. CSEN[1-0] adds CSEN to larger value to reduce the sensitivity in case of noisy environment. CSEN[0] adds 5pF. CSEN[1] adds 10pF. The maximum CSEN is thus 20pF.
PU[3-0]	Pull-Up Selection For DC current, PU[3-0] enables 8uA/4uA/2uA/1uA current source. For Resistor, PU[3-0] enables 5K/10K/20K/40K resistor.

To estimate the compensation effect using DC pull-up through resistors or current source, please use the following estimation. The equivalent pull-down current of $C_{KEY\ PARASITIC}$ is $F_{TK} * C_{KEY\ PARASITIC}$. The pull-up current using resistor is VD15 (1.5V) – VREF (either 2/3 VD15 or ½ VD15). For example, if $C_{KEY\ PARASITIC}$ is 100pF, then the equivalent current is 100uA for TCK of 1MHz. If VREF is selected as 2/3 VD15, the a equivalent 5K is needed to compensate. This can be roughly achieved by putting 5K.

TK3HDTYL (0x4000_C008) TK3 High Duty Count Register L RO (0x00)

	7	6	5	4	3	2	1	0
RD	TK3HDTY[7-0]							
WR	-							

TK3HDTY[7-0]	High Duty Count Storage The lower 8 bits of output high level count register.

TK3HDTYH(0x4000_C009) TK3 High Duty Count Register H RO (0x00)

	7	6	5	4	3	2	1	0
RD	TK3HDTY[15-8]							
WR	-							

TK3HDTY[15-8]	High Duty Count Storage The higher 8 bits of output high level count register, high duty count starts to accumulate with cycle count, Max is 65535.

TK3LDTYL (0x4000_C00C) TK3 Low Duty Count Register L RO (0x00)

	7	6	5	4	3	2	1	0
RD	TK3LDTY[7-0]							
WR	-							

TK3LDTY[7-0] Low Duty Count Storage
The lower 8 bits of output low level count register.

TK3LDTYH(0x4000_C00D) TK3 Low Duty Count Register H RO (0x00)

	7	6	5	4	3	2	1	0
RD	TK3LDTY[15-8]							
WR	-							

TK3LDTY[15-8] Low Duty Count Storage
The lower 8 bits of output low level count register, low duty count starts to accumulate with cycle count, Max is 65535.

TK3BASEL (0x4000_C010) TK3 Baseline Register L R/W (0x00)

	7	6	5	4	3	2	1	0
RD	TK3BASE[7-0]							
WR	TK3BASE[7-0]							

TK3BASEL[7-0] Baseline Count Storage
The lower 8 bits of baseline number register.

TK3BASEH (0x4000_C011) TK3 Baseline Register H R/W (0x00)

	7	6	5	4	3	2	1	0
RD	TK3BASE[15-8]							
WR	TK3BASE[15-8]							

TK3BASE[15-8] Baseline Count Storage
The higher 8 bits of baseline number register, the baseline reference count number is hardware updated using moving average, it can be set by an initial value or use the first duty count result.

TK3THDL (0x4000_C014) TK3 Threshold Register L R/W (0x00)

	7	6	5	4	3	2	1	0
RD	TK3THD[7-0]							
WR	TK3THD[7-0]							

TK3THD[7-0] Threshold Storage
The lower 8 bits of threshold register.

TK3THDH(0x4000_C015) TK3 Threshold Register H R/W (0x00)

	7	6	5	4	3	2	1	0
RD	TK3THD[15-8]							
WR	TK3THD[15-8]							

TK3THD[15-8] Threshold Storage
The higher 8 bits of threshold register. It is compared with difference of actual cycle count and baseline for software control.

28. Active Proximity Sensor

The active proximity sensor uses mutual capacitance sensing by driving a transmit electrode and sensing the electric field change at the receive electrode. This is shown as the following illustrations.

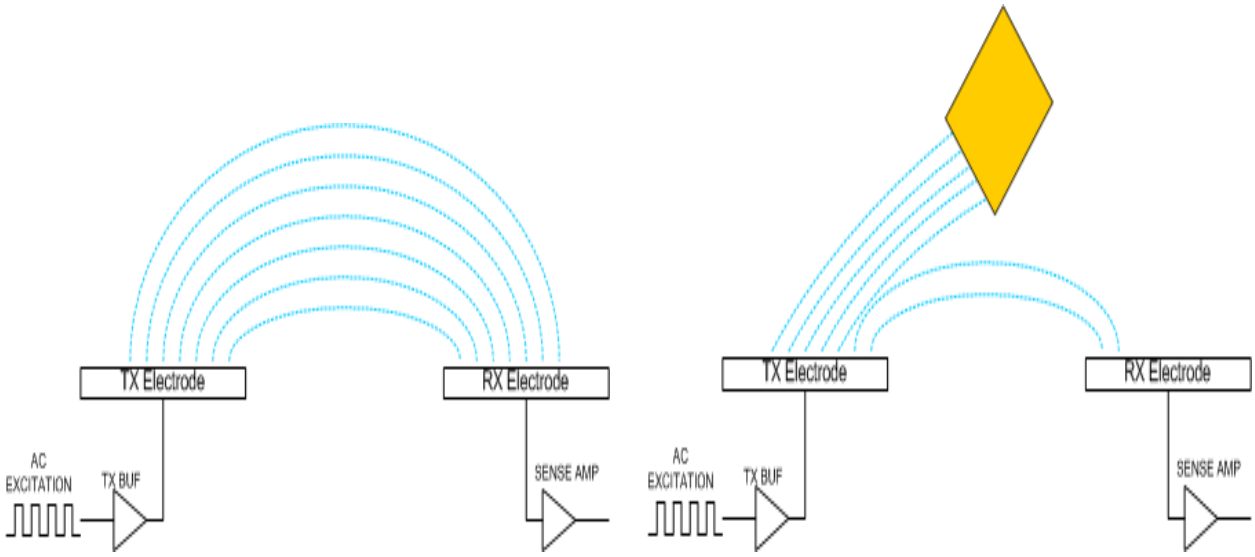


Figure 28-1 Mutual Capacitance Proximity Sensor

On the left, an AC excitation voltage is driving the TX electrode which leads to an electric field established between the TX and RX electrode. When a mass-conductive object such as finger approaches, the flux lines between the electrodes are disturbed. Using a charge sense amplifier, the change of flux lines can be amplified and used for proximity sensing. In the diagram, if the distance between TX and RX electrode is increased, then detection is increased. It is intuitive that larger TX amplitudes leads to increased detection.

The proximity sensor is tightly coupled to the Touch Key controller. It consists of an excitation waveform generator, and a synchronous charge amplifier is followed by a programmable amplifier and serves as a sense amplifier. The output of the sense amplifier is connected as an input to the Touch Key Controller and Touch Key Controller is used to detect the change of sense amplifier output as proximity detections. The excitation signal operates between 32KHz to 128KHz. Since PS is at the same clock domain with Touch Key controller, setting Touch Key clock determines the excitation frequency. The Touch Key clock is 64KHz (typ).

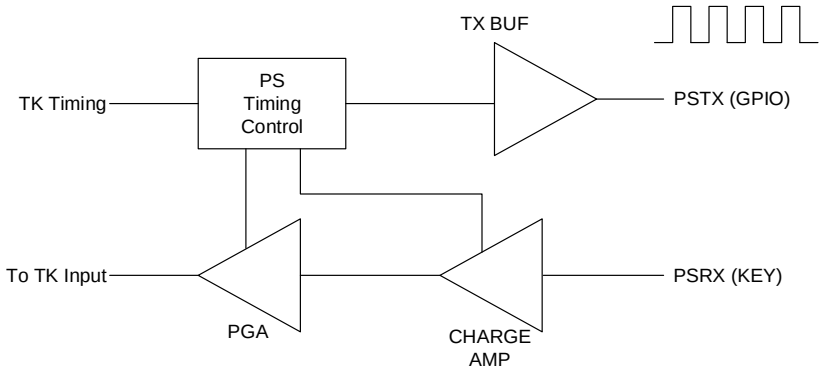


Figure 28-2 Active Proximity Sensing Block Diagram

Please note the output PSTX is routed to externally through the multi-function select of the GPIO. Hence any GPIO pin can be used for PSTX purposes. The input PSRX shares the ANIO multiplexer and is used for Touch Key input. Therefore any pin can be configured as an Active Proximity Sense (APS) input through ANIO1.

APSCFGA (0x4000_C100) Active Proximity Sensor Configuration Register A R/W (0x00)

	7	6	5	4	3	2	1	0
RD	APSEN	RXCAL[6-0]						
WR	APSEN	RXCAL[6-0]						

APSEN Active PS Enable

APSEN=1 enables the APS. If APS is enabled, the TK controller is connected to PS output.

RXCAL[6-0] Receive Electrode Capacitance Calibration

RXCAL is used to adjust the cancelation of the parasitic capacitance on RX electrode. Each bit controls one of the binary weighted capacitance array.

RXCAL[0]=43fF
RXCAL[1]=86fF
RXCAL[2]=172fF
RXCAL[3]=344fF
RXCAL[4]=688fF
RXCAL[5]=1376fF
RXCAL[6]=2752fF
The range is 43fF to 5.4pF.

APSCFGB (0x4000_C101) Active Proximity Sensor Charge Amplifier Configuration Register B R/W (0x00)

	7	6	5	4	3	2	1	0
RD	CREFSEL[3-0]				CAGAIN[3-0]			
WR	CREFSEL[3-0]				CAGAIN[3-0]			

CREFSEL[3-0] Output Charge Capacitance Setting

This is equivalent of CCHG setting of TK controller.
Each bit of CREFSEL[3-0] selects a binary weighted capacitor array.
CREFSET[0]=115fF
CREFSET[1]=230fF
CREFSET[2]=460fF
CREFSET[3]=920fF
CREFSET[3-0]=0000 is not allowed.
Ideally, CREF should be set to between 400fF to 800fF.

CAGAIN[3-0] Charge Amplifier Gain Setting

Charge Amplifier is always enabled when PS is enabled.
Each bit of CAGAIN[3-0] selects a binary weighted capacitor array for the feedback capacitor of the charge amplifier. The ratio of mutual capacitance between TX/RX electrodes and the feedback capacitor determines the gain of the charge amplifier. The smaller the feedback capacitance, the gain is higher however noise is higher too.
CAGAIN[0]= 86fF
CAGAIN[1]= 172fF
CAGAIN[2]= 344fF
CAGAIN[3]= 688fF
The range is from 86fF to 1290fF.

APSCFGC (0x4000_C102) Active Proximity Sensor PGA Configuration Register C R/W (0x00)

	7	6	5	4	3	2	1	0
RD	PGAEN	PC[2-0]			PGASET[3-0]			
WR	PGAEN	PC[2-0]			PGASET[3-0]			

PGAEN 2nd Stage PGA Enable

PC[2-0] Power Control Setting

PC[2-0] sets the power consumption of the charge amplifier and PGA. Each bit turns on one of the binary weighted current sources. The higher the setting results higher power and faster speed when parasitic receive capacitance is high which requires faster settling time of the amplifiers.
PC[0]=0.3uA
PC[1]=0.6uA
PC[2]=1.2uA
PC[2-0]=000 is not allowed.

PGASET[3-0] Charge Amplifier Setting

GAIN = 8/(4*PGASET[3] + 2*PGASET[2] + PGASET[1] + PGASET[0])
Maximum gain is 8 when PGASET[3-0]=0001 or 0010.

Minimum gain is 1 when PGASET[3-0]=1111
PGASET[3-0]=0000 is not allowed.
Charge Amplifier is always enabled when PS is enabled.

APSCFGD (0x4000_C103) Active Proximity Sensor PGA Configuration Register D R/W (0x00)

	7	6	5	4	3	2	1	0
RD	-	FRXCAL[2-0]			PSLOAD[3-0]			
WR	-	FRXCAL[2-0]			PSLOAD[3-0]			

FRXCAL[2-0] Fine RXCAL
FRXCAL[0] = 20fF
FRXCAL[1] = 40fF
FRXVAL[2] = 80fF

PSLOAD[3-0] Charge Amplifier Output Load Setting
PSLOAD[0] = 120fF
PSLOAD[1] = 240fF
PSLOAD[2] = 480fF
PSLOAD[3] = 960fF

29. GPIOs

Each GPIO port pin is configured by a 32-bit register which can be byte-accessed. The configuration includes its port data/flag manipulation, interrupt configuration, I/O drive configuration, and multi-function select.

GPIO00A (0x5000_2000) GPIO P00 Register A R/W (0x00)

	7	6	5	4	3	2	1	0
RD	RIF	FIF	-	IOERF	PINDB	PIN	-	POUT
WR	RIF	FIF	-	IOERF	-	-	PS[1-0]	

RIF — Rising edge interrupt flag
Write 1 to clear.

FIF — Falling edge interrupt flag
Writing 1 to clear.

IOERF — IO Compare Error flag
Write 1 to clear.

PINDB — Debounced input state

PIN — Input state

POUT — Current registered output value

PS[1-0] — POUT Set/Clear
00 – unchanged
01 – set POUT=1
10 – clear POUT=0
11 – toggle POUT

GPIO00B (0x5000_2001) GPIO P00 Register B R/W (0x00)

	7	6	5	4	3	2	1	0
RD	INTREN	INTFEN	-		DBEN	FAST	INEN	IPOL
WR	INTREN	INTFEN	-		DBEN	FAST	INEN	IPOL

INTREN — Input Rising Edge Interrupt Enable (Debounced Input)

INTFEN — Input Falling Edge Interrupt Enable (Debounced Input)

DBEN — De-Bounce Enable
DBEN=1 enables de-bounce of 3 SYSCLK. This is automatically turned off during sleep/stop mode.
DBEN=0 turns off de-bounce.

FAST — Output Buffer Speed Control
FAST=1 enables output buffer in fast mode. This allows up to 20MHz output. However, this will cause larger ground bounce thus creating more noise.
FAST=0 put output buffer in slow mode. This allows up to 8MHz.

INEN — Input Buffer Enable
INEN=1 enables the input buffer.
INEN=0 disables the input buffer.
In the disabled state, the output of input buffer is logic 0.
If input is floating or not solid 0 and 1 voltage level, DC current may flow in the input buffer. Disabling input buffer can remove DC leakage of input buffer due to this reason.

IPOL — Input Polarity
IPOL=1 reverse the input logic. IPOL=0 for normal logic polarity.

GPIO00C (0x5000_2002) GPIO P00 Register C R/W (0x00)

	7	6	5	4	3	2	1	0
RD	PDRVEN	NDRVEN	IOCMPEN	OPOL	PUEN	PDEN	ANEN2	ANEN1
WR	PDRVEN	NDRVEN	IOCMPEN	OPOL	PUEN	PDEN	ANEN2	ANEN1

PDRVEN — Output PMOS driver enable. Set this bit to enable the PMOS of the output driver. DISABLE is the default value.

NDRVEN — Output NMOS driver enable. Set this bit to enable the NMOS of the output driver. DISABLE is the default value.

IOCMPEN — Input and Output Compare Enable

	IOCMPEN=1 enables comparison of pad output state with input state. The compare status is sampled 2 SYSCLK after output change state. This can be used to detect output short or open. If the comparison is not matched, it generates an interrupt. The flag is shown in IOERF flag bit.
OPOL	Output Polarity Control Output data polarity control.
PUEN	Pull up resistor control. Set this bit to enable pull-up resistor connection to the pin. The pull-up resistor is approximately 6K Ohm. DISABLE is the default value.
PDEN	Pull down resistor control. Set this bit to enable pull-down resistor connection to the pin. The pull-down resistor is approximately 6K Ohm. DISABLE is the default value
ANEN2	Analog MUX 2 enables control. Set this bit to connect the pin to the internal analog peripheral. DISABLE is the default value.
ANEN1	Analog MUX 1 enables control. Set this bit to connect the pin to the internal analog peripheral. DISABLE is the default value.

GPIO00D (0x5000_2003) GPIO P00 Register D R/W (0x00)

	7	6	5	4	3	2	1	0
RD	-	-	MFCFG[5-0]					
WR	-	-	MFCFG[5-0]					

MFCFG[5-0] defines the switch box of peripheral external connections to the GPIO port I/O.

MFCFG[4-0]	Function	Function Description
000000	LOW	This forces the output to logic low state.
000001	GPIO	GPIO port
000010	SCK	SPI1 SCK input or output depending on SPI MS setting.
000011	SDI	SPI1 SDI input corresponding to MI or SI depending on SPI MS setting.
000100	SDO	SPI1 SDO output corresponding to MO or SO depending on SPI MS setting.
000101	SSN	SPI1 SSN input or output depending on SPI MS setting.
000110	SSCL	I^2C Slave 1 SCL I/O
000111	SSDA	I^2C Slave 1 SDA I/O
001000	MSCL	I^2C Master SCL I/O
001001	MSDA	I^2C Master SDA I/O
001010	TX1	EUART1 TX output
001011	RX1	EUART1 RX input
001100	TX2	EUART2/LIN TX output
001101	RX2	EUART2/LIN RX input
001110	BZ/POW	Even port us Buzzer/Melody output. Odd port is POW output.
001111	EXCLK	External system clock input
010000	-	Reserved.
010001	LTX	LMC TX output
010010	LTR	LMC RX input
010011	XCAPT2	TCC2 (Timer Compare/Capture) Capture Input
010100	TC2	TCC2 (Timer Compare/Capture) Terminal Count output
010101	CC2	TCC2 (Timer Compare/Capture) Compare Count output
010110	XCAPT1	TCC1 (Timer Compare/Capture) Capture Input
010111	TC1	TCC1 (Timer Compare/Capture) Terminal Count output
011000	CC1	TCC1 (Timer Compare/Capture) Compare Count output

MFCFG[4-0]	Function	Function Description
011001	PWM01	PWM Channel 0/1*
011010	PWM23	PWM Channel 2/3*
011011	PWM45	PWM Channel 4/5*
011100	PWM67	PWM Channel 6/7*
011101	CLKO	Clock output
011110	PSTX	Proximity sensor TX output
011111	HIGH	This forces the output to logic high state.
1xxxxxx	Special Function	

Note: * For even port number is 0/2/4/6, for odd port number is 1/3/5/7

The following tables lists the GPIO configuration addresses.

GPIO Number	Register Address	GPIO Number	Register Address	GPIO Number	Register Address	GPIO Number	Register Address
GPIO00	5000_2000	GPIO20	5000_2040	GPIO40	5000_2080	GPIO60	5000_20C0
GPIO01	5000_2004	GPIO21	5000_2044	GPIO41	5000_2084	GPIO61	5000_20C4
GPIO02	5000_2008	GPIO22	5000_2048	GPIO42	5000_2088	GPIO62	5000_20C8
GPIO03	5000_200C	GPIO23	5000_204C	GPIO43	5000_208C	GPIO63	5000_20CC
GPIO04	5000_2010	GPIO24	5000_2050	GPIO44	5000_2090	GPIO64	5000_20D0
GPIO05	5000_2014	GPIO25	5000_2054	GPIO45	5000_2094	GPIO65	5000_20D4
GPIO06	5000_2018	GPIO26	5000_2058	GPIO46	5000_2098	GPIO66	5000_20D8
GPIO07	5000_201C	GPIO27	5000_205C	GPIO47	5000_209C	GPIO67	5000_20DC
GPIO10	5000_2020	GPIO30	5000_2060	GPIO50	5000_20A0	GPIO70	5000_20E0
GPIO11	5000_2024	GPIO31	5000_2064	GPIO51	5000_20A4	GPIO71	5000_20E4
GPIO12	5000_2028	GPIO32	5000_2068	GPIO51	5000_20A8	GPIO72	5000_20E8
GPIO13	5000_202C	GPIO33	5000_206C	GPIO53	5000_20AC	GPIO73	5000_20EC
GPIO14	5000_2030	GPIO34	5000_2070	GPIO54	5000_20B0	GPIO74	5000_20F0
GPIO15	5000_2034	GPIO35	5000_2074	GPIO55	5000_20B4	GPIO75	5000_20F4
GPIO16	5000_2038	GPIO36	5000_2078	GPIO56	5000_20B8	GPIO76	5000_20F8
GPIO17	5000_203C	GPIO37	5000_207C	GPIO57	5000_20BC	GPIO77	5000_20FC

Table 29-1 GPIO configuration address table

The port information of GPIO is also grouped for 32-bit access for ease of access and data processing. The following register can be accessed as byte, word, and double word.

GP01OUT (0x5000_2100) GP00-GP07、GP10-GP17、GP20-GP27 and GP30-GP33 Output Register RW (0x00000000)

	31-24	23-16	15-8	7-0
RD	POUT3[7-0]	POUT2[7-0]	POUT1[7-0]	POUT0[7-0]
WR	POUT3[7-0]	POUT2[7-0]	POUT1[7-0]	POUT0[7-0]

GP01IN (0x5000_2104) GP00-GP07、GP10-GP17、GP20-GP27 and GP30-GP33 Input Status Register RO (0x00000000)

	31-24	23-16	15-8	7-0
RD	PIN3[7-0]	PIN2[7-0]	PIN1[7-0]	PIN0[7-0]
WR	-	-	-	-

GP01INDB (0x5000_2108) GP00-GP07、GP10-GP17、GP20-GP27 and GP30-GP33 Debounced Input Status Register RO (0x00000000)

	31-24	23-16	15-8	7-0
RD	PINDB3[7-0]	PINDB2[7-0]	PINDB1[7-0]	PINDB0[7-0]
WR	-	-	-	-

GP01IF (0x5000_2110) GP00-GP07、GP10-GP17、GP20-GP27 and GP30-GP33 Edge Interrupt Flag Register RO (0x00000000)

	31-24	23-16	15-8	7-0
RD	RIF3[7-0]+FIF3[7-0]	RIF2[7-0]+FIF2[7-0]	RIF1[7-0]+FIF1[7-0]	RIF0[7-0]+FIF0[7-0]
WR	-	-	-	-

GP01ERF (0x5000_2124) GP00-GP07、GP10-GP17、GP20-GP27 and GP30-GP33 Compare Mismatch Flag Register RO (0x00000000)

	31-24	23-16	15-8	7-0
RD	IOERF3[7-0]	IOERF2[7-0]	IOERF1[7-0]	IOERF0[7-0]
WR	-	-	-	-

GP02OUT (0x5000_2140) GP40-GP42 Output Register RW (0x00000000)

	31-24	23-16	15-8	7-0
RD				POUT0[2-0]
WR				POUT0[2-0]

GP02IN (0x5000_2144) GP40-GP42 Input Status Register RO (0x00000000)

	31-24	23-16	15-8	7-0
RD				PIN0[2-0]
WR	-	-	-	-

GP02INDB (0x5000_2148) GP40-GP42 Debounced Input Status Register RO (0x00000000)

	31-24	23-16	15-8	7-0
RD				PINDB0[2-0]
WR	-	-	-	-

GP02IF (0x5000_2150) GP40-GP42 Edge Interrupt Flag Register RO (0x00000000)

	31-24	23-16	15-8	7-0
RD				RIF0[2-0]+FIF0[2-0]
WR	-	-	-	-

GP02ERF (0x5000_2164) GP40-GP42 Compare Mismatch Flag Register RO (0x00000000)

	31-24	23-16	15-8	7-0
RD				IOERF0[2-0]
WR	-	-	-	-

All GPIO can have clock output. The clock output is enabled when MFCF[7-6]=0x01 and MFCF[4-0]=0x00000. The output clock is defined by CLKOUT register.

CLKOUT (0x5000_2300) Clock Out Control Register RO (0x00000000)

	31-9	8	7-5	4-0
RD	-	CLKOEN	CLKSEL[2-0]	CLKDIV[4-0]
WR	-	CLKOEN	CLKSEL[2-0]	CLKDIV[4-0]

CLKOEN Clock Out Enable

CLKOEN=0 will disable clock out function
CLKOEN=1 enables the divider

CLKSEL[2-0] Clock Source Select
000 = SYSCLK
001 = IOSC
010 = SOSC
011 = POSC
1XX = Reserved

CLKDIV[4-0] Clock Divider
The clock output is Clock Source divided by (CLKDIV[4-0]+1).

TESTSEL (0x5000_2304) Test Out Select Register RW (0x00000000)

	31-14	13	12	11	10-8	7-5	4-0
RD	-	TESTCHEN	TEMPSEL	TESTDCDCEN	TESTSEL[10-8]	TESTSEL[7-5]	TESTSEL[4-0]
WR	-	TESTCHEN	TEMPSEL	TESTDCDCEN	TESTSEL[10-8]	TESTSEL[7-5]	TESTSEL[4-0]

TESTSEL[10-8] TESTOUT Selection
TESTOUT is selected for ANIO2 for P15.
000 BGOUTTEST
001 VBGTEST
010 VD15
011 PORPTEST
100 VDDKTEST
101 STRTEST
110 TEMPOUT_TEST
111 IREFTEST2

TESTSEL[7-5] TESTOUT Selection
TESTOUT is selected for ANIO2 for P25.
000 DAC2TEST
001 DACFB2TEST

TESTSEL[4-0] TESTOUT Selection
TESTOUT is selected for special function for P00.
00011 LVD
00101 TBIT
00111 LINRESET
01000 MBSTFINISH
01001 MBSTFAIL
01010 DMAMBSTFAIL
10001 IOSC/16
10011 SIOSC
10101 POSC

30. Information Block (IFB)

There are two IFBs each is 1Kbyte size in 256 x 39 organizations. The upper 7-bit is the ECC code, and lower 32-bit is data. IFB0 is for manufacturing, and IFB1 are for user.

30.1 IFB0 Address 0x1F00-0000~0x1F00-03FF

Word Address	Type	Description
00	M	IFB Version
01	M	Product Name
02	M	Package and Product Code
03	M	Product Version and Revision
04	M	Flash Memory Size
05	M	SRAM Size
06	M	Flash Segment Size
07	M	Flash Data Width
08~0E	M	Reserved
0F	M	Checksum for 0x00 – 0x0E
10	M	CP1 Information
11	M	CP2 Information
12	M	CP3 Version
13	M	CP3 BIN
14	M	FT Version
15	M	FT BIN
16	M	Last Test Date
17	M	Boot Code Version
18	M	Boot Code Segment
19	M	Customer Specific Code – Customer Name
1A	M	Customer Specific Code - Version
1B– 1E	M	Reserved
1F	M	Checksum for 0x10 – 0x1E
20	M	REGTRM value for 1.5V
21	M	POSC ITRM/VTRM value for 16MHz and 32MHz
22	M	IOSC ITRM/VTRM value for 16MHz
23	M	IOSC ITRM/VTRM value for 32MHz
24	M	SOSC TRM
25	M	PLL TRM
26	M	LVDTHD value for detection of 4.0V/3.0V/2.4V
27	M	ADC-12 Offset and Trim 1, voltage in 1mV (14-bit), ADC value in LSB (14-bit), offset[7-4]
28	M	ADC-12 Offset and Trim 2, voltage in 1mV (14-bit), ADC value in LSB (14-bit), offset[3-0]
29	M	Temperature Offset/Coefficient (Negative) [31-24] temperature coefficient LSB/K [23-16] FT temperature in Celsius [15-0] ADC measurement at FT

Word Address	Type	Description
2A	M	Temperature Offset/Coefficient (Positive) [31-24] Ideal temperature coefficient LSB/K [23-16] FT temperature in Celsius [15-0] ADC measurement at FT
2B	M	Precision Timer Trim
2C	M	ADC-12 Offset and Trim 1
2D	M	ADC-12 Offset and Trim 2
2E	M	Precision Timer Trim based on 32MHz IOSC
2F	M	Checksum for 0x20 – 0x2E
30	M	LED DRIVER BG Trim Value
31	M	LED DRIVER OT Trim Value
32	M	LED DRIVER IREF Trim Value
33	M	LED DRIVER SM ISET Trim Value
34	M	LED DRIVER SWPD Trim Value
35	M	LED DRIVER CSPU Trim Value
36	M	LED DRIVER OC Trim Value
37	M	LED DRIVER CS OFFSET Trim Value
38	M	LED DRIVER CS OFFSET RANGE Trim Value
39	M	OVP_VREF Trim Value
3A	M	Reserved
3B ~3E	M	Reserved
3F	M	Checksum for 0x30 – 0x3E
40 – 4F	M	Retention Value 1
50 – 5F	M	Retention Value 2
60 – 6F	M	Endurance Value 1
70 – 7F	M	Endurance Value 2
80 – EF	M	Reserved
F0 – FD	M	Reserved
FE	M	MKEY0
FF	M	MKEY1

Table 30-1 IFB0 Address 0x1F00-0000~0x1F00-03FF

30.2 IFB1 Address 0x1FFF-0000~0x1FFF-03FF

Word Address	Type	Description
00 – EF	U	User programmable
F0	U	Wait time
F1	U	ISP Interface
F2 – FD	U	Reserved
FE – FF	U	UKEY[63-0]

Note: The actual Byte address should be word address*4

Table 30-2 IFB1 Address 0x1FFF-0000~0x1FFF-03FF

31. RISC-V Debug Module and Debug Interface

The debug module is tightly coupled with the RISC-V core. The entire debug path is shown in the following block diagram. The external interface is through a 2-wire CJTAG and translated between CJTAG and a JTAG controller (Debug Transport). The Debug Module is shown in yellow and blue. The debug path can be used for debugging as well as flash programming.

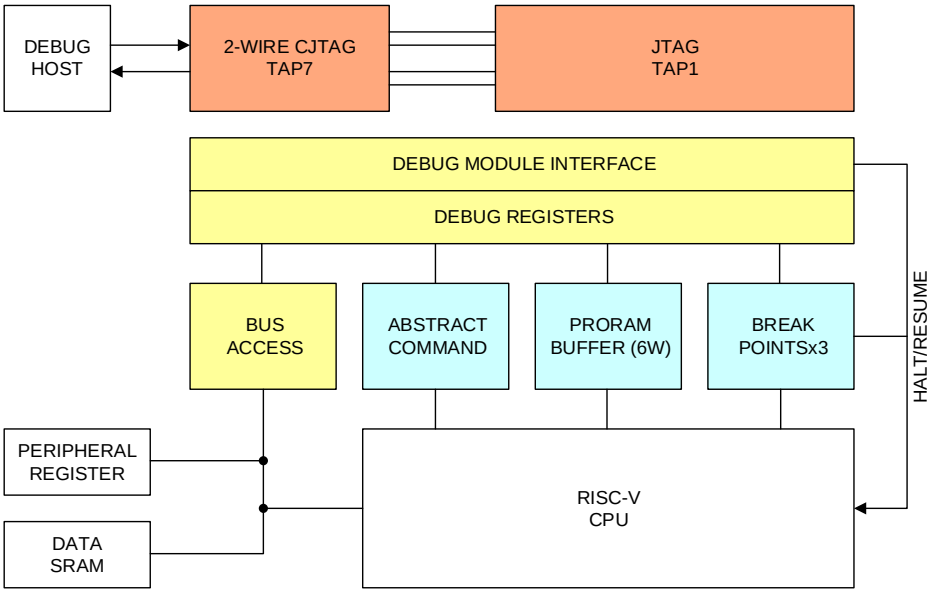


Figure 31-1 RISC-V Debug Module and Debug Interface

The debug module includes a Debug Module Interface (DMI) for JTAG connections, and a Debug Register (DR). Details of debug can be found in RISC-V's external debug support information. The debug module supports four access paths to the data path and the CPU core. These include Bus Access, Abstract Command, Program Buffer, and Breakpoint module. The bus access unit is used to access data bus which connects to peripheral registers and data SRAM. Abstract command provide accesses to the GPRs (General Purpose Register). The Program Buffer units achieve similar objectives to allow the CPU to execute specific instructions. The Program Buffer contains 6 lines of instruction. Break Points unit contains breakpoint setting and three breakpoints can be set in this implementation. Bus Access allows access to the memory bus without the CPU.

Full features of debugging are not open until the unlock operation is completed. In the locked state, only bus access is allowed which can be used to operate the e-Flash controller for unlocking the security keys.

31.1 2-Wire JTAG Interface

The 2-wire JTAG also known as JTAG 1149.7 (subset) or compact JTAG which uses reduced number of pins for accomplishing test access port (TAP). It is compatible with traditional JTAG standard. It uses two signals TCKC and TMSC, and a hardware block that converts TCKC and TMSC signals into traditional 4-wire JTAG interface. This is as shown in the following block diagram.

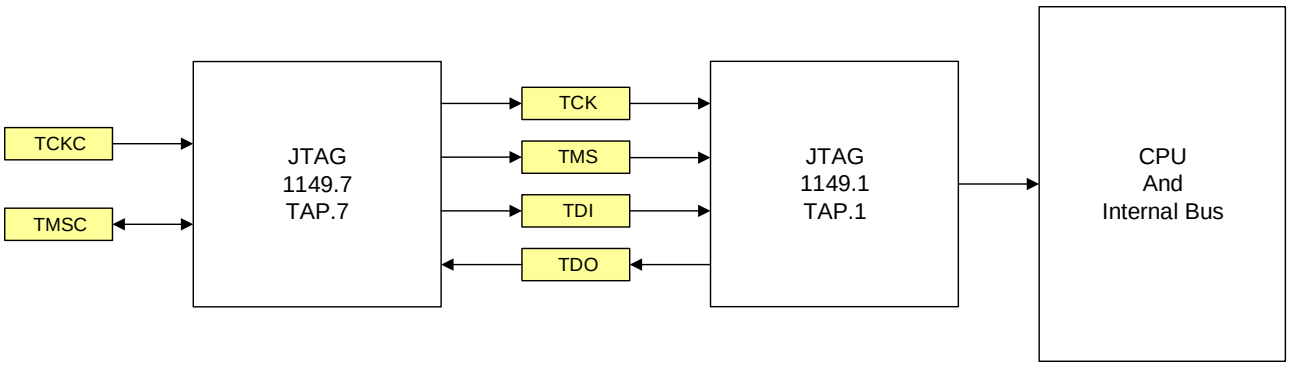


Figure 31-2 CJTAG to JTAG converter

An escape reset sequence must be first send to slave to reset TAP7, the sequence is shown in the following Figure 31-2.

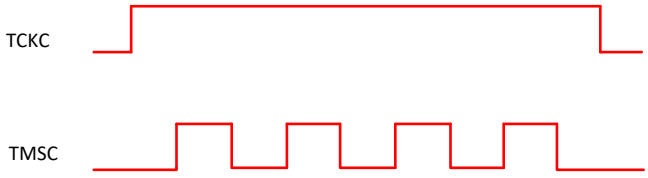


Figure 31-3 CJTAG Escape Reset

The following sequence in Figure 31-4 followed by escape reset is necessary. The red part of the waveform is to switch to the ONLINE state of RSU, and the blue part of the waveform is to separate from the previous escape sequence.

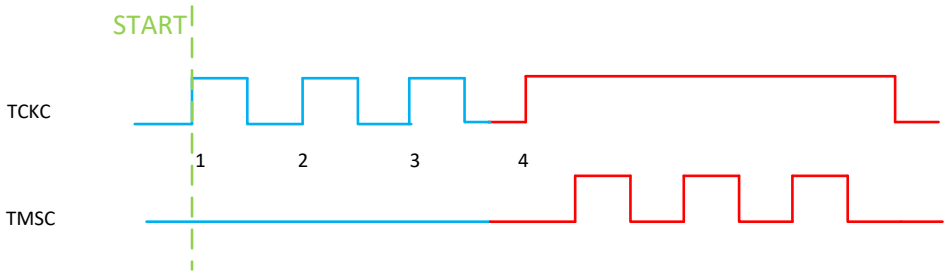


Figure 31-4 CJTAG START

It is necessary to set TMSC to 0 for 12 rising edges of TCKC clock after switching to ONLINE state as shown in Figure 31-5. Then the two-wire JTAG mode is configured. Please also note between the START in Figure 31-4 and the END in Figure 31-5, 16 rising edges of TCKC are required, and the counter has been marked in Figure 31-4 and Figure 31-5.

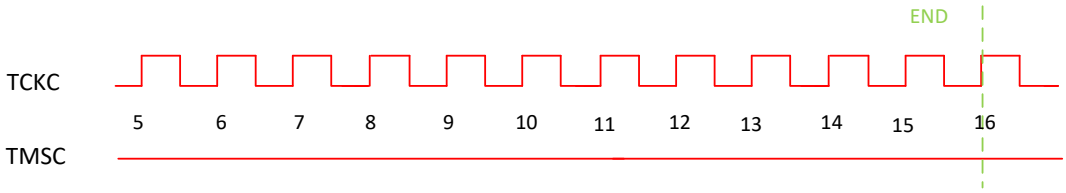


Figure 31-5 CJTAG ONLINE

31.2 Debug Module

The DM is implemented according to RISC-V External Debug Support V0.13

31.3 Debug Module Registers

Address	Name	Descriptions
0x04	DATA0	Abstract Data 0 in 32-bit
0x05	DATA1	Abstract Data 1 in 32-bit
0x10	DMCONTROL	Debug Module Control
0x11	DMSTATUS	Debug Module Status
0x12	HARTINFO	Hart Information
0x13	HALTSUM1	Halt Summary 1
0x16	ABSTRACTCS	Abstract Control and Status
0x17	COMMAND	Abstract Command
0x18	ABSTRACTAUTO	Abstract Command Autoexec
0x20	PROGBUF0	Program Buffer 0
0x21	PROGBUF1	Program Buffer 1
0x22	PROGBUF2	Program Buffer 2

Address	Name	Descriptions
0x23	PROGBUF3	Program Buffer 3
0x24	PROGBUF4	Program Buffer 4
0x25	PROGBUF5	Program Buffer 5 (Hardware EBREAK instruction)*
0x34	HALTSUM2	Halt Summary 2 (haltsum2)
0x35	HALTSUM3	Halt Summary 3 (haltsum3)
0x38	SBCS	System Bus Access Control and Status
0x39	SBADDRESS0	System Bus Access [31-0]
0x3C	SBDATA0	System Bus Data [31-0]
0x40	HALTSUM0	Halt Summary 0 (haltsum0)

Note: PROGBUF5 is hardware EBREAK instruction. For total length of instructions less than 5, the last instruction should be EBREAK. Or always fill the PROGBUF[4-0] with 5 instructions with unused filled with NOP.

31.4 Debug Mode Entry Timing Window

Since TMSC and TCKC for CJTAG or TMS, TCK, TDI, TDO for JTAG are multi-function pins shared with GPIO, there is a need to allow IS3XCS9310 to enter such mode for enabling these special functions. This is accomplished by opening a short time window for detections of active CJTAG interface. The time window is open for one second after power on, or after a rising edge of RSTN preceded by an extended period (longer than 100msec) of RSTN=0. In other words, the time window is open after SP reset.

Within this time window, the host must establish CJTAG communication link and perform register access to JTAG control registers, JTAGCFGA and JTAGCFGB, to enable the CJTAG/JTAG interface. The transactions include the CJTAG initialization and key unlock of the debug interfaces.

Please note, JTAGCFGA and JTAGCFGB can be modified only in this time window. In addition, at system board level, the CJTAG/JTAG interface pins TMS, TCK and TDI/TDO (if JTAG is used) must be free of interference by other application circuits these are connected. To allow successfully establishing the debug port for debugging and flash programming, these pins must not be driven by other circuits in the application and should have minimum parasitic load impedance and capacitance.

There is a caveat in turning on the debug interface as described in 25.5. After reset, the device will start executing the user program immediately. If the user program inadvertently sets the GPIO sharing with the CJTAG/JTAG pins, then the mode entry cannot proceed successfully.

32. Special Modes

Included on the IS3XCS9310 are special modes. This feature allows for test, debug and e-Flash erase. The special modes are entered using waveform sequence on the RSTN or SWC/JCK pins. The mode detection logic is illustrated on the following block diagram.

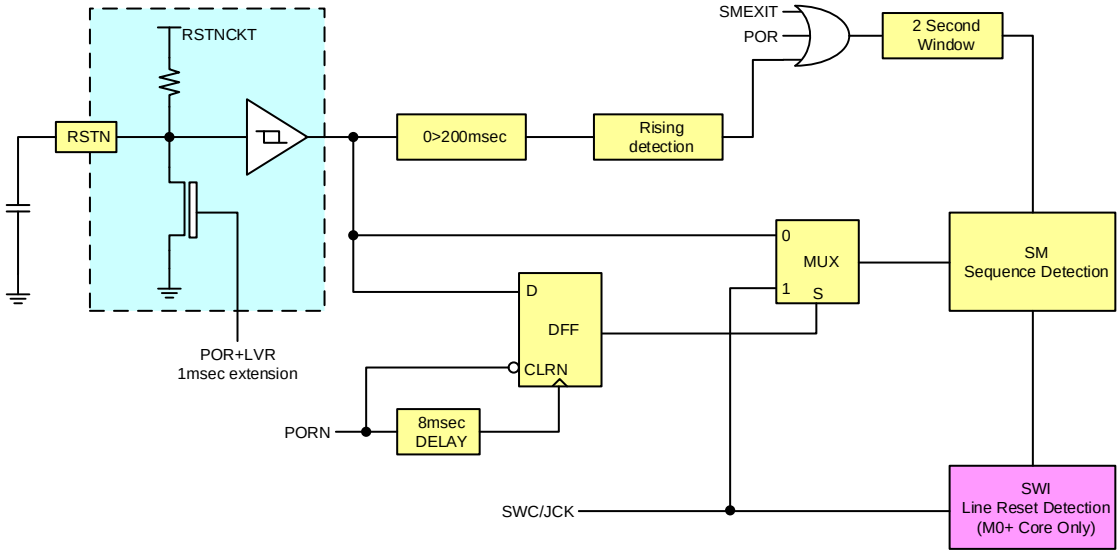


Figure 32-1 Special mode Block Diagram

The special mode detection first selects which pin is used for sequence input. RSTN is sampled 8ms after power on. If RSTN is high, then SWC/JCK pin is used if RSTN is low then RSTN is used. For the host using RSTN control, the host should force RSTN low during power-on and should be released after 50msec.

The detection window of two second is opened after power-on, or RSTN=low longer than 200ms (host should pull RSTN low for 250ms to ensure proper detection), or SMEXIT is issued for exiting previous special mode.

Please also note that for the M0+, the 2s window is also used to allow for the M0+ SWIO debug controller to detect for initialization of the debug interfacing using the “line reset” signal After the initial connection of SWI interface is established, the debug mode with SWI interface is locked until exited.

The special mode sequence is built upon duty cycle bit encoding. The waveform follows a duty cycle encoded bit stream including synchronization bit and logic 1/0 bits. The coding mechanism is shown in the following diagram. Each bit time consists of 16 TQ with TQ range from 0.2ms to 2.0ms. Using JLINK TQ can be set to 0.5ms minimum using 1ms steps.

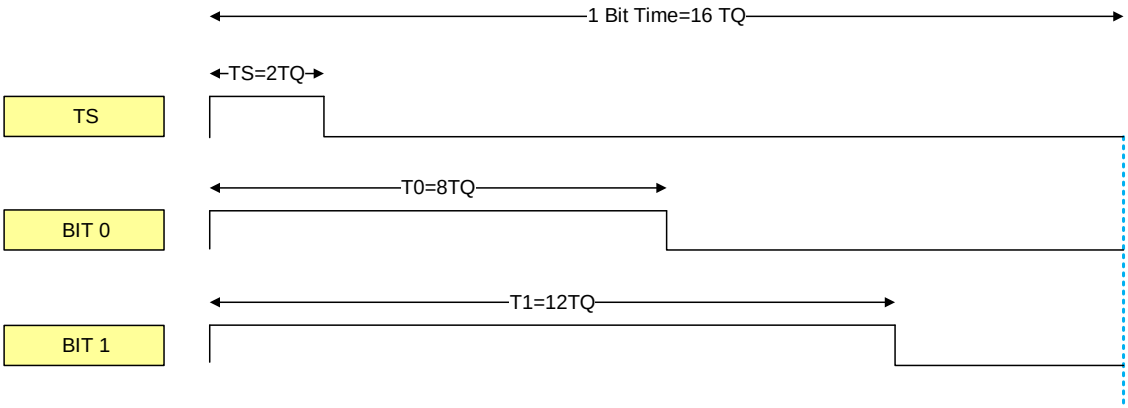


Figure 32-2 Special mode bit configuration

The Mode entry must follow the following waveform sequence and the time window for recognizing the sequence is limited to 2s.

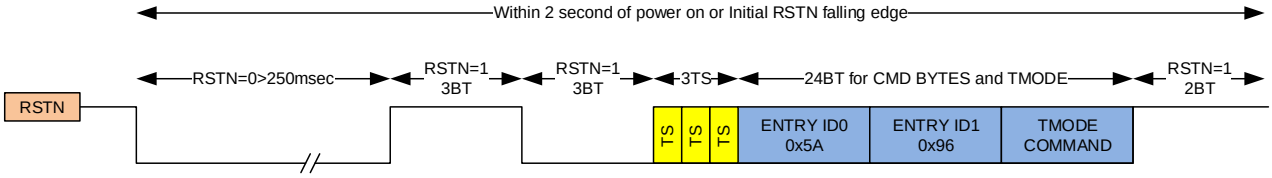


Figure 32-3 Enter special mode by RSTN

The following TMODE Command are allowed.

Function	TMODE[7-0]	Comments
Enable SWI interface	0x3C	This forces the SWI interface pins configurations to allow debugging mode.
Enable CJTAG interface	0x4B	This force CJTAG pins in correct IO configurations to allow CJTAG interface. To access debug, the unlock procedure still needs to be carried out.
Enable JTAG interface	0x5A	This force JTAG pins in correct IO configurations to allow JTAG interface. To access debug, the unlock procedure still needs to be carried out.
Enable Scan Test	0x94	Scan test mode.
Force Erase Whole Chip	0xE5	This should be avoided as it also erases IFB0 and Boot Code.
Force Erase MM and IFB1	0xE9	Restore the devices to default blank statue.

Entry ID0 = 0x5A and Entry ID1=0x96. This should be confidential.

To exit the special mode,

1. Power on/off.

2. Hold RSTN=0 for > 250msec then release RSTN=1.

3. Writing to the special mode exit register (SMEXIT 0x5000_0500) with data 0x55AA9669 followed by 0xAA556996. This clears the special mode status and performs an equivalent system reset, then open 2s of special mode detection window. Please note SMEXIT is not accessible from CPU and only accessible by debug interface when debug mode is on.

33. Electrical Characteristics

33.1 Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit	Note
VDDH	Positive Power Supply	5.5	V	
TA	Ambient Operating Temperature	-40 – 85	°C	(IS31CS9310)
TA	Ambient Operating Temperature	-40 – 125	°C	(IS32CS9310)
TSTG	Storage Temperature	-65 – 150	°C	
ESD	HBM CDM	4000 500	V	

33.2 Recommended Operating Condition

Symbol	Parameter	Rating	Unit	Note
VDDH	Positive Power Supply	3 – 5.5	V	
TA	Ambient Operating Temperature	-40 – 85	°C	(IS31CS9310)
TA	Ambient Operating Temperature	-40 – 125	°C	(IS32CS9310)

33.3 DC Electrical Characteristics (VDDH = 3.0V to 5.5V, TA = -40°C to 85°C (IS31CS9310),TA = -40°C to 125°C (IS32CS9310), TJ = -40°C to 125°C)

Symbol	Parameter	Min	Typ	Max	Unit	Note
Power Supply Current						
IDD, normal	Supply Current (Total)		22		mA	2
	Supply Current (led driver) VLEDEN=PVDD with PWM=0xFF SRS = 24kHz @ 8bit mode		7		mA	
	Supply Current (digital) @ 32MHz		10		mA	
	Supply Current (analog) @ 4MHz		5		mA	
IDD, Sleep	IDD, Deep Sleep Mode, 25℃	-	20	50	μA	Main regulator off, IOSC off
	IDD, Light Sleep Mode, 25℃		1	2	mA	Main regulator on, IOSC on
	IDD, Standby Mode, 25℃		0.5	0.8	mA	Main regulator on, IOSC off
Digital IO Characteristics						
VOH,4.5V	Output High Voltage 1 mA	-	-0.2	-0.5	V	refer to VDDH
VOL,4.5V	Output Low Voltage 8 mA	-	0.3	0.5	V	refer to VSS
VOH,3.0V	Output High Voltage 1 mA	-	-0.3	-0.6	V	refer to VDDH
VOL,3.0V	Output Low Voltage 8 mA	-	0.3	0.6	V	refer to VSS
IIOT	Total IO Sink and Source Current	-80	-	80	mA	
VIH	Input High Voltage	¾VDDH	-	-	V	
VIL	Input Low Voltage	-	-	¼VDDH	V	
VIHYS	Input Hysteresis	-	1	-	-	
RPU	Equivalent Pull-Up resistance	-	12K	-	Ohm	
RPU RSTN2	RSTN2 Pull-Up resistance	-	5K	-	Ohm	

Symbol	Parameter	Min	Typ	Max	Unit	Note
RPD	Equivalent Pull-Down Resistance	-	12K	-	Ohm	
REQAN1	Equivalent ANIO Switch Resistance @3.3V	-	110	-	Ohm	ANIO1 Switch
	Equivalent ANIO Switch Resistance @5V	-	50	-	Ohm	ANIO1 Switch
REQAN2	Equivalent ANIO Switch Resistance @3.3V	-	600	-	Ohm	ANIO2 Switch
	Equivalent ANIO Switch Resistance @5V	-	350	-	Ohm	ANIO2 Switch
VD15 Characteristics						
VD15N	Normal Core Voltage 1.5V (Calibrated)	1.45	1.5	1.55	V	Normal Mode
VD15S	Sleep Core Voltage 1.5V	-	1.40	-	V	Sleep Mode
Low Supply (VDDH) Voltage Detection						
VDET	Detection Range	2.0	-	4.8	V	
VDETHYS	Detection Hysteresis	-	100	-	mV	
SAR ADC12 Characteristics						
ADCLIN	ADC Linearity, Center range	-	+/- 5	-	LSB	
	ADC Linearity, 0.2V to FS-0.2V	-	+/- 8	-	LSB	
ADCFQ	ADC Frequency	-	1	2	MHz	
CRSAR ADC12 Characteristics						
ADCLIN	ADC Linearity, Center range		+/- 5	-	LSB	
	ADC Linearity, 0.2V to FS-0.4V		+/- 8	-	LSB	
ADCFQ	ADC Frequency		8	16	MHz	

Note:

1. Measured through the VDDH and PVDD pin in Sleep mode.
2. Measured through the VDDH and PVDD pin.

33.4 AC Electrical Characteristics (VDDH = 3.0V to 5.5V, TA = -40℃ to 85℃ (S31CS9310), TA = -40℃ to 125℃ (IS32CS9310), TJ = -40℃ to 125℃)

Symbol	Parameter	Min	Typ	Max	Unit	Note
System Clock and Reset						
FSYS	System Clock Frequency	-	16	33	MHz	
Supply Timing						
TSUPRU	VDDH Ramp Up Time	1	-	50	msec	WTST = 0 for 16MHz
TSUPRD	VDDH Ramp Down Time	-	-	50	msec	
TPOR	Power On Reset Delay	-	5	-	msec	
IOSC						
FIOSC	IOSC Calibrated 16MHz/32MHz	-1	0	+1	%	
	IOSC Startup Time	-	-	1	µs	
	Temperature and VDDH variation at 50℃	-1.5	0	+1.5	%	
	Temperature and VDDH variation at 85℃	-2	0	2	%	

Symbol	Parameter	Min	Typ	Max	Unit	Note
SOSC						
SOSC	Slow Oscillator frequency	-	128	-	KHz	
IO Timing						
TPD5 ++	Propagation Delay,5V, No load	-	5	-	ns	
TPD5 ++	Propagation Delay, 5V,25pF load	-	12	-	ns	
TPD5 ++	Propagation Delay, 5V, 50pF load	-	16	-	ns	
TPD5 --	Propagation Delay, 5V, No load	-	4	-	ns	
TPD5 --	Propagation Delay, 5V, 25pF load	-	9	-	ns	
TPD5 --	Propagation Delay, 5V, 50pF load	-	12	-	ns	
Flash Memory Timing						
TEMAC	Embedded Flash Access Time	-	40	45	ns	TWAIT must > TEMAC
TEMWR	Embedded Flash Write Time	-	20	25	μs	
TEMSER	Embedded Flash Sector Erase Time	-	2	2.5	ms	
TEMMER	Embedded Flash Mass Erase Time	-	10	12	ms	

33.5 Led Driver Characteristics

The following specifications apply for PVDD = 3.5~5.5V, (VDDH = 3.0V to 5.5V, TA = -40°C to 85°C (IS31CS9310)，TA = -40°C to 125°C (IS32CS9310)，TJ = -40°C to 125°C), unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit	Note
PVDD	Supply voltage	3.5		5.5	V	
ICC	Quiescent power supply current		3		mA	VLEDEN= PVDD, IOUT=40mA all LEDs off with PWM=0x00 SRS = 24kHz @ 8bit mode
			9	11		VLEDEN = PVDD, IOUT=60mA all LEDs on with PWM=0xFF SRS = 24kHz @ 8bit mode
IOUT	Maximum constant current of CSx		80 +-6%		mA	GCC=0xFF, SL=0xFF
VHR	Current switch headroom voltage SWx		500	600	mV	ISWITCH=960mA, GCC=0xFF, SL=0xFF
	Current sink headroom voltage CSx		600	800		ISINK=80mA, GCC=0xFF, SL=0xFF
tSCAN	Period of scanning		8		μs	8-bit mode, frequency is maxi.
tNOL1	Non-overlap blanking time during scan, the SWx and CSy are all off during this time		0.6		μs	FRS=000
VO	Open threshold	0.08	0.1		V	
HYS	Open threshold hysteresis		50		mV	
VS	short threshold		VDDH -1	VDDH -1.5	V	

33.6 I²C AC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Note
FSCL	Clock Frequency	0	-	400	KHz	
TLOW	Clock Pulse Width Low	1.3	-	-	μs	

Symbol	Parameter	Min	Typ	Max	Unit	Note
THIGH	Clock Pulse Width High	0.6	-	-	µs	
THD.STA	Start Hold Time	0.6	-	-	µs	
TSU.STA	Start Set-up Time	0.6	-	-	µs	
THD.DAT	Data In Hold Time	0	-	0.9	µs	
TSU.DAT	Data In Set-up Time	100	-	-	ns	
tR	Rise Time of both HSDA and HSCL signals	-	-	300	ns	
tF	Fall Time of both HSDA and HSCL signals	-	-	300	ns	
tSU.STO	Stop Set-up Time	0.6	-	-	µs	
tBUF	Time the bus must be free before a new transmission can start	1.3	-	-	µs	

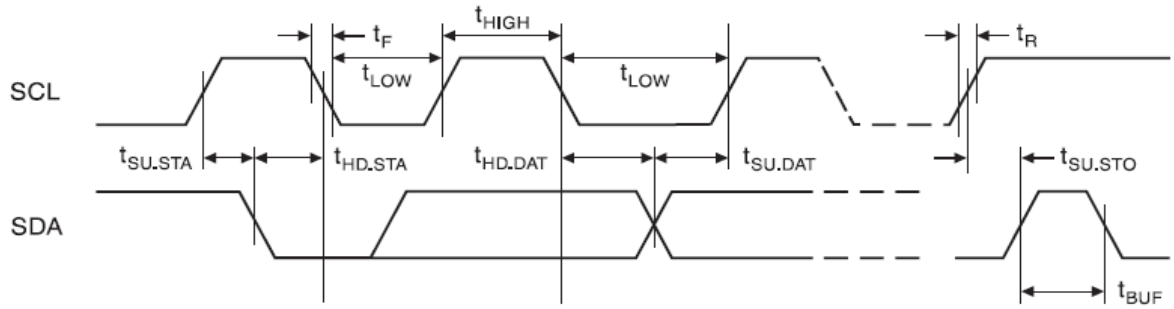
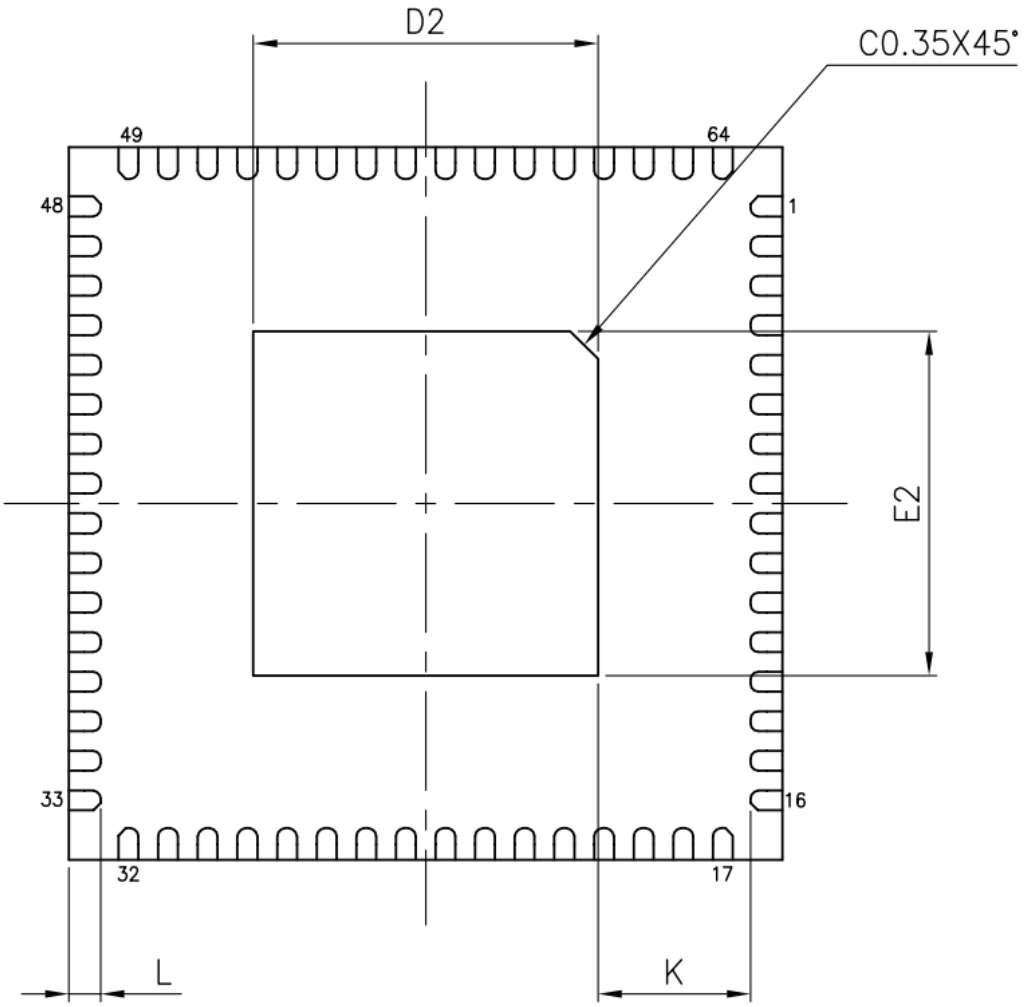


Figure 33-1 I²C Timing diagram

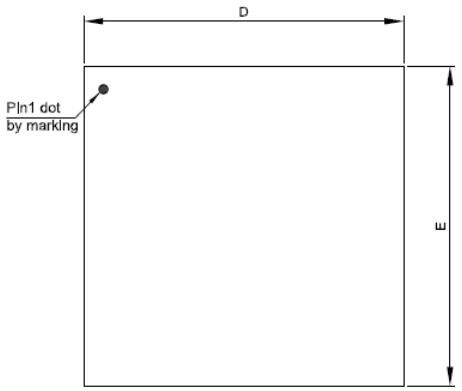
34. Package Outline

34.1 64-pin eLQFP (7mmx7mm body size, 0.4mm pin pitch)

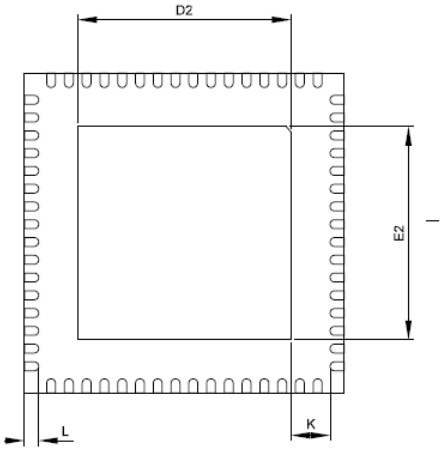
34.1.1 Land Pattern



34.1.2POD

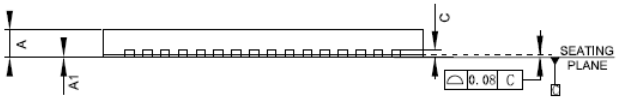


TOP VIEW



BOTTOM VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
c		0.203 REF.	
b	0.18	0.25	0.30
D		9.00 BSC	
E		9.00 BSC	
L	0.35	0.40	0.45
e		0.50BSC	
K	0.20	-	-



SIDE VIEW

L/F SIZE (mil) \ SIZE (mm)	D2			E2		
	MIN	NOM	MAX	MIN	NOM	MAX
244x244	5.90	6.00	6.10	5.90	6.00	6.10

NOTE:
1. CONTROLLING DIMENSION : MM
2. REFERENCE DOCUMENT: JEDEC MO-220
3. THE PIN'S SHARP AND THERMAL PAD SHOWS DIFFERENT SHAPE AMONG DIFFERENT FACTORIES.

35. Ordering Information

Operating temperature -40°C to 85°C

Order Part No	Package	QTY/Reel	Remark
IS31CS9310-LQLS2-TR	eLQFP -64, Lead-free	2500	
IS32CS9310-LQLCA3-TR	eLQFP -64, Lead-free	2500	Cu bonding wire

36. Errata

37. Revision History

Revision	Detailed Information	Date
0A	Preliminary version	2024.03.04
0B	Modified after test Modified EC Specification	2024.06.13
0C	Register default value updated, initial release	2024.08.12