IS32PM3426

3.8V TO 36V, 2A, 2.2MHZ, SYNCHRONOUS STEP-DOWN VOLTAGE REGULATOR

August 2024

GENERAL DESCRIPTION

The IS32PM3426 regulator is a fully integrated and high frequency synchronous step-down DC-DC converter that can drive a load current of up to 2A. It can operate within an input voltage range of 3.8V to 36V. The IS32PM3426 provides exceptional efficiency, output accuracy and drop-out voltage in a very small solution size. Constant on-time control mode is employed to achieve simple control-loop compensation and fast transient response. The IS32PM3426 supports both Forced Continuous Conduction Mode (FCCM) and Pulse Frequency Modulation mode (PFM) at light-load condition, which is selected by the FPWM pin. It requires few external components. Pin arrangement allows simple, optimum PCB layout. Protection features include thermal shutdown, VDD under-voltage lockout, cycle-by-cycle current limit, over-voltage and output short-circuit protection.

The IS32PM3426 device is available in the WFCQFN-14 (3mm × 4mm) package.

APPLICATIONS

- General-purpose power supply
- Automotive LED lighting system
- Automotive body electronics

FEATURES

- Input voltage range from 3.8V to 36V
- 1μA (Typ.) shutdown current
- 25μA quiescent current (typical, no switching)
- Up to 2A output current capability
- Adjustable output voltage, 1V to 24V
- Output regulation accuracy:
  - ±1% at 25°C
  - ±2% over -40°C ~ +150°C
- 95% efficiency at full load (5V/2A)
- >91% efficiency at light load (5V/100mA)
- Integrated 80mΩ High-Side and 40mΩ Low-Side MOSFETs
- Operating frequency range: 100kHz to 2.2MHz
  - Programmed by a single resistor
  - Synchronized to external clock
- Pin-selectable FCCM or PFM operation mode
- Spread spectrum to minimize EMI
- Few external components
  - Internal loop compensation
  - Internal soft-start
- Power good flag output
- Fault protections
  - Cycle by cycle current limit
  - Precision enable to program system UVLO
  - Output short-circuit protection with hiccup mode
  - Output over-voltage protection
  - VDD under-voltage lockout
  - Thermal shutdown protection
- Operating junction temperature range from -40°C ~ +150°C
- WFCQFN-14 (3mm × 4mm) compact package
- RoHS & Halogen-Free Compliance
- TSCA Compliance
- AEC-Q100 Qualified with Temperature Grade 1: -40°C to 125°C

TYPICAL APPLICATION CIRCUIT

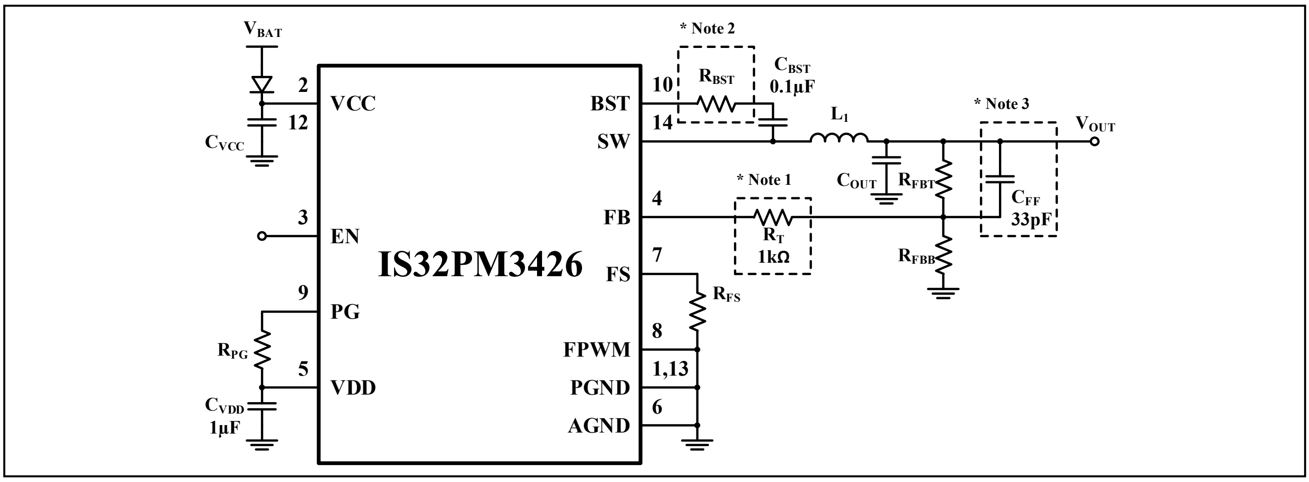
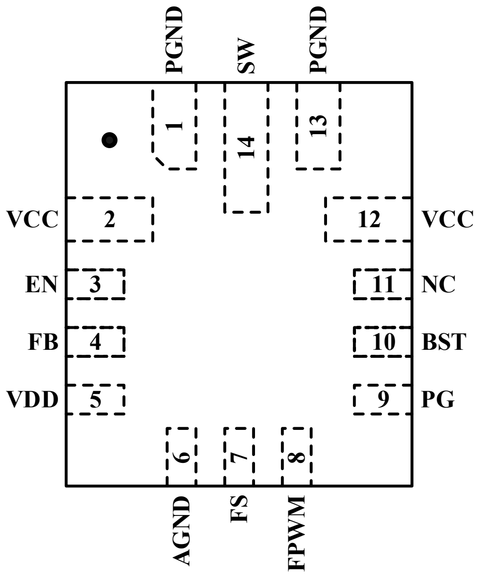


Figure 1 Typical Application Circuit

Note 1: The resistor (R_T) must be connected to FB pin with fixed value 1kΩ.
Note 2: If add the resistor (R_{BST}), the value must not exceed 20Ω.
Note 3: The capacitor (C_{FF}) must be connected in parallel to the resistor (R_{FBT}) with fixed value 33pF.

PIN CONFIGURATION

Package	Pin Configuration (Top View)
WFCQFN-14	

PIN DESCRIPTION

No.	Pin	Description
1, 13	PGND	Power ground for the ground connection of internal synchronous rectifier FET.
2, 12	VCC	Power supply input. Connect a bypass capacitor C_{VCC} from this pin to the ground. The path from C_{VCC} to PGND and VCC pins should be as short as possible.
3	EN	Enable input to the regulator. Pulled high to enable and pull low to disable. Connecting a resistor divider from VCC can program external system UVLO. Do not float.
4	FB	Feedback input to regulator. Connect to the tap point of the feedback voltage divider through a 1kΩ resistor. Do not either float or ground.
5	VDD	Internal 5V LDO output. Used as supply to internal control circuits. Do not connect to any external loads. It can be used as a logic supply for control inputs. Connect a high quality 1μF X7R ceramic capacitor from this pin to GND.
6	AGND	Analog ground for internal references and control circuits.
7	FS	An external resistor to ground on this pin sets the operating frequency. This pin can also be used to synchronize two or more IS32PM3426s in the system. Apply an external clock signal to this pin on two or more ICs for operating frequency synchronization.
8	FPWM	Regulator operation mode selection pin. Connect to VDD for FCCM mode and connect to AGND for PFM mode. Do not float.
9	PG	Open drain power-good flag output. Connect to suitable voltage supply through a current limit resistor. High=power ok. Low=power bad. Can be left open or grounded if not used.
10	BST	Bootstrap supply voltage for internal high-side MOSFET gate driver. Connect a 0.1μF X7R ceramic capacitor from this pin to the SW pin.
11	NC	Not connect.
14	SW	Regulator switch node. Connect it to the power inductor.

ORDERING INFORMATION
Automotive Range: -40°C to +125°C

Order Part No.	Package	QTY/Reel
IS32PM3426-QWCLA3-TR	WFCQFN-14, Lead-free	2500

ABSOLUTE MAXIMUM RATINGS

Input voltages of VCC and EN to AGND, PGND	-0.3V ~ +42V
Input voltages of FB, FS, FPWM to AGND, PGND	-0.3V ~ +6V
Voltage of AGND to PGND	-0.3V ~ +0.3V
Output voltage of VDD to AGND, PGND	-0.3V ~ +6V
Voltage of PG to AGND, PGND	-0.3V ~ V_{CC} +0.3V
Voltage of SW to AGND, PGND	-0.3V ~ V_{CC} +0.3V
Voltage of BST to SW	-0.3V ~ +6V
Storage temperature range, T_{STG}	-65°C ~ +150°C
Operating temperature range, $T_A = T_J$	-40°C ~ +150°C
Power dissipation, $P_{D(MAX)}$	2.33W
Package thermal resistance, junction to ambient (4-layer standard test PCB based on JESD 51-2A), θ_{JA}	53.7°C/W
Package thermal resistance, junction to pin (4-layer standard test PCB based on JESD 51-8), θ_{JP}	17.7°C/W
ESD (HBM) ESD (CDM)	±2.5kV ±750V

Note 4: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range (unless otherwise noted). (Note 5)

Parameter		Min.	Typ.	Max.	Unit
Input voltages	VCC to PGND	3.8		36	V
	EN	0		V_{CC}	
	FB	0		1.5	
	PG	0		V_{CC}	
	FPWM	0		V_{DD}	
	FS	0		V_{DD}	
Output voltage, V_{OUT}		1		24	V
Output current, I_{OUT}		0		2	A
Operating junction temperature range, T_J		-40		150	°C

Note 5: Recommended Operating Conditions indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For verified specifications, see Electrical Characteristics.

ELECTRICAL CHARACTERISTICS

Limits apply over the recommended operating junction temperature (T_J) range of -40°C to +150°C, unless otherwise stated. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J= 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{CC}= 12V.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Power Supply						
V_{CC_UV}	VCC under-voltage lockout threshold	V_{CC} rising		3.5	3.75	V
V_{CC_UVHY}	VCC under-voltage lockout hysteresis	V_{CC} falling		200		mV
I_{SD}	Shutdown current	V_{EN}= 0V		1	5	μA
I_{CC}	Operating quiescent current (non-switching)	V_{EN}= 5V, V_{FB}= 1.05V, T_J= 25°C		25	35	μA

ELECTRICAL CHARACTERISTICS (CONTINUE)

Limits apply over the recommended operating junction temperature (T_J) range of -40°C to +150°C, unless otherwise stated. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J= 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{CC}= 12V.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Enable						
$V_{EN\_VDD\_H}$	Input voltage level to enable the internal LDO output, V_{DD}	V_{EN} rising	1.05			V
$V_{EN\_VDD\_L}$	Input voltage level to disable the internal LDO output, V_{DD}	V_{EN} falling			0.4	V
$V_{EN\_VOUT\_H}$	Precision enable level for switching and regulator output, V_{OUT}	V_{EN} rising	1.16	1.2	1.24	V
$V_{EN\_VOUT\_HY}$	Precision enable level hysteresis	V_{EN} falling		100		mV
I_{EN_LKG}	EN pin input leakage current	V_{EN}= 5V		0.2	50	nA
Soft-Start						
t_{SS}	Internal soft-start time	V_{OUT} from 10% to 90%	1.5	2	2.5	ms
Forced PWM						
V_{FPWM_IH}	FPWM input high threshold		1.5			V
V_{FPWM_IL}	FPWM input low threshold				0.4	V
Internal LDO						
V_{DD}	Internal LDO output voltage	5.5V≤ V_{CC} ≤ 36V, I_{DD}=10mA	4.75	5	5.25	V
I_{DD_LIM}	Internal LDO output current limit		20	45		mA
V_{DD_UV}	VDD under-voltage lockout thresholds	V_{DD} rising	3	3.25	3.5	V
V_{DD_UVHY}	VDD under-voltage lockout hysteresis	V_{DD} falling		200		mV
Voltage Reference						
V_{FB_TH}	Feedback voltage	T_J= 25°C	0.990	1.000	1.010	V
		T_J= -40°C to 150°C	0.98	1.000	1.02	
I_{FB_LKG}	FB pin input leakage current	V_{FB}= 1V		20	100	nA
MOSFETS						
R_{DSON_HS}	High-side MOSFET ON-resistance	I_{SW}= -1A		80		mΩ
R_{DSON_LS}	Low-side MOSFET ON-resistance	I_{SW}= 1A		40		mΩ
t_{ON_MIN}	Minimum switch ON-time			100		ns
t_{OFF_MIN}	Minimum switch OFF-time			90		ns
I_{SW_LKG}	SW pin leakage current	V_{EN}= 0V, V_{SW}= 36V, T_J= -40°C to 125°C			5	μA

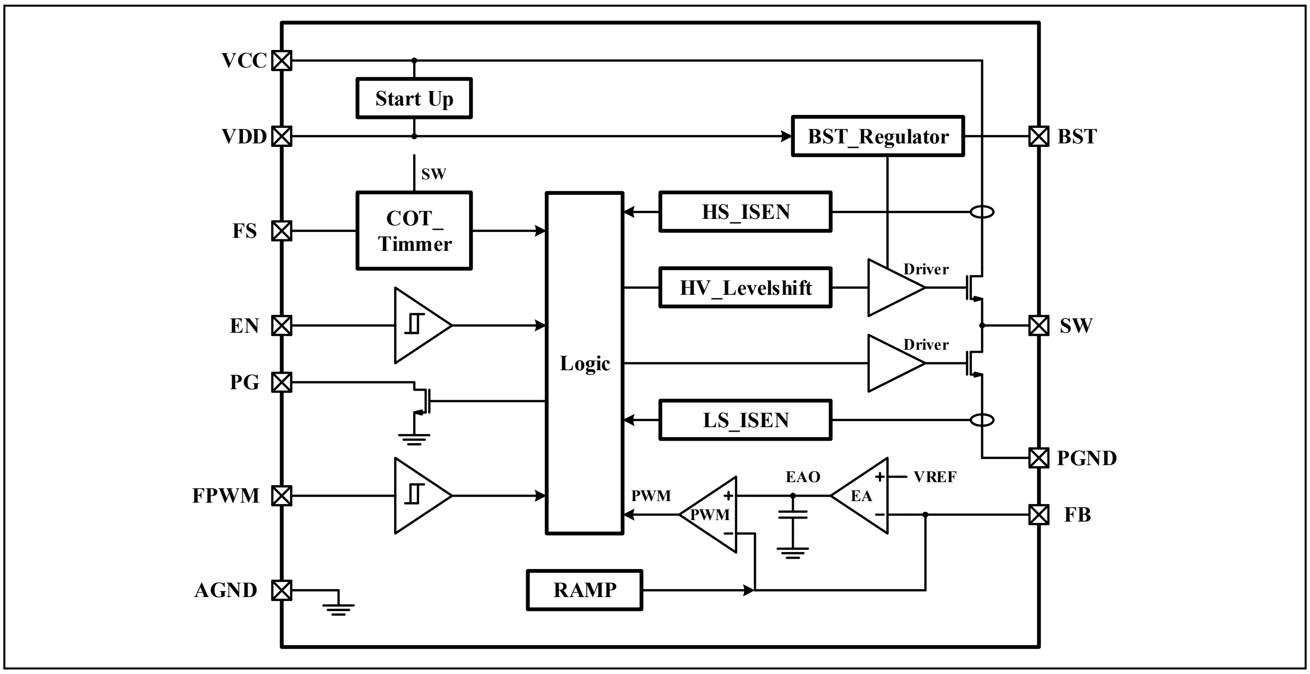
ELECTRICAL CHARACTERISTICS (CONTINUE)

Limits apply over the recommended operating junction temperature (T_J) range of -40°C to +150°C, unless otherwise stated. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J= 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{CC}= 12V.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Current Limit						
I_{HSLIM}	High-side MOSFET current limit		3	4	5	A
I_{LSLIM}	Low-side MOSFET current limit		2	2.5	3.7	A
I_{L_ZC}	Zero cross detection threshold			-0.1		A
I_{PK_MIN}	Minimum inductor peak current			1		A
I_{LSRS}	Negative current limit			-2		A
t_{HC}	Over current hiccup time		16.5	22	27.5	ms
Power Good						
V_{PG_PD}	PG pin pull down capability	Sink current = 5mA		0.1	0.4	V
I_{PG_LKG}	PG pin leakage current				100	nA
V_{PG_UP}	Power-good upper threshold	V_{OUT} rising, % of FB voltage	105	107	110	%
V_{PG_DN}	Power-good lower threshold	V_{OUT} falling, % of FB voltage	90	93	95	%
V_{PG_HY}	Power-good hysteresis	V_{OUT} falling/rising, % of FB voltage		2		%
t_{PG_RF}	PG rising/falling delay time			120	200	μs
Oscillator						
V_{FS}	FS pin voltage			1.2		V
f_{S_DEF}	Oscillator default frequency	FS pin open circuit	360	400	460	kHz
f_S	Minimum adjustable frequency	With 1% resistors at FS pin		100		kHz
	Maximum adjustable frequency		1950	2100	2250	kHz
f_{SS_P}	Spread spectrum pattern frequency	(Note 6)		800		Hz
f_{SS_S}	Frequency span of spread spectrum	(Note 6)		±5		%
V_{SYNC_H}	Sync clock input logic high		2			V
V_{SYNC_L}	Sync clock input logic low				0.4	V
t_{SYNC_MIN}	Minimum sync clock ON-time and OFF-time		80			ns
f_{SYNC_RG}	Sync clock frequency range		100		2200	kHz
Thermal Shutdown						
T_{SD}	Thermal shutdown	(Note 6)		175		°C
T_{SDHY}	Thermal shutdown hysteresis	(Note 6)		155		°C

Note 6: Guaranteed by design.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL PERFORMANCE CHARACTERISTICS

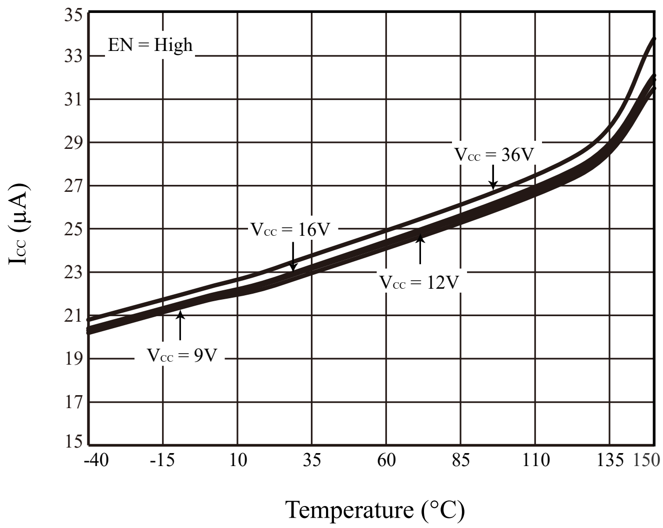


Figure 2 I_{CC} vs. Temperature

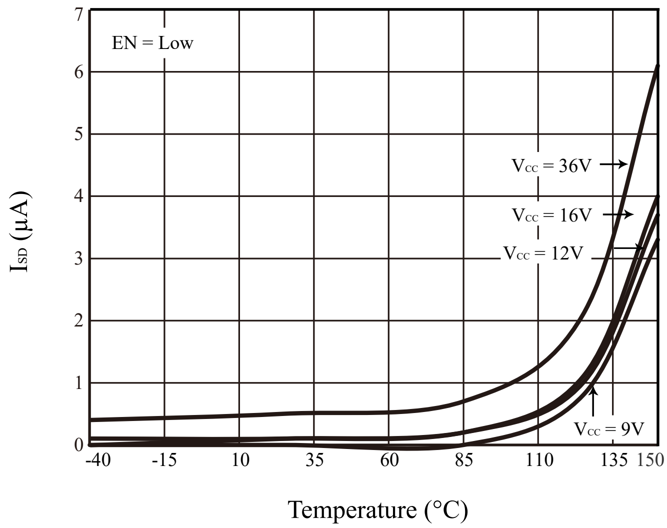


Figure 3 I_{SD} vs. Temperature

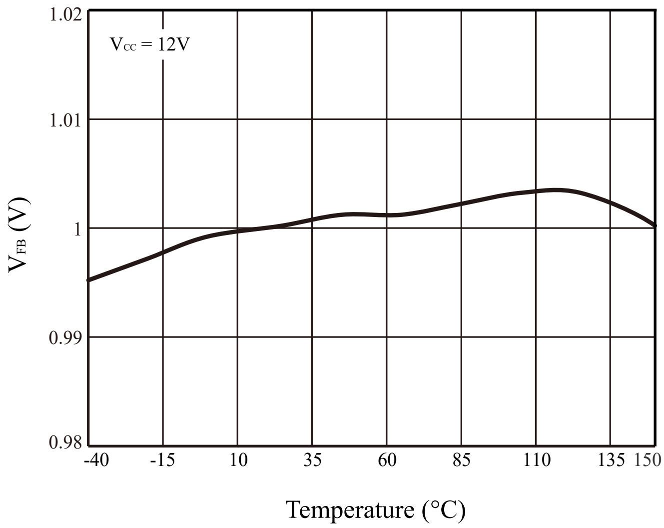


Figure 4 V_{FB} vs. Temperature

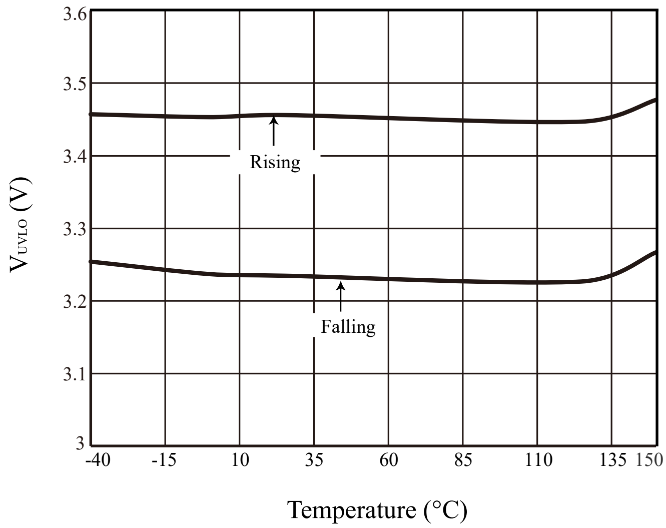


Figure 5 V_{UVLO} vs. Temperature

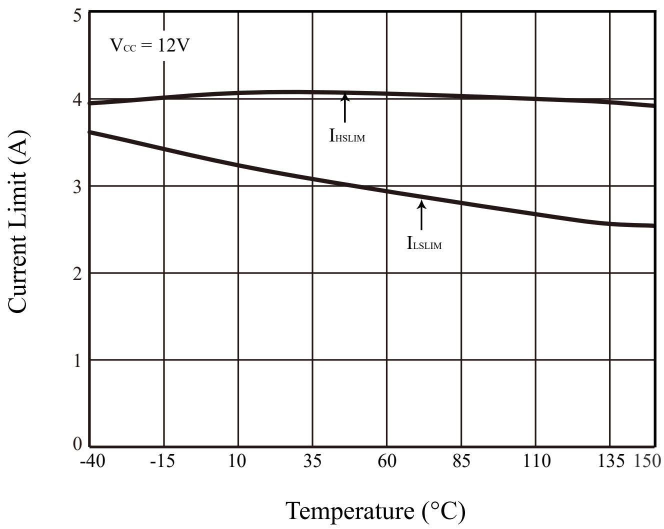


Figure 6 Current Limit vs. Temperature

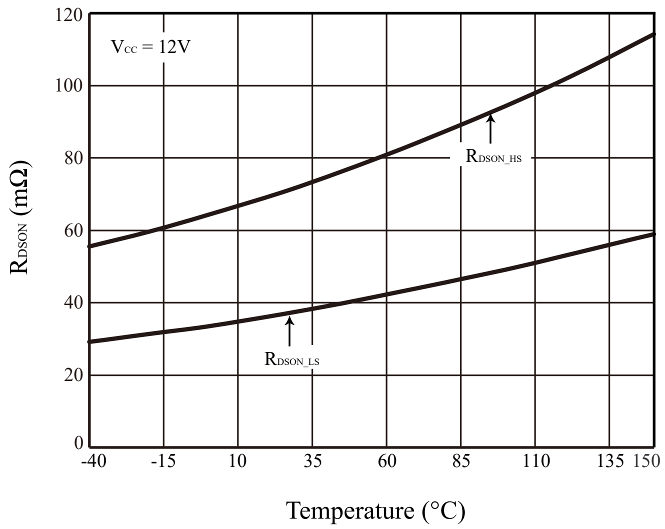


Figure 7 R_{DSON} vs. Temperature

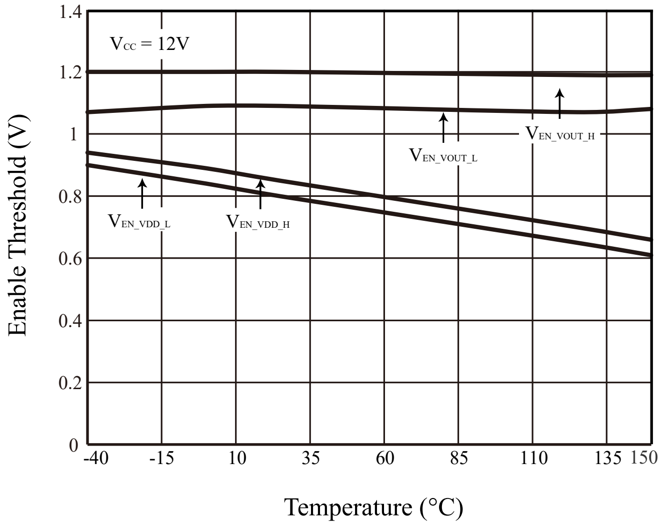


Figure 8 Enable Threshold vs. Temperature

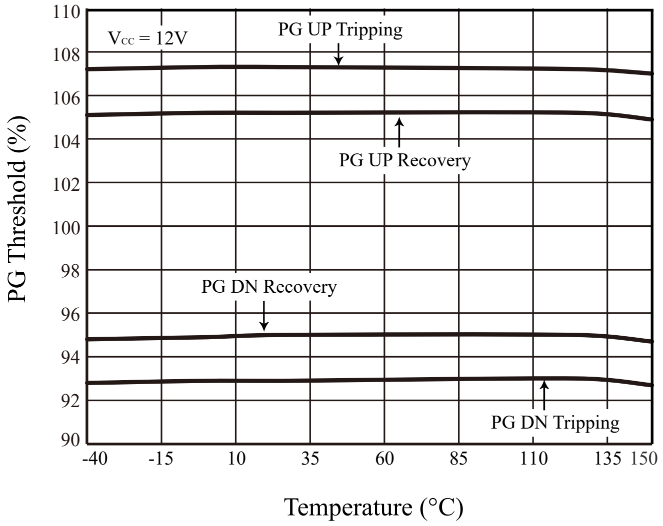


Figure 9 PG Threshold vs. Temperature

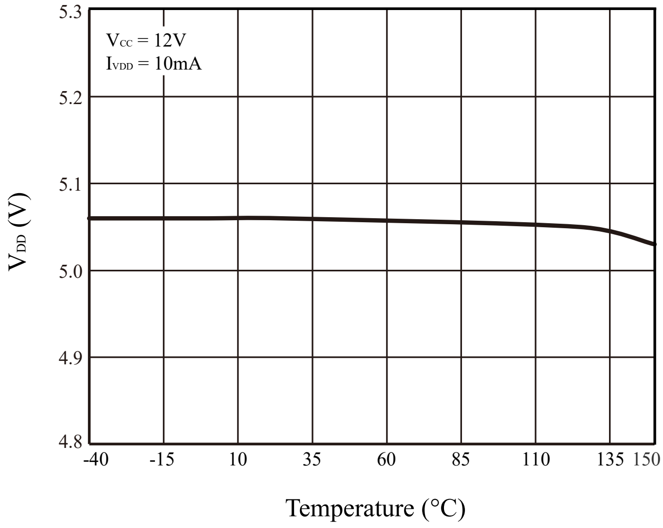


Figure 10 V_{DD} vs. Temperature

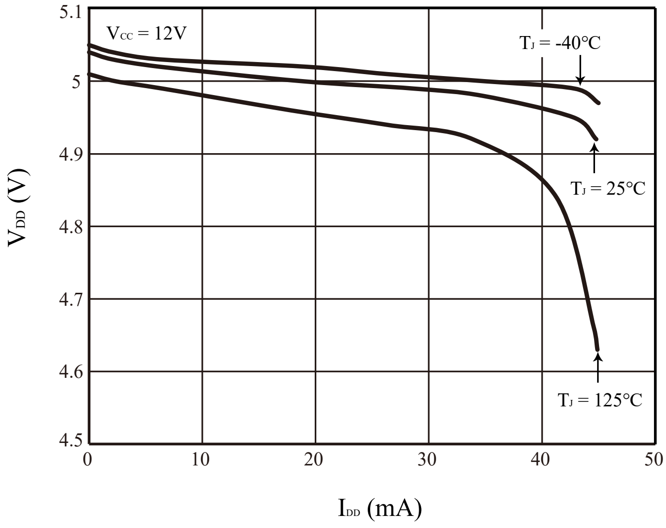


Figure 11 V_{DD} vs. I_{DD}

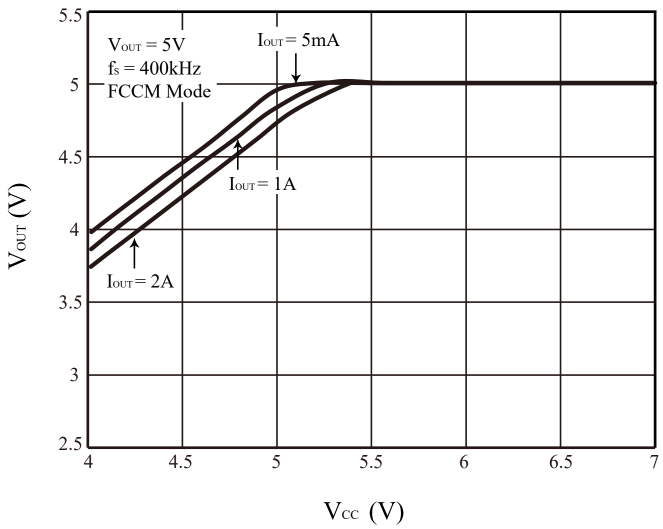


Figure 12 V_{OUT} vs. V_{CC}

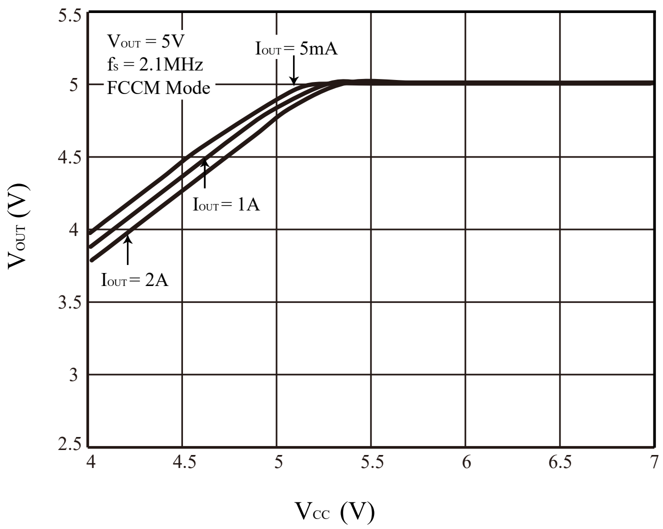


Figure 13 V_{OUT} vs. V_{CC}

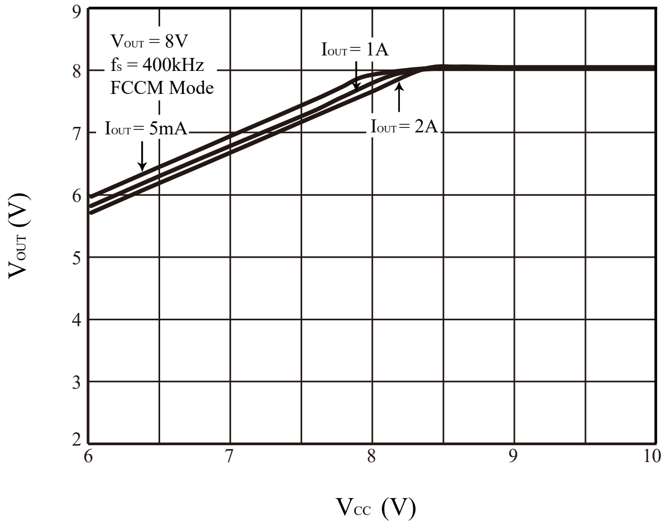


Figure 14 V_{OUT} vs. V_{CC}

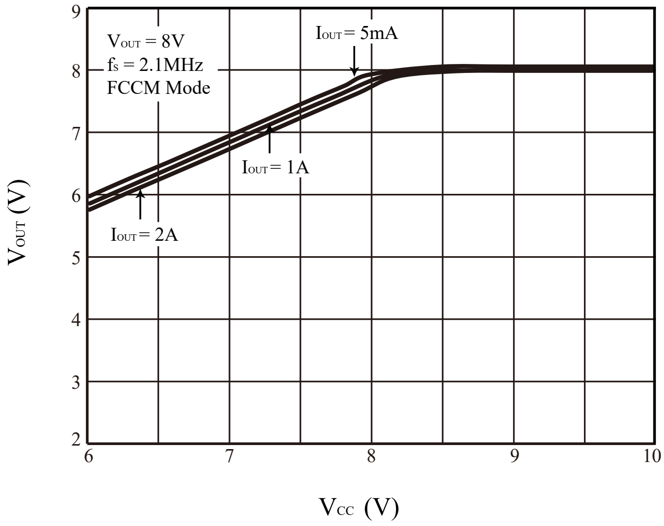


Figure 15 V_{OUT} vs. V_{CC}

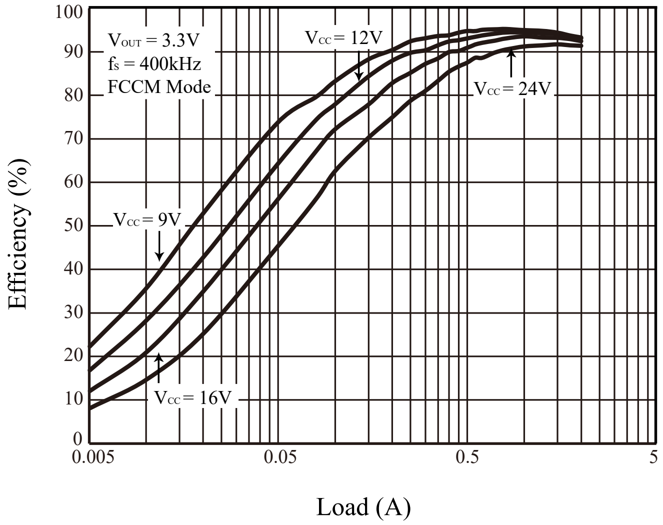


Figure 16 Efficiency vs. Load

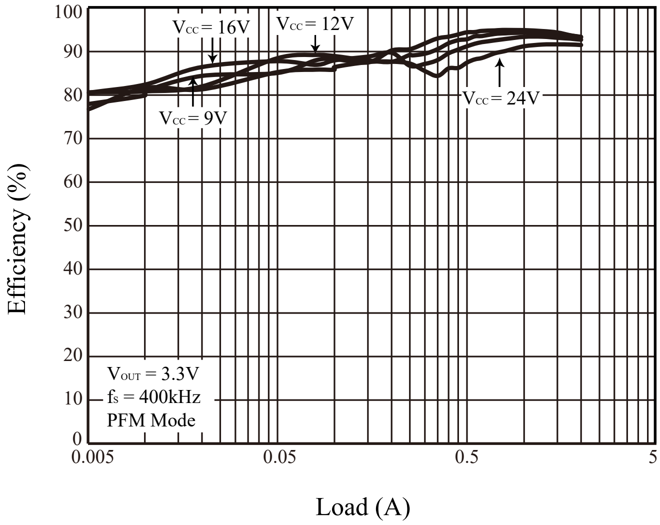


Figure 17 Efficiency vs. Load

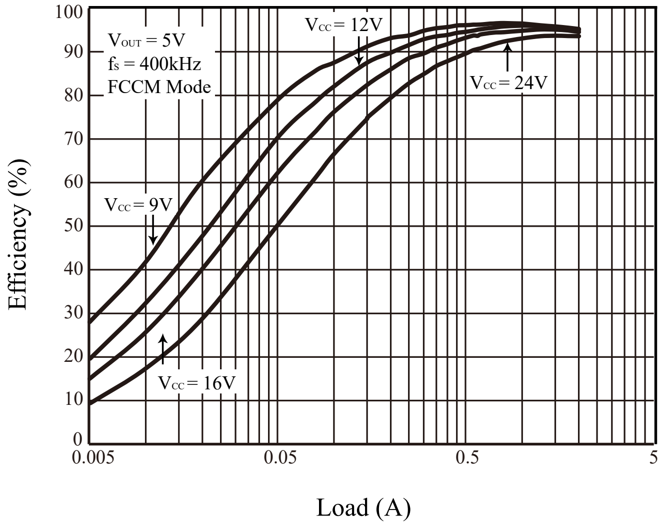


Figure 18 Efficiency vs. Load

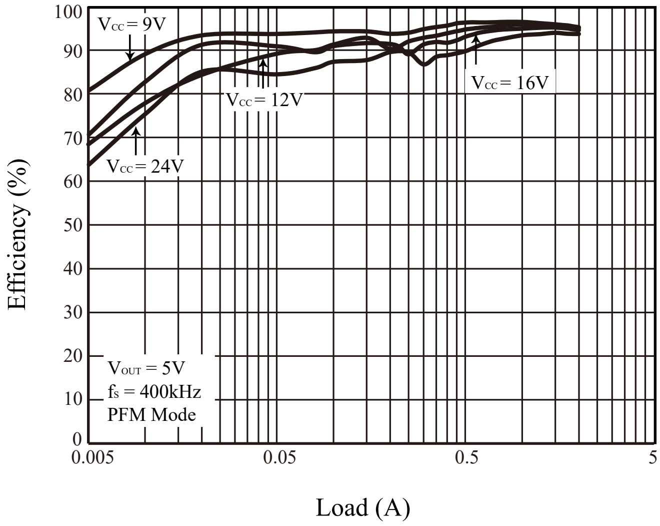


Figure 19 Efficiency vs. Load

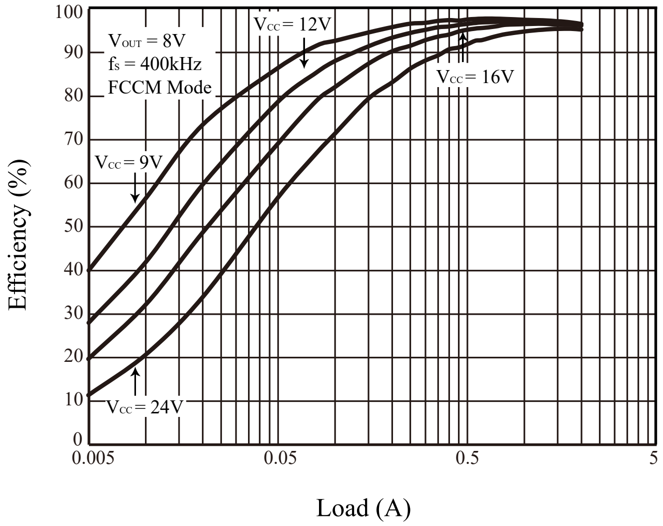


Figure 20 Efficiency vs. Load

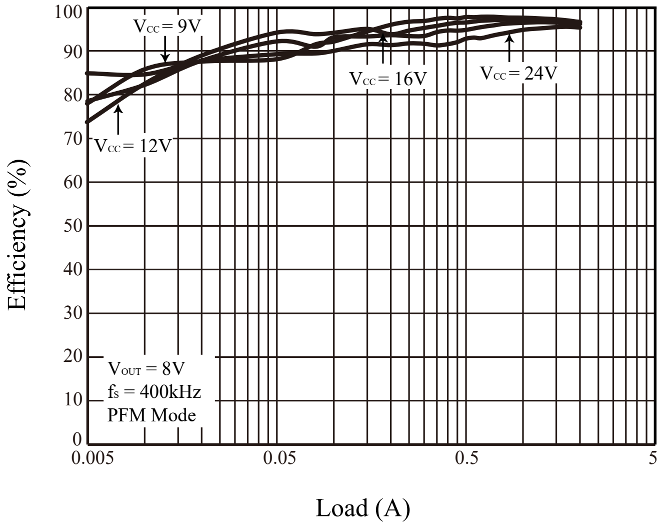


Figure 21 Efficiency vs. Load

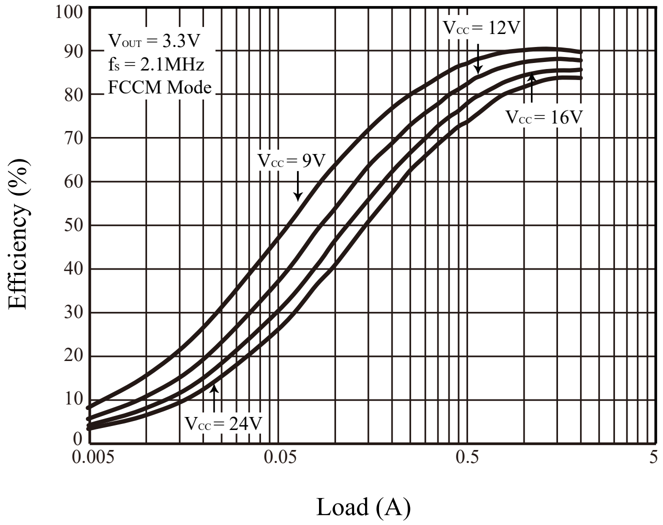


Figure 22 Efficiency vs. Load

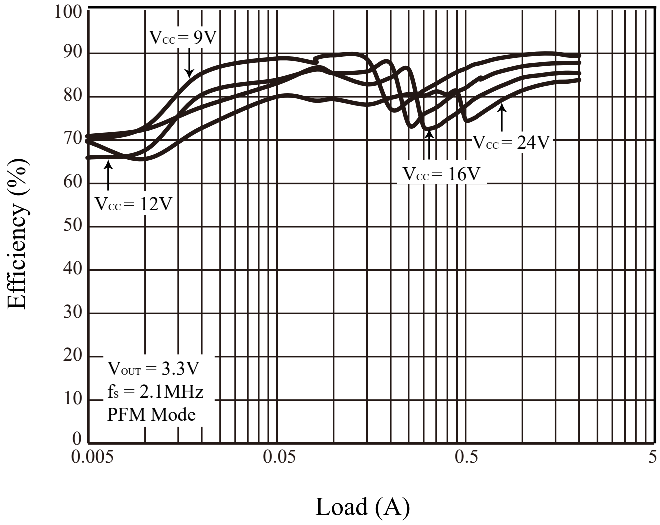


Figure 23 Efficiency vs. Load

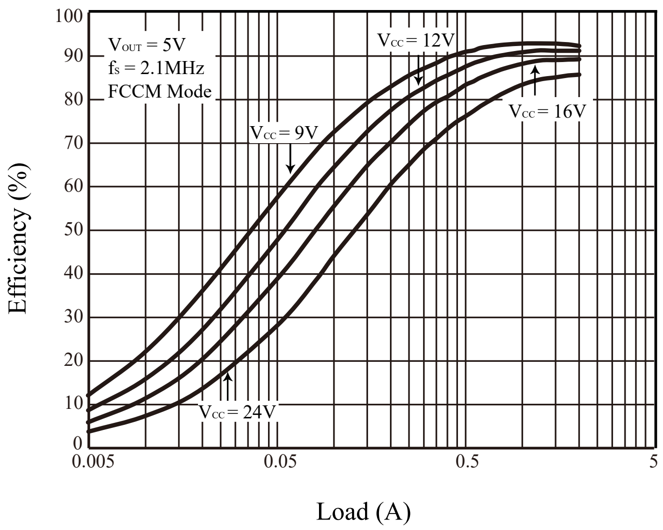


Figure 24 Efficiency vs. Load

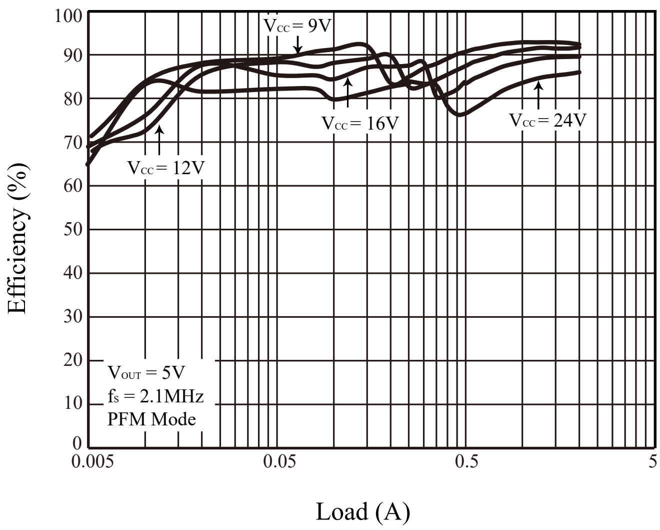


Figure 25 Efficiency vs. Load

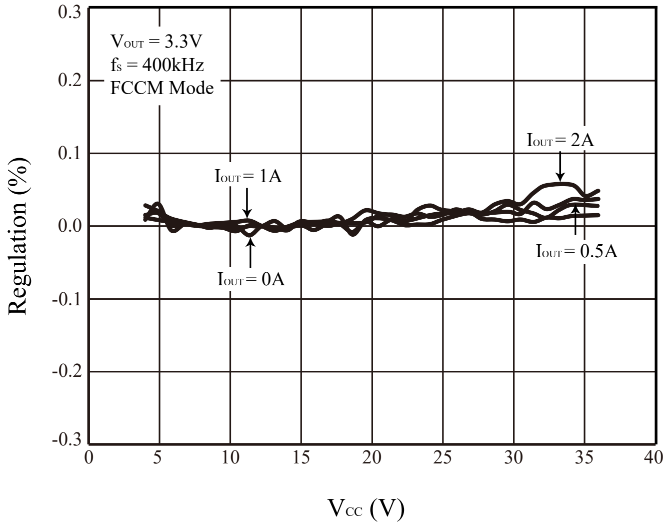


Figure 26 Line Regulation

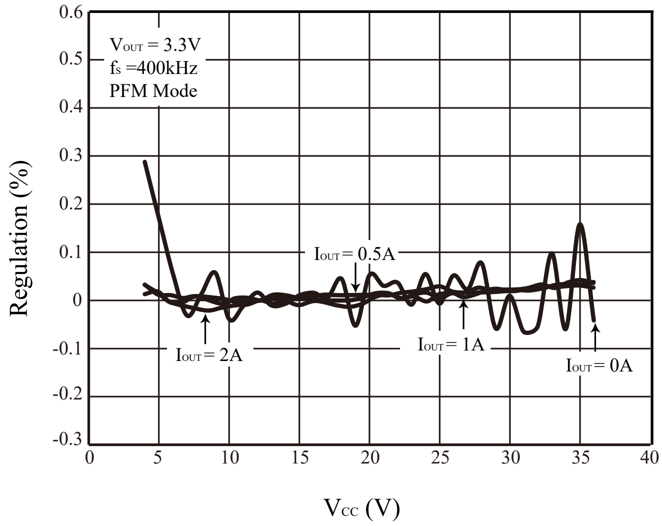


Figure 27 Line Regulation

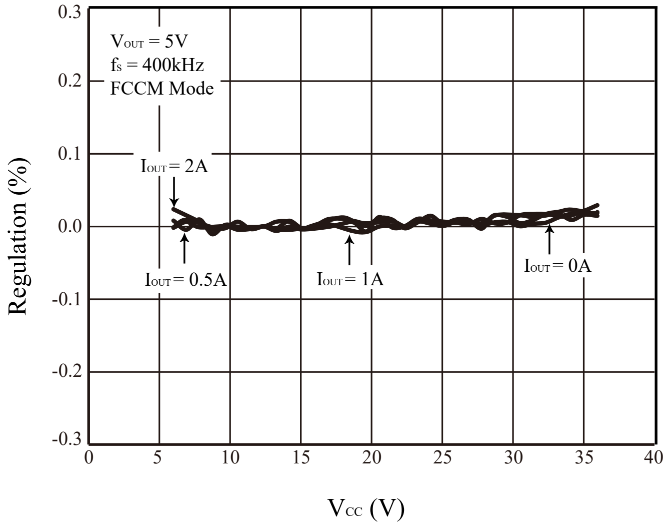


Figure 28 Line Regulation

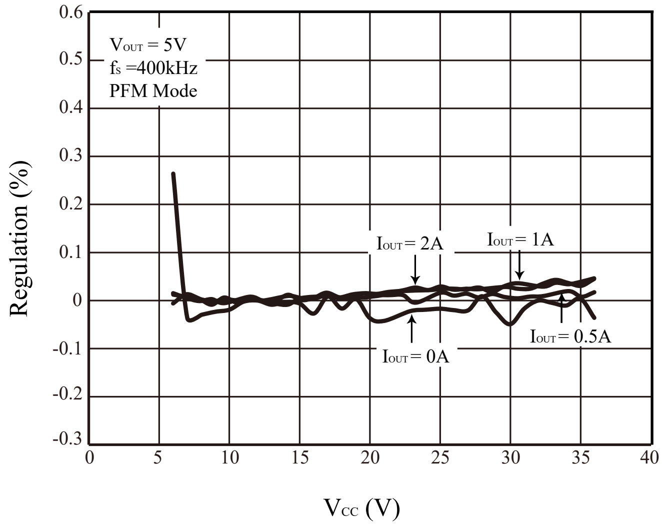


Figure 29 Line Regulation

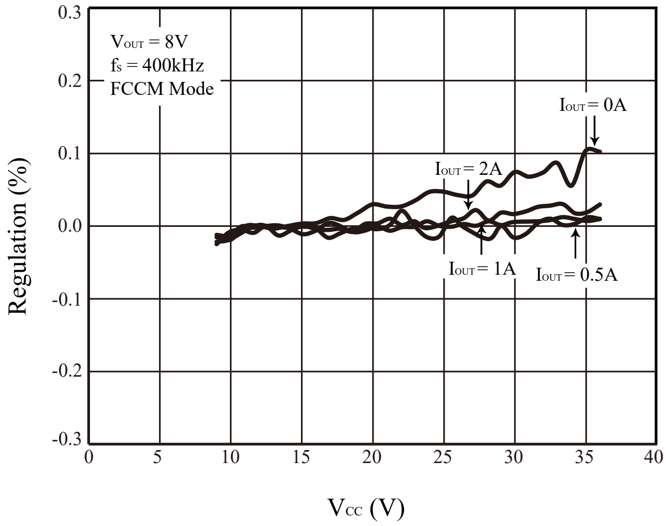


Figure 30 Line Regulation

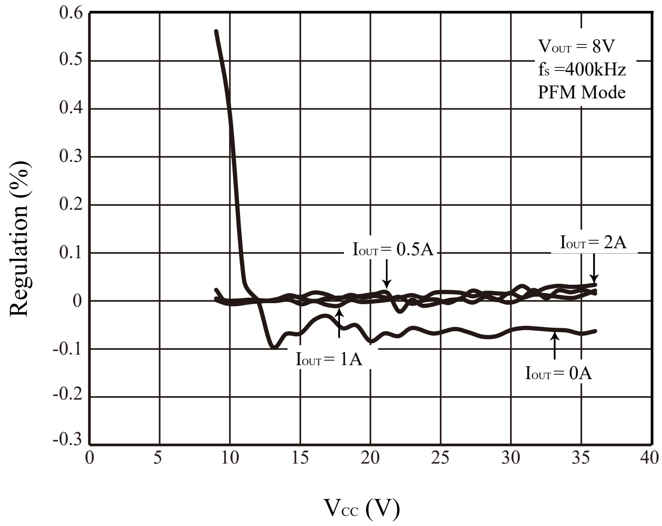


Figure 31 Line Regulation

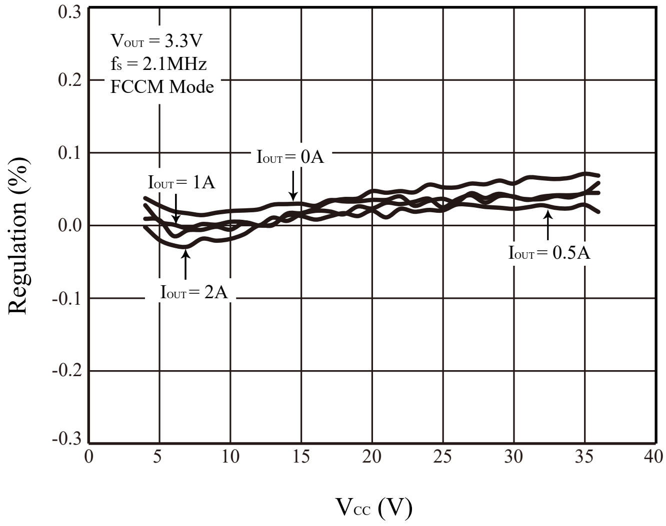


Figure 32 Line Regulation

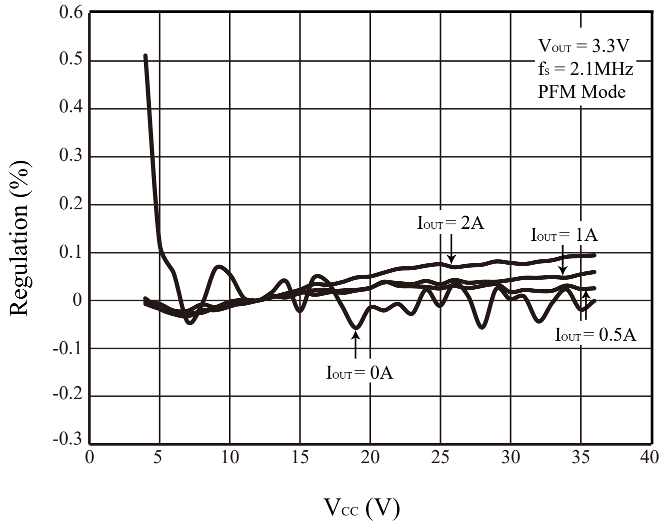


Figure 33 Line Regulation

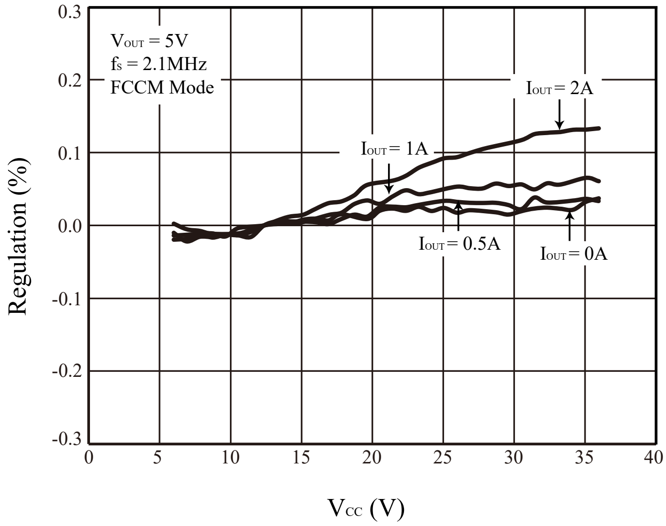


Figure 34 Line Regulation

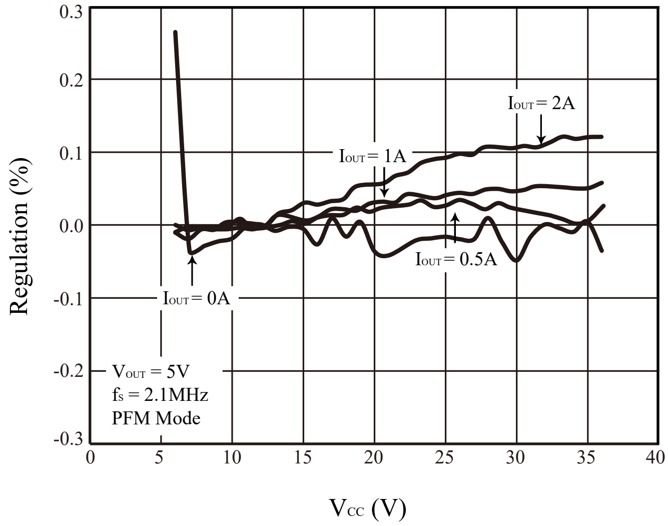


Figure 35 Line Regulation

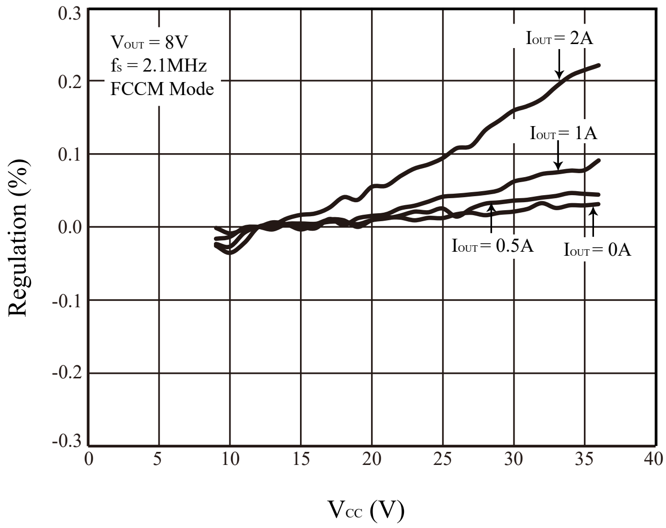


Figure 36 Line Regulation

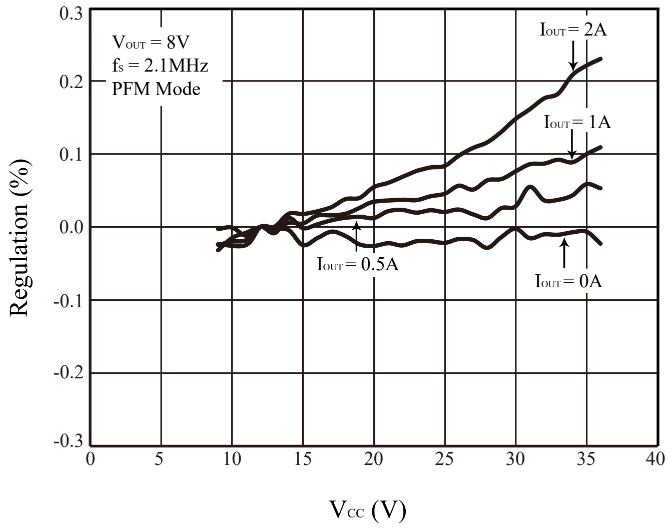


Figure 37 Line Regulation

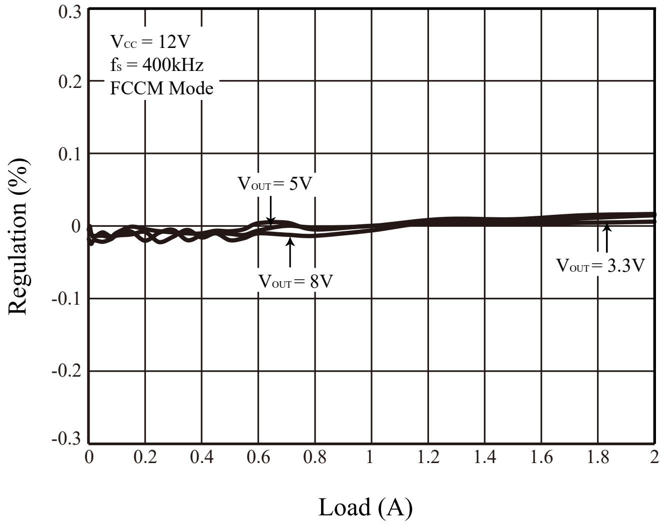


Figure 38 Load Regulation

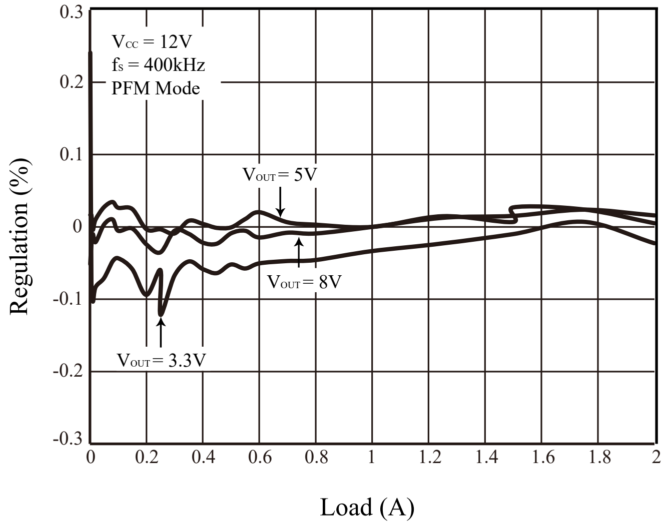
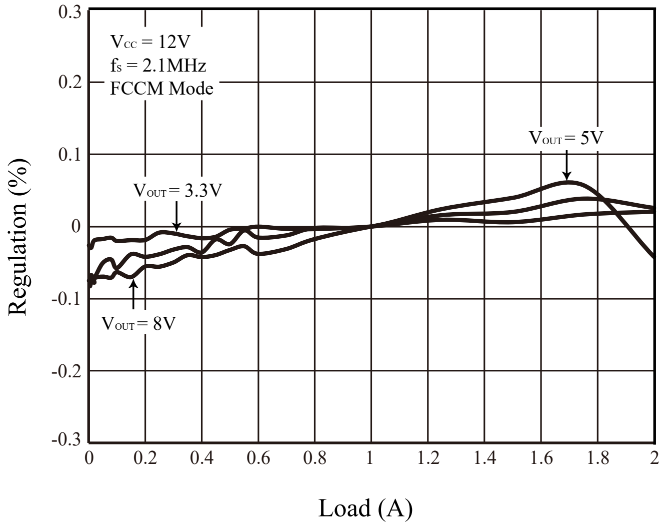


Figure 39 Load Regulation



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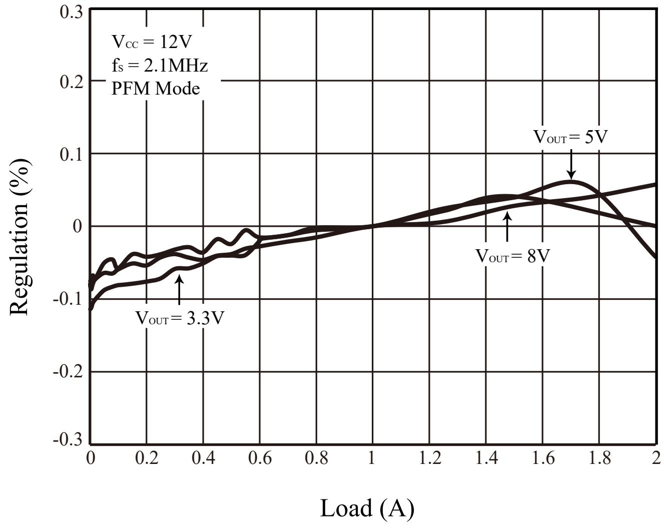


Figure 41 Load Regulation

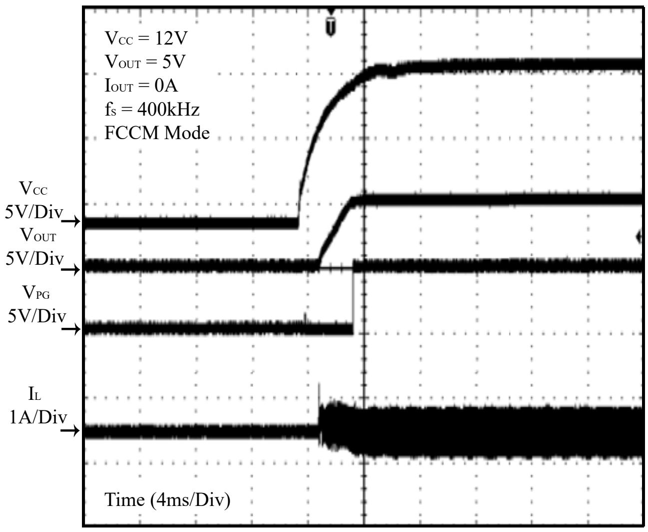


Figure 42 Start Up with VCC

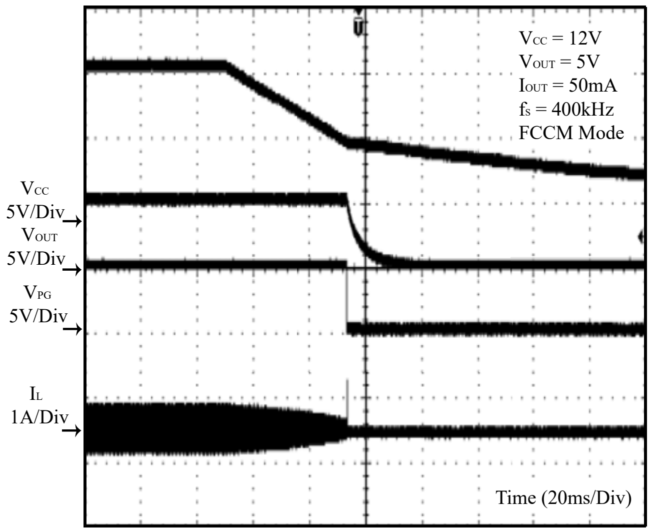
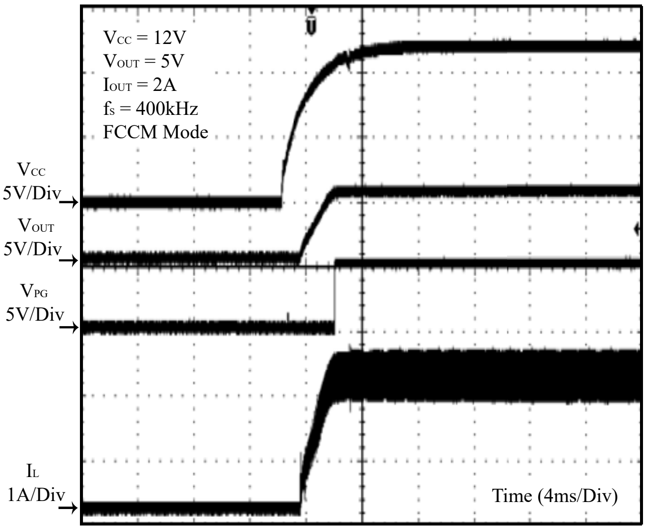


Figure 43 Shut Down with VCC



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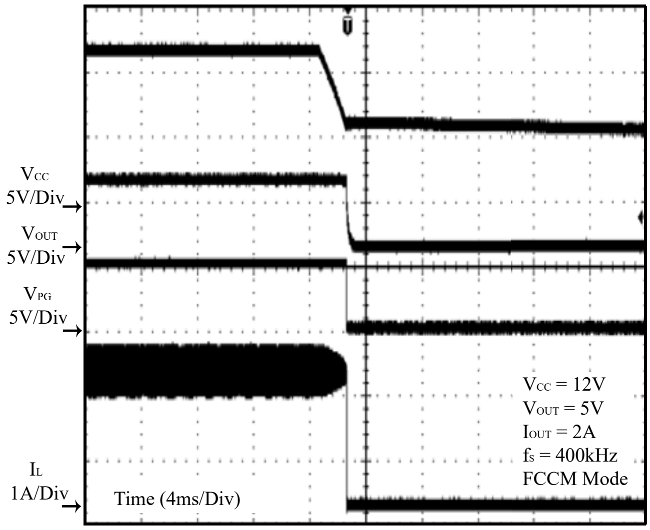


Figure 45 Shut Down with VCC

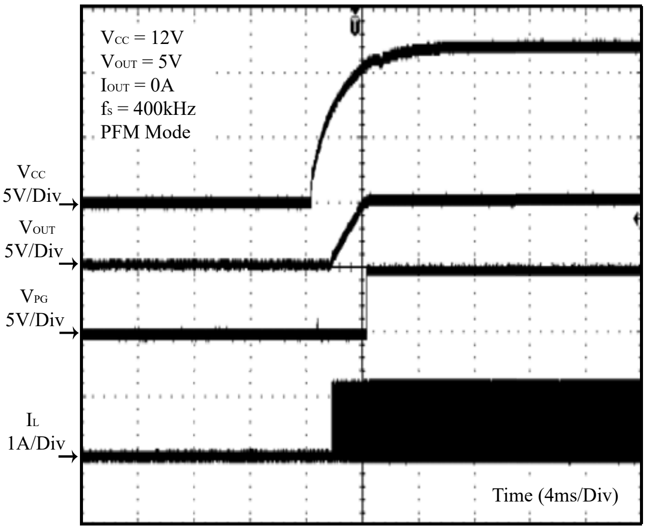


Figure 46 Start Up with VCC

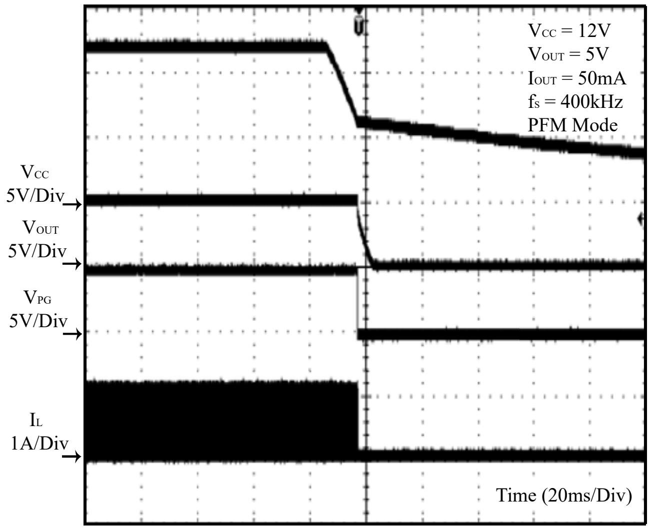


Figure 47 Shut Down with VCC

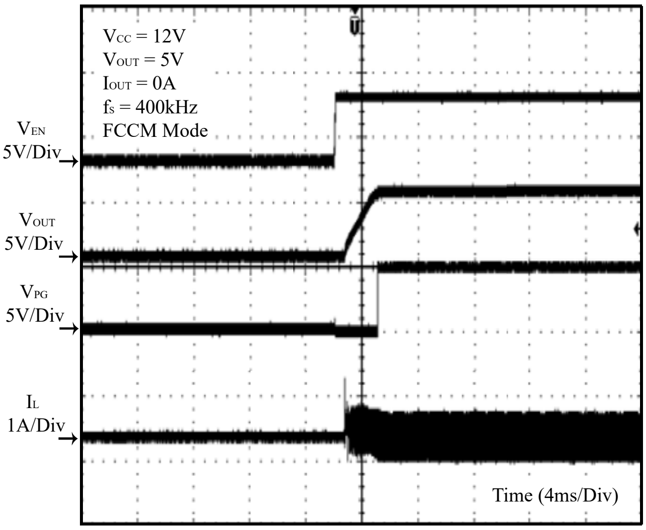


Figure 48 Start Up with EN

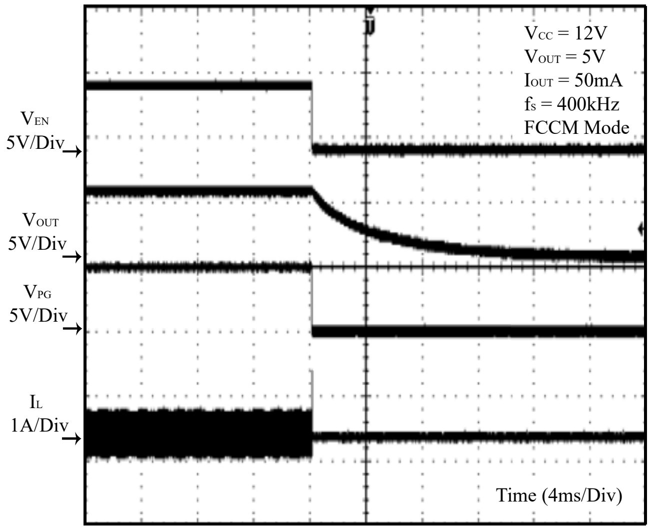
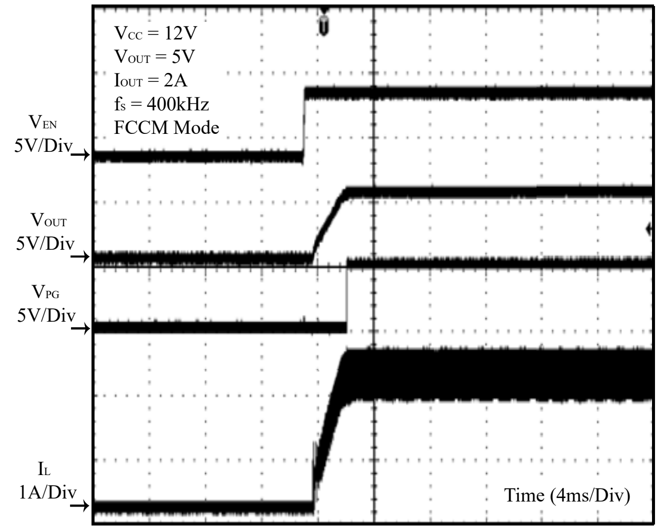


Figure 49 Shut Down with EN



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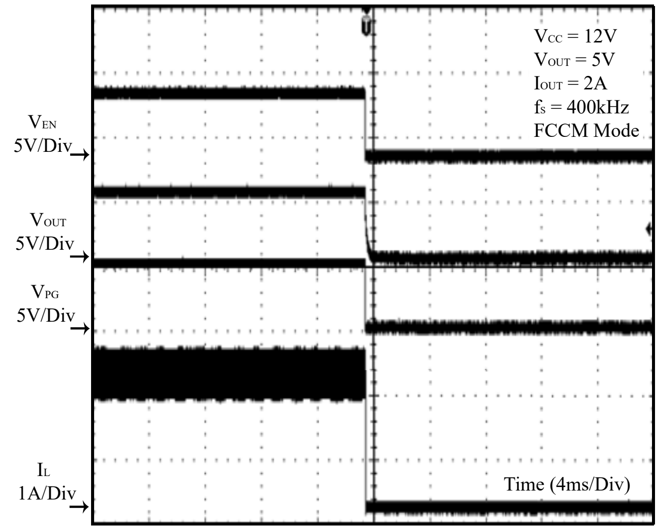

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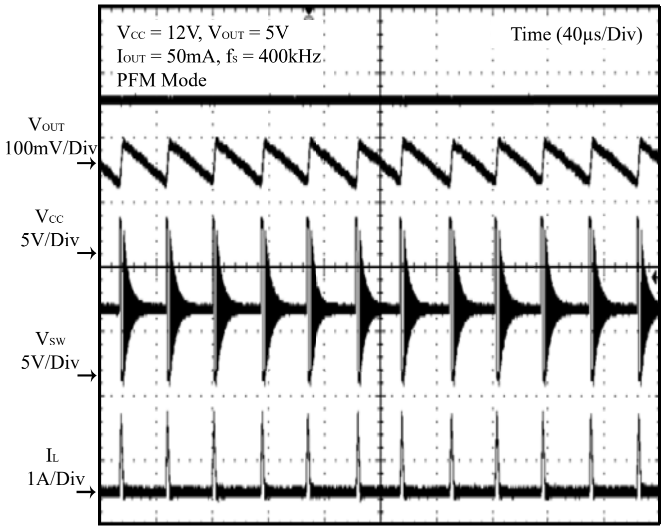


Figure 52 Output Ripple

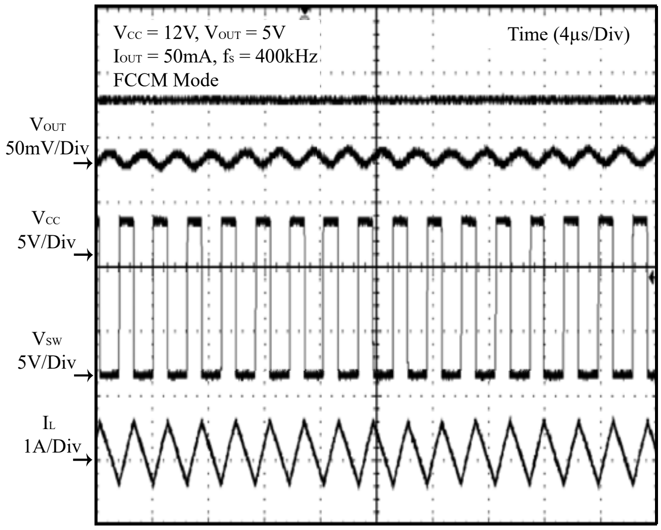


Figure 53 Output Ripple

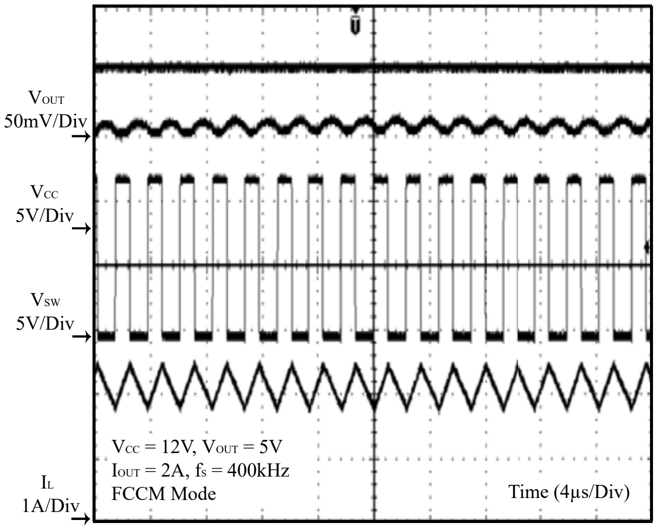


Figure 54 Output Ripple

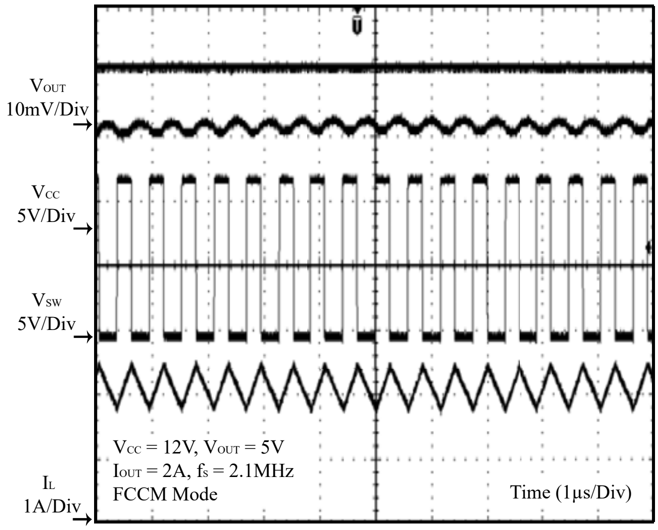


Figure 55 Output Ripple

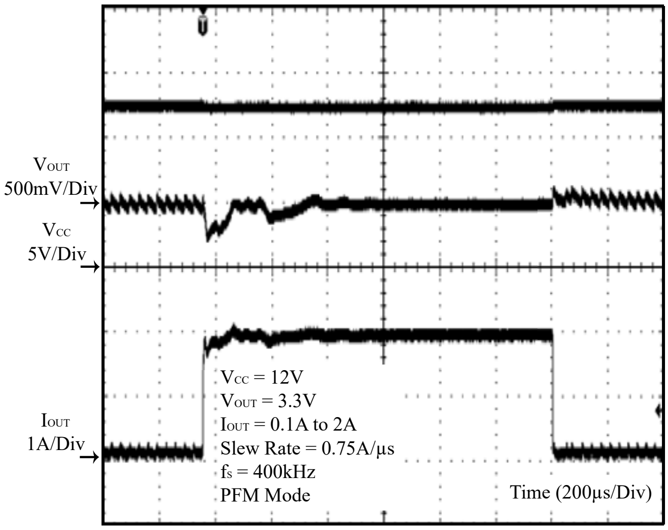
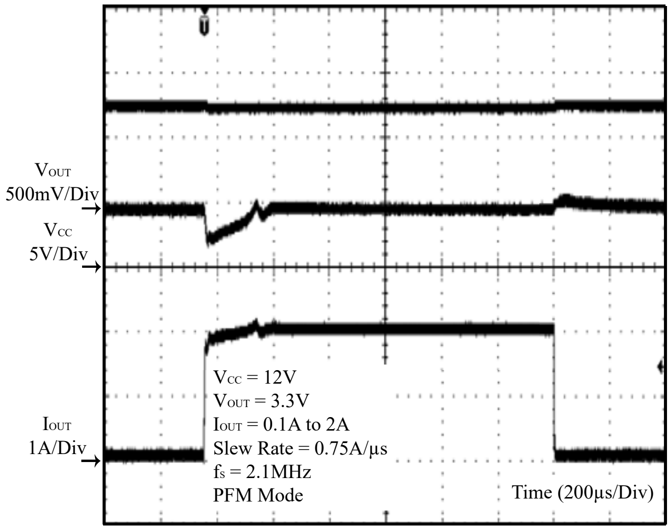


Figure 56 Load Transient



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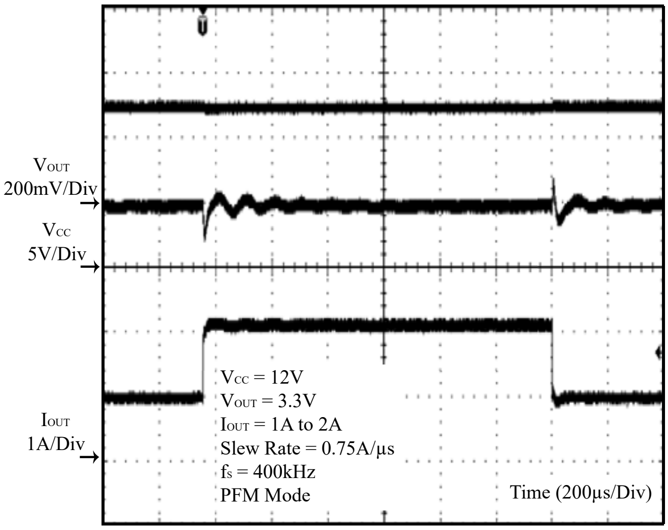


Figure 58 Load Transient

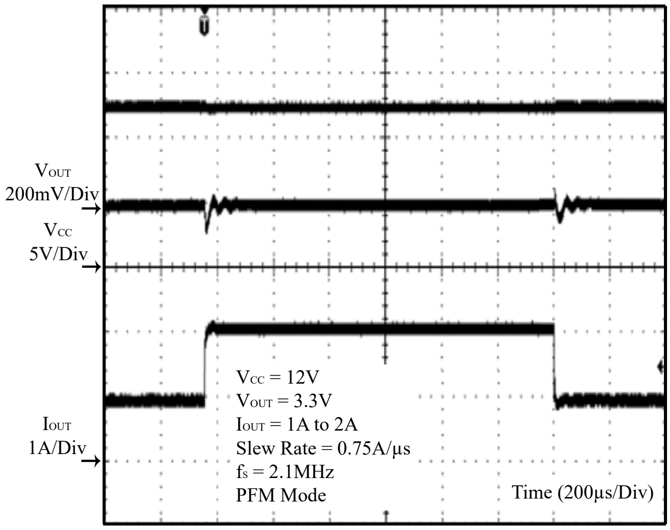


Figure 59 Load Transient

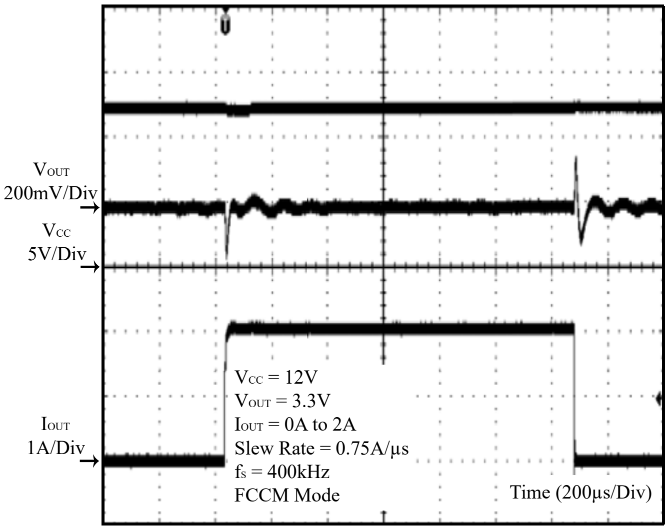


Figure 60 Load Transient

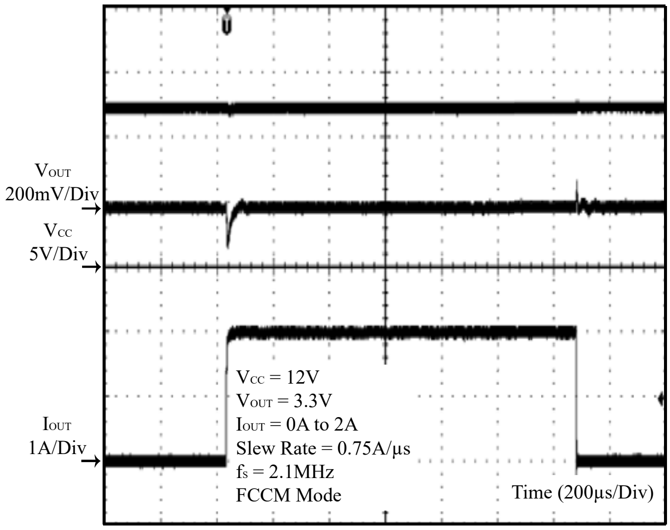


Figure 61 Load Transient

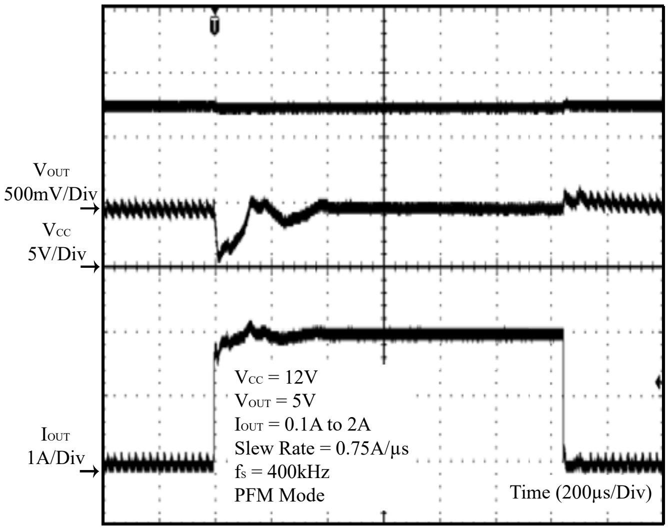


Figure 62 Load Transient

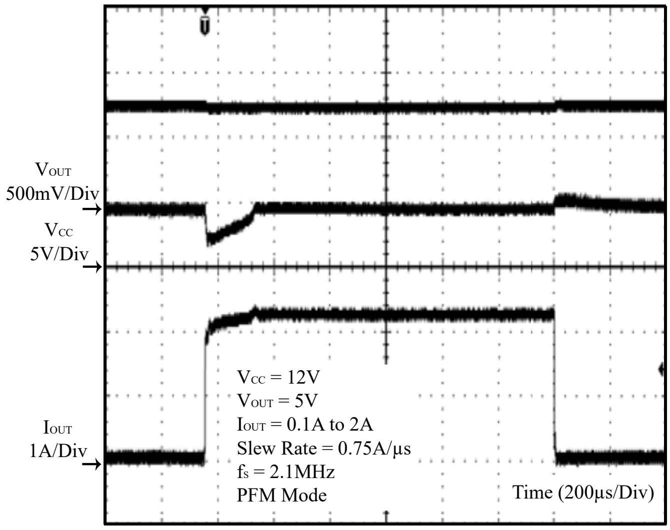


Figure 63 Load Transient

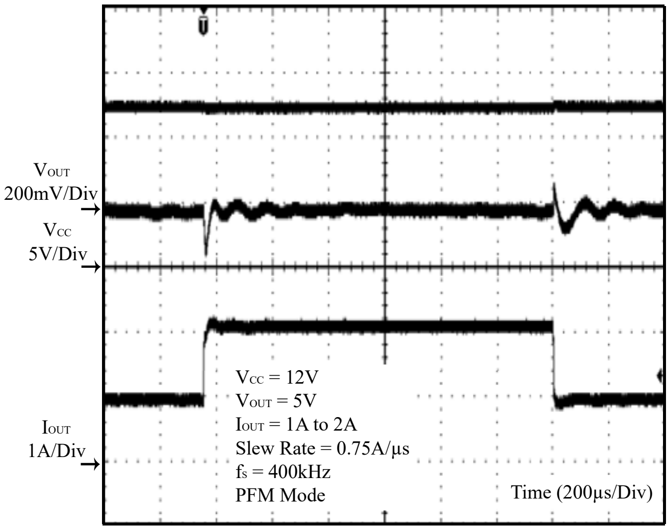


Figure 64 Load Transient

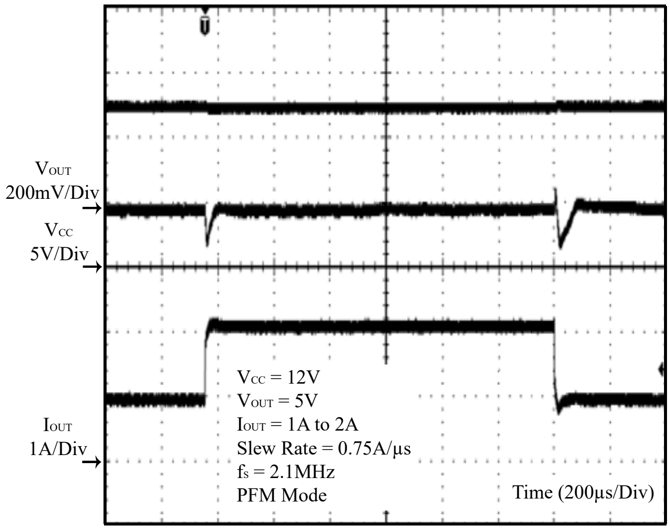


Figure 65 Load Transient

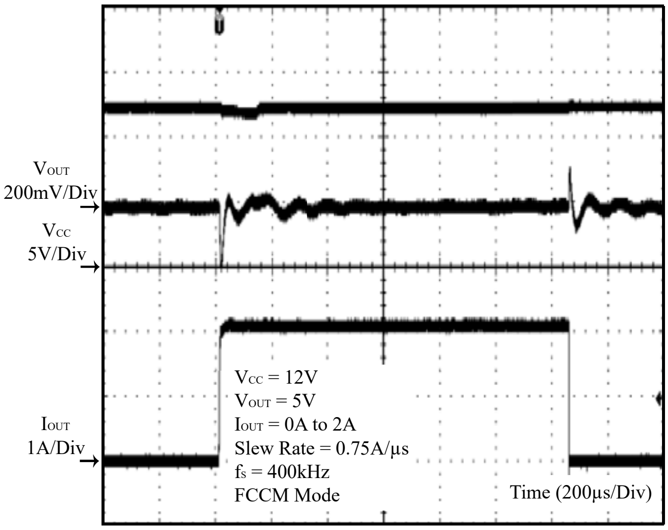


Figure 66 Load Transient

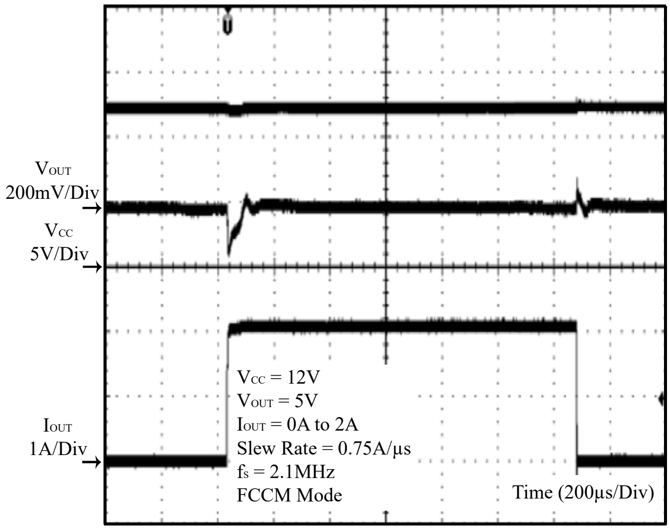


Figure 67 Load Transient

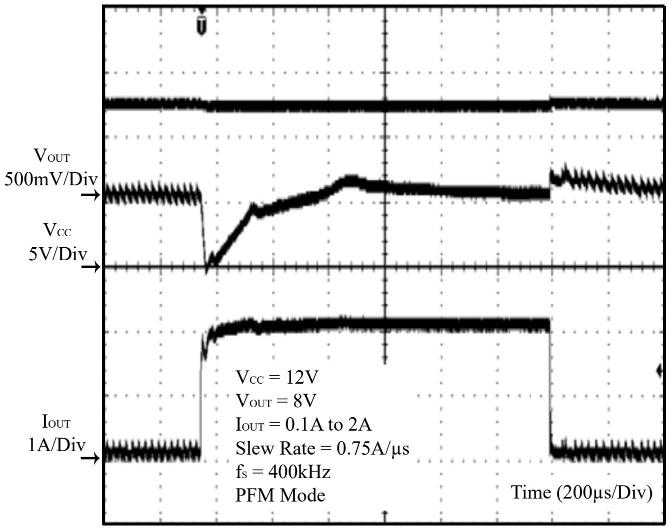


Figure 68 Load Transient

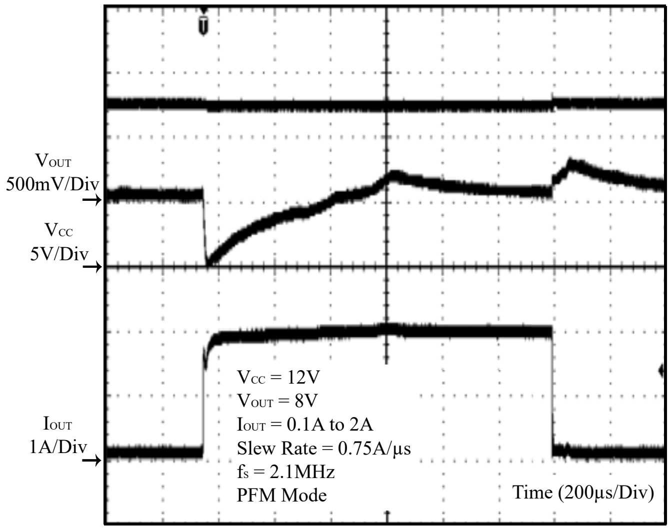


Figure 69 Load Transient

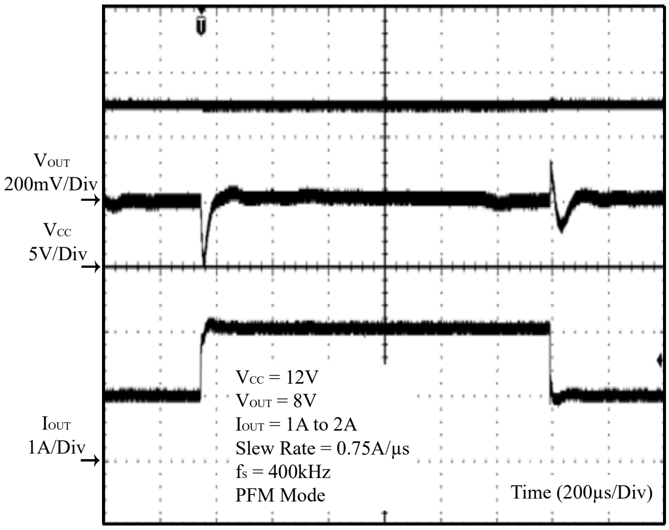


Figure 70 Load Transient

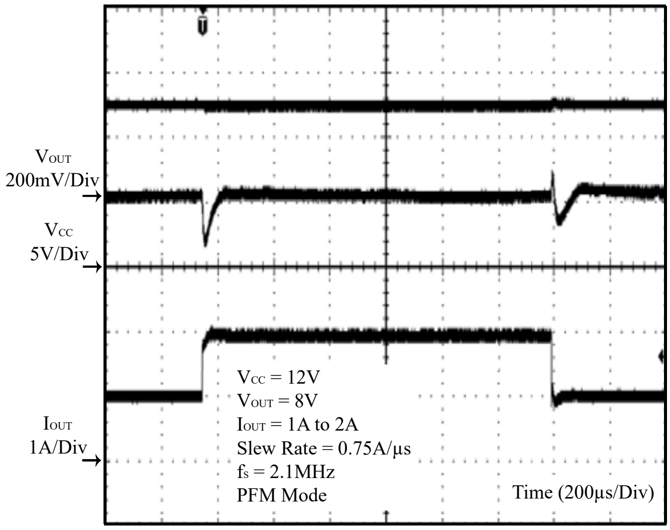


Figure 71 Load Transient

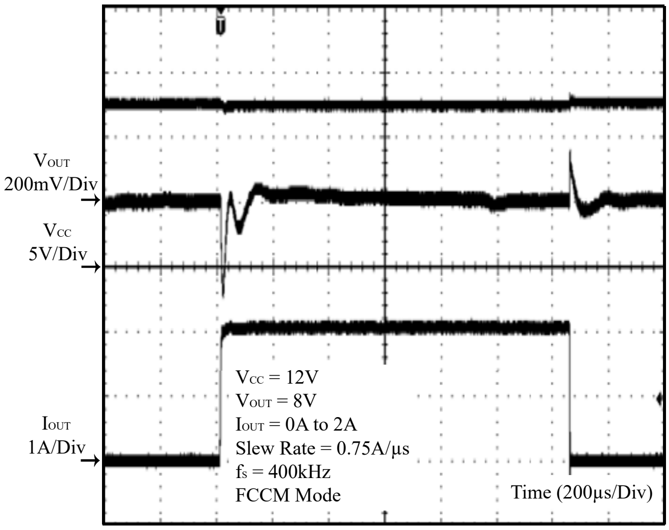


Figure 72 Load Transient

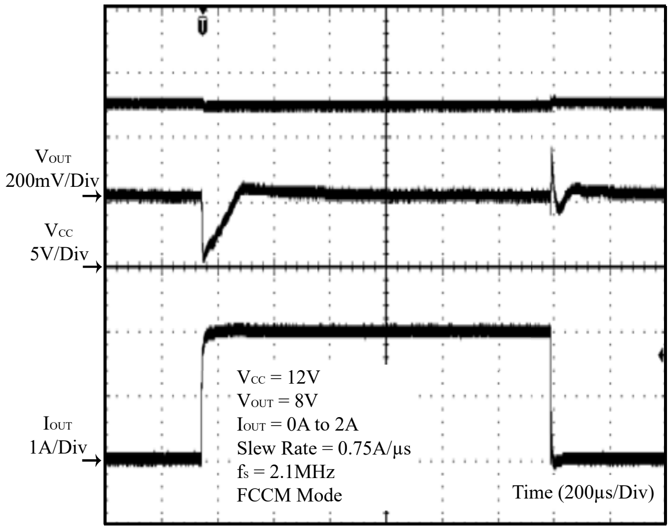


Figure 73 Load Transient

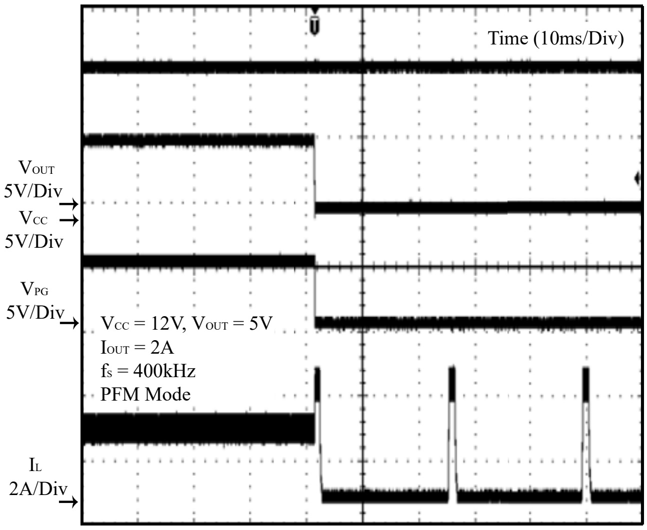


Figure 74 V_{OUT} Short to GND

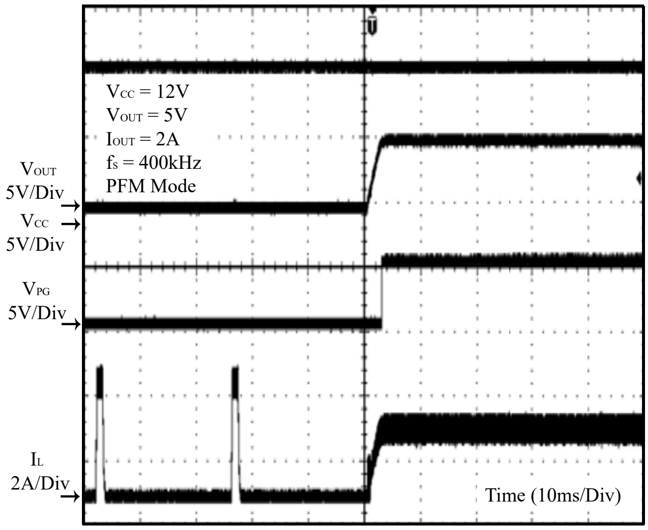


Figure 75 Short Circuit Recovery

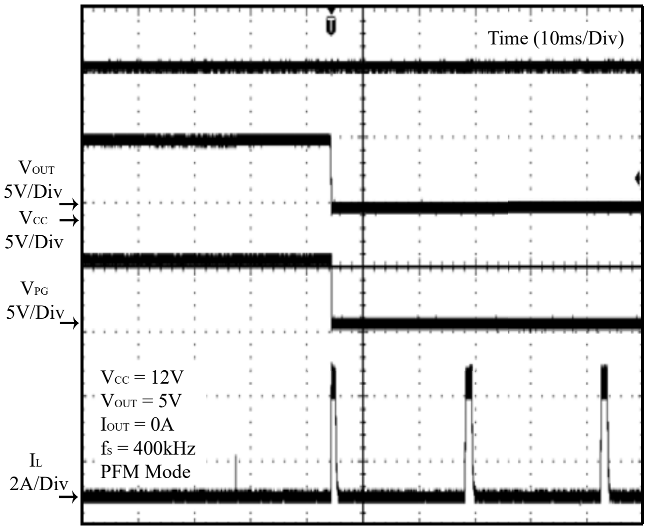


Figure 76 V_{OUT} Short to GND

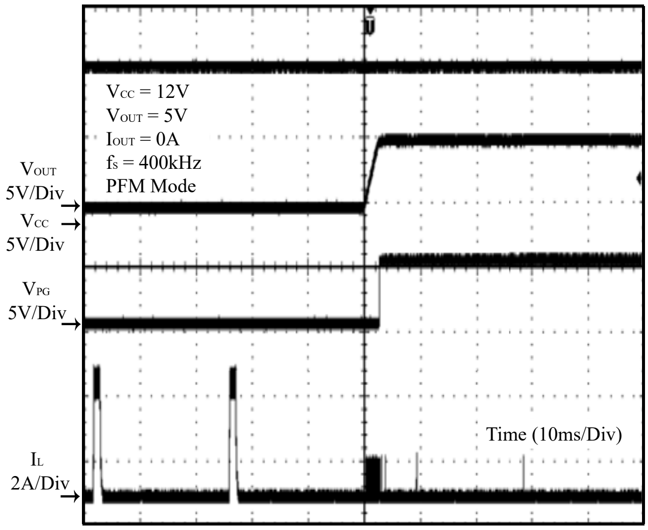


Figure 77 Short Circuit Recovery

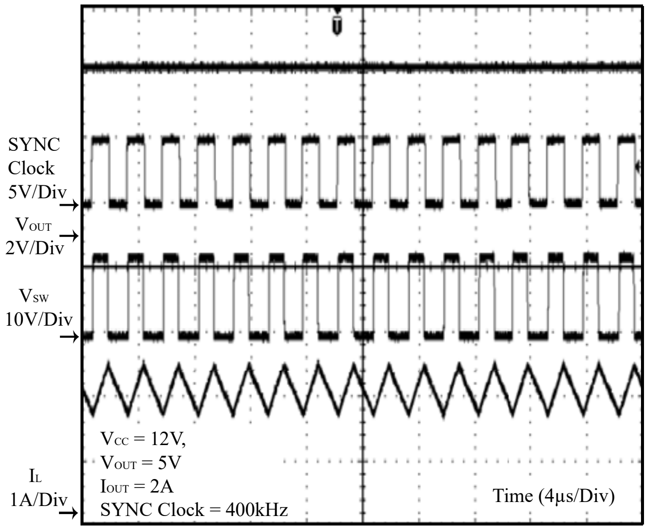


Figure 78 SYNC Clock

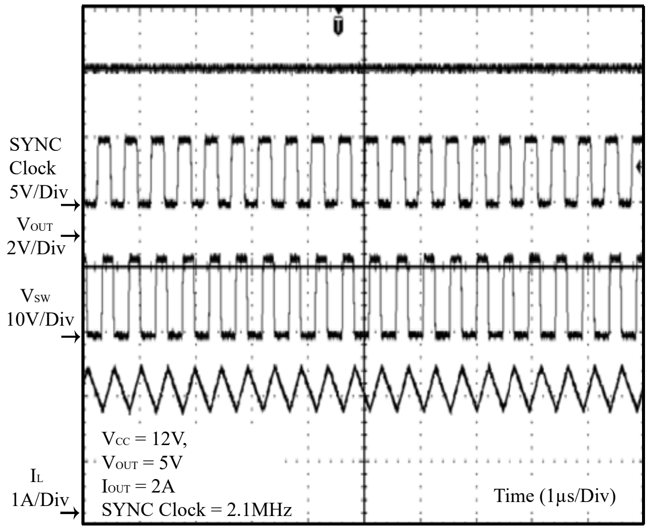


Figure 79 SYNC Clock

DETAILS DESCRIPTION

The IS32PM3426 is a fully integrated Synchronous rectified step-down switch-mode converter. Constant-on time (COT) control is employed to provide fast transient response and easy loop stabilization. At the beginning of each cycle, the high-side MOSFET (HS-FET) is turned on when the FB pin voltage (V_{FB}) is below the error amplifier output voltage (EAO), which indicates an insufficient output voltage. The output voltage and input voltage determine the on-period, keeping the switching frequency fairly constant over the input voltage range.

After the on-period elapses, the HS-FET is turned off, it is turned on again when V_{FB} drops below EAO. The converter regulates the output voltage by repeating the operation in this way. The integrated low-side MOSFET (LS-FET) is turned on when the HS-FET is in its off state to minimize conduction loss. There is a dead short between the input and GND if both the HS-FET and LS-FET are turned on at the same time. This is called shoot-through. To avoid shoot-through, a dead-time (DT) is generated internally between the HS-FET off and LS-FET on period or the LS-FET off and HS-FET on period.

Internal compensation is applied for COT control to provide a more stable operation and fast transient response, even when ceramic capacitors are used as output capacitors.

MODE SELECTION AT LIGHT-LOAD OPERATION

The IS32PM3426 has an FPWM pin that can offer two states of operations, FCCM mode and PFM mode, at light load conditions. If the voltage of the FPWM pin higher than V_{FPWM_IH}, IS32PM3426 operates in Forced Continuous Conduction Mode (FCCM) at light-load conditions allowing the inductor current to become negative. With FCCM mode, the operating frequency is maintained at a fairly constant level over the entire load range from light-load to full-load, which minimizes output voltage ripples and avoids the operating frequency dropping into audible frequency range (≤20kHz) which may introduce some audible noise.

However, if the voltage of the FPWM pin is lower than V_{FPWM_IL}, IS32PM3426 operates in Pulse-Frequency Modulation (PFM) mode during light-load operation and reduces the switching frequency automatically to maintain high efficiency, and the inductor current drops almost to zero. As shown in Figure 80, the HS-FET turns on when the FB pin voltage (V_{FB}) is below the error amplifier output voltage (EAO). The HS-FET turns off when the on-timer elapses and the inductor current is higher than its given threshold. When the inductor current reaches zero, the LS-FET driver goes into tri-state (Hi-Z). Therefore, the output capacitors discharge slowly to GND through the LS-FET and the resistors R_{FBT} and R_{FBB}. This operation improves device efficiency greatly when the output current is low.

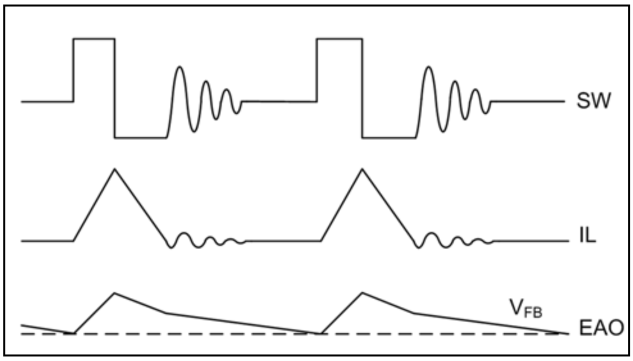


Figure 80 PFM Operation Mode at Light-load

OVER-CURRENT PROTECTION (OCP)

The IS32PM3426 senses both HS-FET and LS-FET currents for cycle-by-cycle peak and valley current limits and protect the output from an over-current or short-circuit protection condition. If the converter is over-current and eventually the HS-FET current hits the HS-FET current limit threshold I_{HSLIM}, the HS-FET turns off to limit the increasing current. Then the LS-FET turns on and monitors the current flowing through it. The HS-FET waits until the LS-FET current ramps down to the LS-FET current limit (I_{LSLIM}) before turning on again. As a result, the converter operates in inductor current hysteretic control, upper threshold I_{HSLIM} and lower threshold I_{LSLIM}. This represents the maximum output current from the converter and is approximately given by the following equation:

$$I_{OUT\_MAX} = \frac{(I_{HSLIM} + I_{LSLIM})}{2} \quad (1)$$

When the load current is higher than I_{OUT_MAX}, the output voltage tends to drop because the load current demand is higher than what the converter can support. If the hysteretic control operating persists for 32 switching cycles, and the output voltage falls below the output under-voltage threshold (Typ. 40% of the regulation voltage), in this case, the converter enters hiccup mode to restart the part periodically with the hiccup time t_{HC} (Typ. 22ms), as shown in Figure 81. The hiccup protection mode is especially useful when the output is dead-shorted to the ground. This reduces the average short-circuit current greatly, alleviating thermal issues and protecting the converter. The converter exits hiccup mode once the over-current or short-circuit condition is removed.

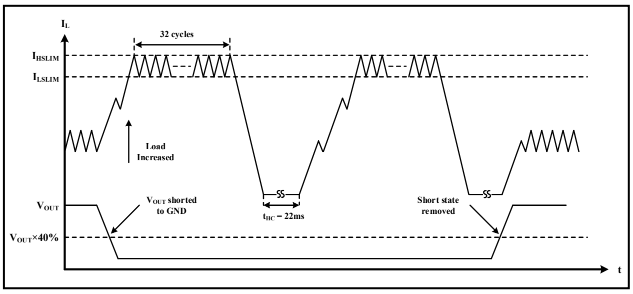


Figure 81 Hiccup Mode

Due to FCCM operation, when the output current is less than half of the peak-to-peak inductor current ripple, the inductor valley current ramps down to negative (LS-FET sinks current). The IS32PM3426 also incorporates a negative current limit to protect the LS-FET against sinking excessive current and possibly damaging the converter. If the LS-FET sink current hits the negative current limit (I_{LSRS}), the LS-FET turns off until after the next HS-FET on-time.

OVER-VOLTAGE PROTECTION (OVP)

The IS32PM3426 monitors the FB pin voltage to detect over-voltage condition. When V_{FB} becomes higher than 110% (Typ.) of the regulation feedback voltage V_{FB_TH}, the over-voltage protection (OVP) is triggered after a deglitch time of 16µs (Typ.). The converter stops switching and does not resume until the V_{FB} drops to V_{FB_TH}. The OVP function protects the downstream devices from over-voltage damage.

VDD REGULATOR

The IS32PM3426 contains a linear regulator (V_{DD}) with 5V (Typ.) output voltage to supply internal circuit blocks including the control logic circuits and the HS-/LS-FET gate drivers. The V_{DD} regulator is internally current limited to I_{DD_LIM} (Min. 20mA). It operates in the full V_{CC} range, When the V_{CC} voltage exceeds 5V, the regulator will stabilize at 5V (Typ.) output, but if V_{CC} is lower than 5V, its output decreases with V_{CC}. During operation, driving HS-/LS-FET gates will draw transient high current from this linear regulator. Therefore, a 1µF low ESR, X7R type ceramic capacitor is necessary from the VDD pin to GND; it must be placed as close to the VDD pin as possible. V_{DD} can bias external low current circuitry requiring a reference supply, such as pulling up bias voltage for PG pin, however, do not recommend powering any high current external device with the VDD pin to ensure system stability.

FLOATING DRIVER AND BOOTSTRAP CHARGING

The gate driver of the integrated HS-FET requires a voltage above V_{CC} as an input power supply. As the circuit diagram shown in Figure 82, the VDD regulator is the power supply of the gate driver. The BST pin is internally connected to the output of the VDD regulator through a P-FET switch. Connect a ceramic capacitor between BST and SW pins. The VDD regulator charges the C_{BST} capacitor during HS-FET off and LS-FET on cycles. Then in HS-FET on cycles, the C_{BST} charge voltage is used to boost the BST pin to 5V higher than the SW pin.

A 0.1µF X7R ceramic capacitor will work well in most applications. The gate driver also has an under-voltage lockout detection. The gate driver is enabled when the voltage on the C_{BST} rises to above 2.86V (Typ.) and disabled when the voltage on the C_{BST} drops below 2.55V (Typ.).

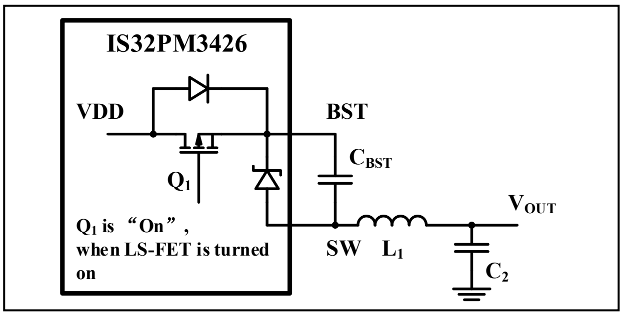


Figure 82 Bootstrap Charging Circuit

SWITCHING FREQUENCY

During switching, the IS32PM3426 operates in a constant on-time mode. The on-time is adjusted by the external resistor, R_{FS}, which is connected from the FS pin to AGND. The IS32PM3426 supports switching frequency (f_{SW}) from 100kHz to 2.2MHz which can be calculated by the below Equation:

$$f_{SW} = \frac{1}{(1+R_{FS})\times 0.029} \quad (2)$$

Where f_{SW} is in MHz and R_{FS} is in kΩ.

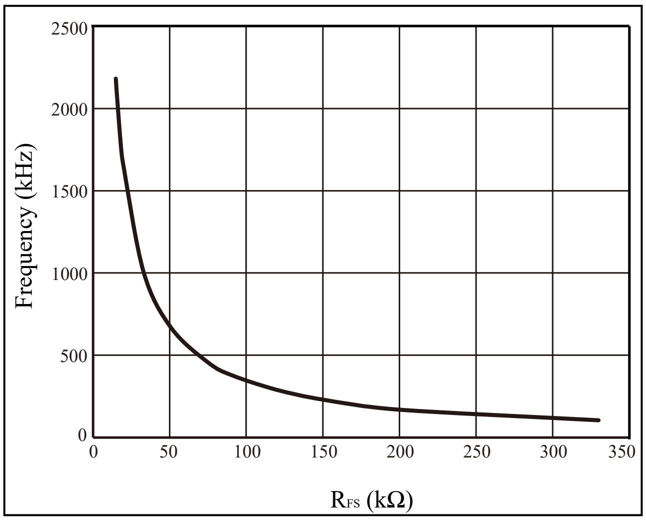


Figure 83 Frequency vs. R_{FS}

Higher frequency operation results in smaller component size but increases the switching losses. It may also increase the high-side MOSFET gate driving current and may not allow sufficient high or low duty cycle. Lower frequency gives better performance but results in larger component size.

SWITCHING FREQUENCY SYNCHRONIZATION

The FS pin can also be used as a synchronization input, allowing the IS32PM3426 to operate with an external clock in the range of 100kHz to 2.2MHz as long as its pulse width satisfies the requirements of t_{SYNC_MIN}. Figure 84 shows the timing for a synchronization clock into the IS32PM3426 at 2MHz. Any pulse with a duty cycle of 16% to 84% at 2MHz can be used to synchronize the IC. However, driving FS pin with a 50% duty cycle waveform is always a good choice.

Table 1 Synchronization Duty Cycle Range

SYNC Clock Frequency(kHz)	Duty Cycle Range (%)
2000	16~84
1000	8~92
400	3.2~96.8

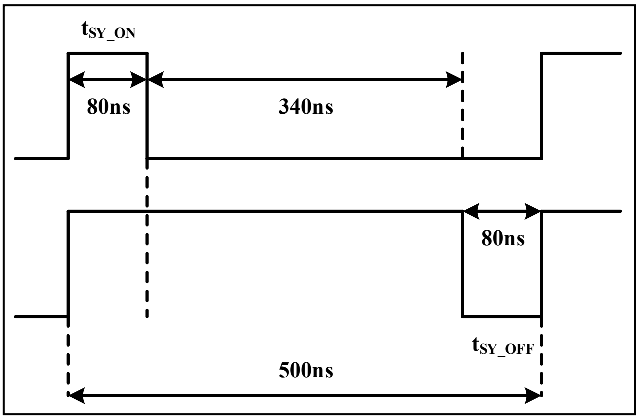


Figure 84 2MHz SYNC Application Example

When an external synchronization clock is applied to the FS pin, the internal oscillator is over-driven so that each switching cycle begins at the rising edge of an external clock. The high level of the external clock must be not lower than 2V and low level must be not higher than 0.4V. The FS pin should not be left floating. Otherwise, the operating switching frequency will be 400kHz. It recommends connecting a resistor R_{FS} from the FS pin to GND, as shown in Figure 85, such that the internal oscillator frequency is the same as the target clock frequency when the IS32PM3426 is synchronized to an external clock. This allows the regulator to continue operating at approximately the same switching frequency if the external clock fails.

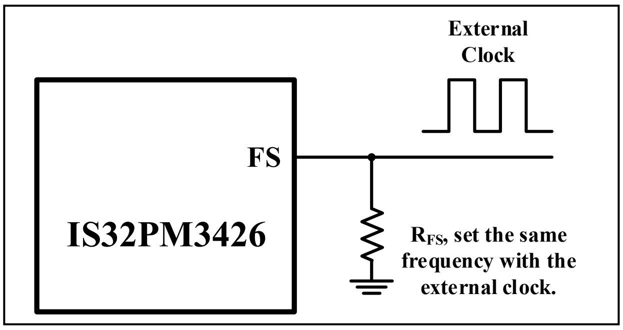


Figure 85 FS Pin Configuration

SPREAD SPECTRUM

A switch mode controller can be troublesome when EMI is concerned. To optimize EMI performance, IS32PM3426 includes a spread spectrum feature, which is an 800Hz (Typ.) with ±5% (Typ.) operating frequency jitter. It can spread the total electromagnetic emitting energy into a wider range that significantly degrades the peak energy of the EMI profile. With a spread spectrum, the EMI test can be passed with a smaller size and lower cost filter circuit.

SOFT-START

The IS32PM3426 features an internal 2ms (Typ.) soft-start function. The soft-start function of IS32PM3426 allows the converter to gradually reach a steady-state operating point, thereby dampening the inrush current to an acceptable value at startup. When the EN pin is set to start the converter operation, the internal soft-start circuitry generates a ramping up voltage with a controlled slope. When it is lower than the internal reference of the error amplifier (EA), the soft-start voltage overrides the EA's reference, so the EA uses the soft-start voltage as the reference. Once the soft-start voltage exceeds EA's reference, EA's reference regains loop control. The soft-start period time is internally fixed at 2ms (Typ.) and not adjustable.

If the output capacitor is pre-biased at startup, the converter starts switching and ramping up only after the internal soft-start voltage exceeds the FB pin voltage V_{FB}. This scheme ensures that the converters ramp up smoothly into a regulation point.

POWER GOOD (PG)

The IS32PM3426 has a dedicated flag output pin, PG, to indicate output power good state. The PG pin is an open drain structure which requires an external pull-up resistor connected to a voltage source. The recommended pull-up resistor is 47kΩ. The PG pin goes high after a delay time t_{PG_RF} (Typ. 120µs) if the output voltage is within 93% to 107% of the nominal voltage; while it goes low after a delay time t_{PG_RF} (Typ. 120µs) if the output voltage is above 107% or below 93% of the nominal voltage. To prevent glitch both the upper and lower thresholds include 2% of hysteresis.

The PG pin is also actively pulled low during several other conditions, including EN low, VCC/VDD UVLO protection, output OVP protection and thermal shutdown protection.

LOW DROPOUT OPERATION

The IS32PM3426 supports low dropout operation. When the V_{CC} voltage is close to the output voltage and the minimum off-time is triggered, the switching on timer is extended to avoid output voltage drops. The switching frequency decreases accordingly. After the maximum on time is triggered (Typ. 10μs), switching enters max duty cycle operation. If the V_{CC} voltage continues to decrease, the output voltage will begin to decrease gradually with the V_{CC} voltage.

ENABLE CONTROL

The EN pin has a dual-level threshold. When the EN voltage is below $V_{EN\_VDD\_L}$, the regulator is in an ultra-low current shutdown mode. When the EN voltage is greater than $V_{EN\_VDD\_H}$, but less than $V_{EN\_VOUT\_H}$, the V_{DD} regulator is in standby mode. In standby mode, the V_{CC} bias V_{DD} regulator is active but converter switching remains disabled. Normal switching operation begins when the voltage at the EN pin exceeds the threshold $V_{EN\_VOUT\_H}$. Use an external resistor voltage divider from VCC to GND to set the minimum operating voltage of the convertor. If the EN voltage is lower than $V_{EN\_VDD\_L}$, the whole system will shut down.

Never leave the EN pin floating. It has high impedance and high-voltage tolerance and can be connected directly to the VCC pin if it is unused. However, a series resistor (recommended value of 47kΩ) is required to limit the current flowing in to the EN pin if it is higher than the V_{CC} voltage at any time.

UNDER-VOLTAGE LOCKOUT PROTECTION

The IS32PM3426 has two Under-voltage Lockout (UVLO) protections: V_{DD} UVLO and V_{CC} UVLO. The IS32PM3426 starts up only when both V_{DD} and V_{CC} exceed their respective UVLO threshold and shuts down when either V_{DD} is lower than the V_{DD} UVLO falling threshold voltage or V_{CC} is lower than the V_{CC} UVLO falling threshold. Both are non-latch off protections.

Besides this internal fixed UVLO, it may be desirable to externally set a higher UVLO threshold for some applications. As shown in Figure 86, a precise EN threshold voltage can be set by using a resistor voltage divider between VCC and GND with the center connected to the EN pin. The external UVLO threshold voltage can be computed by the following Equations:

$$V_{CC\_UVEXR} = \frac{(R_{EN1}+R_{EN2})}{R_{EN2}} \times V_{EN\_VOUT\_H} \quad (3)$$

$$V_{CC\_UVEXF} = \frac{(R_{EN1}+R_{EN2})}{R_{EN2}} \times (V_{EN\_VOUT\_H} - V_{EN\_VOUT\_HY}) \quad (4)$$

The output regulation is enabled when the V_{CC} voltage exceeds V_{CC_UVEXR} and disabled when the V_{CC} voltage falls below V_{CC_UVEXF}.

It is recommended that R_{EN1} and R_{EN2} be 1% accuracy resistors with good temperature characteristics to ensure a precise detection. This resistor divider must be placed as close as possible to the EN pin on the PCB layout to avoid noise coupling into the UVLO detection.

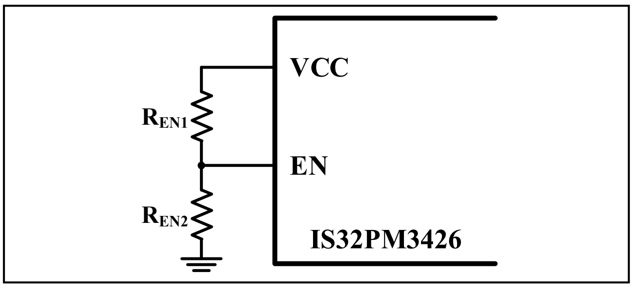


Figure 86 EN Configuration

THERMAL SHUTDOWN

The temperature of the die is monitored to protect the converter from damage when the maximum junction temperature is exceeded. If the die temperature exceeds the thermal shutdown temperature of 175°C (Typ.) the converter will stop switching and enter standby mode. After a thermal shutdown event, the IS32PM3426 will try to restart when its die temperature is less than 155°C (Typ.).

SETTING THE OUTPUT VOLTAGE

The external resistor divider, R_{FBT} and R_{FBB}, is used to set the output voltage (As shown in Figure 87), according to the following equation:

$$V_{OUT} = \frac{(R_{FBB}+R_{FBT})}{R_{FBB}} \times V_{FB\_TH} \quad (5)$$

Where V_{FB_TH}=1V (Typ.).

Choosing a value for the resistor R_{FBB} should be reasonable. Usually, a small R_{FBB} leads to considerable quiescent current loss, while a large R_{FBB} makes the FB pin noise-sensitive and voltage errors from the V_{FB} input current are noticeable.

In order to have an accurate output voltage, precision resistors are preferred (±1% recommended). The R_{FBT} and R_{FBB} resistors should be placed as close as possible to the IS32PM3426 with minimal trace length to the FB and AGND pins.

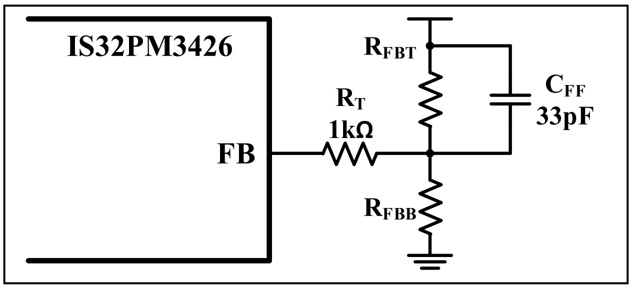


Figure 87 Feedback Network

In addition, it should be noted that the resistor R_T and capacitor C_{FF} are required. The R_T is fixed at 1kΩ, while the C_{FF} is fixed at 33pF.

SELECTING THE INDUCTOR

An inductor is necessary for supplying constant current to the output load while being driven by the switched input voltage. Inductor value involves trade-offs in performance. A larger inductance reduces the output current ripple and output voltage ripple but brings a large physical size, higher Direct Current Resistance (DCR) and lower saturation current. A small inductance has a compact physical size and lower cost but introduces a higher ripple in the output. Use the following Equation (6) to estimate the approximate inductor value:

$$L = \frac{(V_{CC} - V_{OUT}) \times V_{OUT}}{f_{SW} \times \Delta I_L \times V_{CC}} \quad (6)$$

Where ΔI_L is the peak-to-peak inductor current ripple which usually is chosen to be 30%~50% of the maximum output current.

Select an inductor with a rated current greater than the maximum output current. To prevent inductance saturation, the saturation current of the selected inductor (I_{SAT}) must be higher than the maximum inductor peak current (I_{L_PK}) with some safety margin. The peak current can be calculated with Equation (7):

$$I_{L\_PK} = I_{OUT\_MAX} + \frac{1}{2} \times \Delta I_L \quad (7)$$

Where I_{OUT_MAX} is the maximum output current.

Meanwhile, the I_{L_PK} should not exceed the minimum value of the HS-FET current limit (I_{HSLIM}). Otherwise the converter may not be able to delivery desired output current. If needed, increase the inductor value to reduce the inductor current ripple (ΔI_L) and ensure that I_{L_PK} does not exceed the HS-FET current limit level. A shielded type of inductor with low DCR is recommended in most applications, which gives better EMI and efficient performance.

SELECTING THE INPUT CAPACITOR

The input current is discontinuous for a step-down converter, which requires a capacitor to supply the AC input current to maintaining the DC input voltage. The X7R type ceramic capacitors are recommended for best performance, and make sure that the capacitors are placed as close to VCC pin as possible.

It requires the capacitor ripple current rating should be higher than the converter maximum input ripple current, which can be calculated with Equation (8):

$$I_{CVCC} = I_{OUT\_MAX} \times \sqrt{\frac{V_{OUT}}{V_{CC}} \times \left(1 - \frac{V_{OUT}}{V_{CC}}\right)} \quad (8)$$

The worse-case condition occurs at V_{CC}= $2V_{OUT}$,

As shown in Equation (9):

$$I_{CVCC} = \frac{I_{OUT\_MAX}}{2} \quad (9)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current. The capacitance value determines the input voltage ripple of the converter. When select the desired input voltage ripple ΔV_{CC}, the minimum input capacitor C_{VCC} can be calculated with Equation (10):

$$C_{VCC} = \frac{I_{OUT\_MAX}}{f_{SW} \times \Delta V_{CC}} \times \frac{V_{OUT}}{V_{CC}} \times \left(1 - \frac{V_{OUT}}{V_{CC}}\right) \quad (10)$$

The worse-case condition occurs at V_{CC}= $2V_{OUT}$.

As shown in Equation (11):

$$C_{VCC} = \frac{1}{4} \times \frac{I_{OUT\_MAX}}{f_{SW} \times \Delta V_{CC}} \quad (11)$$

SELECTING THE OUTPUT CAPACITOR

An output capacitor is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors can be used. But for best performance, use low ESR capacitors to keep output ripple low.

If the desired output voltage ripple ΔV_{OUT} is determined, the minimum C_{OUT} can be calculated with Equation (12):

$$C_{OUT} = \frac{\Delta I_L}{8 \times f_{SW}(\Delta V_{OUT} - \Delta I_L \times ESR)} \quad (12)$$

However, in the case of ceramic applications, the output voltage ripple is caused mainly by the capacitance due to the low ESR of ceramic. For simplification, the minimum C_{OUT} can be estimated with Equation (13):

$$C_{OUT} = \frac{\Delta I_L}{8 \times f_{SW} \times \Delta V_{OUT}} \quad (13)$$

Note that the effective capacitance of ceramic capacitors decreases with DC bias. For larger bulk values of capacitance and lower cost, low ESR type electrolytic capacitors are usually used to be connected in parallel with the ceramic capacitors. However, electrolytic capacitors have poor tolerance, especially over temperature, and the selected value should be larger than the calculated value to allow for temperature variation.

Table 1 Recommended Component Values (V_{CC}= 12V)

Switching Frequency(kHz)	Output Voltage (V)	R_{FBT} (kΩ)	R_{FBB} (kΩ)	L_1 (µH)	C_{FF} (pF)	C_{OUT} (µF)
400	3.3	100	43.5	8.2	33	40 to 66
	5	100	25	10	33	40 to 66
	8	100	14.3	8.2	33	40 to 66
2100	3.3	100	43.5	1.8	33	40 to 66
	5	100	25	2.2	33	40 to 66
	8	100	14.3	1.8	33	40 to 66

Application Example

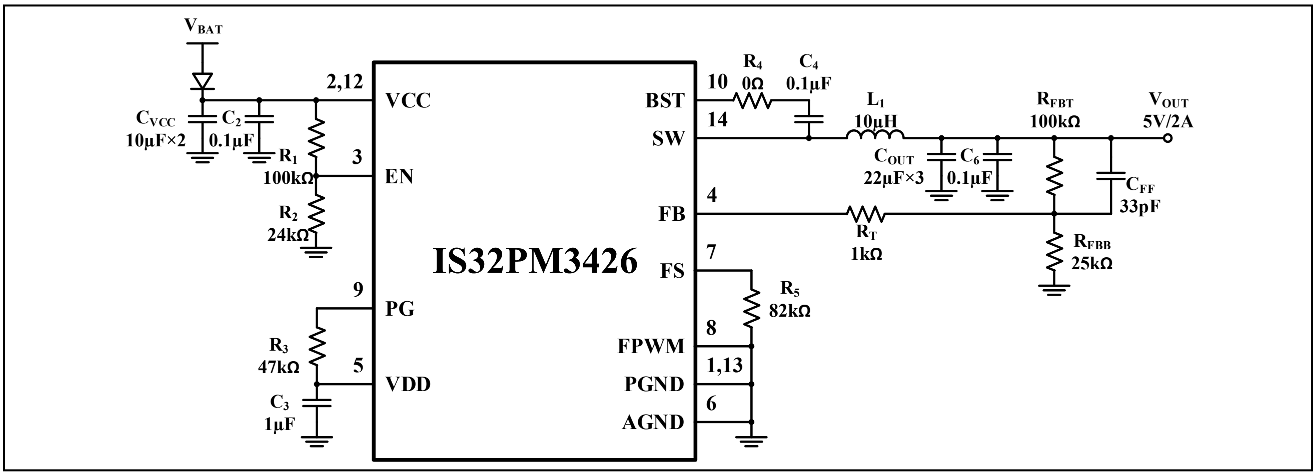


Figure 88 f_{SW}= 400kHz 5V/2A Output Application Example

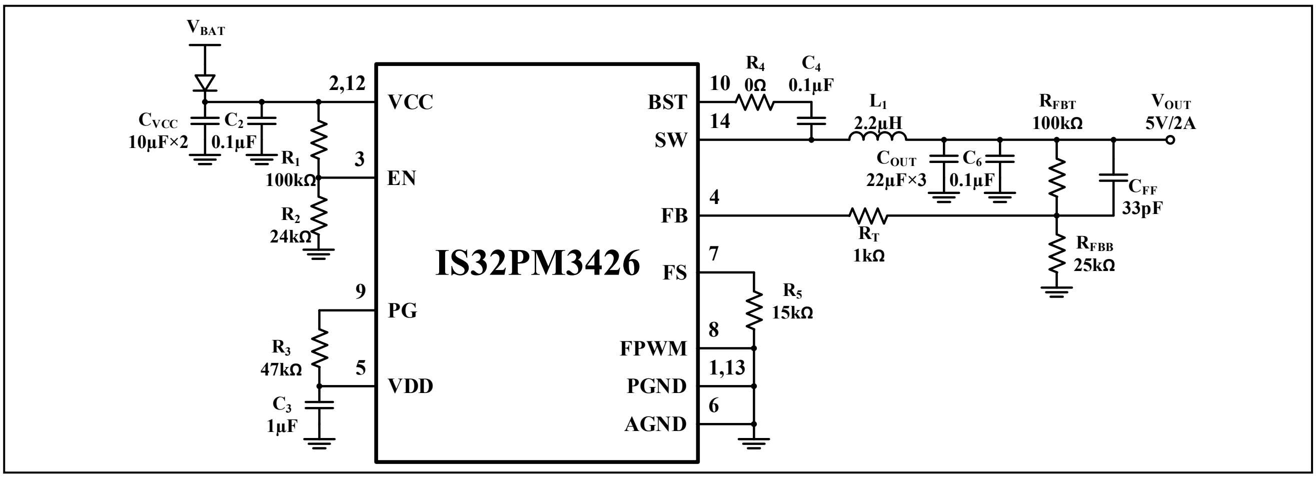


Figure 89 f_{SW}= 2.1MHz 5V/2A Output Application Example

LAYOUT CONSIDERATION

Layout is an important design step for all switching power supplies, especially those providing high current and using high switching frequencies. If layout is not carefully done, the operation could show instability as well as EMI problems.

The high dV/dt surface and dI/dt loops are big noise emission source. To optimize the EMI performance, keep the area size of all high switching frequency points with high voltage compact. Meantime keep all traces carrying high current as short as possible to minimize the loops.

(1) Wide traces should be used for connection of the high current paths that helps to achieve better efficiency and EMI performance. Such as the traces of power supply, inductor L_1, output load and ground.

(2) Keep the traces of the switching points shorter. The inductor L_1 should be placed as close to the SW pin as possible and the traces of connection between them should be as short and wide as possible.

(3) To avoid ground jitter, the components of parameter setting should be placed close to the corresponding pins and return to the AGND and keep the traces length to the pins as short as possible. On the other side, to prevent noise coupling, the output voltage setting resistor divider must be placed as close to FB and AGND as possible. the traces of FB should either be far away or be isolated from high-current paths and high-speed switching nodes. These practices are essential for better accuracy and stability.

(4) The capacitors C_{VCC} and C_{VDD} must be placed as close as possible to VCC and VDD pins for good filtering.

(5) Place the bootstrap capacitor C_{BST} close to the BST pin and SW pin to ensure the traces are as short as possible.

(6) The connection to the output load should be kept short to minimize radiated emission.

(7) The VCC and PGND pins must be soldered to copper ground plane of enough size with sufficient vias to conduct the heat to opposite side of the PCB for adequate cooling. Flood all unused areas on all layers with copper that reduces the temperature rise of the power components. Connect the copper areas to the ground.

THERMAL CONSIDERATION

The package thermal resistance, θ_{JA}, determines the amount of heat that can pass from the silicon die to the surrounding ambient environment. The θ_{JA} is a measure of the temperature rise created by power dissipation and is usually measured in degree Celsius per watt (°C/W).

When operating the chip at high ambient temperatures, or when driving maximum load current, care must be taken to avoid exceeding the package power dissipation limits. The maximum power dissipation can be calculated using the following Equation (14):

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}} \qquad (14)$$

Where $T_{J(MAX)}$ is the recommended maximum operating junction temperature.

So,

$$P_{D(MAX)} = \frac{150°C - 25°C}{53.7°C/W} \approx 2.33W$$

Figure 90, shows the power derating of the IS32PM3426 on a JEDEC boards (in accordance with JESD 51-5 and JESD 51-7) standing in still air.

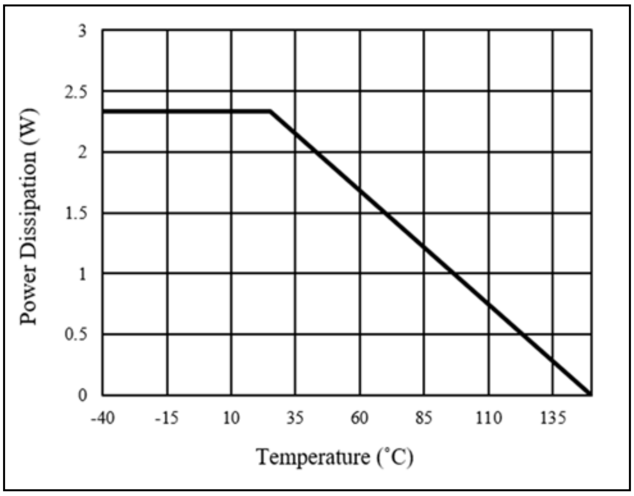


Figure 90 Dissipation Curve

The thermal resistance is achieved by mounting the IS32PM3426 on a standard FR4 double-sided printed circuit board (PCB) with a copper area of a few square inches on each side of the board under the IS32PM3426. The thermal resistance can be reduced by using a four-layer PCB board. A four-layer layout is strongly recommended to achieve better thermal and EMI performance.

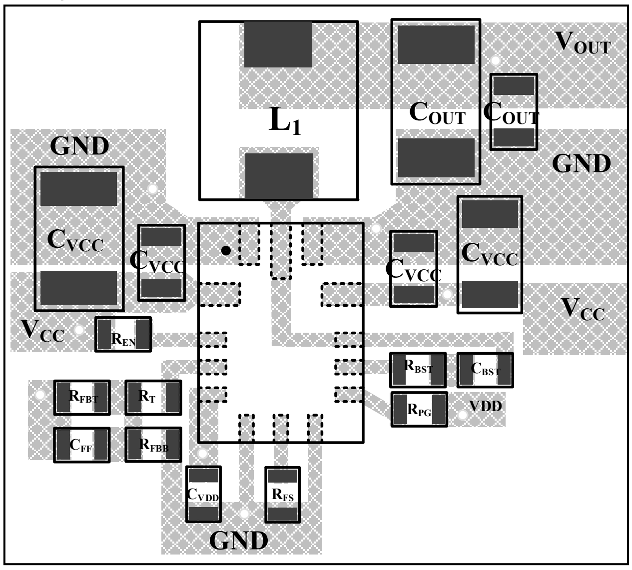


Figure 91 PCB Layout Example (Top Layer)

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

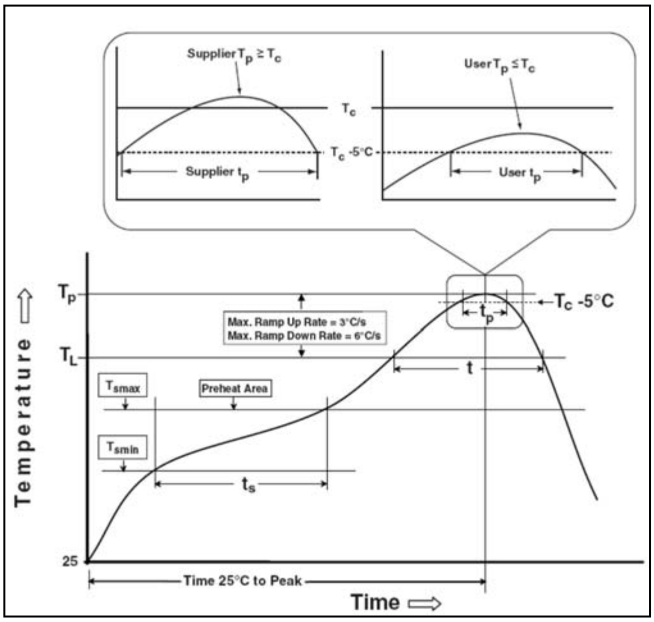
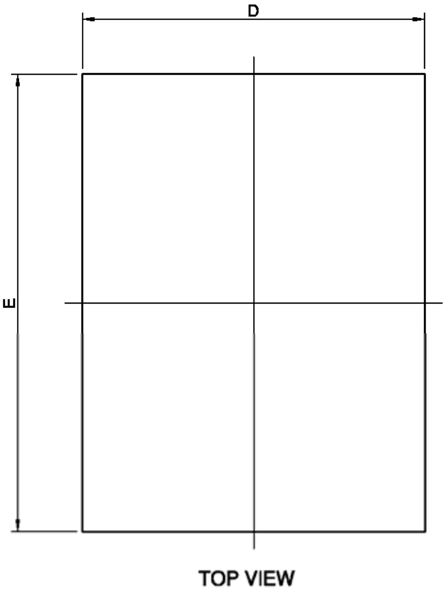
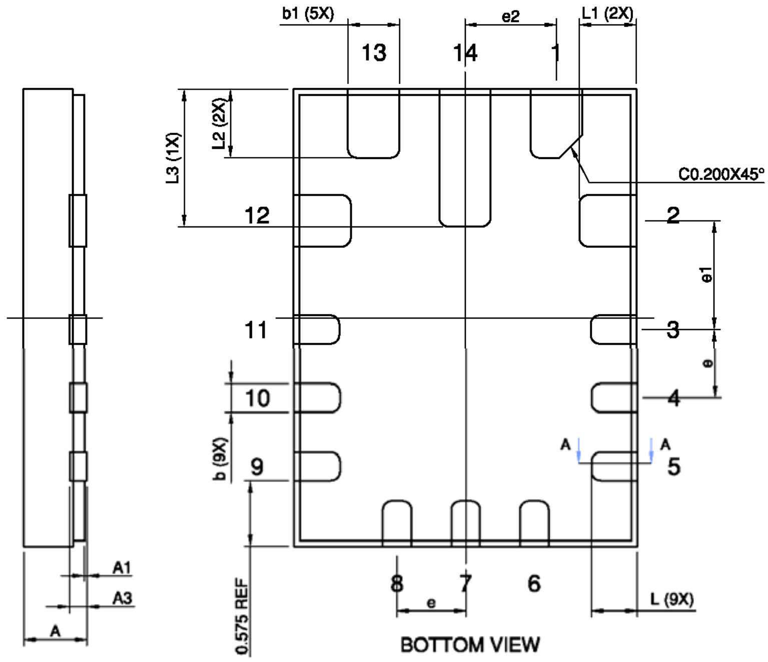


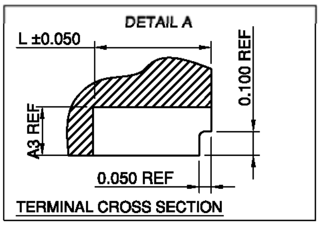
Figure 92 Classification Profile

PACKAGE INFORMATION

WFCQFN-14





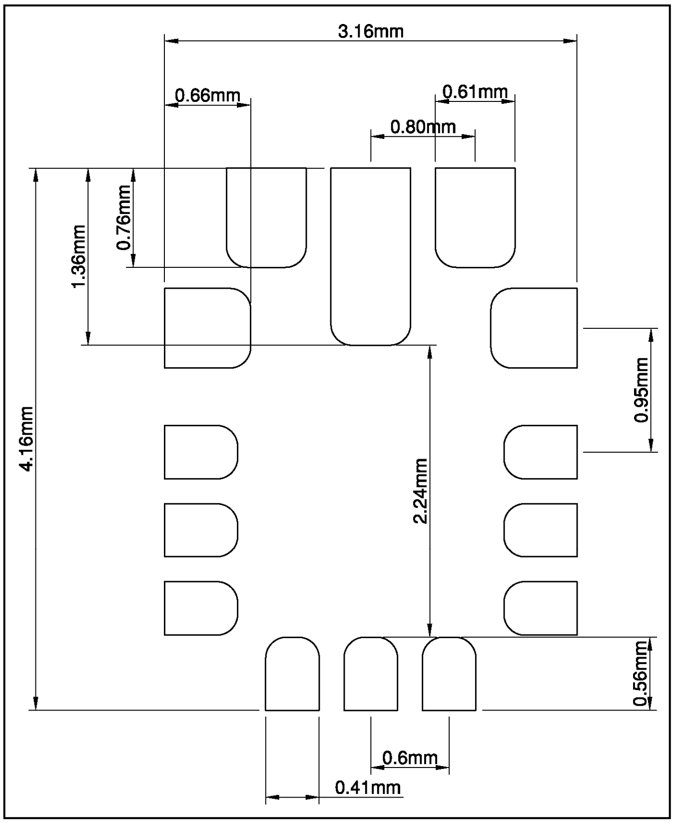


SYMBOLS	MIN.	NOM.	MAX.
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
A3	0.150 REF.		
b	0.20	0.25	0.30
b1	0.40	0.45	0.50
D	2.90	3.00	3.10
E	3.90	4.00	4.10
e	0.60 BSC		
e1	0.95 BSC		
e2	0.80 BSC		
L	0.35	0.40	0.45
L1	0.45	0.50	0.55
L2	0.55	0.60	0.65
L3	1.15	1.20	1.25

233-570-389 Rev. B

RECOMMENDED LAND PATTERN

WFCQFN-14



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (e.g. user's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
0A	Initial release	2024.05.06
A	Update to final version	2024.07.17
B	Correct AECQ description	2024.08.19