

# IS32PM3420B

## 3.8V TO 36V, 3A, 400KHZ, SYNCHRONOUS STEP-DOWN VOLTAGE REGULATOR

August 2024

### GENERAL DESCRIPTION

The IS32PM3420B regulator is a fully integrated and high frequency synchronous step-down DC-DC converter that can drive a load current of up to 3A. It can operate within an input voltage range of 3.8V to 36V. The IS32PM3420B provides exceptional efficiency, output accuracy and drop-out voltage in a very small solution size. Constant on-time control mode is employed to achieve simple control-loop compensation and fast transient response. The IS32PM3420B supports both Forced Continuous Conduction Mode (FCCM) and Pulse Frequency Modulation mode (PFM) at light-load condition, which is selected by the FPWM pin. It requires few external components. Pin arrangement allows simple, optimum PCB layout. Protection features include thermal shutdown, VDD under-voltage lockout, cycle-by-cycle current limit, over-voltage and output short-circuit protection.

The IS32PM3420B device is available in the SOP-8-EP package with an exposed pad for enhanced thermal dissipation.

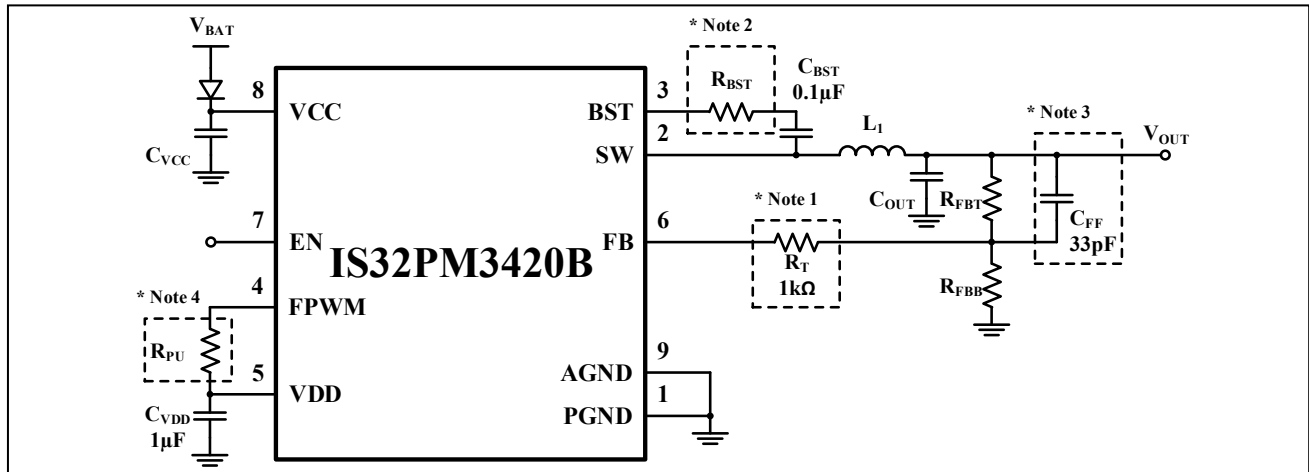
### APPLICATIONS

- General-purpose power supply
- Automotive LED lighting system
- Automotive body electronics

### FEATURES

- Input voltage range from 3.8V to 36V
- 1 $\mu$ A (Typ.) shutdown current
- 25 $\mu$ A quiescent current (typical, no switching)
- Up to 3A output current capability
- Adjustable output voltage, 1V to 24V
- Output regulation accuracy:
  - $\pm 1\%$  at 25°C
  - $\pm 2\%$  over -40°C ~150°C
- 91% efficiency at full load (5V/3A)
- >90% efficiency at light load (5V/100mA)
- Integrated synchronous rectifier
- Fixed operating frequency: 400kHz
- Pin-selectable FCCM or PFM operation mode
- Spread spectrum to minimize EMI
- Few external components
  - Internal loop compensation
  - Internal soft-start
- Fault protections
  - Cycle by cycle current limit
  - Precision enable to program system UVLO
  - Output short-circuit protection with hiccup mode
  - Output over-voltage protection
  - VDD under-voltage lockout
  - Thermal shutdown protection
- Operating junction temperature range from -40°C ~ +150°C
- SOP-8-EP compact package
- RoHS & Halogen-Free Compliance
- TSCA Compliance
- AEC-Q100 Qualified with Temperature Grade 1: -40°C to 125°C

## TYPICAL APPLICATION CIRCUIT



**Figure 1** Typical Application Circuit

**Note 1:** The resistor ( $R_T$ ) must be connected to FB pin with fixed value  $1k\Omega$ .

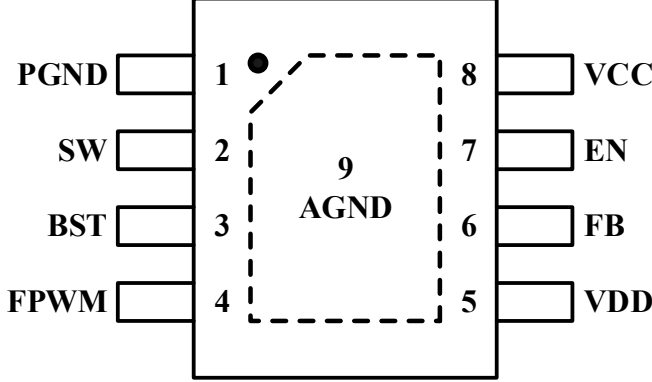
**Note 2:** If add the resistor ( $R_{BST}$ ), the value must not exceed  $20\Omega$ .

**Note 3:** The capacitor ( $C_{FF}$ ) must be connected in parallel to the resistor ( $R_{FBT}$ ) with fixed value  $33pF$ .

**Note 4:** The resistor ( $R_{PU}$ ) should be fixed with  $10k\Omega$ .

# IS32PM3420B

## PIN CONFIGURATION

Package	Pin Configuration (Top View)
SOP-8-EP	

## PIN DESCRIPTION

No.	Pin	Description
1	PGND	Power ground for the ground connection of internal synchronous rectifier FET.
2	SW	Regulator switch node. Connect it to the power inductor.
3	BST	Bootstrap supply voltage for internal high-side MOSFET gate driver. Connect a 0.1μF X7R ceramic capacitor from this pin to the SW pin.
4	FPWM	Regulator operation mode selection pin. Pull up to the VDD through a fixed resistor of 10kΩ for FCCM mode and connect to the AGND for PFM mode. Do not float.
5	VDD	Internal 5V LDO output. Used as supply to internal control circuits. Do not connect to any external loads. It can be used as a logic supply for control inputs. Connect a high quality 1μF X7R ceramic capacitor from this pin to GND.
6	FB	Feedback input to regulator. Connect to the tap point of the feedback voltage divider through a 1kΩ resistor. Do not either float or ground.
7	EN	Enable input to the regulator. Pulled high to enable and pull low to disable. Connecting a resistor divider from VCC can program external system UVLO. Do not float.
8	VCC	Power supply input. Connect a bypass capacitor $C_{VCC}$ from this pin to the ground. The path from $C_{VCC}$ to PGND and VCC pins should be as short as possible.
9	Thermal Pad (AGND)	Analog ground for internal references and control circuits. It also is a major heat dissipation path for the die. Must be soldered to a large size GND copper plane using multiple vias for good thermal performance.

# IS32PM3420B



## ORDERING INFORMATION

Automotive Range: -40°C to +125°C

Order Part No.	Package	QTY/Reel
IS32PM3420B-GRLA3-TR	SOP-8-EP, Lead-free	2500

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**ABSOLUTE MAXIMUM RATINGS**

Input voltages of VCC and EN to AGND, PGND	-0.3V ~ +42V
Input voltage of FB, to AGND, PGND	-0.3V ~ +6V
Voltage of AGND to PGND	-0.3V ~ +0.3V
Output voltage of VDD to AGND, PGND	-0.3V ~ +6V
Voltage of FPWM to AGND, PGND	-0.3V ~ V <sub>DD</sub>
Voltage of SW to AGND, PGND	-0.3V ~ V <sub>CC</sub> +0.3V
Voltage of BST to SW	-0.3V ~ +6V
Storage temperature range, T <sub>STG</sub>	-65°C ~ +150°C
Operating temperature range, T <sub>A</sub> = T <sub>J</sub>	-40°C ~ +150°C
Power dissipation, P <sub>D(MAX)</sub>	2.85W
Package thermal resistance, junction to ambient (4-layer standard test PCB based on JESD 51-2A), $\theta_{JA}$	43.9°C/W
Package thermal resistance, junction to thermal PAD (4-layer standard test PCB based on JESD 51-8), $\theta_{JP}$	1.41°C/W
ESD (HBM)	±2.5kV
ESD (CDM)	±750V

**Note 5:** Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**RECOMMENDED OPERATING CONDITIONS**

Over operating free-air temperature range (unless otherwise noted). (Note 6)

Parameter		Min.	Typ.	Max.	Unit
Input voltages	VCC to PGND	3.8		36	V
	EN	0		V <sub>CC</sub>	
	FB	0		1.5	
	FPWM	0		V <sub>DD</sub>	
Output voltage, V <sub>OUT</sub>		1		24	V
Output current, I <sub>OUT</sub>		0		3	A
Operating junction temperature range, T <sub>J</sub>		-40		150	°C

**Note 6:** Recommended Operating Conditions indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For verified specifications, see Electrical Characteristics.

**ELECTRICAL CHARACTERISTICS**

Limits apply over the recommended operating junction temperature ( $T_J$ ) range of  $-40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ , unless otherwise stated. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at  $T_J = 25^{\circ}\text{C}$ , and are provided for reference purposes only. Unless otherwise stated, the following conditions apply:  $V_{CC} = 12\text{V}$ .

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
<b>Power Supply</b>						
$V_{CC\_UV}$	VCC under-voltage lockout threshold	$V_{CC}$ rising		3.5	3.75	V
$V_{CC\_UVHY}$	VCC under-voltage lockout hysteresis	$V_{CC}$ falling		200		mV
$I_{SD}$	Shutdown current	$V_{EN} = 0\text{V}$		1	5	$\mu\text{A}$
$I_{CC}$	Operating quiescent current (non-switching)	$V_{EN} = 5\text{V}$ , $V_{FB} = 1.05\text{V}$ $T_J = 25^{\circ}\text{C}$		25	35	$\mu\text{A}$
<b>Enable</b>						
$V_{EN\_VDD\_H}$	Input voltage level to enable the internal LDO output, $V_{DD}$	$V_{EN}$ rising	1.05			V
$V_{EN\_VDD\_L}$	Input voltage level to disable the internal LDO output, $V_{DD}$	$V_{EN}$ falling			0.4	V
$V_{EN\_VOUT\_H}$	Precision enable level for switching and regulator output, $V_{OUT}$	$V_{EN}$ rising	1.16	1.2	1.24	V
$V_{EN\_VOUT\_HY}$	Precision enable level hysteresis	$V_{EN}$ falling		100		mV
$I_{EN\_LKG}$	EN pin input leakage current	$V_{EN} = 5\text{V}$		0.2	50	nA
<b>Soft-Start</b>						
$t_{SS}$	Internal soft-start time	$V_{OUT}$ from 10% to 90%	1.5	2	2.5	ms
<b>Forced PWM</b>						
$V_{FPWM\_IH}$	FPWM input high threshold		1.5			V
$V_{FPWM\_IL}$	FPWM input low threshold	(Note 7)			0.4	V
<b>Internal LDO</b>						
$V_{DD}$	Internal LDO output voltage	$5.5\text{V} \leq V_{CC} \leq 36\text{V}$ , $I_{DD} = 10\text{mA}$	4.75	5	5.25	V
$I_{DD\_LIM}$	Internal LDO output current limit		20	45		mA
$V_{DD\_UV}$	VDD under-voltage lockout thresholds	$V_{DD}$ rising	3	3.25	3.5	V
$V_{DD\_UVHY}$	VDD under-voltage lockout hysteresis	$V_{DD}$ falling		200		mV
<b>Voltage Reference</b>						
$V_{FB\_TH}$	Feedback voltage	$T_J = 25^{\circ}\text{C}$	0.990	1.000	1.010	V
		$T_J = -40^{\circ}\text{C}$ to $150^{\circ}\text{C}$	0.98	1.000	1.02	
$I_{FB\_LKG}$	FB pin input leakage current	$V_{FB} = 1\text{V}$		20	100	nA

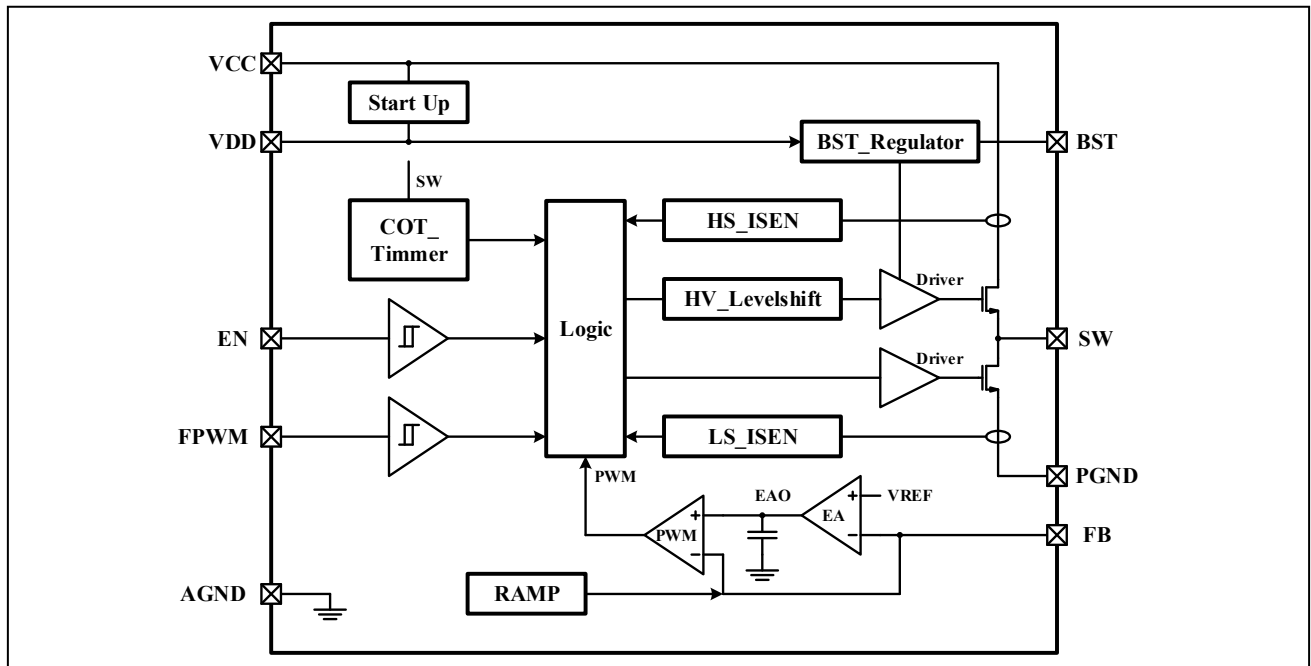
**ELECTRICAL CHARACTERISTICS (CONTINUE)**

Limits apply over the recommended operating junction temperature ( $T_J$ ) range of  $-40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ , unless otherwise stated. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at  $T_J = 25^{\circ}\text{C}$ , and are provided for reference purposes only. Unless otherwise stated, the following conditions apply:  $V_{CC} = 12\text{V}$ .

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
<b>MOSFETS</b>						
$R_{DS(on)_{HS}}$	High-side MOSFET ON-resistance	$I_{SW} = -1\text{A}$		130		m $\Omega$
$R_{DS(on)_{LS}}$	Low-side MOSFET ON-resistance	$I_{SW} = 1\text{A}$		80		m $\Omega$
$t_{ON\_MIN}$	Minimum switch ON-time			100		ns
$t_{OFF\_MIN}$	Minimum switch OFF-time			90		ns
$I_{SW\_LKG}$	SW pin leakage current	$V_{EN} = 0\text{V}$ , $V_{SW} = 36\text{V}$ , $T_J = -40^{\circ}\text{C}$ to $125^{\circ}\text{C}$			5	$\mu\text{A}$
<b>Current Limit</b>						
$I_{HSLIM}$	High-side MOSFET current limit		4	5	6	A
$I_{LSLIM}$	Low-side MOSFET current limit		3	3.5	5.5	A
$I_{L\_ZC}$	Zero cross detection threshold			-0.1		A
$I_{PK\_MIN}$	Minimum inductor peak current			1		A
$I_{LSRS}$	Negative current limit			-3		A
$t_{HC}$	Over current hiccup time		16.5	22	27.5	ms
<b>Oscillator</b>						
$f_{SW}$	Oscillator frequency		360	400	460	kHz
$f_{SS\_P}$	Spread spectrum pattern frequency	(Note 7)		800		Hz
$f_{SS\_S}$	Frequency span of spread spectrum	(Note 7)		$\pm 5$		%
<b>Thermal Shutdown</b>						
$T_{SD}$	Thermal shutdown	(Note 7)		175		$^{\circ}\text{C}$
$T_{SDHY}$	Thermal shutdown hysteresis	(Note 7)		155		$^{\circ}\text{C}$

**Note 7:** Guaranteed by design.

## FUNCTIONAL BLOCK DIAGRAM



## TYPICAL PERFORMANCE CHARACTERISTICS

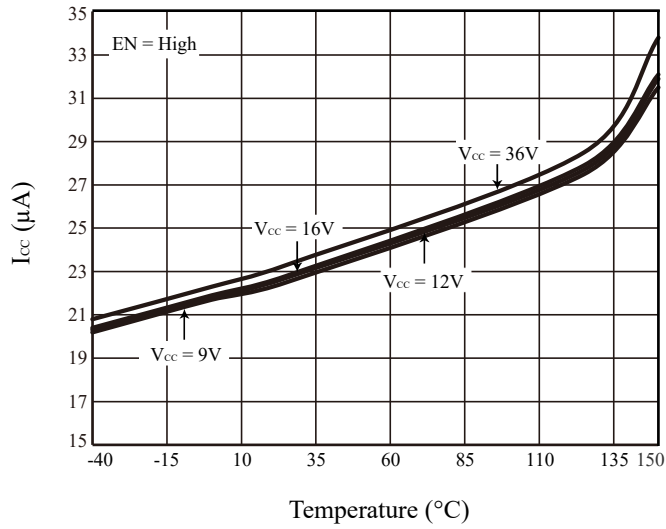


Figure 2  $I_{CC}$  vs. Temperature

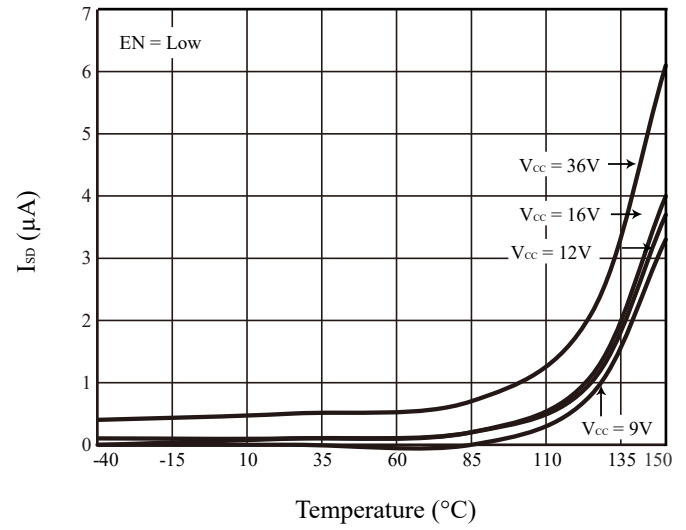


Figure 3  $I_{SD}$  vs. Temperature

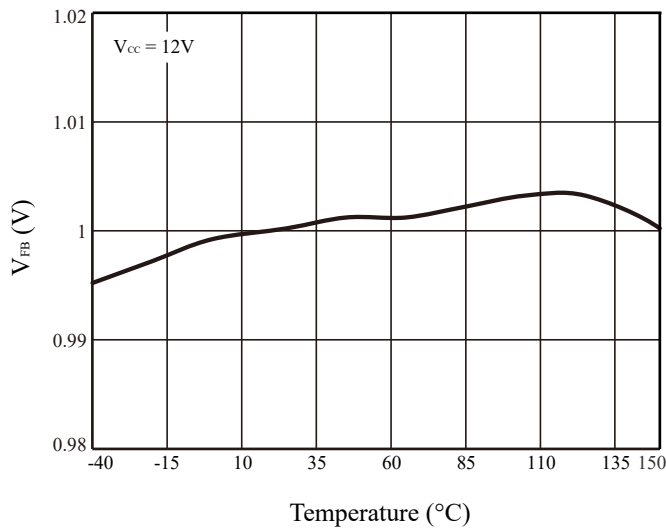


Figure 4  $V_{FB}$  vs. Temperature

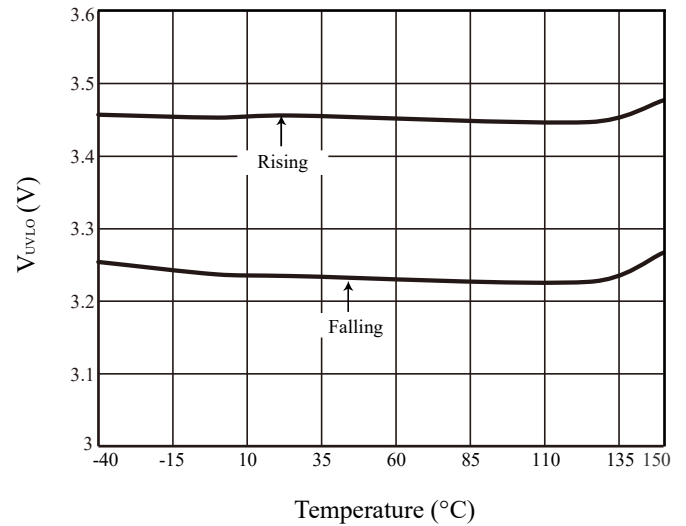


Figure 5  $V_{UVLO}$  vs. Temperature

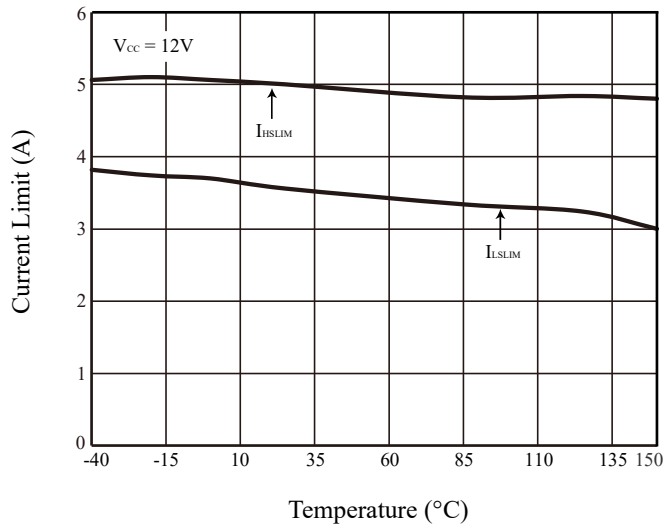


Figure 6 Current Limit vs. Temperature

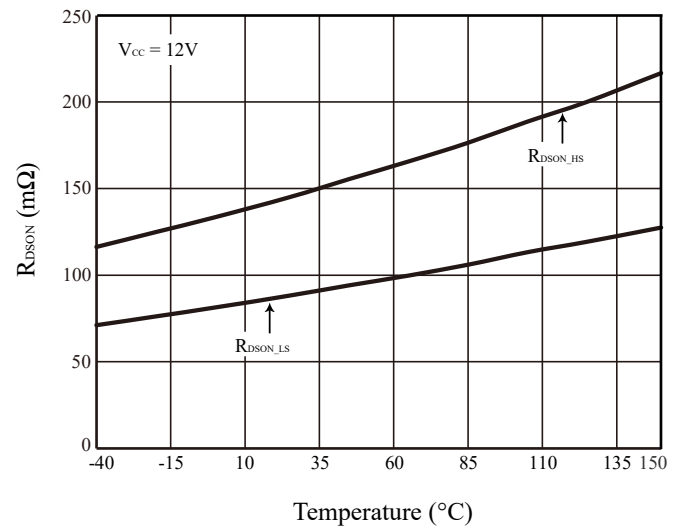
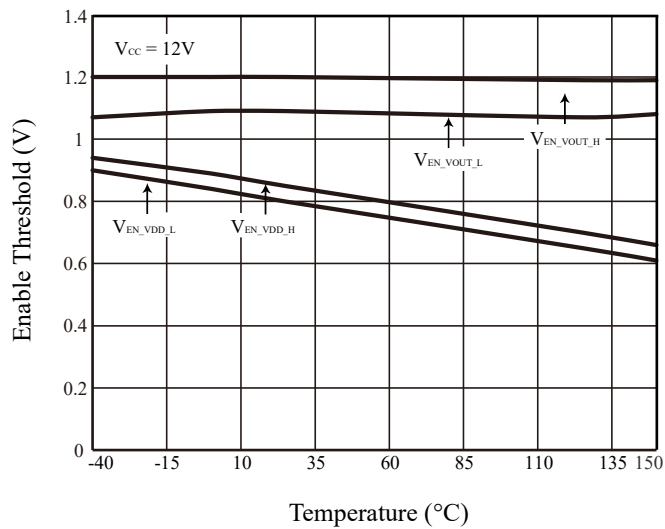
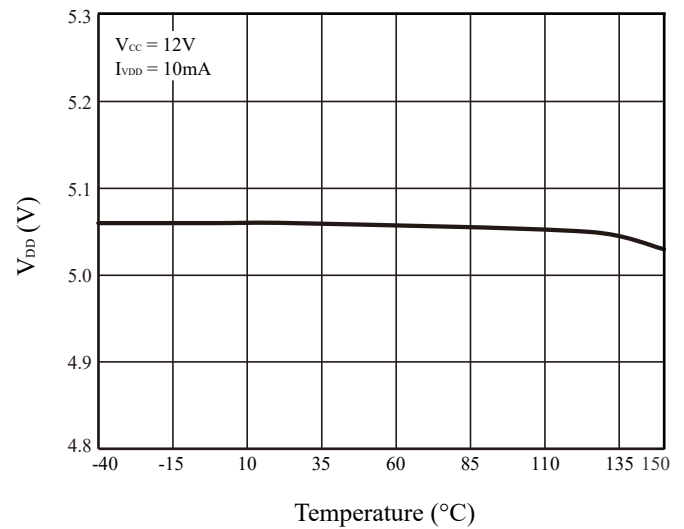


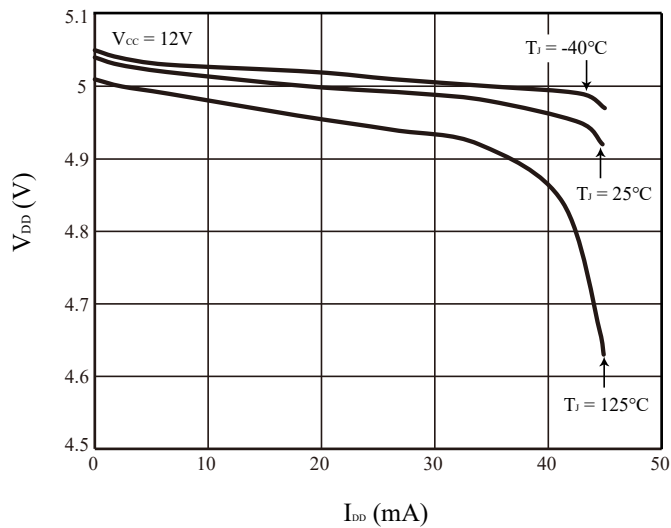
Figure 7  $R_{DS(on)}$  vs. Temperature



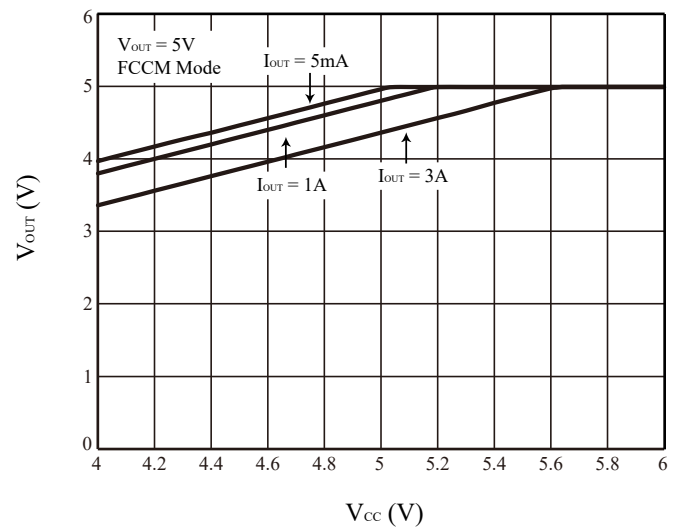
**Figure 8** Enable Threshold vs. Temperature



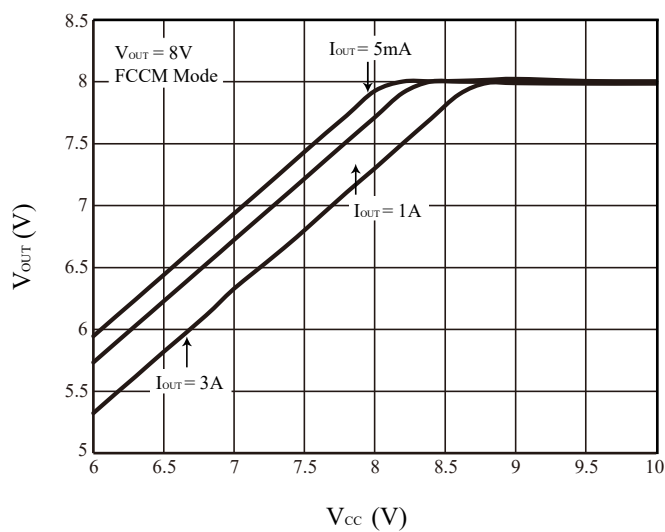
**Figure 9**  $V_{DD}$  vs. Temperature



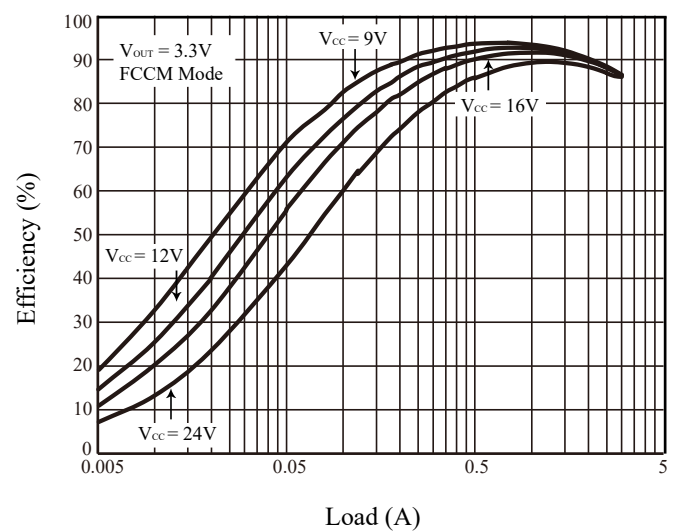
**Figure 10**  $V_{DD}$  vs.  $I_{DD}$



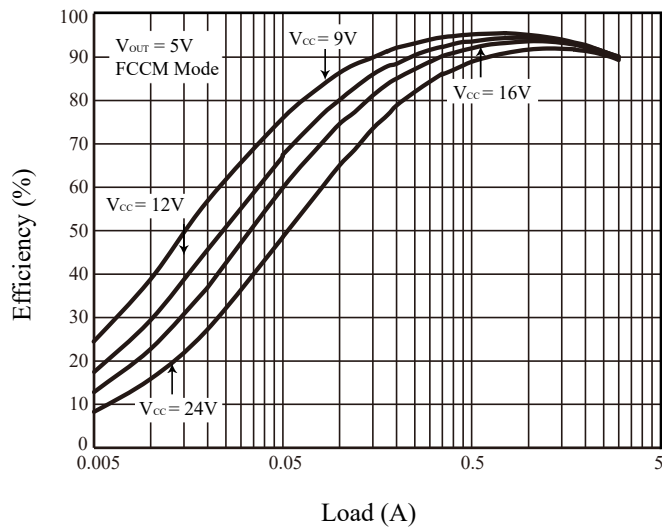
**Figure 11**  $V_{OUT}$  vs.  $V_{CC}$



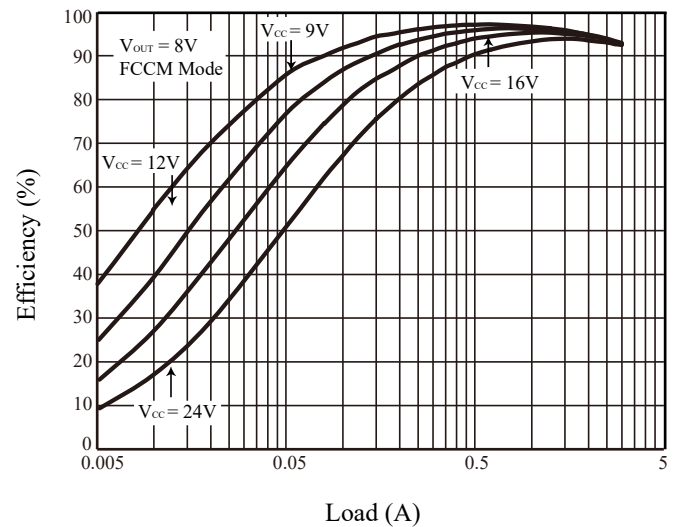
**Figure 12**  $V_{OUT}$  vs.  $V_{CC}$



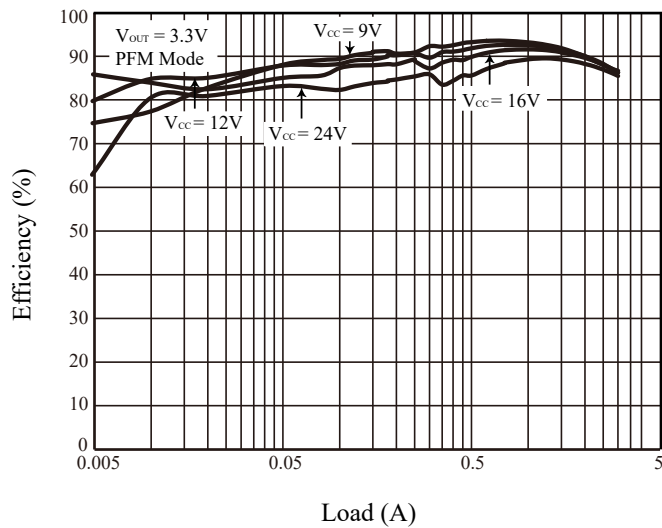
**Figure 13** Efficiency vs. Load



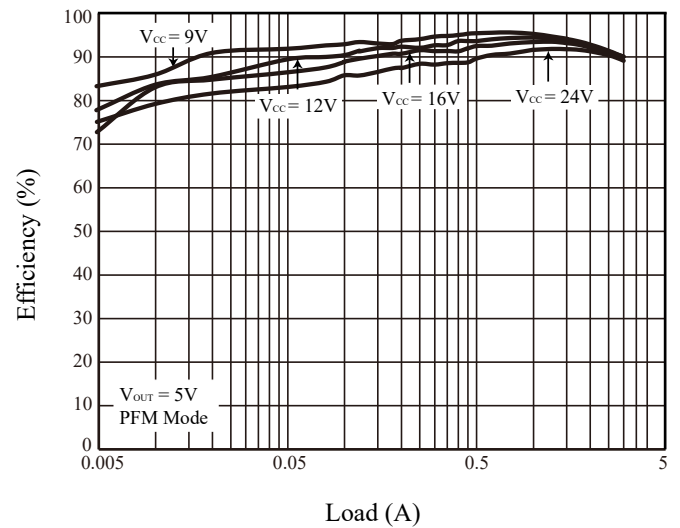
**Figure 14** Efficiency vs. Load



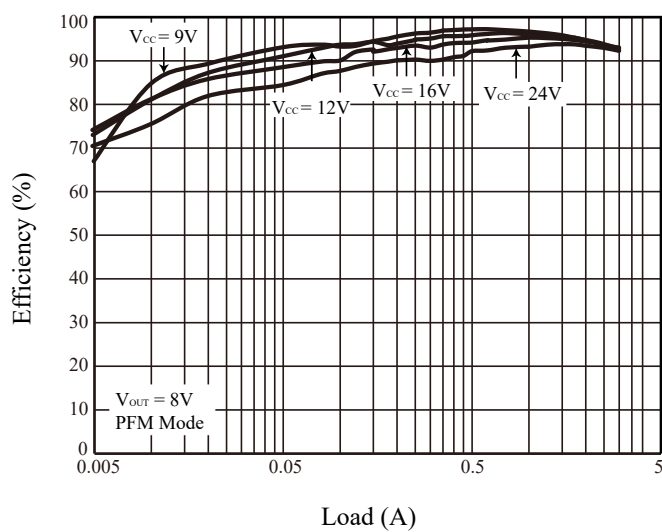
**Figure 15** Efficiency vs. Load



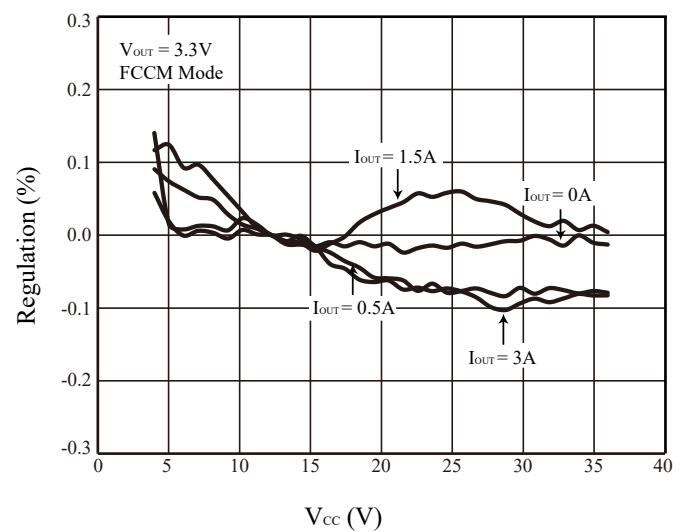
**Figure 16** Efficiency vs. Load



**Figure 17** Efficiency vs. Load



**Figure 18** Efficiency vs. Load



**Figure 19** Line Regulation

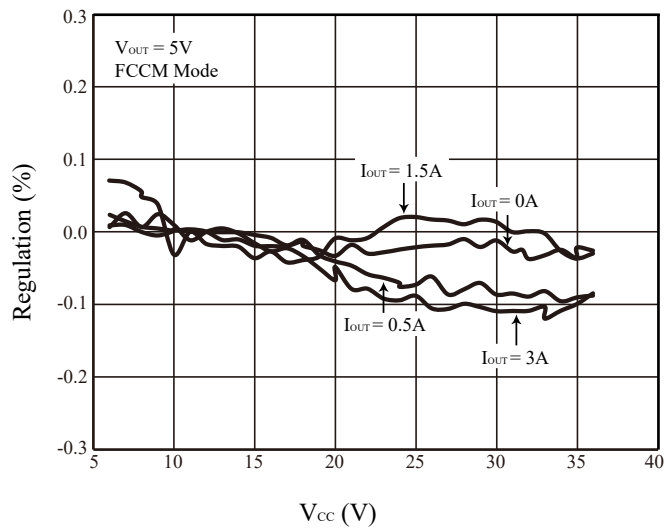


Figure 20 Line Regulation

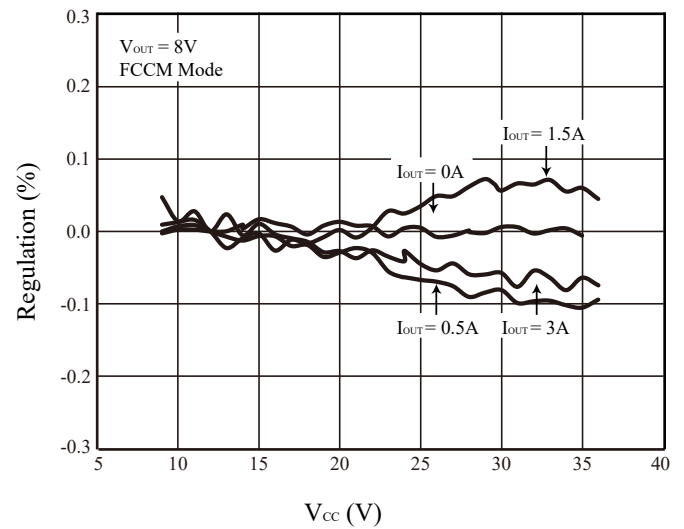


Figure 21 Line Regulation

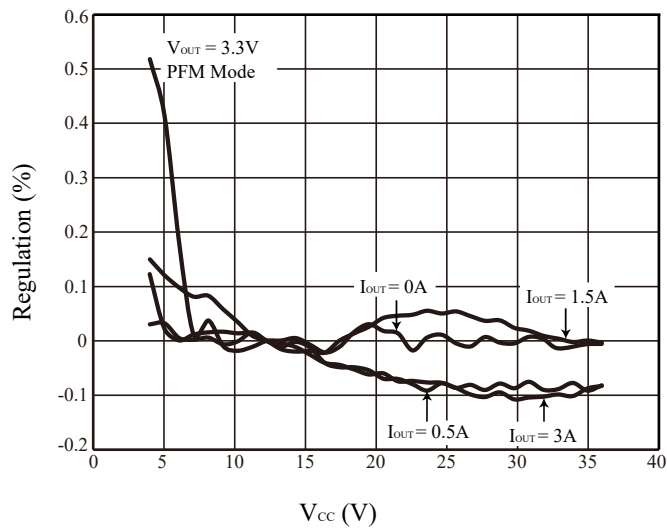


Figure 22 Line Regulation

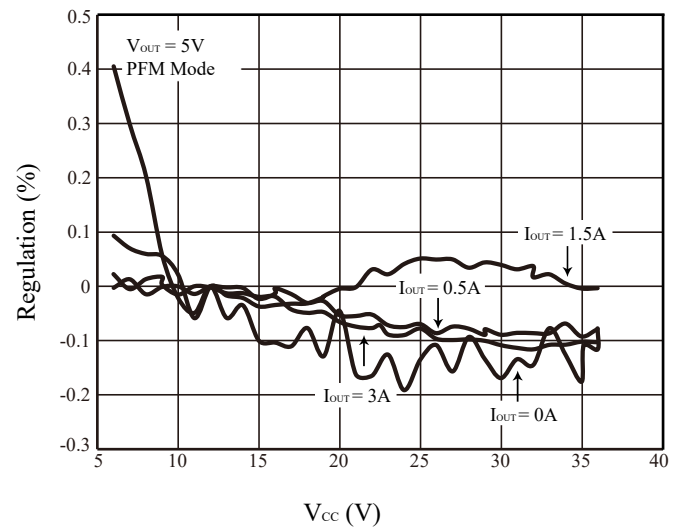


Figure 23 Line Regulation

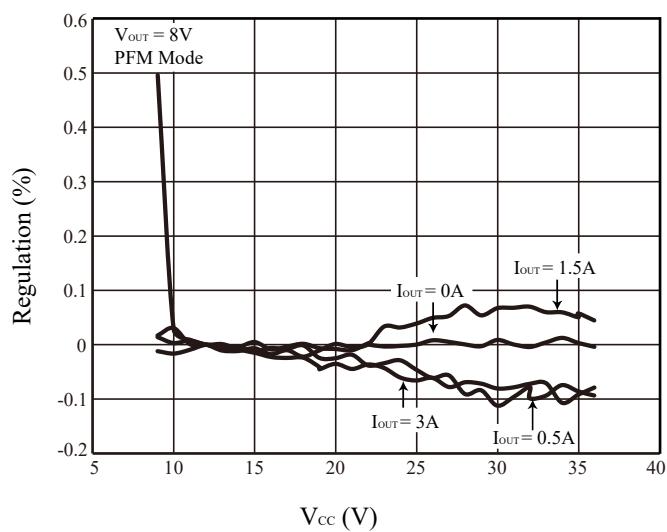


Figure 24 Line Regulation

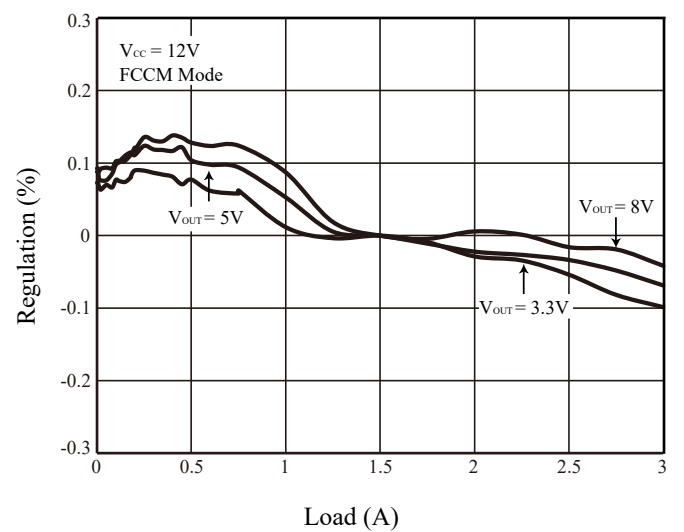


Figure 25 Load Regulation

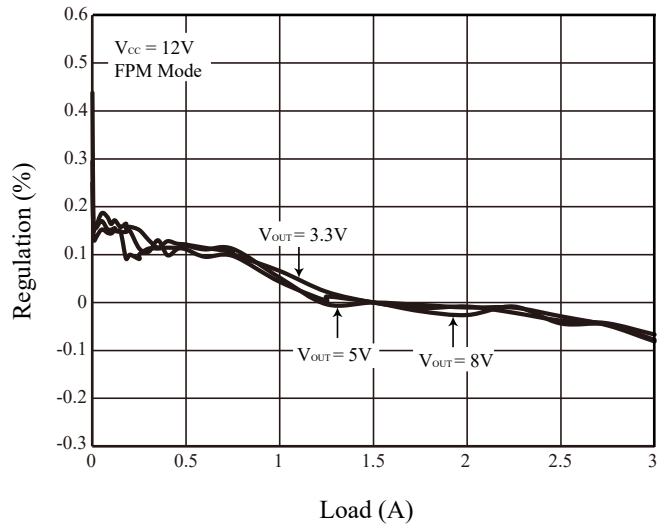


Figure 26 Load Regulation

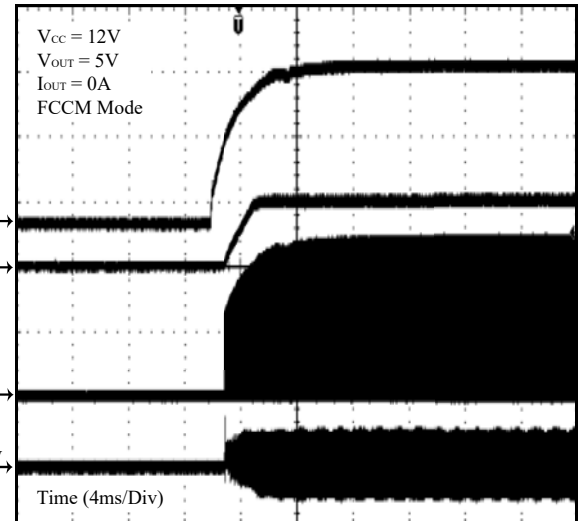


Figure 27 Start Up with VCC

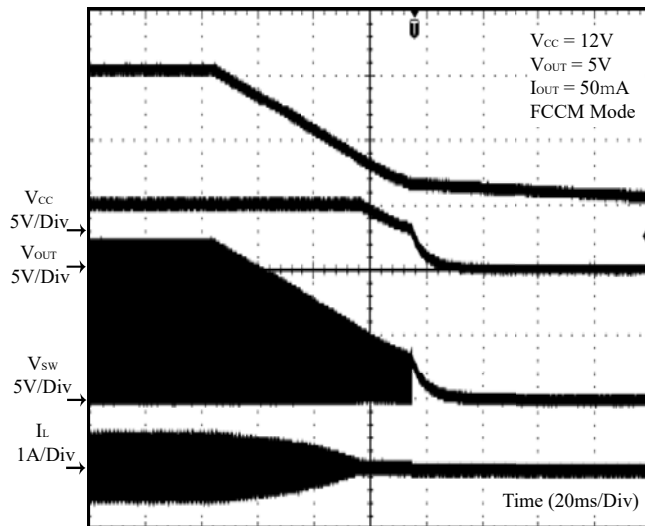


Figure 28 Shut Down with VCC

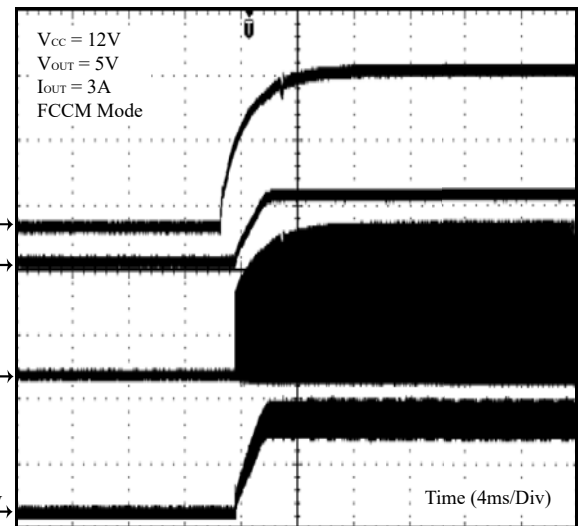


Figure 29 Start Up with VCC

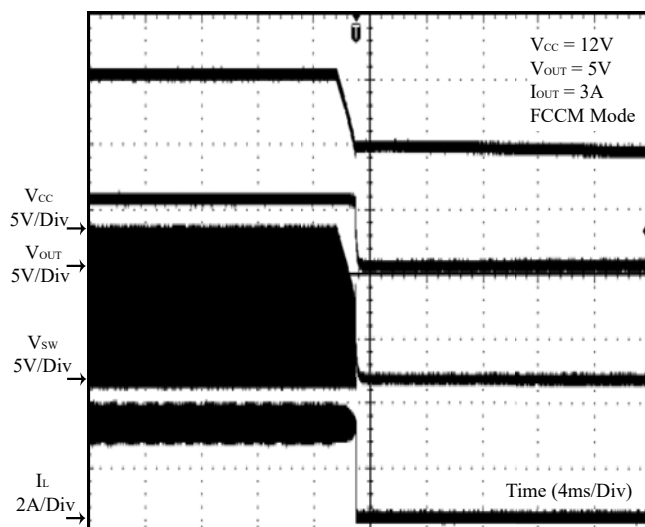


Figure 30 Shut Down with VCC

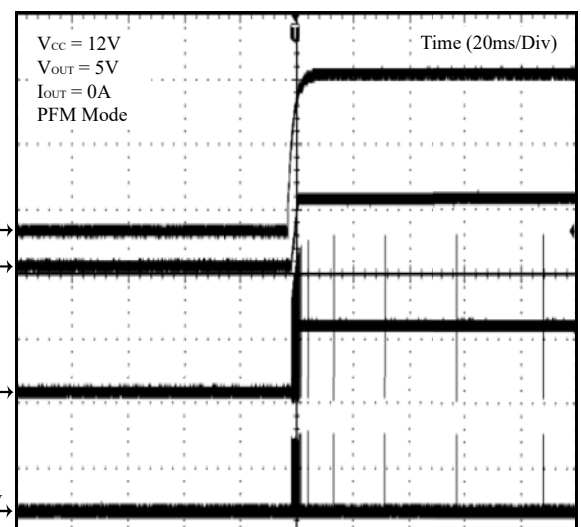
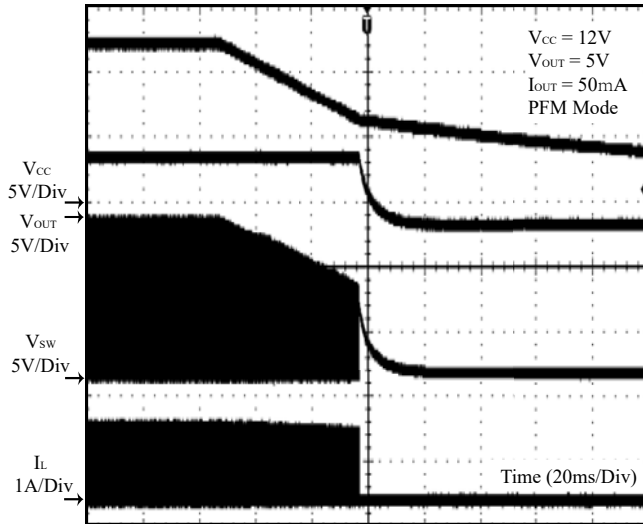
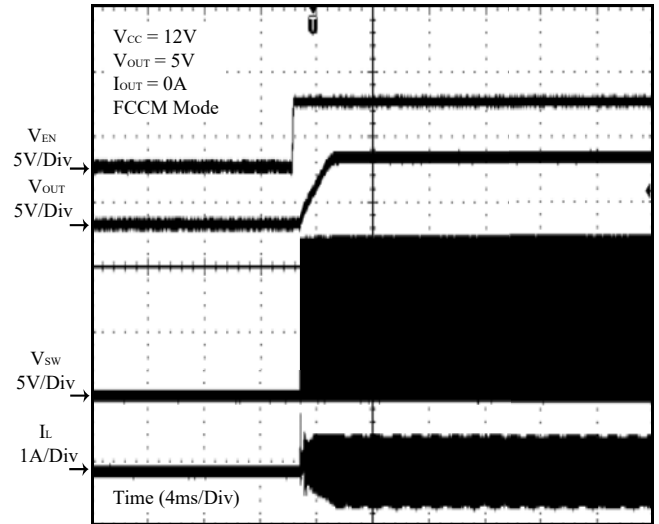


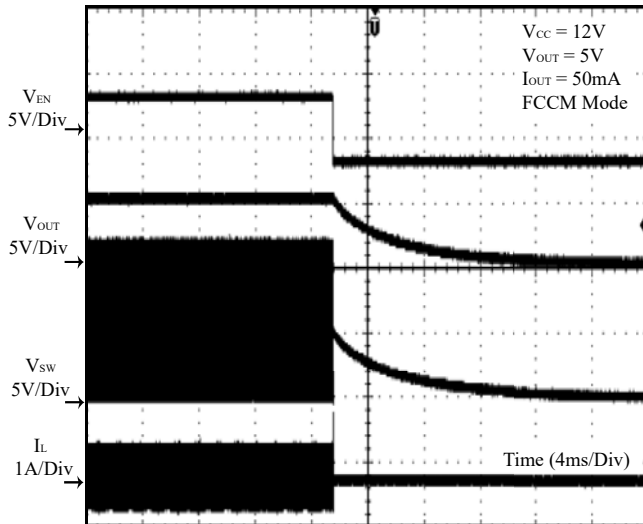
Figure 31 Start Up with VCC



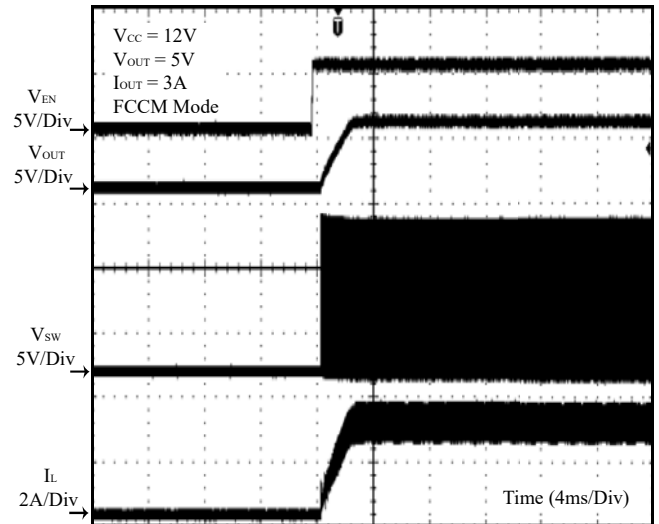
**Figure 32** Shut Down with VCC



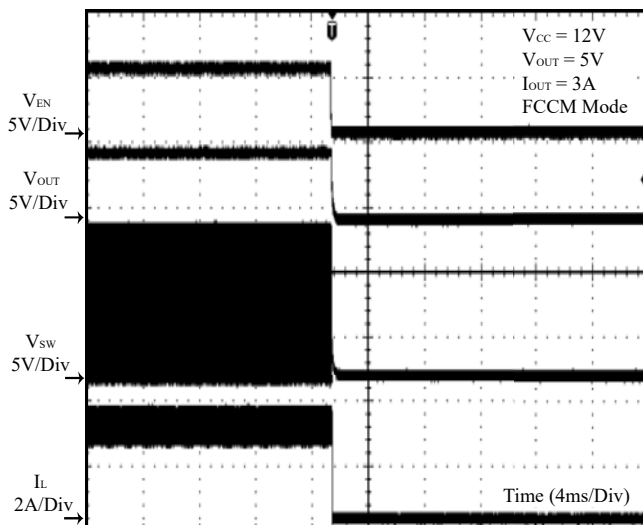
**Figure 33** Start Up with EN



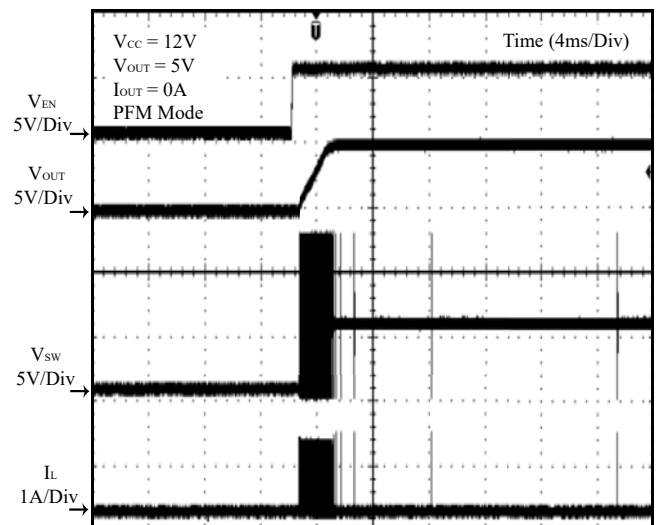
**Figure 34** Shut Down with EN



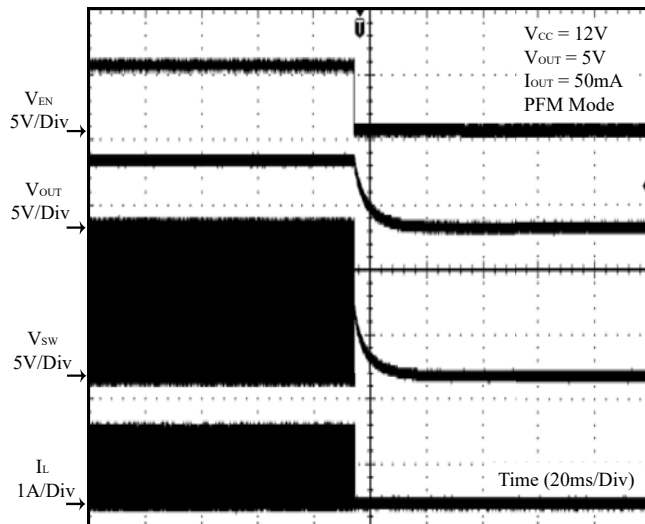
**Figure 35** Start Up with EN



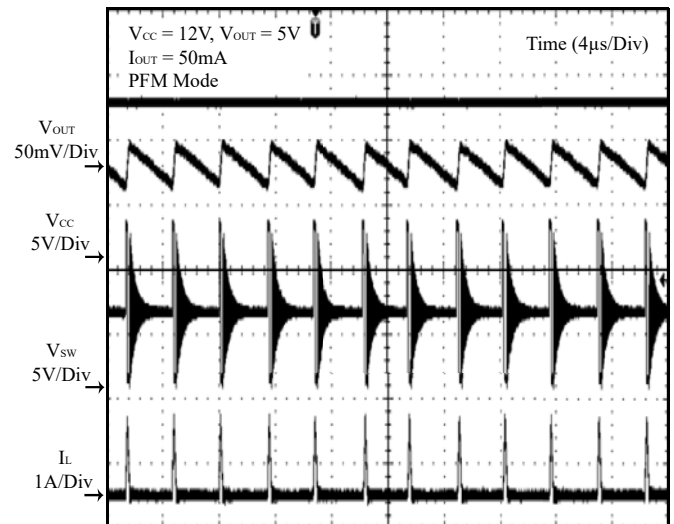
**Figure 36** Shut Down with EN



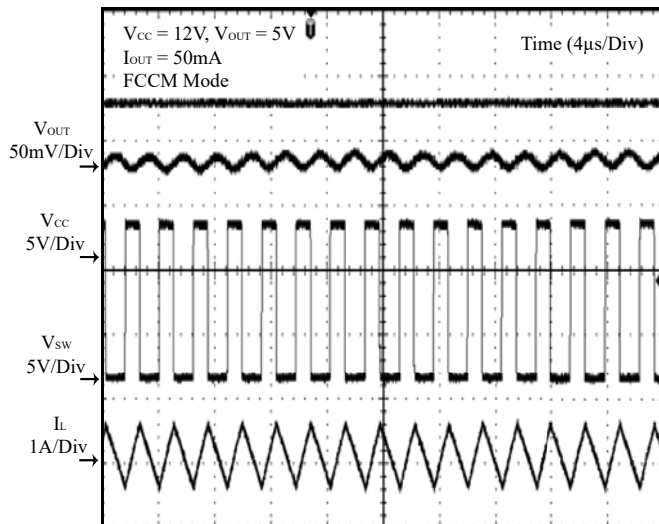
**Figure 37** Start Up with EN



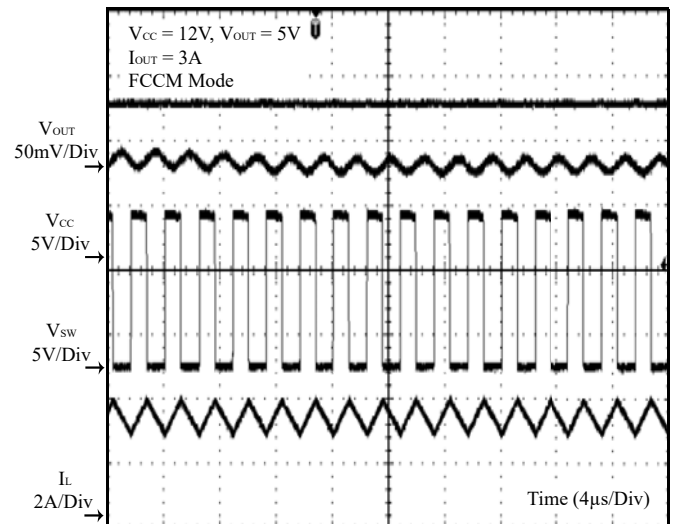
**Figure 38** Shut Down with EN



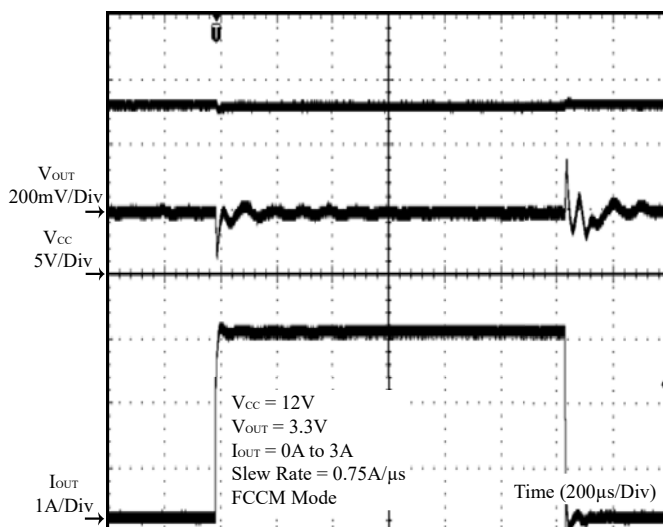
**Figure 39** Output Ripple



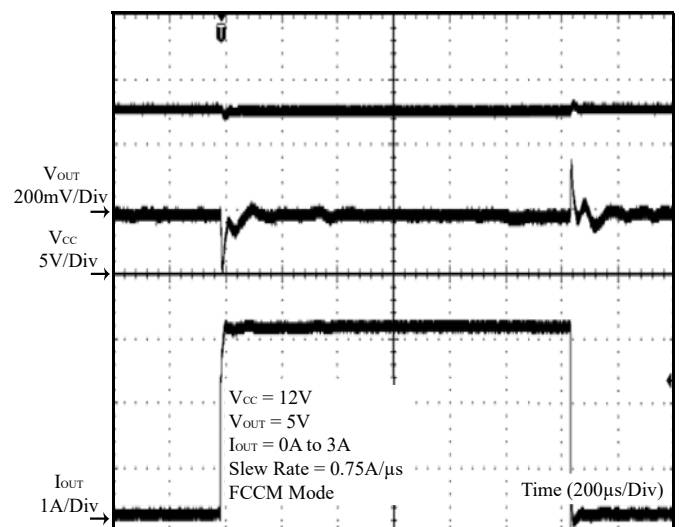
**Figure 40** Output Ripple



**Figure 41** Output Ripple



**Figure 42** Load Transient



**Figure 43** Load Transient

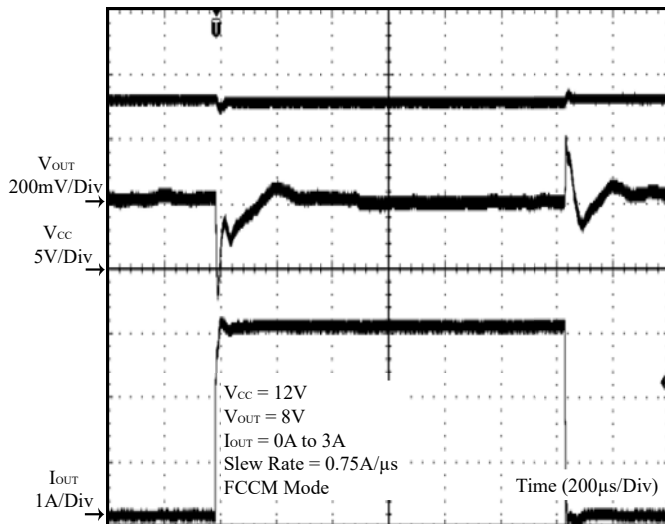


Figure 44 Load Transient

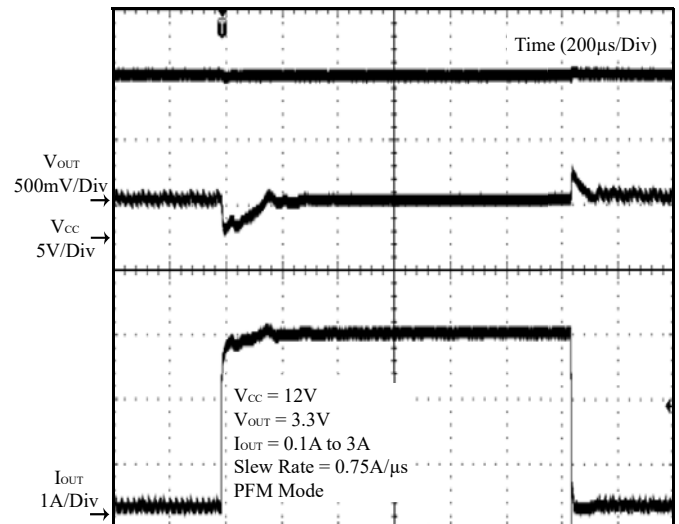


Figure 45 Load Transient

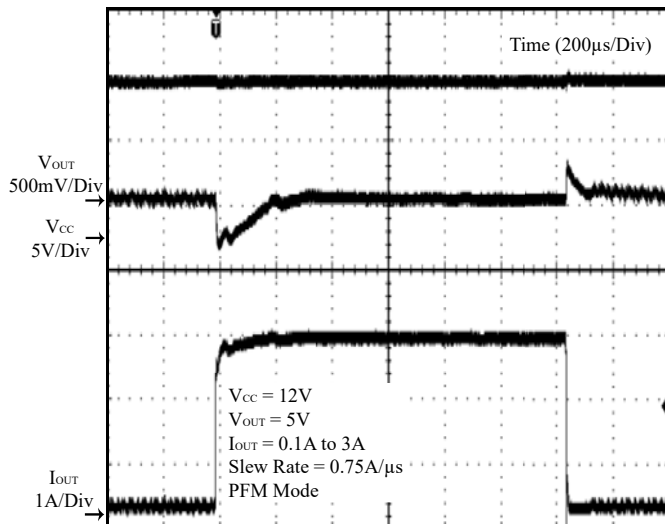


Figure 46 Load Transient

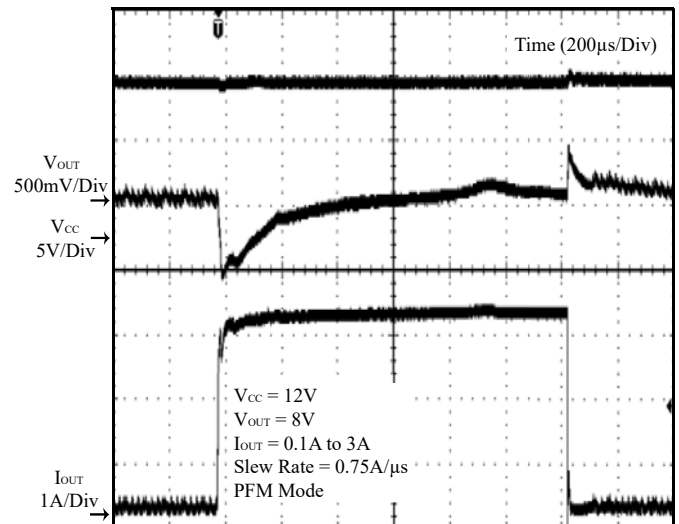


Figure 47 Load Transient

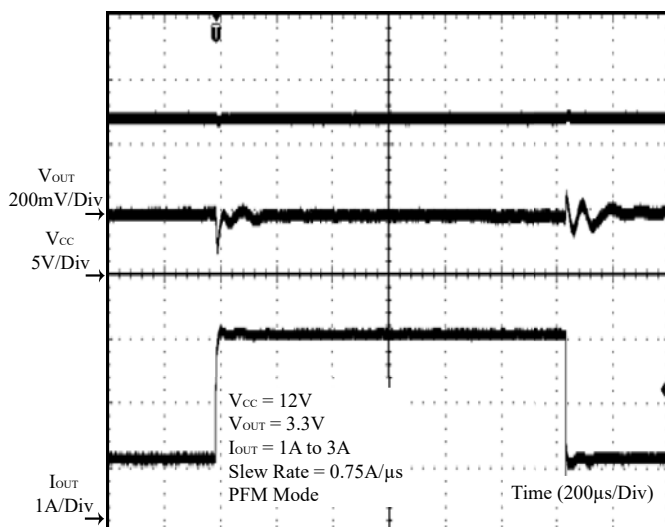


Figure 48 Load Transient

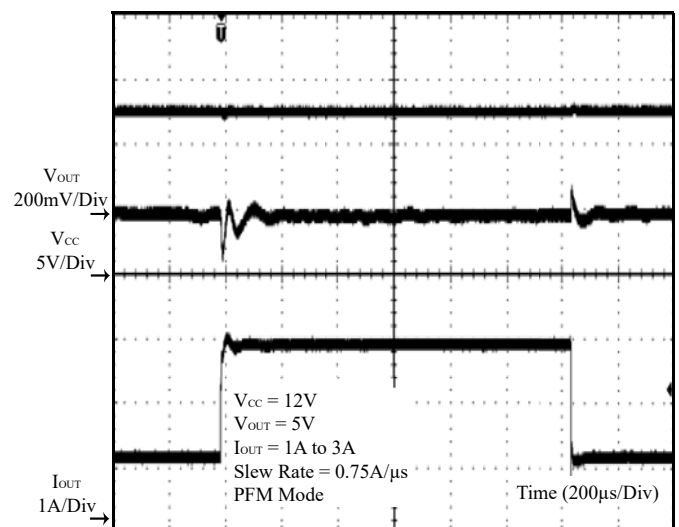
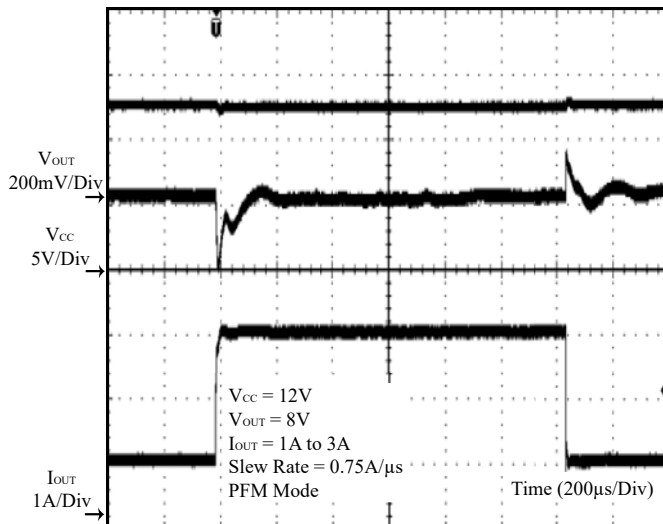
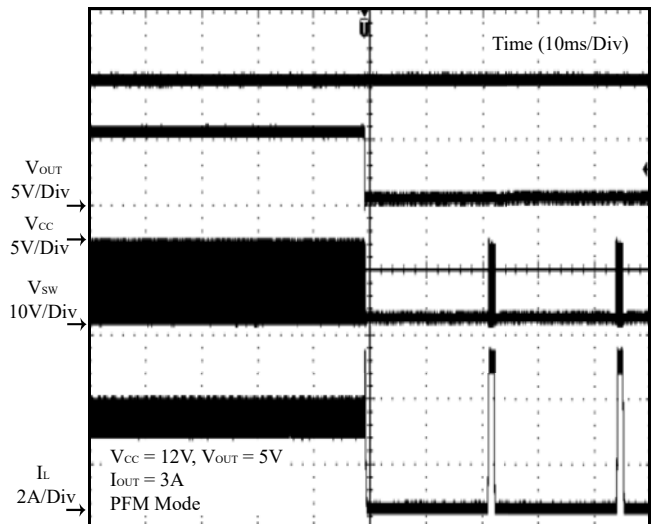


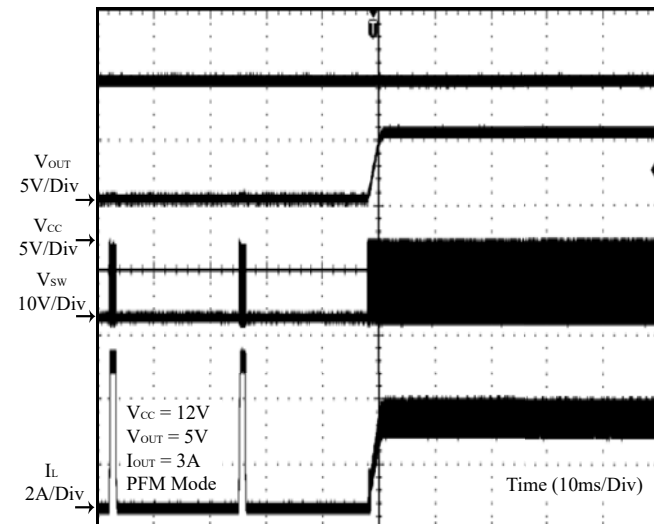
Figure 49 Load Transient



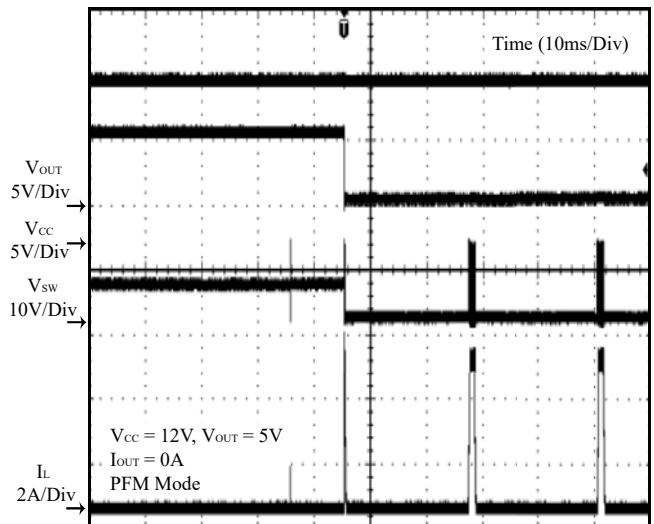
**Figure 50** Load Transient



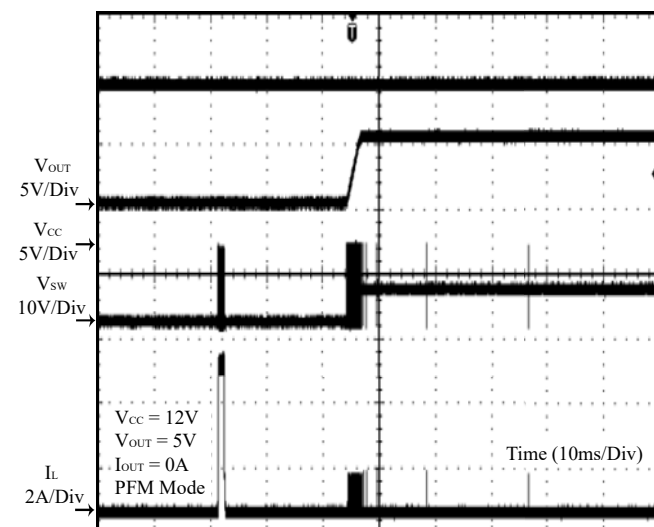
**Figure 51**  $V_{OUT}$  Short to GND



**Figure 52** Short Circuit Recovery



**Figure 53**  $V_{OUT}$  Short to GND



**Figure 54** Short Circuit Recovery

# IS32PM3420B

## DETAILS DESCRIPTION

The IS32PM3420B is a fully integrated Synchronous rectified step-down switch-mode converter. Constant-on time (COT) control is employed to provide fast transient response and easy loop stabilization. At the beginning of each cycle, the high-side MOSFET (HS-FET) is turned on when the FB pin voltage ( $V_{FB}$ ) is below the error amplifier output voltage (EAO), which indicates an insufficient output voltage. The output voltage and input voltage determine the on-period, keeping the switching frequency fairly constant over the input voltage range.

After the on-period elapses, the HS-FET is turned off, it is turned on again when  $V_{FB}$  drops below EAO. The converter regulates the output voltage by repeating the operation in this way. The integrated low-side MOSFET (LS-FET) is turned on when the HS-FET is in its off state to minimize conduction loss. There is a dead short between the input and GND if both the HS-FET and LS-FET are turned on at the same time. This is called shoot-through. To avoid shoot-through, a dead-time (DT) is generated internally between the HS-FET off and LS-FET on period or the LS-FET off and HS-FET on period.

Internal compensation is applied for COT control to provide a more stable operation and fast transient response, even when ceramic capacitors are used as output capacitors.

### MODE SELECTION AT LIGHT-LOAD OPERATION

The IS32PM3420B has an FPWM pin that can offer two states of operations, FCCM mode and PFM mode, at light load conditions. If the voltage of the FPWM pin higher than  $V_{FPWM\_IH}$ , IS32PM3420B operates in Forced Continuous Conduction Mode (FCCM) at light-load conditions allowing the inductor current to become negative. With FCCM mode, the operating frequency is maintained at a fairly constant level over the entire load range from light-load to full-load, which minimizes output voltage ripples and avoids the operating frequency dropping into audible frequency range ( $\leq 20\text{kHz}$ ) which may introduce some audible noise.

However, if the voltage of the FPWM pin is lower than  $V_{FPWM\_IL}$ , IS32PM3420B operates in Pulse-Frequency Modulation (PFM) mode during light-load operation and reduces the switching frequency automatically to maintain high efficiency, and the inductor current drops almost to zero. As shown in Figure 55, the HS-FET turns on when the FB pin voltage ( $V_{FB}$ ) is below the error amplifier output voltage (EAO). The HS-FET turns off when the on-timer elapses and the inductor current is higher than its given threshold. When the inductor current reaches zero, the LS-FET driver goes into tri-state (Hi-Z). Therefore, the output capacitors discharge slowly to GND through the LS-FET and the resistors  $R_{FBT}$  and  $R_{FBB}$ . This operation improves

device efficiency greatly when the output current is low.

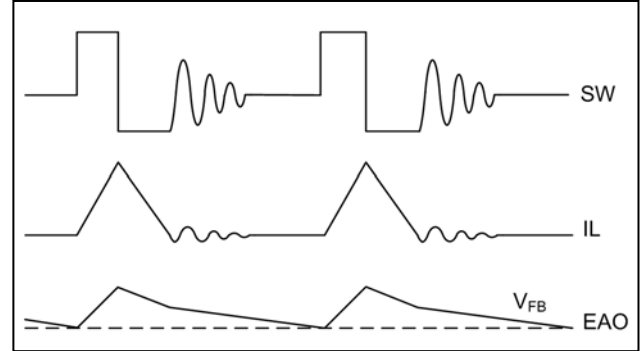


Figure 55 PFM Operation Mode at Light-load

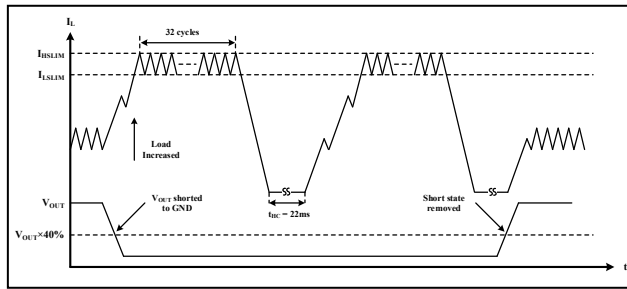
### OVER-CURRENT PROTECTION (OCP)

The IS32PM3420B senses both HS-FET and LS-FET currents for cycle-by-cycle peak and valley current limits and protect the output from an over-current or short-circuit protection condition. If the converter is over-current and eventually the HS-FET current hits the HS-FET current limit threshold  $I_{HSLIM}$ , the HS-FET turns off to limit the increasing current. Then the LS-FET turns on and monitors the current flowing through it. The HS-FET waits until the LS-FET current ramps down to the LS-FET current limit ( $I_{LSLIM}$ ) before turning on again. As a result, the converter operates in inductor current hysteresis control, upper threshold  $I_{HSLIM}$  and lower threshold  $I_{LSLIM}$ . This represents the maximum output current from the converter and is approximately given by the following equation:

$$I_{OUT\_MAX} = \frac{(I_{HSLIM} + I_{LSLIM})}{2} \quad (1)$$

When the load current is higher than  $I_{OUT\_MAX}$ , the output voltage tends to drop because the load current demand is higher than what the converter can support. If the hysteresis control operating persists for 32 switching cycles, and the output voltage falls below the output under-voltage threshold (Typ. 40% of the regulation voltage), in this case, the converter enters hiccup mode to restart the part periodically with the hiccup time  $t_{HC}$  (Typ. 22ms), as shown in Figure 56. The hiccup protection mode is especially useful when the output is dead-short to the ground. This reduces the average short-circuit current greatly, alleviating thermal issues and protecting the converter. The converter exits hiccup mode once the over-current or short-circuit condition is removed.

# IS32PM3420B



**Figure 56** Hiccup Mode

Due to FCCM operation, when the output current is less than half of the peak-to-peak inductor current ripple, the inductor valley current ramps down to negative (LS-FET sinks current). The IS32PM3420B also incorporates a negative current limit to protect the LS-FET against sinking excessive current and possibly damaging the converter. If the LS-FET sink current hits the negative current limit ( $I_{LSRS}$ ), the LS-FET turns off until after the next HS-FET on-time.

## OVER-VOLTAGE PROTECTION (OVP)

The IS32PM3420B monitors the FB pin voltage to detect over-voltage condition. When  $V_{FB}$  becomes higher than 110% (Typ.) of the regulation feedback voltage  $V_{FB\_TH}$ , the over-voltage protection (OVP) is triggered after a deglitch time of 16 $\mu$ s (Typ.). The converter stops switching and does not resume until the  $V_{FB}$  drops to  $V_{FB\_TH}$ . The OVP function protects the downstream devices from over-voltage damage.

## VDD REGULATOR

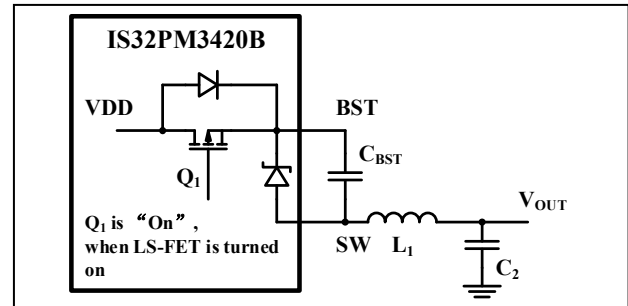
The IS32PM3420B contains a linear regulator ( $V_{DD}$ ) with 5V (Typ.) output voltage to supply internal circuit blocks including the control logic circuits and the HS-/LS-FET gate drivers. The  $V_{DD}$  regulator is internally current limited to  $I_{DD\_LIM}$  (Min. 20mA). It operates in the full  $V_{CC}$  range. When the  $V_{CC}$  voltage exceeds 5V, the regulator will stabilize at 5V (Typ.) output, but if  $V_{CC}$  is lower than 5V, its output decreases with  $V_{CC}$ . During operation, driving HS-/LS-FET gates will draw transient high current from this linear regulator. Therefore, a 1 $\mu$ F low ESR, X7R type ceramic capacitor is necessary from the  $V_{DD}$  pin to GND; it must be placed as close to the  $V_{DD}$  pin as possible.  $V_{DD}$  can bias external low current circuitry requiring a reference supply. However, do not recommend powering any high current external device with the  $V_{DD}$  pin to ensure system stability.

## FLOATING DRIVER AND BOOTSTRAP CHARGING

The gate driver of the integrated HS-FET requires a voltage above  $V_{CC}$  as an input power supply. As the circuit diagram shown in Figure 57, the  $V_{DD}$  regulator is the power supply of the gate driver. The BST pin is internally connected to the output of the  $V_{DD}$  regulator through a P-FET switch. Connect a ceramic capacitor between BST and SW pins. The  $V_{DD}$  regulator charges the  $C_{BST}$  capacitor during HS-FET

off and LS-FET on cycles. Then in HS-FET on cycles, the  $C_{BST}$  charge voltage is used to boost the BST pin to 5V higher than the SW pin.

A 0.1 $\mu$ F X7R ceramic capacitor will work well in most applications. The gate driver also has an under-voltage lockout detection. The gate driver is enabled when the voltage on the  $C_{BST}$  rises to above 2.86V (Typ.) and disabled when the voltage on the  $C_{BST}$  drops below 2.55V (Typ.).



**Figure 57** Bootstrap Charging Circuit

## OPERATION FREQUENCY AND SPREAD SPECTRUM

The IS32PM3420B operates at a fixed frequency of 400kHz (Typ.). To optimize EMI performance, IS32PM3420B includes a spread spectrum feature, an 800Hz (Typ.) with  $\pm 5\%$  (Typ.) operating frequency jitter. It can spread the total electromagnetic emitting energy into a wider range that significantly degrades the peak energy of the EMI profile. With spread spectrum, the EMI test can be passed with smaller size and lower cost filter circuit.

## SOFT-START

The IS32PM3420B features an internal 2ms (Typ.) soft-start function. The soft-start function of IS32PM3420B allows the converter to gradually reach a steady-state operating point, thereby dampening the inrush current to an acceptable value at startup. When the EN pin is set to start the converter operation, the internal soft-start circuitry generates a ramping up voltage with a controlled slope. When it is lower than the internal reference of the error amplifier (EA), the soft-start voltage overrides the EA's reference so the EA uses the soft-start voltage as the reference. Once the soft-start voltage exceeds EA's reference, EA's reference regains loop control. The soft-start period time is internally fixed at 2ms (Typ.) and not adjustable.

If the output capacitor is pre-biased at startup, the converter starts switching and ramping up only after the internal soft-start voltage exceeds the FB pin voltage  $V_{FB}$ . This scheme ensures that the converters ramp up smoothly into a regulation point.

# IS32PM3420B

## LOW DROPOUT OPERATION

The IS32PM3420B supports low dropout operation. When the  $V_{CC}$  voltage is close to the output voltage and the minimum off-time is triggered, the switching on timer is extended to avoid output voltage drops. The switching frequency decreases accordingly. After the maximum on time is triggered (Typ. 10 $\mu$ s), switching enters max duty cycle operation. If the  $V_{CC}$  voltage continues to decrease, the output voltage will begin to decrease gradually with the  $V_{CC}$  voltage.

## ENABLE CONTROL

The EN pin has a dual-level threshold. When the EN voltage is below  $V_{EN\_VDD\_L}$ , the regulator is in an ultra-low current shutdown mode. When the EN voltage is greater than  $V_{EN\_VDD\_H}$ , but less than  $V_{EN\_VOUT\_H}$ , the  $V_{DD}$  regulator is in standby mode. In standby mode, the  $V_{CC}$  bias  $V_{DD}$  regulator is active but converter switching remains disabled. Normal switching operation begins when the voltage at the EN pin exceeds the threshold  $V_{EN\_VOUT\_H}$ . Use an external resistor voltage divider from  $V_{CC}$  to GND to set the minimum operating voltage of the converter. If the EN voltage is lower than  $V_{EN\_VDD\_L}$ , the whole system will shut down.

Never leave the EN pin floating. It has high impedance and high-voltage tolerance and can be connected directly to the  $V_{CC}$  pin if it is unused. However, a series resistor (recommended value of 47k $\Omega$ ) is required to limit the current flowing in to the EN pin if it is higher than the  $V_{CC}$  voltage at any time.

## UNDER-VOLTAGE LOCKOUT PROTECTION

The IS32PM3420B has two Under-voltage Lockout (UVLO) protections:  $V_{DD}$  UVLO and  $V_{CC}$  UVLO. The IS32PM3420B starts up only when both  $V_{DD}$  and  $V_{CC}$  exceed their respective UVLO threshold and shuts down when either  $V_{DD}$  is lower than the  $V_{DD}$  UVLO falling threshold voltage or  $V_{CC}$  is lower than the  $V_{CC}$  UVLO falling threshold. Both are non-latch off protections.

Besides this internal fixed UVLO, it may be desirable to externally set a higher UVLO threshold for some applications. As shown in Figure 58, a precise EN threshold voltage can be set by using a resistor voltage divider between  $V_{CC}$  and GND with the center connected to the EN pin. The external UVLO threshold voltage can be computed by the following Equations:

$$V_{CC\_UVEXR} = \frac{(R_{EN1} + R_{EN2})}{R_{EN2}} \times V_{EN\_VOUT\_H} \quad (2)$$

$$V_{CC\_UVEXF} = \frac{(R_{EN1} + R_{EN2})}{R_{EN2}} \times (V_{EN\_VOUT\_H} - V_{EN\_VOUT\_HY}) \quad (3)$$

The output regulation is enabled when the  $V_{CC}$  voltage exceeds  $V_{CC\_UVEXR}$  and disabled when it falls below  $V_{CC\_UVEXF}$ .

It is recommended that  $R_{EN1}$  and  $R_{EN2}$  be 1% accuracy resistors with good temperature characteristics to ensure a precise detection. This resistor divider must be placed as close as possible to the EN pin on the PCB layout to avoid noise coupling into the UVLO detection.

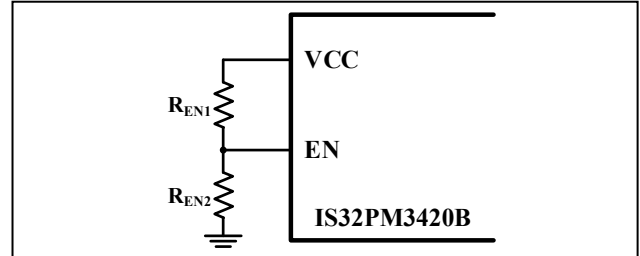


Figure 58 EN Configuration

## THERMAL SHUTDOWN

The temperature of the die is monitored to protect the converter from damage when the maximum junction temperature is exceeded. If the die temperature exceeds the thermal shutdown temperature of 175 $^{\circ}$ C (Typ.) the converter will stop switching and enter standby mode. After a thermal shutdown event, the IS32PM3420B will try to restart when its die temperature is less than 155 $^{\circ}$ C (Typ.).

## SETTING THE OUTPUT VOLTAGE

The external resistor divider,  $R_{FBT}$  and  $R_{FBB}$ , is used to set the output voltage (As shown in Figure 59), according to the following equation:

$$V_{OUT} = \frac{(R_{FBB} + R_{FBT})}{R_{FBB}} \times V_{FB\_TH} \quad (4)$$

Where  $V_{FB\_TH} = 1V$  (Typ.).

Choosing a value for the resistor  $R_{FBB}$  should be reasonable. Usually, a small  $R_{FBB}$  leads to considerable quiescent current loss, while a large  $R_{FBB}$  makes the FB pin noise-sensitive and voltage errors from the  $V_{FB}$  input current are noticeable.

In order to have an accurate output voltage, precision resistors are preferred ( $\pm 1\%$  recommended). The  $R_{FBT}$  and  $R_{FBB}$  resistors should be placed as close as possible to the IS32PM3420B with minimal trace length to the FB and AGND pins.

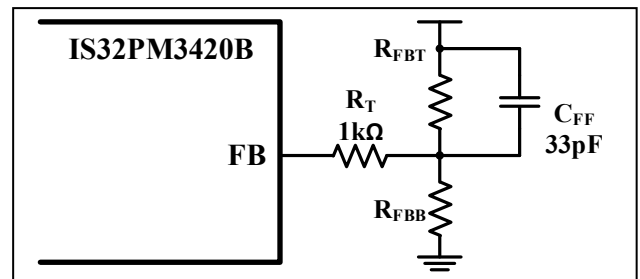


Figure 59 Feedback Network

In addition, it should be noted that the resistor  $R_T$  and capacitor  $C_{FF}$  are required. The  $R_T$  is fixed at 1k $\Omega$ , while the  $C_{FF}$  is fixed at 33pF.

## SELECTING THE INDUCTOR

An inductor is necessary for supplying constant current to the output load while being driven by the switched input voltage. Inductor value involves trade-offs in performance. A larger inductance reduces the output current ripple and output voltage ripple but brings a large physical size, higher Direct Current Resistance (DCR) and lower saturation current. A small inductance has a compact physical size and lower cost but introduces a higher ripple in the output. Use the following Equation (5) to estimate the approximate inductor value:

$$L = \frac{(V_{CC} - V_{OUT}) \times V_{OUT}}{f_{SW} \times \Delta I_L \times V_{CC}} \quad (5)$$

Where  $\Delta I_L$  is the peak-to-peak inductor current ripple which is usually chosen to be 30%~50% of the maximum output current.

Select an inductor with a rated current greater than the maximum output current. To prevent inductance saturation, the saturation current of the selected inductor ( $I_{SAT}$ ) must be higher than the maximum inductor peak current ( $I_{L\_PK}$ ) with some safety margin. The peak current can be calculated with Equation (6):

$$I_{L\_PK} = I_{OUT\_MAX} + \frac{1}{2} \times \Delta I_L \quad (6)$$

Where  $I_{OUT\_MAX}$  is the maximum output current.

Meanwhile, the  $I_{L\_PK}$  should not exceed the minimum value of the HS-FET current limit ( $I_{HSLIM}$ ). Otherwise the converter may not be able to deliver the desired output current. If needed, increase the inductor value to reduce the inductor current ripple ( $\Delta I_L$ ) and ensure that  $I_{L\_PK}$  does not exceed the HS-FET current limit level. A shielded type inductor with low DCR is recommended in most applications, which gives better EMI and efficient performance.

## SELECTING THE INPUT CAPACITOR

The input current is discontinuous for step-down converter, which requires a capacitor to supply the AC input current while maintaining the DC input voltage. The X7R type ceramic capacitors are recommended for best performance, and make sure that the capacitors are placed as close to the VCC pin as possible.

It requires the capacitor ripple current rating should be higher than the converter maximum input ripple current, which can be calculated with Equation (7):

$$I_{CVCC} = I_{OUT\_MAX} \times \sqrt{\frac{V_{OUT}}{V_{CC}}} \times \left(1 - \frac{V_{OUT}}{V_{CC}}\right) \quad (7)$$

The worse-case condition occurs at  $V_{CC} = 2V_{OUT}$ ,

As shown in Equation (8):

$$I_{CVCC} = \frac{I_{OUT\_MAX}}{2} \quad (8)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current. The capacitance value determines the input voltage ripple of the converter. When select the desired input voltage ripple  $\Delta V_{CC}$ , the minimum input capacitor  $C_{VCC}$  can be calculated with Equation (9):

$$C_{VCC} = \frac{I_{OUT\_MAX}}{f_{SW} \times \Delta V_{CC}} \times \frac{V_{OUT}}{V_{CC}} \times \left(1 - \frac{V_{OUT}}{V_{CC}}\right) \quad (9)$$

The worse-case condition occurs at  $V_{CC} = 2V_{OUT}$ .

As shown in Equation (10):

$$C_{VCC} = \frac{1}{4} \times \frac{I_{OUT\_MAX}}{f_{SW} \times \Delta V_{CC}} \quad (10)$$

## SELECTING THE OUTPUT CAPACITOR

An output capacitor is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors can be used. But for best performance, use low ESR capacitors to keep output ripple low.

If the desired output voltage ripple  $\Delta V_{OUT}$  is determined, the minimum  $C_{OUT}$  can be calculated with Equation (11):

$$C_{OUT} = \frac{\Delta I_L}{8 \times f_{SW} (\Delta V_{OUT} - \Delta I_L \times ESR)} \quad (11)$$

However, in the case of ceramic applications, the output voltage ripple is caused mainly by the capacitance due to the low ESR of ceramic. For simplification, the minimum  $C_{OUT}$  can be estimated with Equation (12):

$$C_{OUT} = \frac{\Delta I_L}{8 \times f_{SW} \times \Delta V_{OUT}} \quad (12)$$

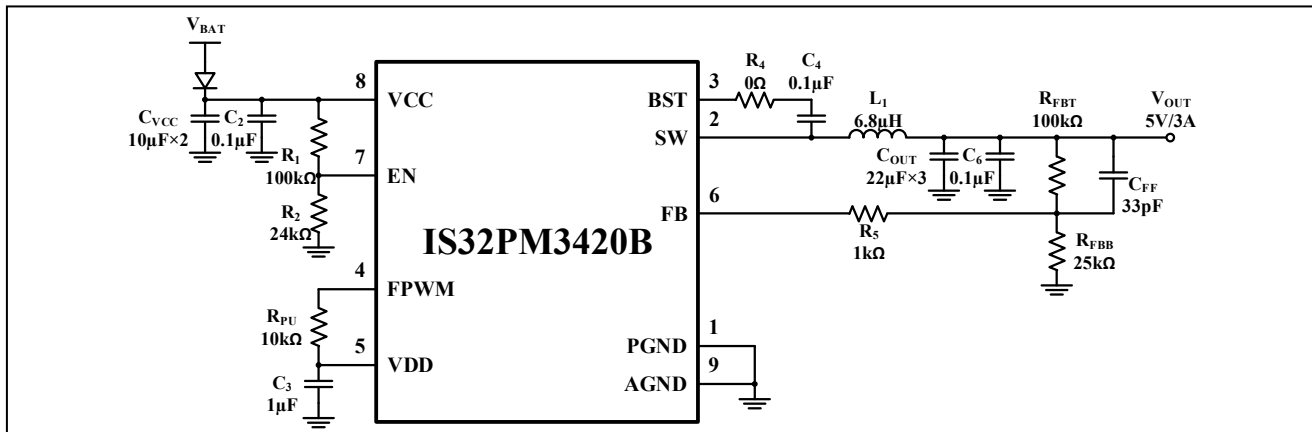
Note that the effective capacitance of ceramic capacitors decreases with DC bias. For larger bulk values of capacitance and lower cost, low ESR type electrolytic capacitors are usually used to be connected in parallel with the ceramic capacitors. However, electrolytic capacitors have poor tolerance, especially over temperature, and the selected value should be larger than the calculated value to allow for temperature variation.

# IS32PM3420B

**Table 1 Recommended Component Values ( $V_{CC}=12V$ )**

Output Voltage (V)	$R_{FBT}$ (k $\Omega$ )	$R_{FBB}$ (k $\Omega$ )	$L_1$ ( $\mu$ H)	$C_{FF}$ (pF)	$C_{OUT}$ ( $\mu$ F)
3.3	100	43.5	5.6	33	40 to 80
5	100	25	6.8	33	40 to 80
8	100	14.3	5.6	33	40 to 80

## Application Example



**Figure 60**  $f_{SW}=400kHz$  5V/3A Output Application Example

## LAYOUT CONSIDERATION

Layout is an important design step for all switching power supplies, especially those providing high current and using high switching frequencies. If a layout is not carefully done, the operation could show instability as well as EMI problems.

The high  $dV/dt$  surface and  $dI/dt$  loops are big noise emission source. To optimize the EMI performance, keep the area size of all high switching frequency points with high voltage compact. Meantime keep all traces carrying high current as short as possible to minimize the loops.

- (1) Wide traces should be used for connection of the high current paths that helps to achieve better efficiency and EMI performance. Such as the traces of power supply, inductor  $L_1$ , output load and ground.
- (2) Keep the traces of the switching points shorter. The inductor  $L_1$  should be placed as close to the SW pin as possible and the traces of connection between them should be as short and wide as possible.
- (3) To avoid ground jitter, the components of the parameter setting should be placed close to the corresponding pins and return to the AGND (thermal PAD) and keep the traces length to the pins as short as possible. On the other side, to prevent noise coupling, the output voltage setting resistor divider must be placed as close to FB and AGND (thermal PAD) as possible. The traces of FB should either be far away or be isolated from

high-current paths and high-speed switching nodes. These practices are essential for better accuracy and stability.

- (4) The capacitors  $C_{VCC}$  and  $C_{VDD}$  must be placed as close as possible to VCC and VDD pins for good filtering.
- (5) Place the bootstrap capacitor  $C_{BST}$  close to the BST pin and SW pin to ensure the traces are as short as possible.
- (6) The connection to the output load should be kept short to minimize radiated emission.
- (7) The thermal PAD of the converter package must be soldered to copper ground plane of enough size with sufficient vias to conduct the heat to opposite side of the PCB for adequate cooling. Flood all unused areas on all layers with copper, to reduce the temperature rise of the power components. Connect the copper areas to the ground.

## THERMAL CONSIDERATION

The package thermal resistance,  $\theta_{JA}$ , determines the amount of heat that can pass from the silicon die to the surrounding ambient environment. The  $\theta_{JA}$  is a measure of the temperature rise created by power dissipation and is usually measured in degree Celsius per watt ( $^{\circ}C/W$ ).

When operating the chip at high ambient temperatures, or when driving maximum load current, care must be taken to avoid exceeding the package power dissipation limits. The maximum power

# IS32PM3420B

dissipation can be calculated using the following Equation (13):

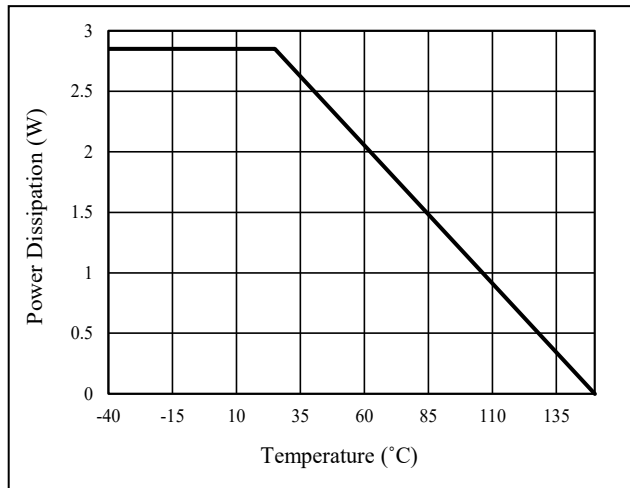
$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}} \quad (13)$$

Where  $T_{J(MAX)}$  is the recommended maximum operating junction temperature.

So,

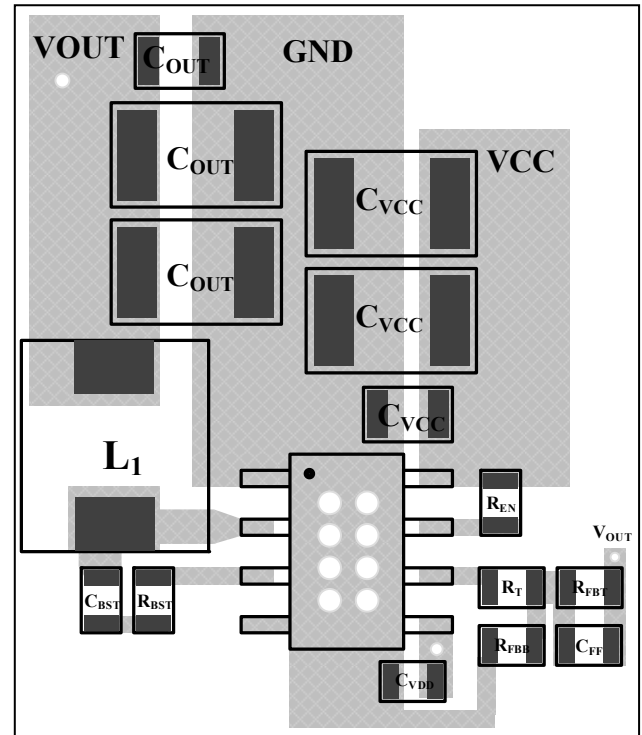
$$P_{D(MAX)} = \frac{150^{\circ}\text{C} - 25^{\circ}\text{C}}{43.9^{\circ}\text{C/W}} \approx 2.85\text{W}$$

Figure 61, shows the power derating of the IS32PM3420B on a JEDEC boards (in accordance with JESD 51-5 and JESD 51-7) standing in still air.



**Figure 61** Dissipation Curve

The thermal resistance is achieved by mounting the IS32PM3420B on a standard FR4 double-sided printed circuit board (PCB) with a copper area of a few square inches on each side of the board under the IS32PM3420B. The thermal resistance can be reduced by using a four-layer PCB board. A four-layer layout is strongly recommended to achieve better thermal and EMI performance.



**Figure 62** PCB Layout Example (Top Layer)

## CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
<b>Preheat &amp; Soak</b> Temperature min (T <sub>smin</sub> ) Temperature max (T <sub>smax</sub> ) Time (T <sub>smin</sub> to T <sub>smax</sub> ) (t <sub>s</sub> )	150°C 200°C 60-120 seconds
Average ramp-up rate (T <sub>smax</sub> to T <sub>p</sub> )	3°C/second max.
Liquidous temperature (T <sub>L</sub> ) Time at liquidous (t <sub>L</sub> )	217°C 60-150 seconds
Peak package body temperature (T <sub>p</sub> )*	Max 260°C
Time (t <sub>p</sub> )** within 5°C of the specified classification temperature (T <sub>c</sub> )	Max 30 seconds
Average ramp-down rate (T <sub>p</sub> to T <sub>smax</sub> )	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

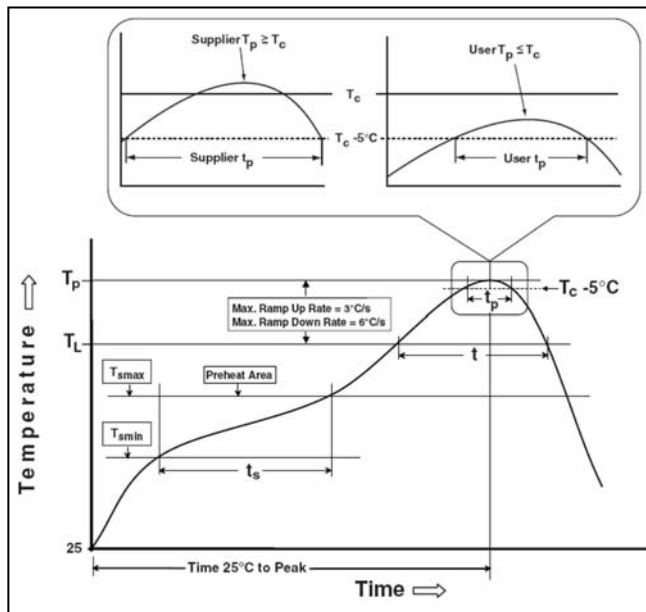
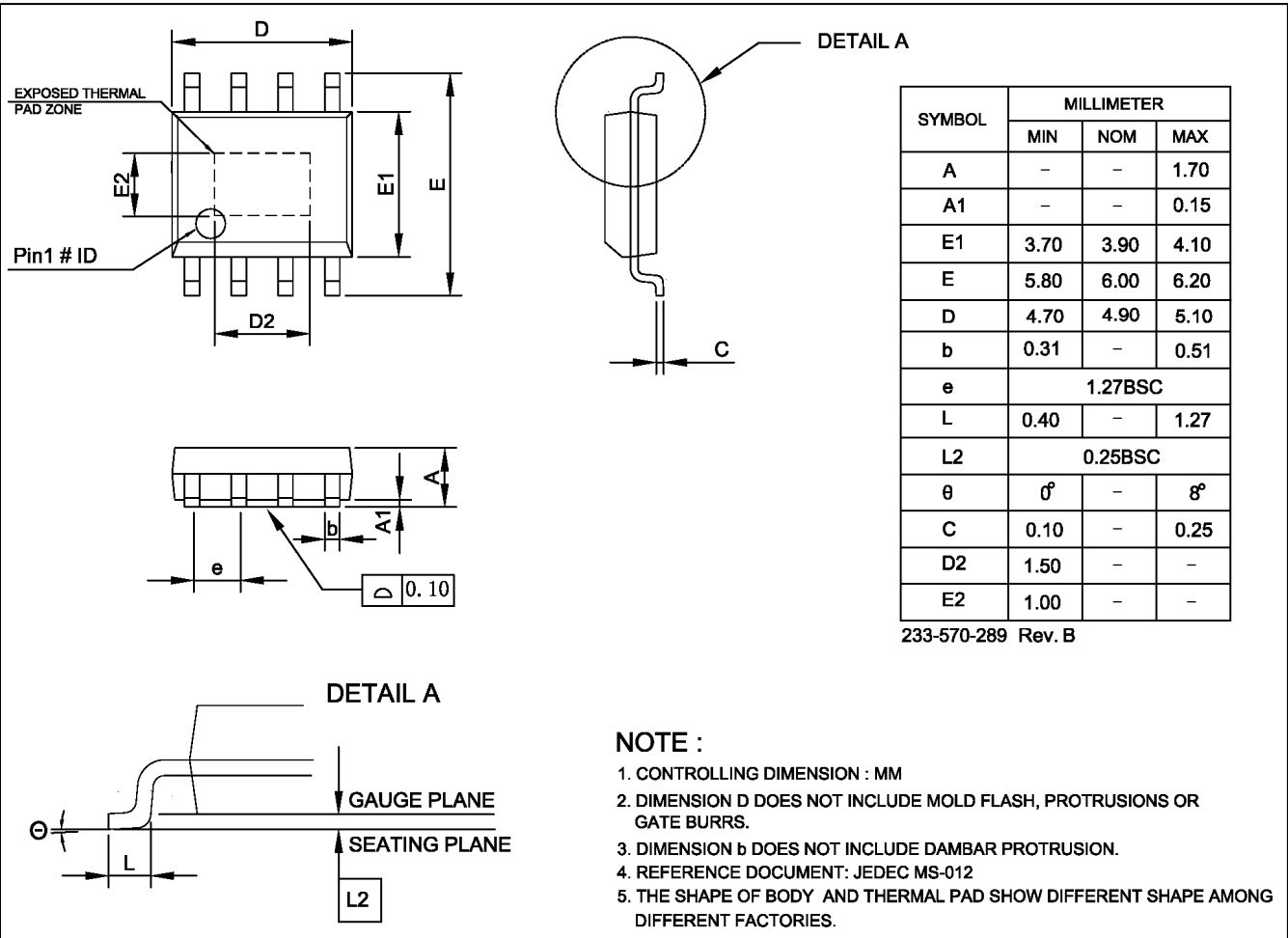


Figure 63 Classification Profile

# IS32PM3420B

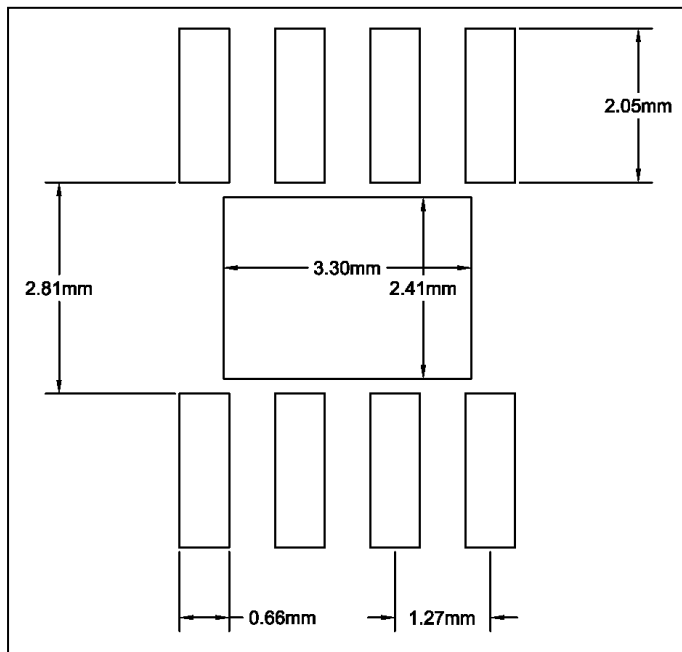
## PACKAGE INFORMATION

### SOP-8-EP



## RECOMMENDED LAND PATTERN

### SOP-8-EP



#### Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (e.g. user's board manufacturing specs), user must determine suitability for use.

## REVISION HISTORY

Revision	Detail Information	Date
0A	Initial release	2024.05.06
A	Update to final version	2024.07.17
B	Correct AECQ description	2024.08.19