IS32LT3958A

HIGH VOLTAGE LED LIGHTING CONTROLLER WITH INTERNAL PWM GENERATOR AND FAULT PROTECTION

June 2023

GENERAL DESCRIPTION

The IS32LT3958A is a current mode PWM controller designed to drive a low side external NMOS FET for wide input/output voltage range and high LED current applications. An external resistor senses the high side output current of the LED string. A high side sense resistor is the most flexible current sensing scheme, since it functions in either boost or buck-boost mode configurations. The controller can be configured with an external resistor to operate between 100kHz~1MHz frequency resulting in small external inductor and capacitors while maintaining high efficiency. A single capacitor is all that is required to set the spread spectrum dither frequency to reduce the radiated peak emission and optimize the system EMI performance.

The IS32LT3958A integrates circuitry to detect output open/short, RT/SYNC pin short, VDD short, VCC undervoltage lockout and over temperature fault conditions. These failure conditions can be reported by the open drain fault reporting FAULTB pin. The current monitor pin (IMON) output can be used for continuous LED status check.

The IS32LT3958A can modulate LED current using either analog and/or PWM dimming techniques. The IS32LT3958A features two independent analog dimming pins, ICTRL and ADJR. Input DC voltage in the range of 0.06V~2V on the ICTRL pin and/or ADJR pin is required for analog dimming. PWM dimming is achieved by directly modulating the PWM/EN pin with desired PWM duty cycle or by enabling the internal PWM generator circuit. With the internal PWM generator circuit, IS32LT3958A can achieve standalone dual brightness level output. The duty cycle and frequency of the internal PWM generator is easily programmed by external resistors.

The soft-start function of the IS32LT3958A has been optimized for achieving excellently smooth LED light on effect when use external low duty cycle PWM dimming to do the fade on control. With this optimization, it can prevent the LED output light on with high brightness rapidly and get a comfort fade on visual effect.

The IS32LT3958A is available in an eTSSOP-20 package with an exposed pad for enhanced thermal dissipation. It operates from 5V to 70V over the temperature range of -40°C to +150°C.

FEATURES

- Wide high voltage input range: 5V to 70V
- Supports boost, buck-boost, SEPIC and buck topology
- Supports either analog, internal PWM dimming or external PWM dimming
- Excellent fade on control by low duty cycle PWM dimming
- Standalone dual brightness output by internal PWM dimming
  - Integrated PWM generator
  - 100Hz~1kHz adjustable PWM frequency
  - 5%~100% adjustable PWM duty cycle
- Excellent analog dimming capability
  - Two analog dimming pins
  - LED binning capability
  - LED over temperature current roll-off
- Externally programmable input undervoltage-lockout
- ±2.8% output current accuracy over -40°C ~ +150°C temperature
- Adjustable operating frequency range of 100kHz~1MHz
- Programmable soft-start to avoid inrush current
- EMI reduction capabilities
  - Programmable spread spectrum function
  - Operating frequency synchronization with external clock source
- Fault protection with reporting:
  - VCC undervoltage lockout (not reported)
  - Programmable output overvoltage protection
  - Output short circuit protection
  - RT/SYNC pin short protection
  - VDD pin short protection
  - VDD undervoltage lockout (not reported)
  - Over temperature protection
- AEC-Q100 Qualified with Temperature Grade 1: -40°C to 125°C
- RoHS & Halogen-Free Compliance
- TSCA Compliance

APPLICATIONS

- Automotive
  - Headlight
  - Daytime running light
  - Fog light
  - Tail light

TYPICAL APPLICATION CIRCUIT

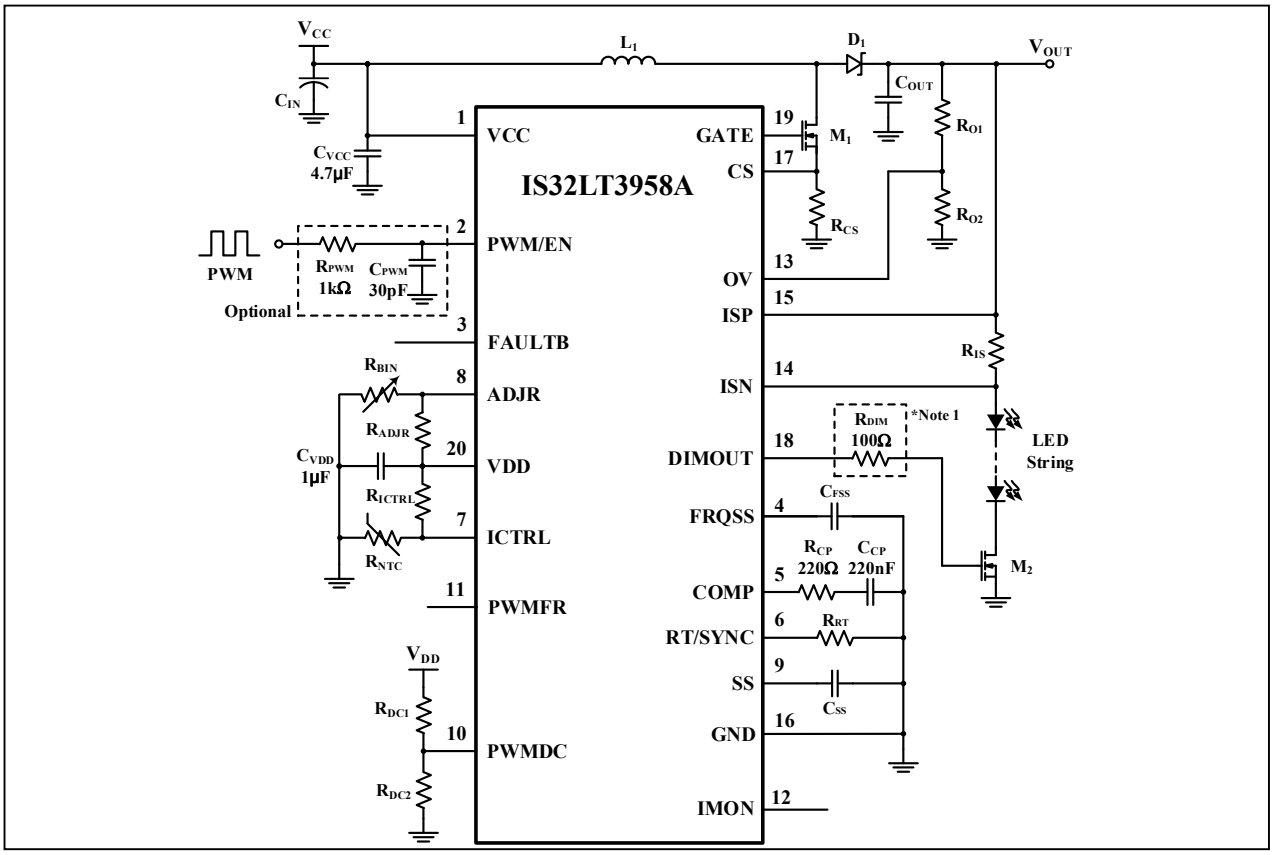


Figure 1 Typical Application Circuit with External PWM Dimming (Boost Configuration)

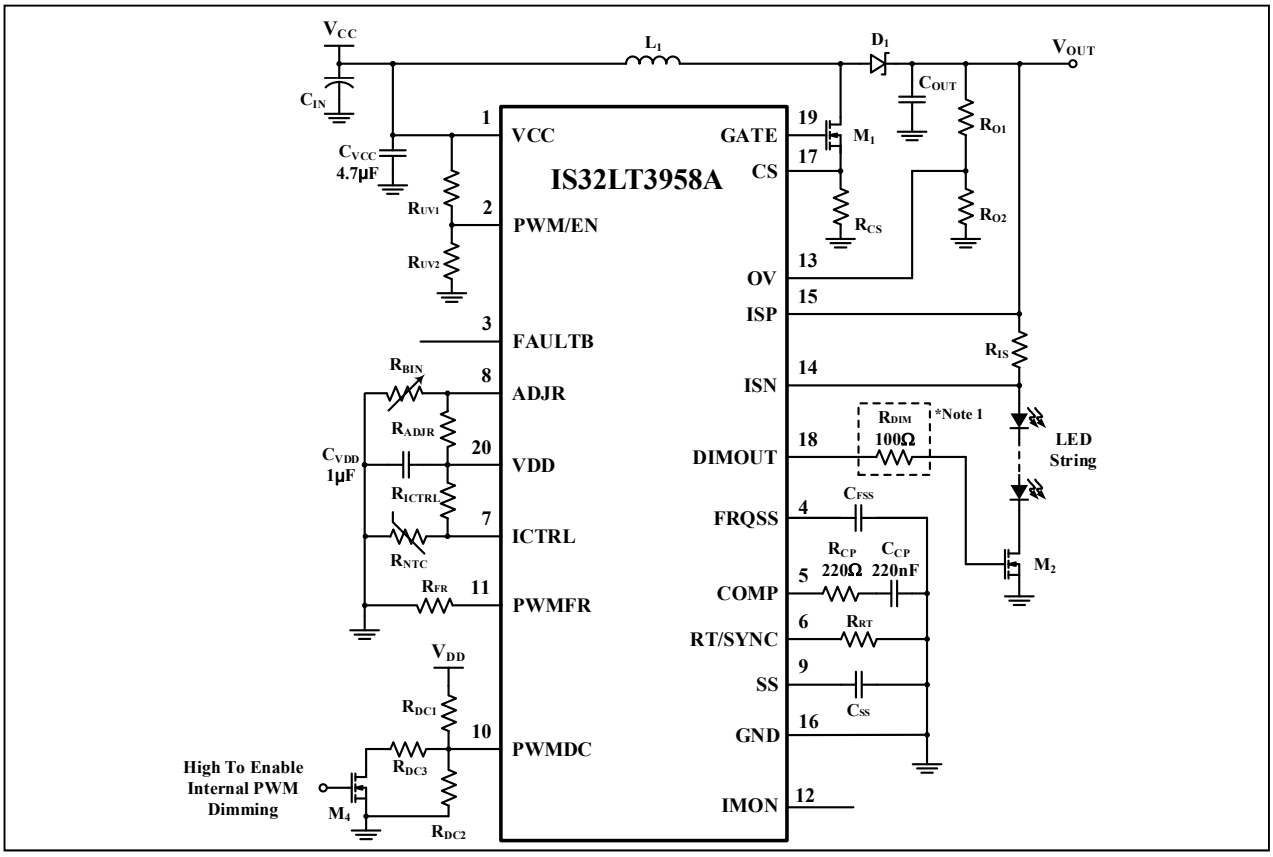


Figure 2 Typical Application Circuit With Internal PWM Dimming (Boost Configuration)

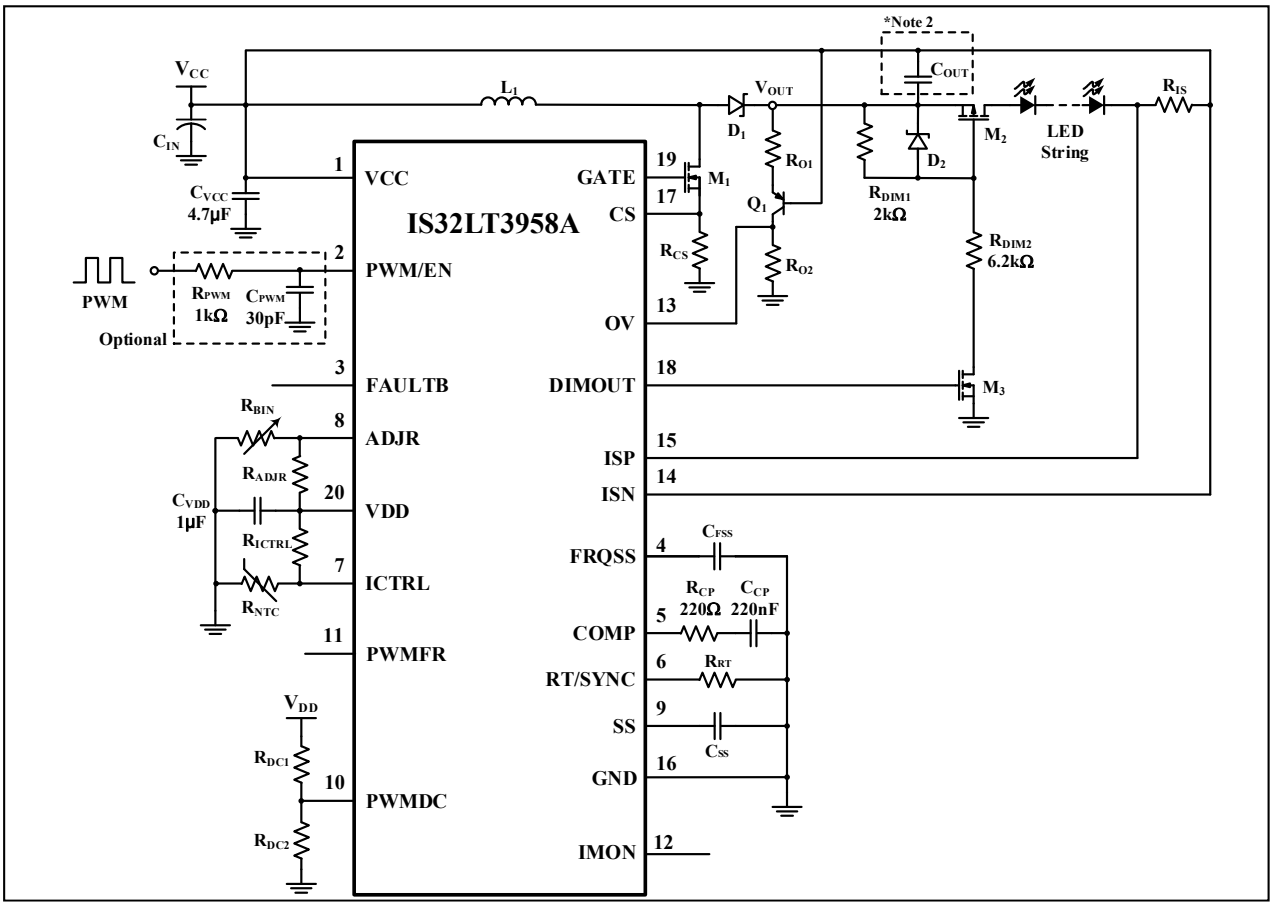


Figure 3 Typical Application Circuit with External PWM Dimming (Buck-Boost Configuration)

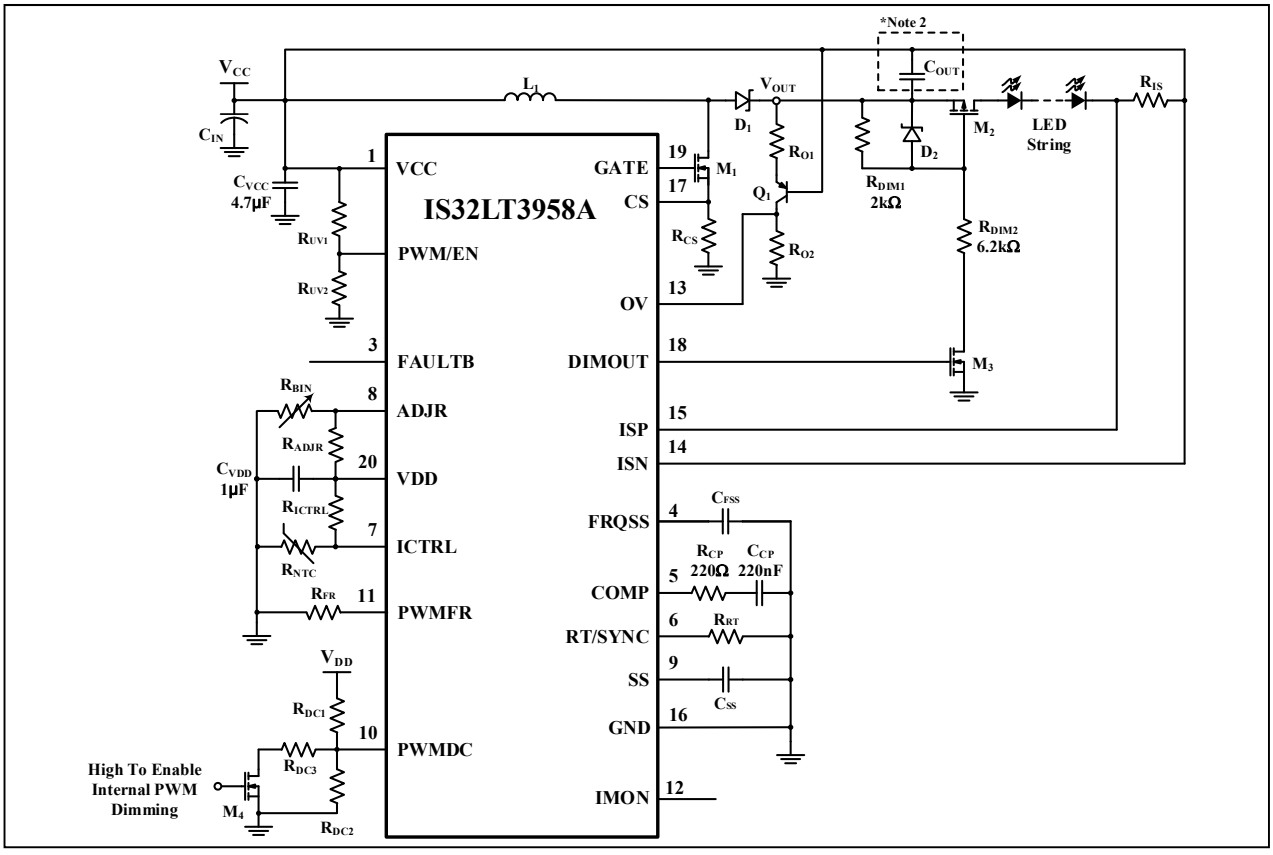


Figure 4 Typical Application Circuit With Internal PWM Dimming (Buck-Boost Configuration)

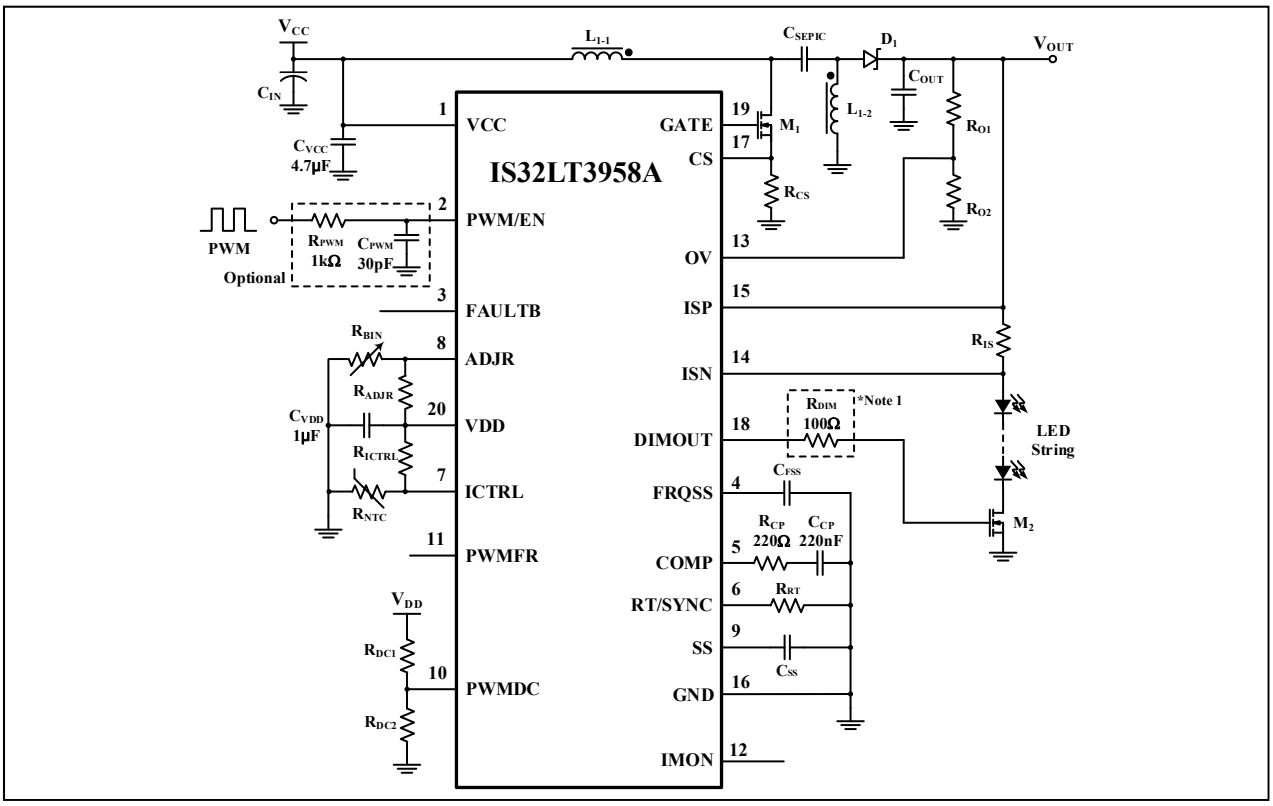


Figure 5 Typical Application Circuit with External PWM Dimming (SEPIC Configuration)

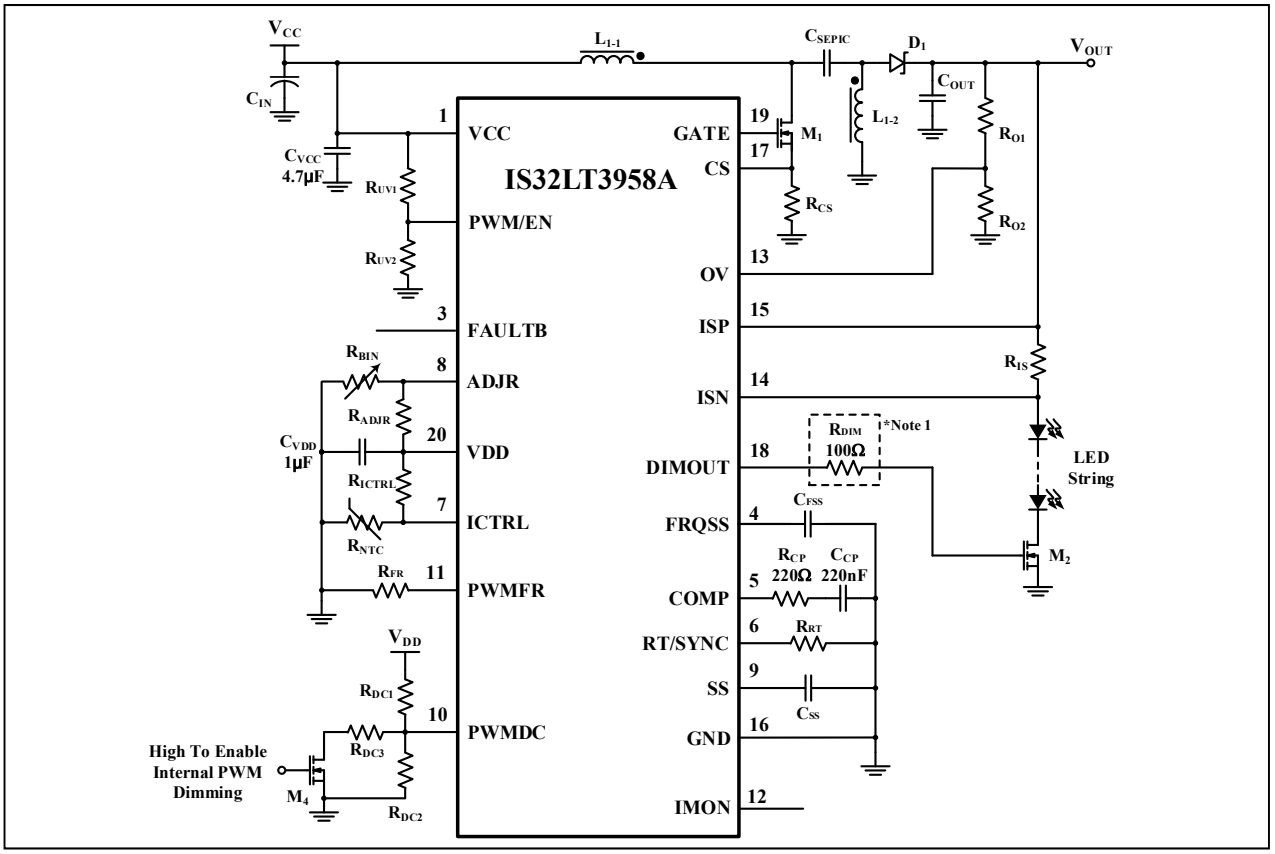


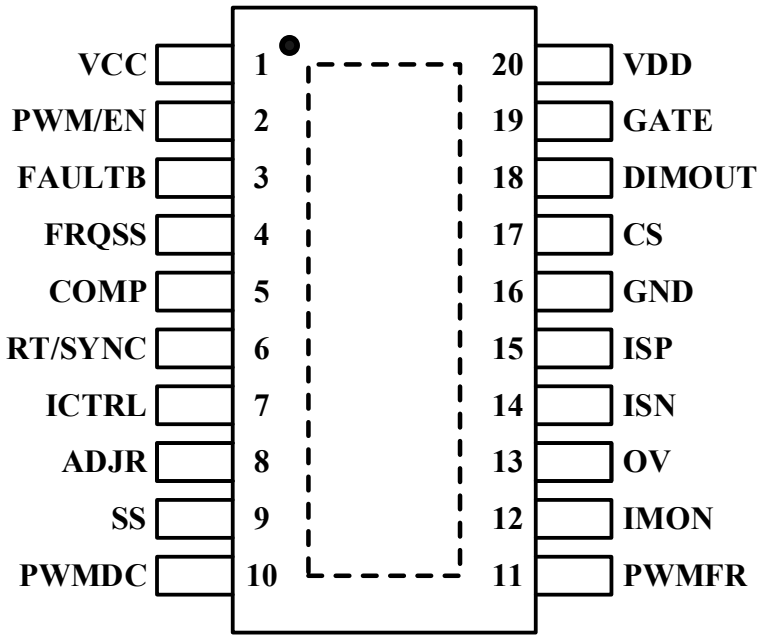
Figure 6 Typical Application Circuit With Internal PWM Dimming (SEPIC Configuration)

Note 1: R_{DIM} is essential for boost and SEPIC configurations; it MUST be a fixed 100Ω, do not change this value.

Note 2: For buck-boost configuration, C_{OUT} MUST be placed close to C_{IN}.

Note 3: R_{PWM} and C_{PWM} are optional. If PWM dimming is not required, the PWM/EN pin should be tied to VCC via a resistor (recommended value is 10kΩ). If PWM dimming is used, this RC filter is recommended and should be placed close to the PWM/EN pin to prevent noise coupling.

PIN CONFIGURATION

Package	Pin Configurations (Top View)
eTSSOP-20	

PIN DESCRIPTION

No.	Pin	Function
1	VCC	The power supply pin.
2	PWM/EN	External PWM dimming and enable pin. Pull high to enable and pull low to disable IC. Pulling low for over t_{DELAY} will force the IC into low current standby mode. Connecting a resistor divider from VCC to GND can be used to set an additional undervoltage lockout threshold. Apply an external PWM signal with biased above V_{EN_IH} on this pin to achieve PWM dimming. Do not allow this pin to float. Connect it to VCC via a resistor (recommended value is 10kΩ) if not used.
3	FAULTB	Open drain fault reporting pin. Active low to report a fault condition. Connect a resistor (recommended value is 47kΩ) between this pin and the required logic level voltage.
4	FRQSS	Spread spectrum frequency setting pin. Connect a capacitor from this pin to ground to set the dither frequency. Connect this pin directly to ground to disable this function.
5	COMP	Loop compensation pin.
6	RT/SYNC	An external resistor to ground on this pin sets the operating frequency. This pin can also be used to synchronize two or more IS32LT3958A in the system. Apply an external clock signal to this pin on two or more ICs for frequency synchronization.
7	ICTRL	Analog dimming pin. The analog dimming range is 0.06V~2V. The output is full current when the pin voltage is between 5V>V_{ICTRL}>2V and zero current when V_{ICTRL} <0.06V. Analog dimming is achieved when this pin voltage varies between 0.06V< V_{ICTRL}<2V. Recommend a 10nF X7R type capacitor close to this pin for noise decoupling. Do not allow this pin to float. When it's connected to VDD, a resistor divider is needed to keep the pin voltage below 5V.
8	ADJR	Analog dimming pin which has identical function as ICTRL pin.
9	SS	Soft-start time programming pin. Connect a capacitor from this pin to GND to set the soft-start time. Do not allow this pin to float.
10	PWMDC	Internal PWM generator duty cycle setting pin. Apply a DC voltage between 0V and 3V to enable the internal PWM generator and set the duty cycle of the internal PWM dimming. Apply a DC voltage between 3V and 5V to disable the internal PWM generator. Do not allow this pin to float. When it's connected to VDD, a resistor divider is needed to keep the pin voltage below 5V.
11	PWMFR	Internal PWM generator frequency programming pin. Connect a resistor from this pin to GND to set the frequency of the internal PWM generator.
12	IMON	Output current reporting pin. The output current is sensed by ISN/ISP input. V_{IMON}=8x(V_{ISP}-V_{ISN}). If not used, leave it floating.
13	OV	Output voltage detection pin. Connect a resistor divider from output voltage to GND to set output overvoltage and undervoltage protection thresholds.
14	ISN	The LED current sense amplifier negative input.
15	ISP	The LED current sense amplifier positive input.
16	GND	Ground pin.
17	CS	External NMOS switch current sense for control loop and overcurrent protection. Connect a resistor from this pin to ground.
18	DIMOUT	Buffer of PWM signal for driving LED string disconnect NMOS to achieve better PWM dimming. High voltage level is determined by internal LDO VDD voltage. This pin also serves in fault protection function. Leave this pin floating if not used.
19	GATE	Gate drive to the external power NMOS. Switches between VDD and GND.
20	VDD	Internal LDO output, needs an external low ESR capacitor (fixed value 1μF) placed close to this pin. This pin is not meant to power any external circuit.
	Thermal Pad	MUST be soldered to a large size GND copper plane.

ORDERING INFORMATION
Automotive Range: -40°C to +125°C

Order Part No.	Package	QTY/Reel
IS32LT3958A-ZLA3-TR	eTSSOP-20, Lead-free	2500

ABSOLUTE MAXIMUM RATINGS

Voltage at VCC, PWM/EN, ISP, ISN, FAULTB pins	-0.3V ~ +75V
Voltage at GATE, VDD, DIMOUT pins	-0.3V ~ +15V
Voltage at COMP, RT/SYNC, ICTRL, OV, CS, FRQSS, SS, PWMFR, IMON, PWMDC, ADJR pins	-0.3V ~ +7V
Operating temperature, T_A=T_J	-40°C ~ +150°C
Maximum operating junction temperature, T_{JMAX}	+150°C
Device storage temperature, T_{STG}	-65°C ~ +150°C
Maximum power dissipation, P_{DMAX}	4.1W
Package thermal resistance, junction to ambient (4-layer standard test PCB based on JESD 51-2A), θ_{JA}	30.5°C/W
Package thermal resistance, junction to thermal PAD (4-layer standard test PCB based on JESD 51-8), θ_{JP}	14.46°C/W
ESD (HBM) ESD (CDM)	±2kV ±750V

Note 4: Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

The specifications are at T_J= T_A= -40°C ~ +150°C, V_{CC}= 12V, unless otherwise noted. Typical values are at T_J= T_A= 25°C. (Note 5)

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
V_{CC}	Input voltage range			5		70	V
I_{CC}	Quiescent current	V_{ICTRL}= 0V			2.5	4	mA
I_{SD}	Shutdown current	$V_{PWM/EN}$= 0V for t_{DELAY}			44	80	μA
V_{UVLO_F}	Undervoltage lock out falling threshold			3.8	4.25	4.7	V
V_{UVLO_R}	Undervoltage lock out rising threshold					4.9	V
V_{UVLO_HY}	Undervoltage lock out hysteresis				250		mV
V_{DD}	Internal regulator output voltage			6.4	6.6	6.8	V
I_{MAX_LDO}	VDD pin maximum drive current	VDD drops less than 1V		18			mA
V_{CS_TH}	Power NMOS current limit threshold			180	200	220	mV
V_{IS_COM}	Output current sense common mode voltage	ISP/ISN pin to GND voltage		5		70	V
V_{SENSE}	Output current sense threshold (V_{ISP}-V_{ISN})	V_{ADJR}=2.5V, V_{ICTRL}=2.5V	T_J= 25°C	247	250	253	mV
			T_J= -40°C~150°C	243	250	257	
V_{SENSE_ADIM}	Output current sense threshold (V_{ISP}-V_{ISN}) with analog dimming down to 10% level	V_{ADJR} and V_{ICTRL} driven by resistor divider from VDD pin	V_{ADJR}=2.5V, V_{ICTRL}=0.2V, T_J= 25°C	24	25	26	mV
			V_{ADJR}=2.5V, V_{ICTRL}=0.2V, T_J= -40°C~150°C	19	25	29	
			V_{ADJR}=0.2V, V_{ICTRL}=2.5V, T_J= 25°C	24	25	26	
			V_{ADJR}=0.2V, V_{ICTRL}=2.5V, T_J= -40°C~150°C	20	25	28	

ELECTRICAL CHARACTERISTICS (CONTINUE)

The specifications are at T_J= T_A= -40°C ~ +150°C, V_{CC}= 12V, unless otherwise noted. Typical values are at T_J= T_A= 25°C. (Note 5)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Fault Protection						
V_{FAULTB_LOW}	FAULTB pull low voltage	Fault condition, sink current I_{OL}= 1mA		200	400	mV
I_{FAULTB_LK}	FAULTB pin leakage current	No fault condition, FAULTB pin pulled up to 24V			1	μA
V_{SENSE_OC}	Output overcurrent threshold (V_{ISP}-V_{ISN})		450	500	550	mV
t_{SKIP}	Output undervoltage and overcurrent skip time			32	50	ms
V_{OVP_TH}	Overvoltage protection threshold	Voltage rising	1.164	1.2	1.236	V
I_{OVP_HY}	OVP hysteresis current		14.2	20	33	μA
V_{UVD_TH}	Undervoltage detection threshold		70	100	130	mV
t_{UVD_BLK}	Undervoltage detection blanking period	(Note 6)		4		μs
T_{SD}	Thermal shutdown protection	(Note 6)		165		°C
T_{SD_HY}	Thermal shutdown hysteresis	(Note 6)		15		°C
Gate Driver						
t_{R_GATE}	GATE pin rise time	10%×V_{MAX} to 5V, C_{GATE}= 3.3nF		25	60	ns
t_{F_GATE}	GATE pin fall time	90%×V_{MAX} to 10%×V_{MAX}, C_{GATE}= 3.3nF		25	60	ns
t_{MIN_ON}	GATE minimum on time			150	240	ns
t_{R_DIMOUT}	DIMOUT pin rise time	10%×V_{MAX} to 5V, C_{DIMOUT}= 1nF		140	200	ns
t_{F_DIMOUT}	DIMOUT pin fall time	90%×V_{MAX} to 10%×V_{MAX}, C_{DIMOUT}= 1nF		120	180	ns
Oscillator						
f_{SWR}	Operating frequency range		100		1000	kHz
$V_{RT/SYNC}$	RT/SYNC pin voltage			1		V
f_{SW}	Operating frequency	R_{RT}= 215kΩ	80	100	120	kHz
		R_{RT}= 50kΩ	340	400	460	
		R_{RT}= 18kΩ	850	1000	1150	
D_{MAX}	Maximum operating duty cycle		88	90		%
f_{SY}	Synchronized PWM frequency		250		500	kHz
t_{SY_OFF}	Synchronization input minimum off-time		200			ns
t_{SY_ON}	Synchronization input minimum on-time		200			ns
V_{SY_H}	Synchronization input logic high	(Note 6)	2.5			V
V_{SY_L}	Synchronization input logic low	(Note 6)			0.8	V

ELECTRICAL CHARACTERISTICS (CONTINUE)

The specifications are at T_J= T_A= -40°C ~ +150°C, V_{CC}= 12V, unless otherwise noted. Typical values are at T_J= T_A= 25°C. (Note 5)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{FRQSS}	FRQSS charging current	(Note 6)		10		μA
	FRQSS discharging current	(Note 6)		10		μA
R_{FRQSS}	Spread spectrum frequency range	(Note 6)		±10		%
Inputs Parameter						
V_{EN_IH}	PWM/EN input high threshold	Voltage rising	1.164	1.2	1.236	V
V_{EN_IL}	PWM/EN input low threshold	Voltage falling	1.008		1.092	V
V_{EN_HY}	PWM/EN input hysteresis			150		mV
t_{DELAY}	The low voltage delay time on PWM/EN pin to enter shutdown mode			32	50	ms
V_{ADJR_RG}	ADJR analog dimming range		0.06		2	V
V_{ADJR_FU}	ADJR analog dimming full on threshold		2.1			V
V_{ADJR_OFF}	ADJR force output off threshold		0.03	0.06		V
R_{IADJR}	ADJR input current limiting series resistor	V_{ADJR}> 2V		24		kΩ
V_{ICTRL_RG}	ICTRL analog dimming range		0.06		2	V
V_{ICTRL_FU}	ICTRL analog dimming full on threshold		2.1			V
V_{ICTRL_OFF}	ICTRL force output off threshold		0.03	0.06		V
Output Current Monitor						
I_{IMON_SC}	IMON source current	(V_{ISP}-V_{ISN})= 250mV, V_{IMON}= 0V		140		μA
V_{IMON_CLP}	IMON output voltage clamp		3.10	3.35	3.75	V
V_{IMON_OS}	IMON buffer offset voltage	(Note 6)	-9		9	mV
V_{IMON}	IMON buffer output voltage	(V_{ISP}-V_{ISN})= 250mV	1.92	2	2.08	V
Soft-Start						
I_{SS}	SS pin source current			10		μA
V_{SS_EN}	Soft-start voltage threshold to enable output undervoltage detection			2		V
V_{SS_RST}	SS pin reset voltage			100		mV
Internal PWM Generator						
V_{PWMFR}	PWMFR pin voltage			0.8		V
f_{INTPWM}	Internal PWM frequency	R_{FR}= 66.7kΩ	270	300	330	Hz
V_{PWMDC_RG}	PWMDC pin voltage range to enable internal PWM generator		0		3	V
V_{PWMDC_FU}	PWMDC 100% PWM duty cycle threshold		3.1			V

ELECTRICAL CHARACTERISTICS (CONTINUE)

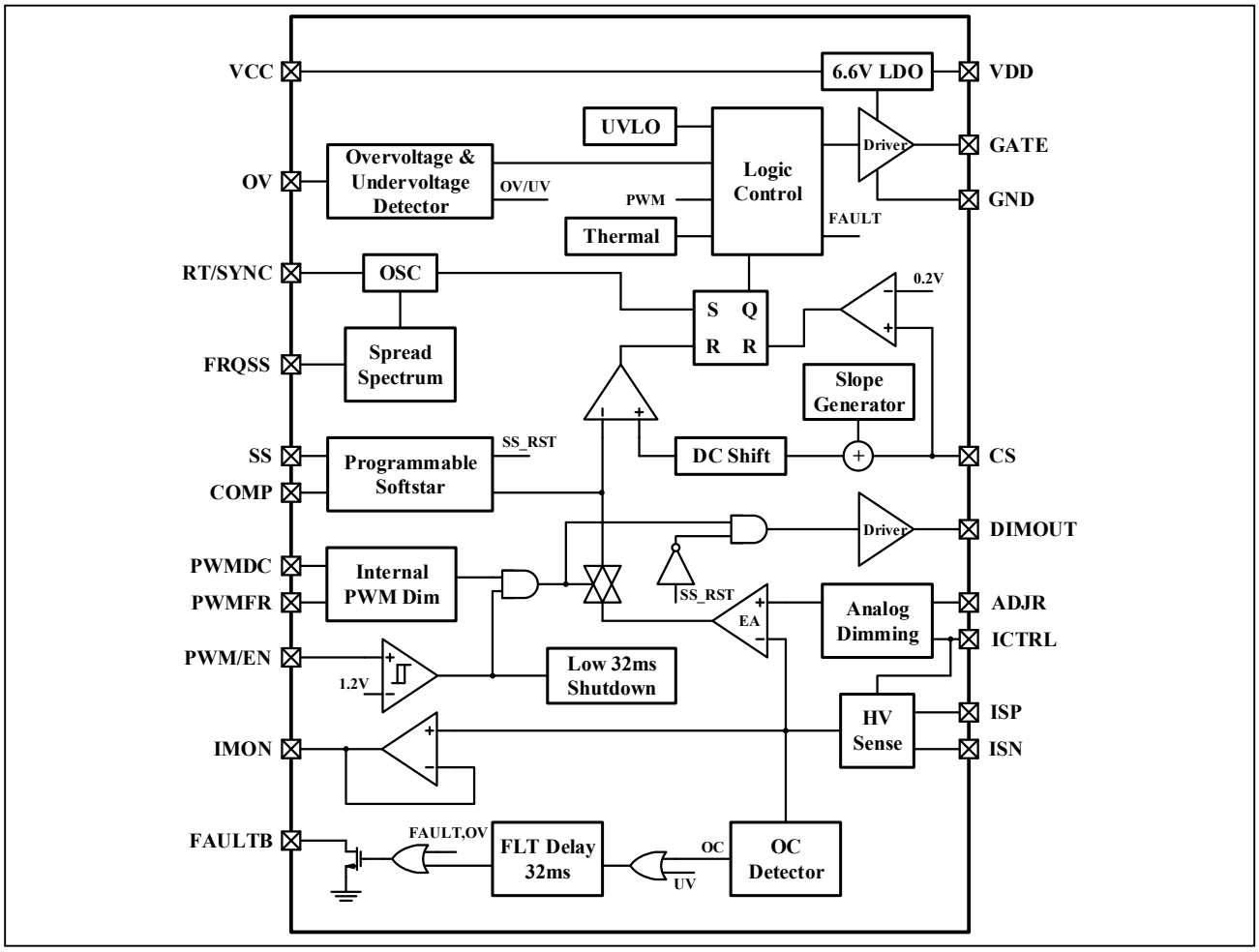
The specifications are at T_J= T_A= -40°C ~ +150°C, V_{CC}= 12V, unless otherwise noted. Typical values are at T_J= T_A= 25°C. (Note 5)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
D_{PWM}	Internal PWM duty cycle	V_{PWMDC} driven by resistor divider from VDD pin, V_{PWMDC}= 0.15V, f_{INTPWM}= 300Hz	4.5	5	5.5	%
		V_{PWMDC} driven by resistor divider from VDD pin, V_{PWMDC}= 1.5V, f_{INTPWM}= 300Hz	47	50	53	%
		V_{PWMDC} driven by resistor divider from VDD pin, V_{PWMDC}= 2.7V, f_{INTPWM}= 300Hz	87	90	93	%

Note 5: All parts are production tested at T_J= -40°C, 25°C and +150°C, unless otherwise noted. Other temperature limits are guaranteed by design.

Note 6: Guaranteed by design.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL OPERATING CHARACTERISTICS

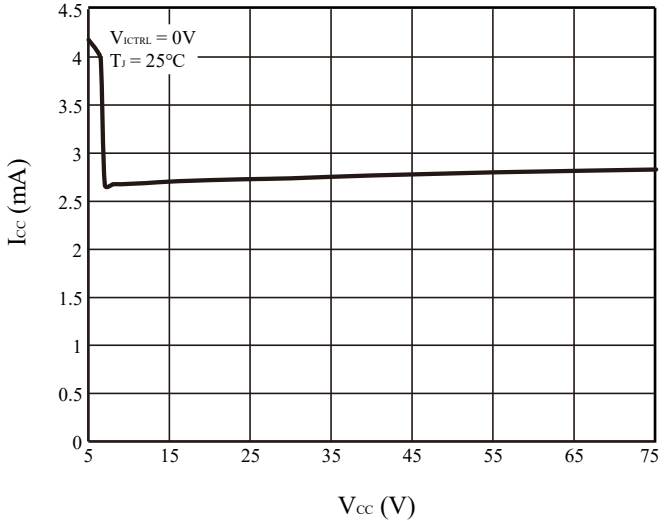


Figure 7 I_{CC} vs. V_{CC}

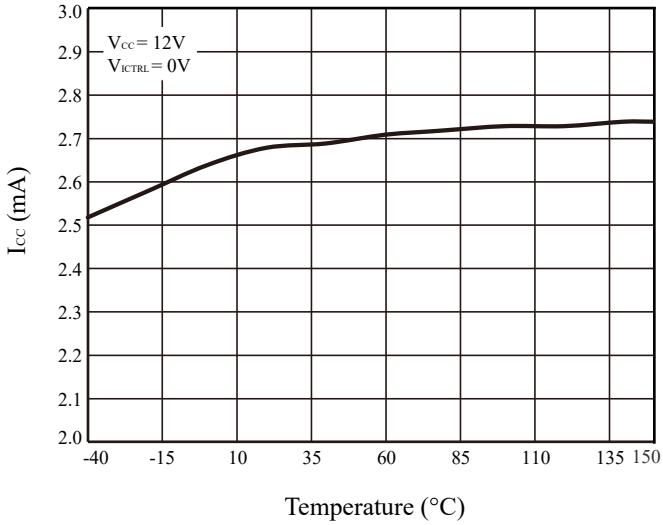


Figure 8 I_{CC} vs. Temperature

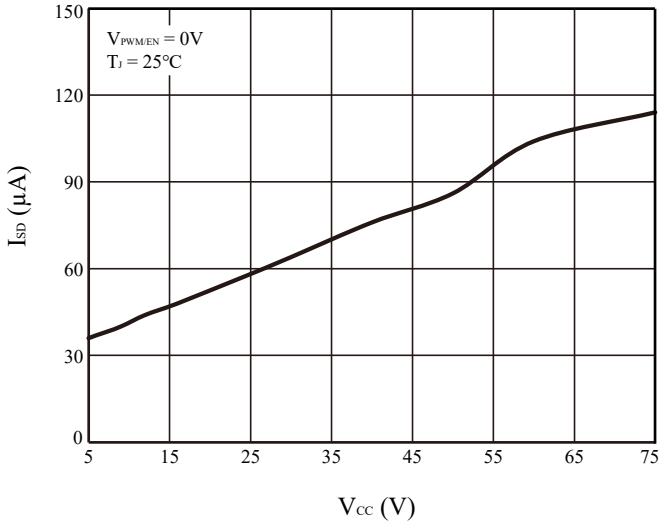


Figure 9 I_{SD} vs. V_{CC}

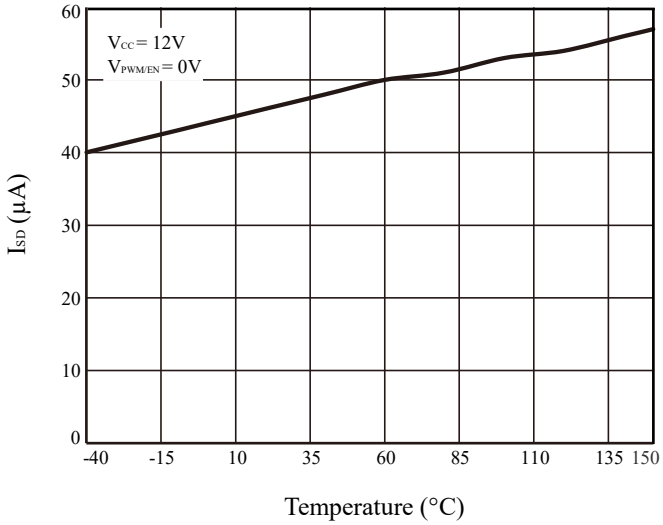


Figure 10 I_{SD} vs. Temperature

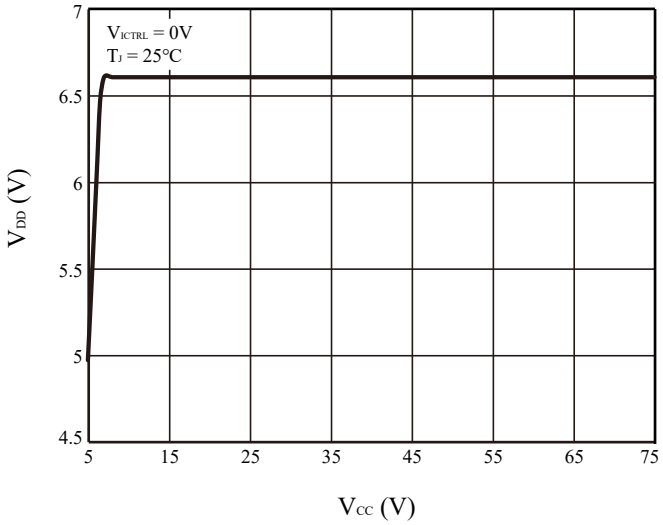


Figure 11 V_{DD} vs. V_{CC}

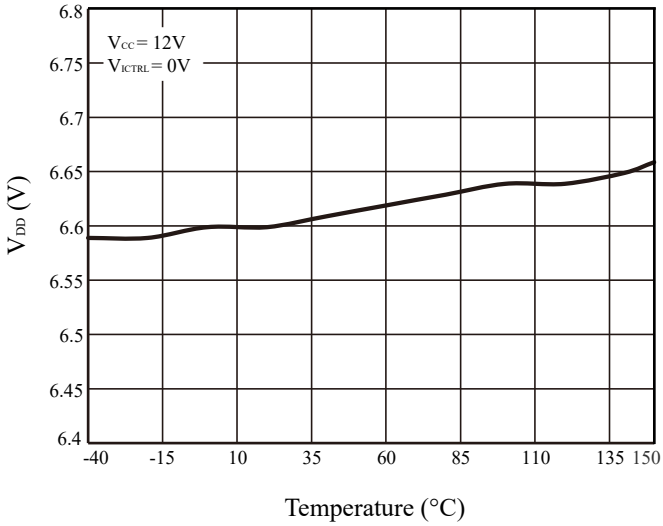


Figure 12 V_{DD} vs. Temperature

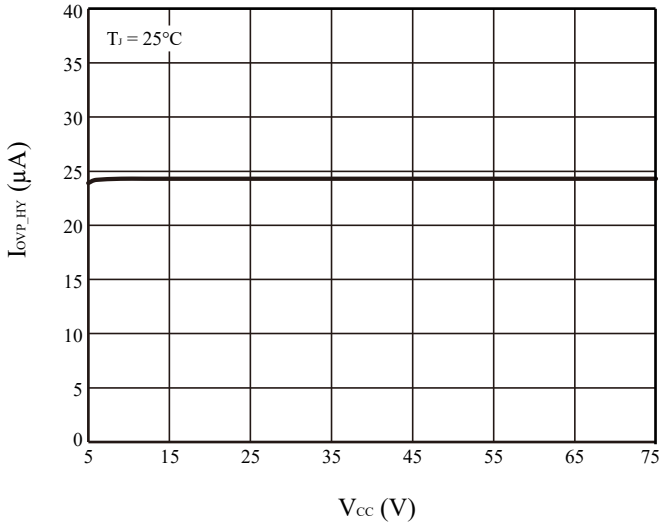


Figure 13 I_{OVP_HY} vs. V_{CC}

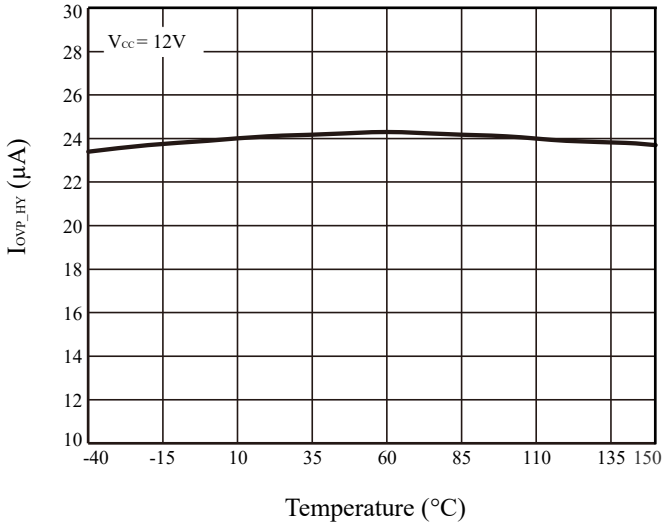


Figure 14 I_{OVP_HY} vs. Temperature

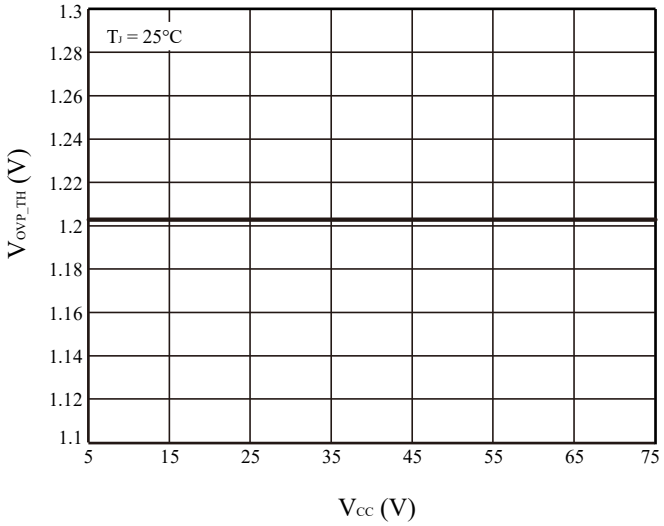


Figure 15 V_{OVP_TH} vs. V_{CC}

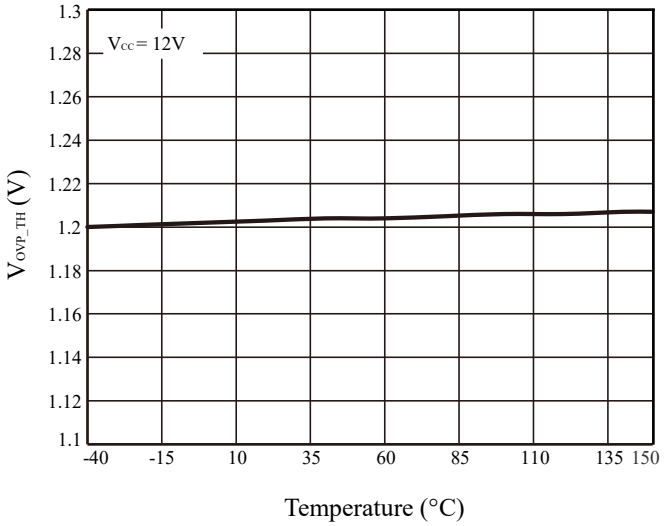


Figure 16 V_{OVP_TH} vs. Temperature

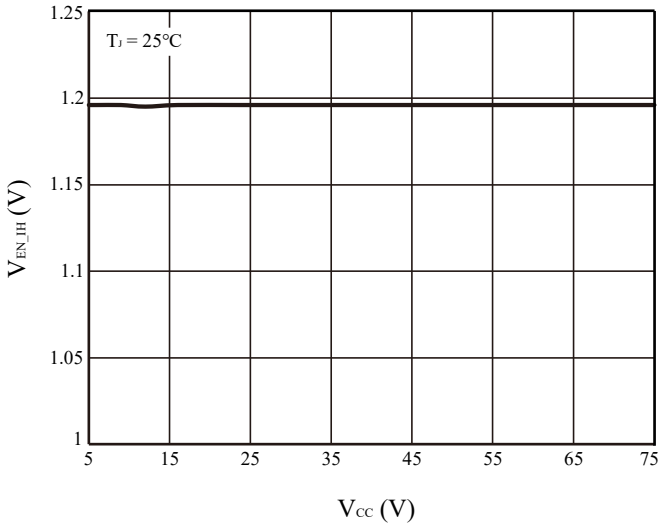


Figure 17 V_{EN_IH} vs. V_{CC}

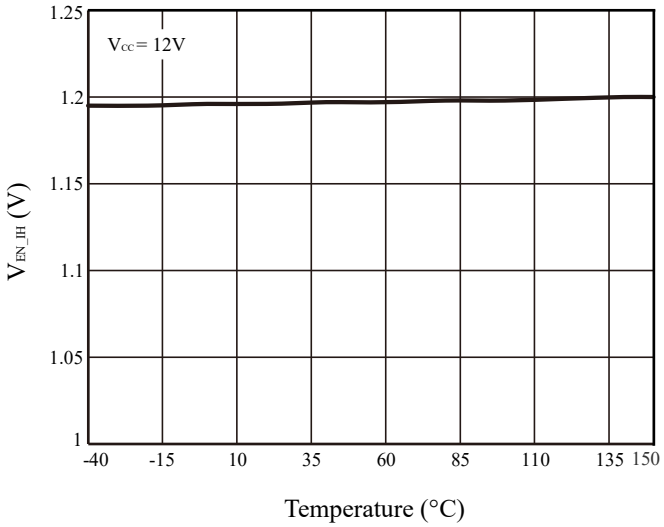


Figure 18 V_{EN_IH} vs. Temperature

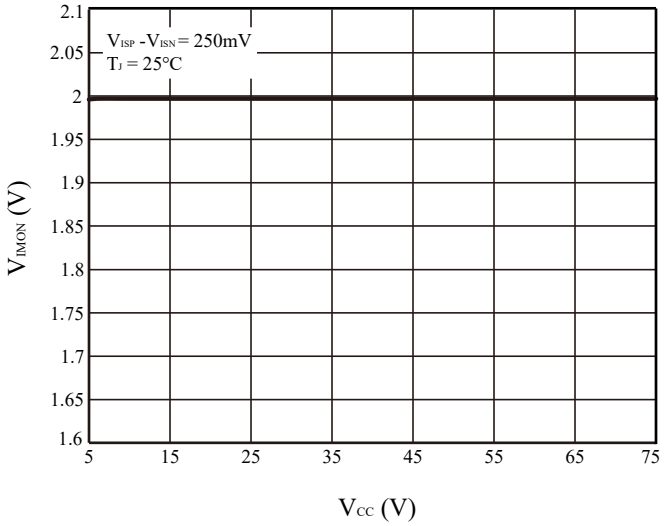


Figure 19 V_{IMON} vs. V_{CC}

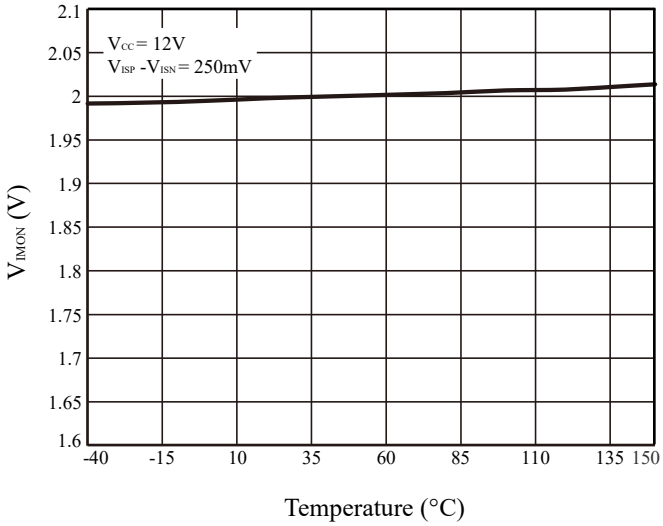


Figure 20 V_{IMON} vs. Temperature

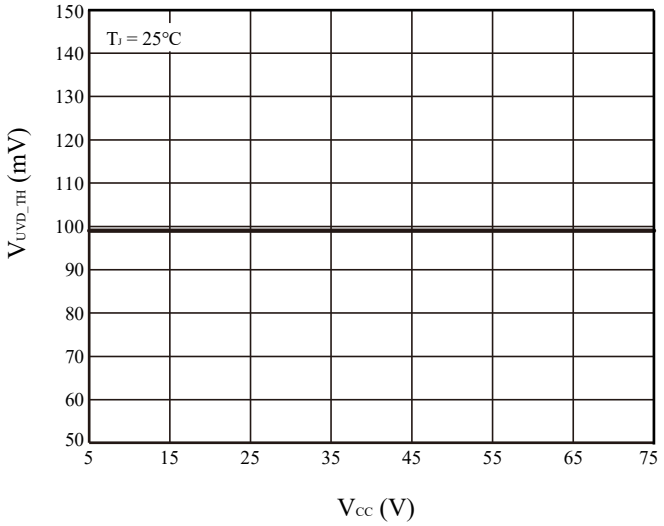


Figure 21 V_{UVD_TH} vs. V_{CC}

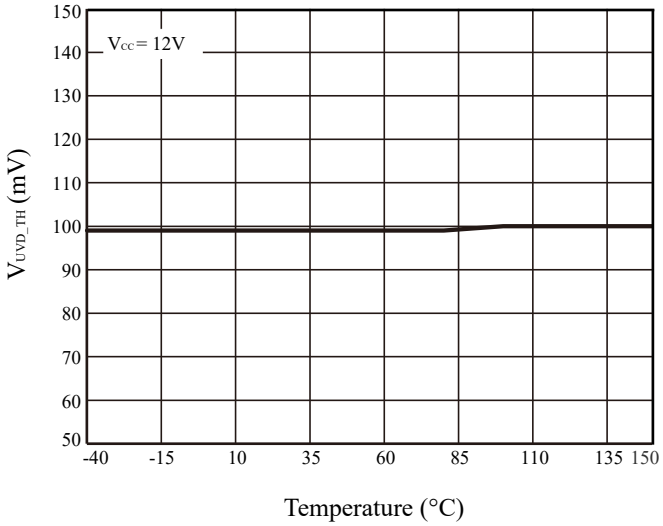


Figure 22 V_{UVD_TH} vs. Temperature

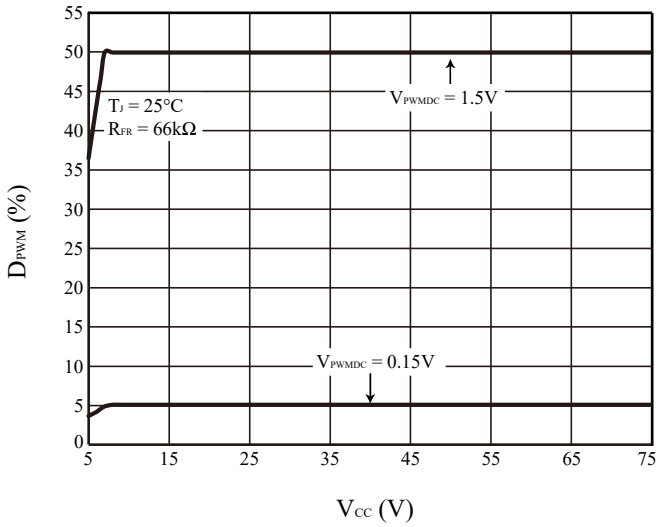


Figure 23 D_{PWM} vs. V_{CC}

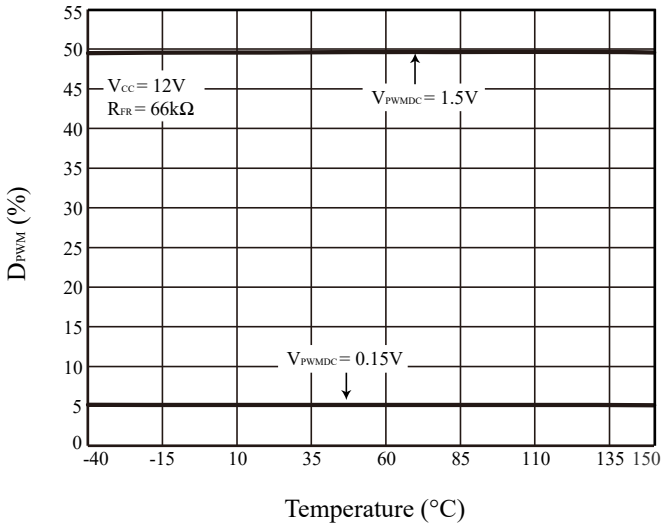


Figure 24 D_{PWM} vs. Temperature

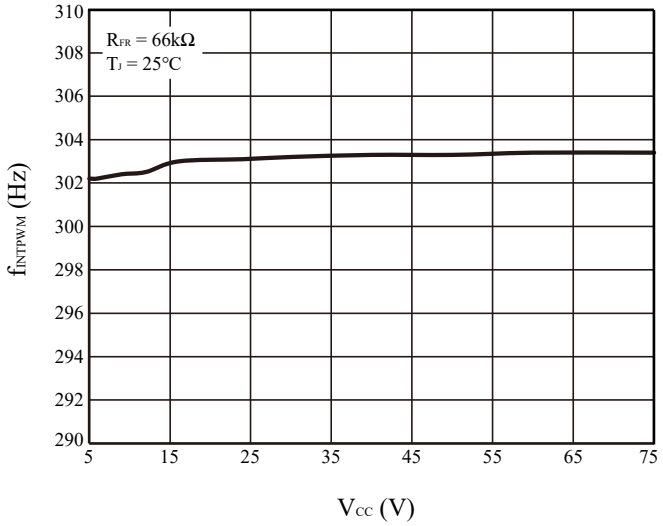


Figure 25 f_{INTPWM} vs. V_{CC}

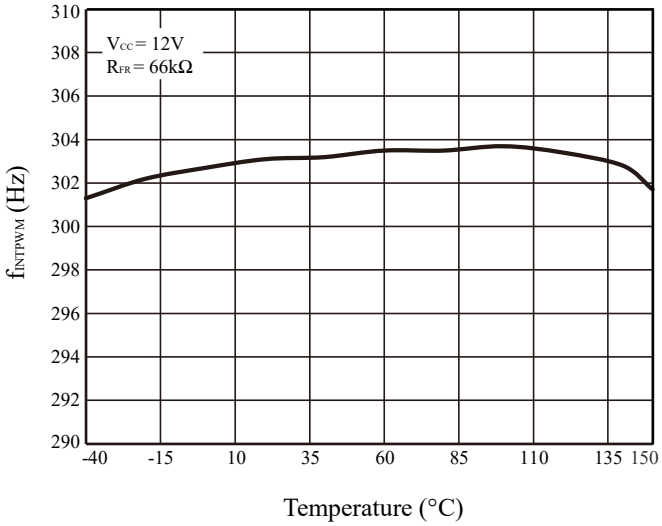


Figure 26 f_{INTPWM} vs. Temperature

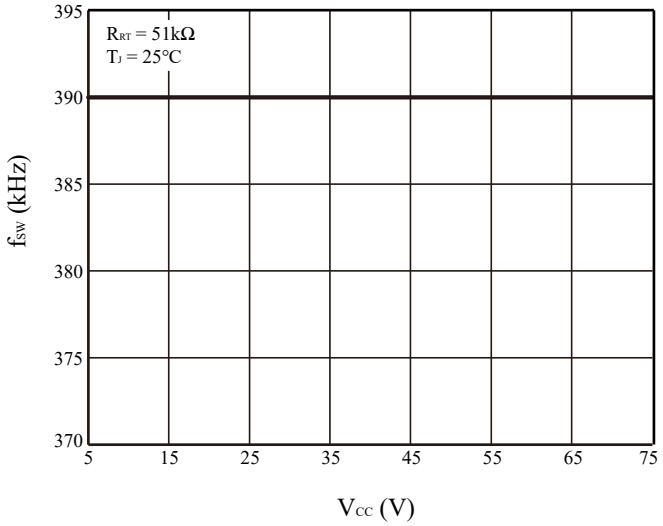


Figure 27 f_{SW} vs. V_{CC}

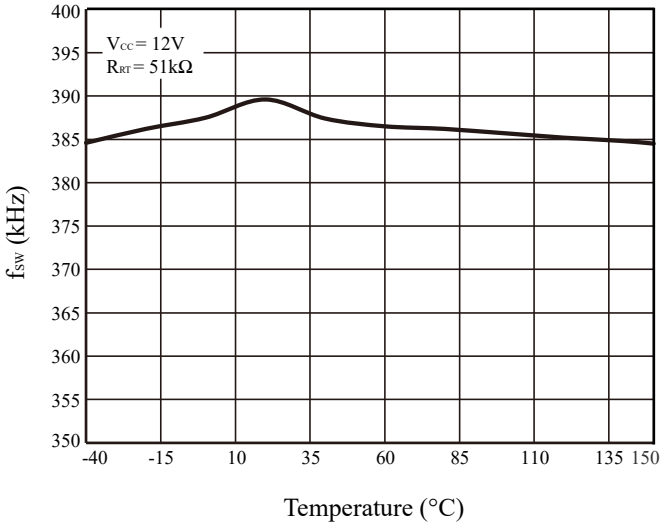


Figure 28 f_{SW} vs. Temperature

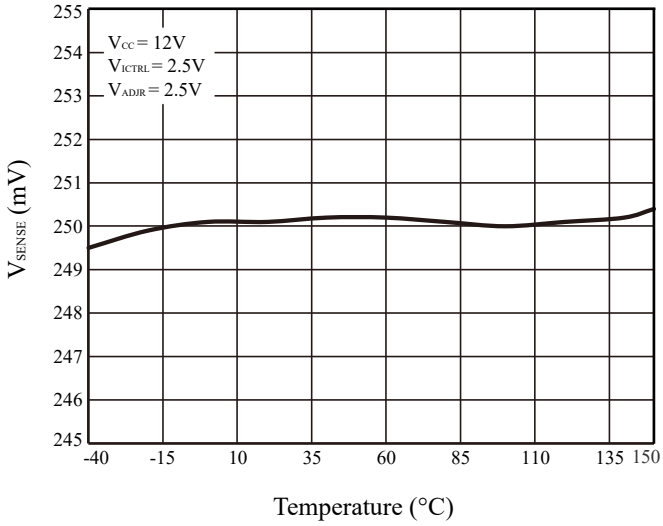


Figure 29 V_{SENSE} vs. Temperature

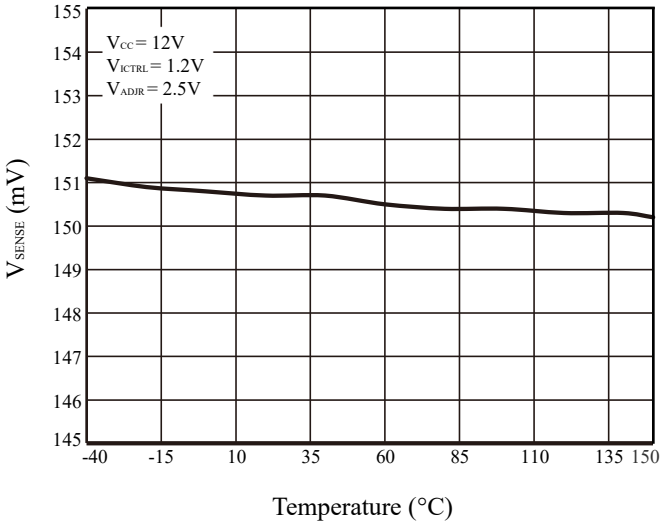


Figure 30 V_{SENSE} vs. Temperature (ICTRL Dimming)

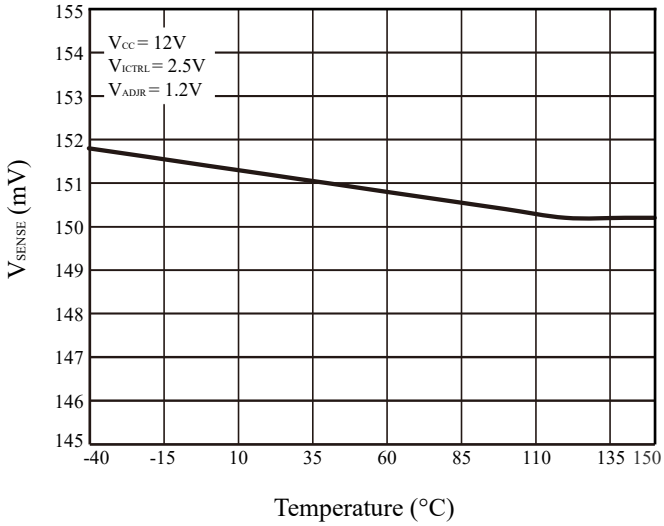


Figure 31 V_{SENSE} vs. Temperature (ADJR Dimming)

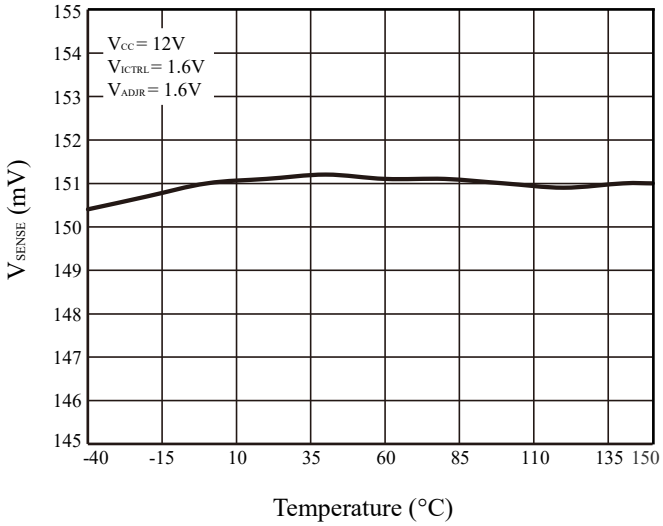


Figure 32 V_{SENSE} vs. Temperature (ICTRL and ADJR Dimming)

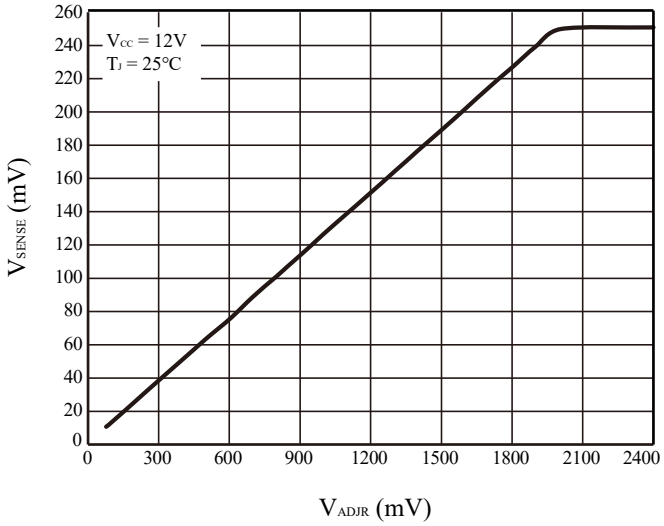


Figure 33 V_{SENSE} vs. V_{ADJR}

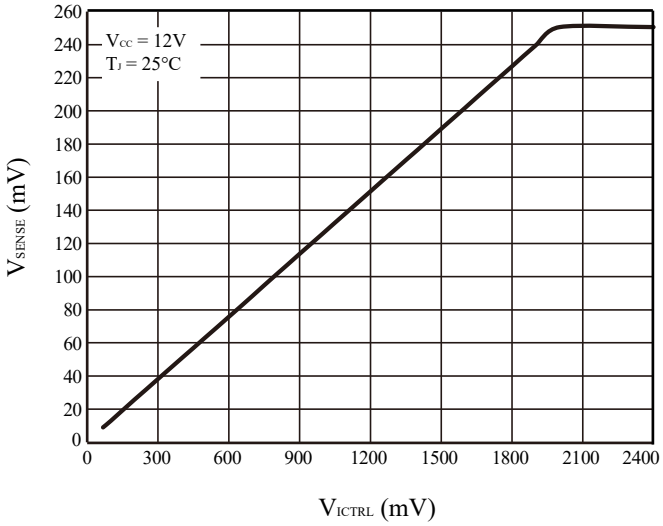


Figure 34 V_{SENSE} vs. V_{ICTRL}

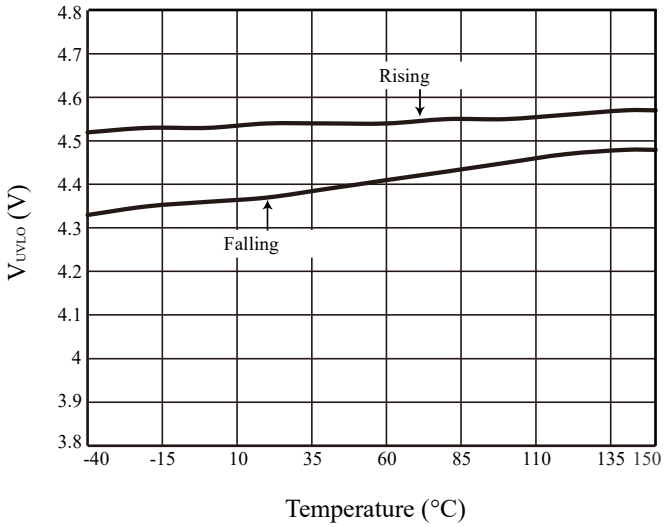


Figure 35 V_{UVLO} vs. Temperature

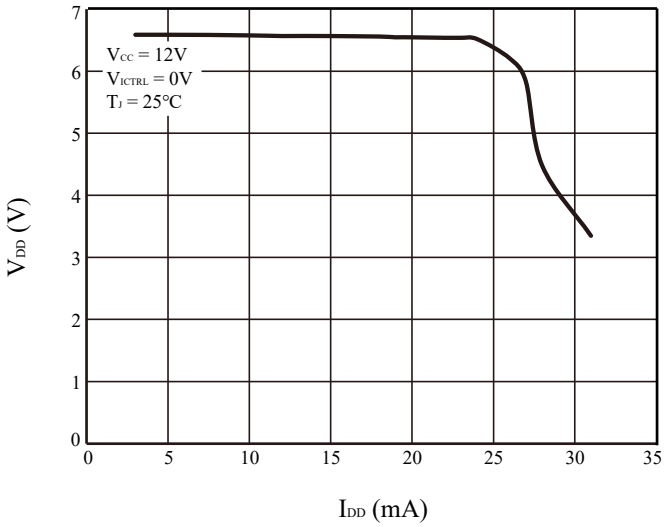


Figure 36 V_{DD} vs. I_{DD}

APPLICATION INFORMATION

The IS32LT3958A is a constant frequency, current mode PWM controller designed for high current LED applications. The low side gate driver can drive the external NMOS in the 100kHz~1MHz frequency range, which is set by a single resistor connected to RT/SYNC pin. The frequency can be dithered for spread spectrum function by connecting a capacitor from FRQSS pin to GND. The LED current is programmable with one external current sense resistor between ISP and ISN pins. The device supports analog dimming, internal PWM dimming and external PWM dimming methods. The IS32LT3958A is ideal for boost, buck-boost, SEPIC and buck operation.

VCC UVLO

The device features the undervoltage lockout (UVLO) function on VCC pin. It is an internally fixed value which cannot be adjusted. The device is enabled when the VCC voltage rises to exceed V_{UVLO_R}, and disabled when the VCC voltage falls below V_{UVLO_F}.

Besides this internal, fixed UVLO, it may be desirable to externally set a higher UVLO threshold for some applications. A precise UVLO threshold voltage can be set by using a resistor voltage divider between VCC and GND with the center connected to the PWM/EN pin.

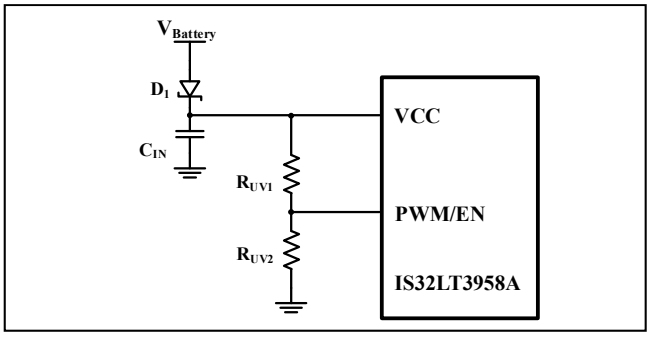


Figure 37 External UVLO for VCC

The external UVLO threshold voltage can be computed by the following Equations:

$$V_{UVLO\_EXTR} = V_{EN\_IH} \times \frac{R_{UV1} + R_{UV2}}{R_{UV2}} \quad (1)$$

$$V_{UVLO\_EXTF} = V_{EN\_IL} \times \frac{R_{UV1} + R_{UV2}}{R_{UV2}} \quad (2)$$

The device is enabled when the V_{CC} voltage exceeds V_{UVLO_EXTR}, and disabled when the V_{CC} voltage falls below V_{UVLO_EXTF}.

It is recommended that R_{UV1} and R_{UV2} be 1% accuracy resistors with good temperature characteristics to ensure a precise detection. On the PCB layout, this resistor divider must be placed as close as possible to the PWM/EN pin to avoid noise coupling into the UVLO detection.

LINEAR REGULATOR VDD

The device integrates a linear regulator (VDD) with I_{MAX_LDO} current capability to power only the GATE and DIMOUT pins and drive the external low side NMOS switches with 6.6V (Typ.). During operation, the external NMOS will draw transient high current from this linear regulator. Therefore, a 1μF low ESR, X7R type ceramic capacitor is necessary from VDD pin to GND; it must be placed as close to VDD pin as possible. VDD is the output of the internal linear regulator and it's not recommended to be driven by an external power supply. This regulator also has the UVLO feature whose voltage threshold is identical with VCC UVLO. When the VDD voltage drops below V_{UVLO_F}, the GATE and DIMOUT will be turned off and will be turned on once the voltage exceeds V_{UVLO_R}. This helps protect the external NMOS from excessive power consumption due to insufficient gate driving voltage.

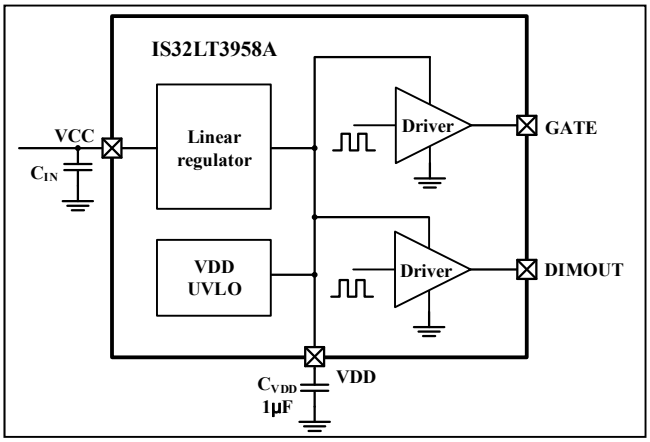


Figure 38 Linear Regulator

An I_{MAX_LDO} current limit on VDD pin protects the IS32LT3958A from excessive power dissipation at high input voltage. Should the VDD pin be externally pulled below 1.4V (Typ.), the IS32LT3958A will be disabled and the FAULTB pin will be pulled low to report the fault condition until VDD rises above 1.4V (Typ.). Most of the VDD current will be supplied to the GATE pin to drive power switching NMOS. The driving current can be calculated from the following Equation (3):

$$I_{GATE} = f_{SW} \times Q_G \quad (3)$$

Where f_{SW} is operating frequency of IS32LT3958A and Q_G is the total gate charge of power NMOS.

Choosing a power NMOS with lower Q_G will improve the efficiency and allow higher switching frequency. It is important to consider the NMOS threshold voltage when operating in the dropout region when the input voltage (V_{CC}) is below the VDD regulation level. Recommend a logic level power NMOS with a threshold voltage below 3V when the device is required to operate at an input voltage less than 6V.

VDD can be used to bias external low current circuitry

requiring a reference supply, such as in conjunction with the resistor divider to set voltage level for ICTRL, ADJR and PWMDC pins. However, to ensure stable operation of the IS32LT3958A, please do not power any external device with VDD.

ENABLE AND SHUTDOWN

The PWM/EN pin is an enable input for the device, pull it higher than V_{EN_IH} to enable the device; pull it lower than V_{EN_IL} for longer than t_{DELAY} to force the device into shutdown mode with an ultra-low shutdown current. The PWM/EN is a high impedance input pin. If unused, connect the PWM/EN pin to the VCC pin via a resistor (recommended value is 10kΩ).

SOFT-START

The IS32LT3958A provides a built-in soft-start function. The function of soft-start is made for suppressing the inrush current to an acceptable value at startup, fault protection and so on. The device clamps the COMP pin to the SS pin, separated by a diode, until LED current nears the regulation threshold. An internal 10μA soft-start current source turns on when the device releases from UVLO. The internal 10μA soft-start current source charges the capacitor C_{SS} on the SS pin causing the COMP pin voltage to gradually ramp up from GND, hence, the input peak current gradually ramps up following COMP pin voltage to the regulated threshold.

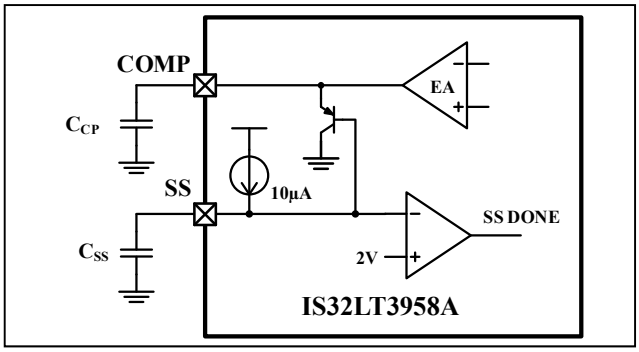


Figure 39 Soft-start Circuit

The soft-start time can be roughly calculated by the following Equation (4):

$$t_{SS} = \frac{C_{CP} \times 0.7V}{100\mu A} + \frac{C_{SS} \times 0.9V}{10\mu A} \qquad (4)$$

The C_{CP} is the capacitor connected to the COMP pin and the C_{SS} is the capacitor connected to the SS pin, whose value is in Farad. The recommended value of C_{SS} is 22nF~100nF.

The SS pin can also be pulled down by an external switch to stop switching. When the SS pin is externally driven to enable switching, the slew-rate on the COMP pin is controlled by the compensation capacitor. In this case, the startup duration and LED current transient is controlled by tuning the compensation network.

In the previous generation IS32LT3958, if PWM dimming is implemented during a soft-start, the C_{CP} and C_{SS} capacitors will be charged only during the PWM on phase and maintain their voltage during the PWM off phase. As a result, the soft-start time will be inversely proportional to the PWM duty cycle. A longer soft-start time is required with lower PWM duty cycles. When PWM dimming is used to achieve a fade on effect, the initial PWM duty cycle can be quite low, for example, less than 1%. As shown in Figure 40, for the IS32LT3958, the output current will be zero until the PWM duty cycle rises to a certain width due to the long soft-start time. This can degrade the fade on performance.

In order to improve this issue, the IS32LT3938A's soft-start function has been optimized. Specifically, up until the output current reaches 6.5% (Typ.) of the I_{LED}, the soft-start process will not be controlled by the PWM signal. This means that both the C_{CP} and C_{SS} capacitors will be charged regardless of whether the PWM signal is on or off. By shortening the soft-start time required for low PWM duty cycles, the output current can be quickly reached. As a result, the fade on performance of the IS32LT3958A is significantly better than that of the IS32LT3958.

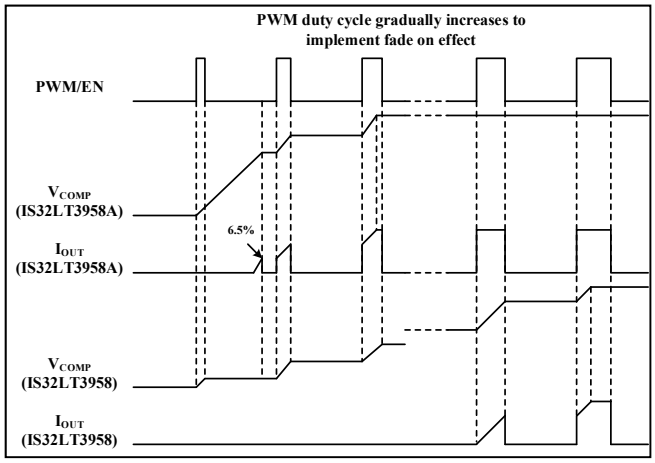


Figure 40 PWM Fade On of IS32LT3958 and IS32LT3958A

OPERATION FREQUENCY

The internal oscillator of the device is programmable from 100kHz to 1MHz range using a single resistor R_{RT} at RT/SYNC pin. Higher frequency operation results in smaller component size but increases the switching losses and power NMOS gate driving current and may not allow sufficiently high or low duty cycle. Lower frequency gives better performance but results in larger component size. To set a desired frequency, the resistor value can be calculated by following Equation (5):

$$R_{RT} = \frac{2.15 \times 10^4}{f_{SW}} - 3.7 \qquad (5)$$

Where R_{RT} is in kΩ. f_{SW} is the operation frequency in kHz. In automotive applications, an operation frequency of 400kHz is a good compromise between component size and efficiency. It also makes the system easier to filter switching noise from sensitive

frequency bands and pass EMI tests.

If the RT/SYNC pin is connected to an extremely low value resistor or accidently shorted to ground, the internal oscillation frequency will be over 1MHz. If it exceeds 2.5MHz, the internal circuit will detect it and turn off the power NMOS for protection. When this fault condition is removed, the frequency drops below 2.5MHz, and the operation will recover.

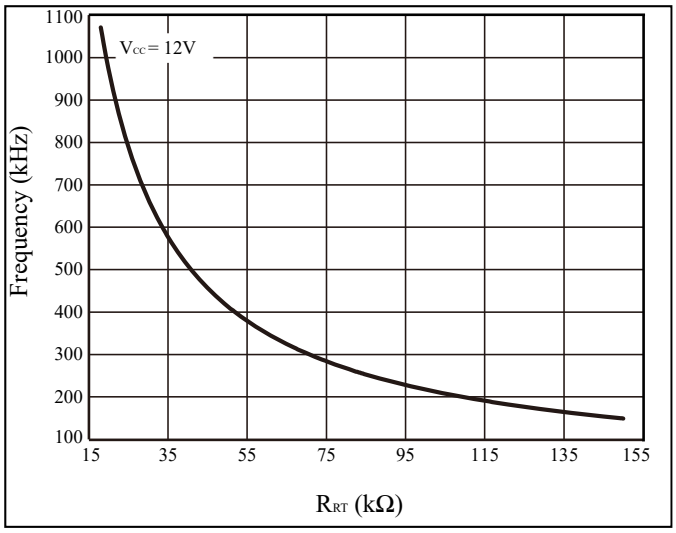


Figure 41 f_{SW} vs. R_{RT}

FREQUENCY SYNCHRONIZATION

The RT/SYNC pin can also be used as a synchronization input, allowing the IS32LT3958A to operate with an external clock in the range of 250kHz to 500kHz as long as it satisfies the requirements of t_{SY_ON} and t_{SY_OFF}. When an external synchronization clock is applied to the RT/SYNC pin, the internal oscillator is over-driven so that each switching cycle begins at the rising edge of external clock. The IS32LT3958A will not be enabled if the RT/SYNC pin is held low during power-up. The IS32LT3958A will start up only when the RT/SYNC pin is tri-stated and allowed to rise to about 1V, or when a synchronization clock is detected, Figure 42 shows the timing for a synchronization clock into the IS32LT3958A at 500kHz. Any pulse with a duty cycle of 10% to 90% at 500kHz can be used to synchronize the IC. However, driving RT/SYNC pin with a 50% duty cycle waveform is always a good choice.

Table 1 Synchronization Duty Cycle Range

SYNC Clock Frequency(kHz)	Duty Cycle Range (%)
500	10 ~ 90
400	8 ~ 92
300	6 ~ 94
250	5 ~ 95

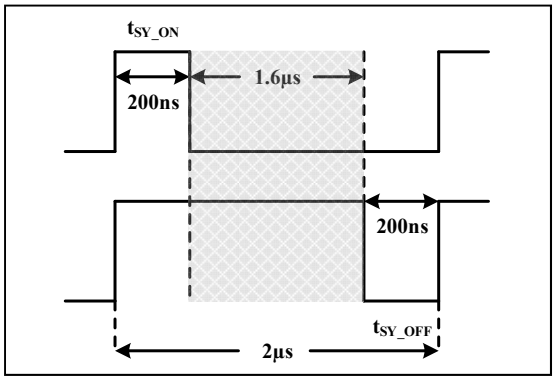


Figure 42 SYNC Pulse On And Off Time Requirements

SPREAD SPECTRUM

A switch mode controller can be particularly troublesome in applications where EMI is of concern. To optimize EMI performance, the IS32LT3958A includes a spread spectrum feature. The spread spectrum can spread the total electromagnetic emitting energy into a wider range to significantly degrade the peak EMI energy. With spread spectrum, the EMI test can pass with smaller sized and lower cost filter circuit.

When a capacitor is connected to FRQSS pin, a triangle waveform is internally generated to modulate the internal oscillator in 90% to 110% of the base frequency which is set by R_{RT} resistor as Figure 43.

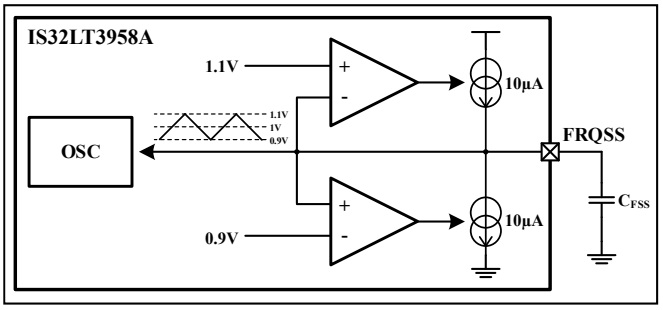


Figure 43 Spread Spectrum Operation

To set the desired modulation frequency, the C_{FSS} capacitor can be calculated by the following Equation (6):

$$C_{FSS} = \frac{10\mu A}{2 \times f_{SS} \times 0.2V} \qquad (6)$$

The C_{FSS} is in Farad. f_{SS} is the modulation frequency in Hertz. A 300Hz frequency is a good starting point to optimize EMI performance. Further adjust this frequency in the actual system to get best EMI performance. Connect FRQSS pin to GND to disable the spread spectrum function.

POWER NMOS CURRENT SENSE

CS is part of the current mode control loop. Connect a resistor R_{CS} from the CS pin to ground to regulate the internal oscillator duty cycle and power NMOS peak current and achieve input cycle-by-cycle peak current limit protection. In order to provide sufficient current to the external power NMOS for driving the load and

prevent this current from exceeding current limit protection, the R_{CS} value should be set to a proper level.

The inductor peak current (I_{PEAK}) during normal operation is given by following Equation (7):

$$I_{PEAK} = I_L + \frac{\Delta I_L}{2} \qquad (7)$$

Where I_L is the inductor average current in amp. ΔI_L is the current ripple of the inductor in amperes.

To ensure a reasonable output current ripple and better operating stability, choose ΔI_L as follows range:

$$20\% \times I_L \le \Delta I_L \le 100\% \times I_L \quad (8)$$

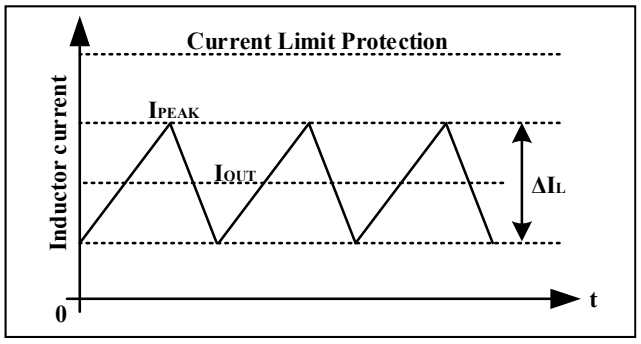


Figure 44 Inductor Current

The inductor ripple current ΔI_L involves trade-offs in performance. Lower ΔI_L requires a larger value and bigger sized inductor which will dissipate more power However, it also reduces the peak current in the external power NMOS and the recirculating diode and derate the power dissipation on them.

For boost application, the I_L is equal to the input average current, so

$$I_{PEAK\_BOOST} = \frac{V_{LED} \times I_{LED}}{\eta \times V_{CC}} + \frac{\Delta I_L}{2} \qquad (9)$$

For buck-boost and SEPIC applications, the I_L is equal to the input average current plus LED average current, so

$$I_{PEAK\_BUCK-BOOST} = \frac{(V_{LED} + V_{CC}) \times I_{LED}}{\eta \times V_{CC}} + \frac{\Delta I_L}{2} \quad (10)$$

Where η is the assumed circuitry efficiency (choose 0.9 for it). V_{CC} uses the minimum input voltage in volts, V_{LED} is the maximum total forward voltage of LED string in volts. I_{LED} is the output LED current in amperes.

The current limit protection should be at least 30% greater than the inductor peak current I_{PEAK}. The current sense resistor R_{CS} is calculated by the following Equation (11):

$$R_{CS} = \frac{V_{CS\_TH}}{1.3 \times I_{PEAK}} \qquad (11)$$

Recommend use of ±1% precision type resistor for best accuracy.

The current limit protection is a cycle-by-cycle detection. Once the CS pin voltage exceeds the current limit threshold, V_{CS_TH}, the GATE immediately pulls low to turn off the power NMOS until the next switching cycle. The current sense resistor should be placed as close as possible to IS32LT3958A device to ensure stable operation.

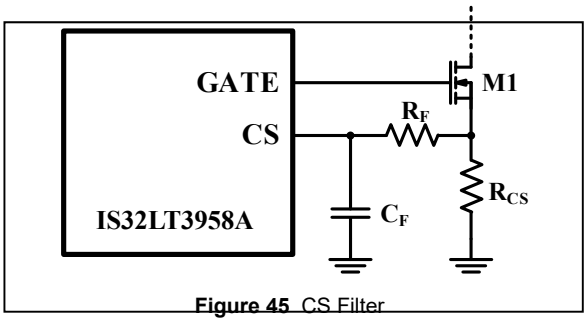


Figure 45 CS Filter

An internal blanking circuit prevents power NMOS switching current spike propagation and premature termination of duty cycle by internally shunting the CS input for 150ns after the beginning of the new switching period. For further noise suppression, the use of low pass RC filter on CS pin can be considered. The recommended value of R_F and C_F are 100Ω and 10pF.

INDUCTOR

Inductor value involves trade-offs in performance. Larger inductance reduces inductor current ripple resulting in smaller output current ripple, however it also brings in unwanted parasitic resistance that degrades performance. Select an inductor with a current rating greater than the input average current and a saturation current greater than the power NMOS current limit set by R_{CS}. Use the following equations to estimate the approximate inductor value:

For boost application:

$$L_{BOOST} = \frac{V_{CC} \times (V_{LED} - V_{CC})}{f_{SW} \times \Delta I_L \times V_{LED}} \qquad (12)$$

For buck-boost and SEPIC application:

$$L_{BUCK-BOOST} = \frac{V_{CC} \times V_{LED}}{f_{SW} \times \Delta I_L \times (V_{LED} + V_{CC})} \qquad (13)$$

Where V_{CC} uses the minimum input voltage in volts, V_{LED} is the maximum total forward voltage of LED string in volts, f_{SW} is the operation frequency in hertz. If the SEPIC inductor is uncoupled, the equation's result can be used as is. If the SEPIC uses two coupled inductors, then each should have an inductance half the result of the equation.

POWER NMOS

A power NMOS must be chosen with its drain voltage rating V_{DS_MAX} greater than the overvoltage protection voltage (V_{OVP}) together with overshoot voltage due to

the ringing caused by parasitic inductances and capacitances. Therefore keeping a 20% safety margin voltage above the overvoltage protection voltage is necessary.

For boost:

$$V_{DS\_MAX} \geq 1.2 \times V_{OVP} \qquad (14)$$

For buck-boost and SEPIC:

$$V_{DS\_MAX} \geq 1.2 \times \left(V_{OVP} + V_{CC\_MAX}\right) \qquad (15)$$

The gate drive current is sourced from the VDD pin whose current capability is limited to protect the device from excessive power dissipation at high input voltage. So low gate charge Q_G at 7V should be carefully considered (refer to Equation 3). The consideration of the $R_{DS(ON)}$ of power NMOS is usually secondary because the switching loss dominates the power lost, especially at high operating frequency. A power NMOS with lower Q_G and $R_{DS(ON)}$ achieves higher efficiency and lower power losses. The continuous current rating of the selected power NMOS should be higher than the input average current and the maximum current rating should be higher than the current limit protection level.

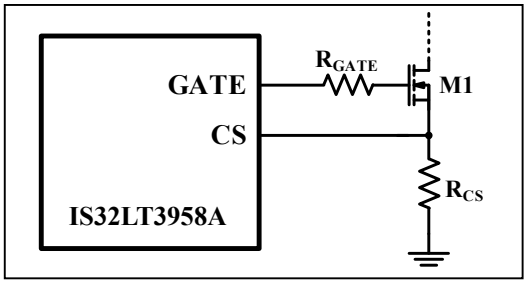


Figure 46 GATE Buffer Resistor

A buffer resistor can be considered in series with the gate drive to slow down the switching rise and fall edges to minimize EMI. However, it increases the switching loss and degrades the efficiency at the same time. So the value should not be too large; ten ohm is a good starting point. Please choose a proper value based on the EMI test result.

RECIRCULATING DIODE

The diode conducts the current during the interval when the power NMOS is turned off. To achieve high efficiency, choose a Schottky diode with low forward voltage and fast switching speed. Ensure that the diode's continuous current rating exceeds the output LED current and its peak current rating exceeds the current protection limit level. The diode's reverse breakdown voltage, V_{BD}, must be higher than the overvoltage protection voltage; with a 20% safety margin.

For boost:

$$V_{BD} \geq 1.2 \times V_{OVP} \qquad (16)$$

For buck-boost and SEPIC:

$$V_{BD} \geq 1.2 \times \left(V_{OVP} + V_{CC\_MAX}\right) \qquad (17)$$

The leakage current of the diode is also a critical feature to consider, which increases with the temperature. High leakage current will degrade the efficiency and PWM dimming performance.

INPUT CAPACITOR

The input capacitor provides the transient current to the inductor. An X7R type ceramic capacitor is a good choice for the input bypass capacitor to handle the ripple current since it has a very low equivalent series resistance (ESR) and low equivalent series inductance (ESL) with good temperature performance. Use the following equation to estimate the approximate capacitance:

For boost application:

$$C_{IN} \geq \frac{\Delta I_L}{8 \times V_{RIPPLE} \times f_{SW}} \qquad (18)$$

For buck-boost and SEPIC application:

$$C_{IN} \geq \frac{I_{LED} \times V_{LED}}{V_{RIPPLE} \times f_{SW} \times \left(V_{LED} + V_{CC}\right)} \qquad (19)$$

Where, V_{RIPPLE} is the acceptable input voltage ripple in volts. C_{IN} is in farads. This input capacitor must be placed close to the IS32LT3958A and the inductor to reduce the ripple. A higher value input capacitor is good for minimizing the input voltage deviation due to the large transient current. An aluminum electrolytic capacitor is recommended to be used in parallel with ceramic capacitors.

OUTPUT CAPACITOR

The output capacitor is used to filter the LED current ripple to an acceptable level. The equivalent series resistance (ESR), equivalent series inductance (ESL) and capacitance of the capacitor contribute to the output current ripple. Therefore, a low-ESR X7R type ceramic capacitor should be used. Use the following equation to estimate the approximate capacitance:

For boost application:

$$C_{OUT} \geq \frac{I_{LED} \times 2 \times (V_{LED} - V_{CC})}{V_{RIPPLE} \times f_{SW} \times V_{LED}} \qquad (20)$$

For buck-boost and SEPIC application:

$$C_{OUT} \geq \frac{I_{LED} \times 2 \times V_{LED}}{V_{RIPPLE} \times f_{SW} \times \left(V_{LED} + V_{CC}\right)} \qquad (21)$$

Where, V_{RIPPLE} is the acceptable output voltage ripple in volts. C_{OUT} is in farads. Based on the above equations, the higher operating frequency decreases proportionally the required output capacitor value which results in smaller capacitor size. The output ceramic capacitor should be placed close to the cathode of D_1

for a better filter effect. An aluminum electrolytic capacitor can be used in parallel with the ceramic capacitors to provide bulk energy storage.

LED CURRENT CONTROL

The IS32LT3958A regulates the LED current by the external resistor, R_{IS}, in series with LED string and connecting to ISP and ISN. The internal current sense voltage threshold V_{SENSE}, which is equal to V_{ISP}-V_{ISN}, is 0.25V (Typ.). Since the ISP/ISN only supports high-side current sensing, their common mode voltage (to ground) must be not less than 5V. When the PWM/EN pin is tied to a DC voltage higher than V_{EN_IH}, ICTRL/ADJR voltage is above 2V and PWMDC voltage is above 3V, this will result in a full-scale current sense voltage threshold and the LED current can be calculated from following equation.

$$I_{LED} = \frac{V_{SENSE}}{R_{IS}} \qquad (22)$$

In order to have an accurate LED current, precision resistors are preferred (±1% recommended). The R_{IS} resistor should be placed as close as possible to the IS32LT3958A device with minimal trace length.

ANALOG DIMMING

The IS32LT3958A offers two analog dimming input pins, ICTRL and ADJR. The dimming voltage range of both pins is 0.06V to 2V. The current sense voltage threshold, V_{SENSE}, can be regulated by the ICTRL pin and/or ADJR pin voltage. If both analog dimming pins are pulled up above 2V, analog dimming is disabled, and the output current is given by Equation (22). When any one pin is driven below 2V, the analog dimming is enabled, and the pin voltage will proportionally control the current sense voltage threshold V_{SENSE} resulting in a change in the output current as given by following equation:

$$I_{LED\_ADIM} = \frac{V_{ICTRL/ADJR}}{2V} \times \frac{V_{SENSE}}{R_{IS}} \qquad (23)$$

If both pins are driven below 2V, the voltage of both pins can control the current sense voltage threshold V_{SENSE} to change the output current:

$$I_{LED\_ADIM} = \frac{(V_{ICTRL} + V_{ADJR}) - 2V}{2V} \times \frac{V_{SENSE}}{R_{IS}} \qquad (24)$$

In this equation, if the (V_{ICTRL}+V_{ADJR})≤2V, the output current will be modulated down close to zero. Due to the GATE minimum on time limitation, the output current will not be completely off. Unless any one of the analog dimming pins is driven below 0.06V (Typ.).

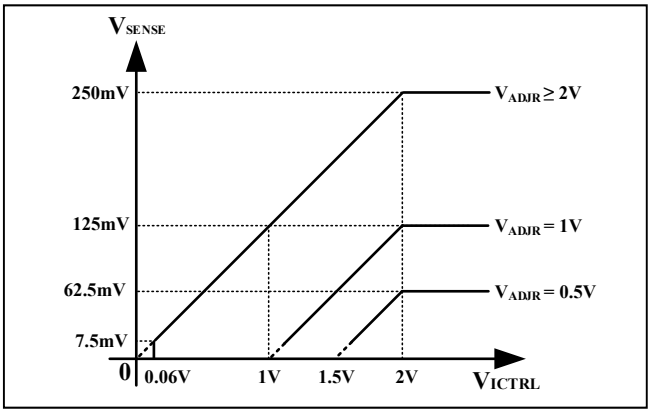


Figure 47 Analog Dimming Curve

The reference voltage of analog dimming internal circuit is derived from a reference voltage identical with the internal LDO of VDD. Therefore, in the applications, the analog dimming voltage should be derived from the VDD instead of an external voltage source to ensure better accuracy.

Note that the relative current accuracy decreases with the decreasing current sense voltage threshold due to the offset of the internal circuit. The recommended minimum analog dimming level is around 10%. Comparing to the ICTRL pin, the ADJR pin has smaller internal circuit offset. When analog dim down to low level, using the ADJR pin gets better current accuracy.

Never leave the ICTRL and ADJR pins floating. If the analog dimming function is not implemented, connect them to a voltage level within 2.5V to 5V. This voltage can be created with a resistor divider (R_1, R_2) from the VDD pin. The ICTRL and ADJR pins cannot be connected directly to the VDD pin because the linear regulator VDD voltage (typical 6.6V) exceeds the maximum voltage rating of the ICTRL and ADJR pins.

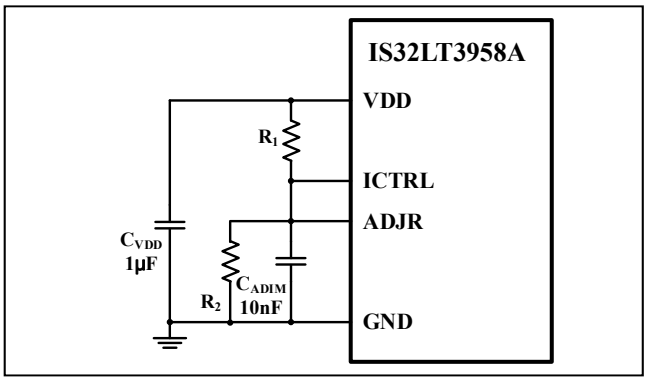


Figure 48 Analog Dimming Pins Unused

When any one pin is driven below 0.06V (Typ.), the output will be turned off. It is recommended to add a 10nF ceramic capacitor from each pin to GND to bypass any high frequency noise, especially if the analog voltage level comes from a long copper trace. This 10nF capacitor should be placed as close to the corresponding pin as possible.

The output LED voltage will decrease when the output

current decreases. Therefore, it must ensure the output voltage always is higher than the input voltage during the dimming in the boost configuration.

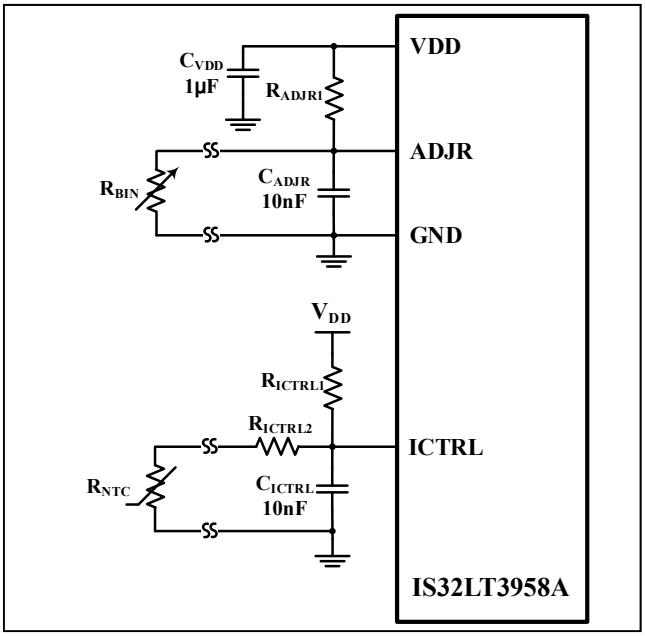


Figure 49 Analog Dimming for Binning and Thermal Roll-off

The ADJR pin can be used to fine tune the output current during mass-production. LEDs are typically sorted into various bins of different luminous intensity and forward voltage. To correct the brightness deviation during mass-production, the mean output current can be adjusted by adjusting the voltage level on the ADJR pin. As shown in Figure 49, fix the R_{ADJR1} resistor value and vary the R_{BIN} resistor value to adjust and maintain the same lumen output across different LED bins. This R_{BIN} resistor can be placed on the LED board.

The ICTRL pin can be used in conjunction with an NTC thermistor to provide over temperature current roll-off protection for the LED load or the system. As shown in Figure 49.

For example, assume the desired current roll-off temperature threshold is T_R and the NTC thermistor resistance is R_{NTCR} at this temperature (R_{NTCR} can be found in the NTC thermistor datasheet), then R_{ICTRL1} and R_{ICTRL2} can be calculated by:

$$R_{ICTRL1} = \frac{\left(R_{NTCR} + R_{ICTRL2}\right) \times \left(V_{DD} - 2V\right)}{2V} \qquad (25)$$

For a given NTC thermistor, the R_{ICTRL1} resistor will adjust the current roll-off temperature threshold. The larger R_{ICTRL1} the lower current roll-off temperature threshold. The R_{ICTRL2} resistor is optional to be used to adjust current derating slope. The larger R_{ICTRL2} the flatter the current derating slope. If R_{ICTRL2} is not used, tie the NTC thermistor directly to ICTRL pin. The NTC thermistor should be placed next to the component to be monitored. Such as the LED board, beside the power MOSFET, and so on.

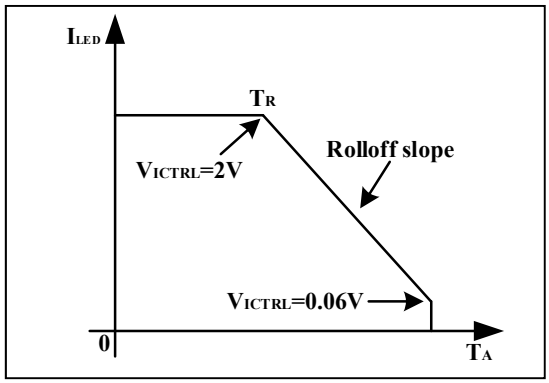


Figure 50 Roll-off Protection

PWM DIMMING

IS32LT3958A supports two PWM (Pulse Width Modulation) dimming approaches: external PWM dimming by an external PWM signal applied on the PWM/EN pin and internal PWM dimming by an integrated PWM generator.

Note that two PWM dimming modes CANNOT be active at the same time, otherwise it will cause an LED flickering issue.

EXTERNAL PWM DIMMING

Besides enable and shutdown function, the PWM/EN pin also supports an external PWM signal to implement pulse-width modulation of the output current.

The DIMOUT pin is a buffered output following the dimming signal on the PWM/EN pin which drives the gate of the dimming MOSFET. When the PWM/EN signal voltage is greater than logic high threshold V_{EN_IH}, the switching is enabled and the dimming MOSFET is turned on. When the PWM voltage is lower than the logic low threshold V_{EN_IL}, the switching is disabled and the dimming MOSFET is turned off. The LED string is dimmed by modulating the duty cycle of PWM signal to vary the LED average current. Apply a low PWM signal frequency with a higher device switching frequency will result in best dimming performance. The PWM dimming output current is calculated by:

$$I_{LED\_PWM} = I_{LED} \times D_{EXTPWM} \qquad (26)$$

Where, D_{EXTPWM} is the external PWM signal duty cycle in %. The recommended frequency of the external PWM signal is 100Hz~1kHz. There is an inherent PWM turn on/off delay time during continuous PWM dimming. A high frequency PWM signal has a shorter period time that will degrade the PWM dimming linearity. Therefore, a low frequency PWM signal is good for achieving better dimming contrast ratio.

An external MOSFET driven by the DIMOUT pin is recommended for a precise PWM dimming function. The dimming MOSFET will disconnect the LED string during PWM low to prevent the V_{OUT} node from discharging which will minimize the recovery time when the PWM goes back high. This shorter recovery time

results in better dimming linearity and stable loop regulation during low PWM duty cycles. Both are critical for ensuring control loop regulation during steady-state operation and to minimize LED current overshoot once PWM returns to high level.

An RC filter (1kΩ resistor and 30pF capacitor) in series with the PWM/EN input is recommended to avoid noise coupling during PWM dimming operation, especially if the PWM signal comes from a long copper trace. If PWM dimming is not used, the PWM/EN pin can be connected to VCC via a resistor (recommended value is 10kΩ).

INTERNAL PWM DIMMING

IS32LT3958A integrates a PWM generator which is controlled by the PWMDC pin. If the PWMDC pin is driven over 3V (Typ.), the internal PWM generator is disabled to get 100% output current which is set by the output current sense resistor, R_{IS}. Once the PWMDC pin is driven below 3V (Typ.), the internal PWM generator is enabled, which drives the switching and the dimming MOSFET to dim the output by its duty cycle. The internal PWM duty cycle is determined by the PWMDC pin voltage:

$$D_{INTPWM} = \frac{V_{PWMDC}}{3V} \times 100 \qquad (27)$$

Where, D_{INTPWM} is the internal PWM duty cycle in %.

The recommended internal PWM duty cycle setting range is 5%~100%. The lower duty cycle results in lower output current accuracy due to the error caused by the offset of the internal circuit and the output current rising and falling response time. The PWM dimming output current is calculated by:

$$I_{LED\_PWM} = I_{LED} \times D_{INTPWM} \qquad (28)$$

The internal PWM frequency is programmed by a single resistor, R_{FR}, connected from PWMFR pin to GND. The PWM frequency can be set in a range of 100Hz~1kHz. Considering the output current rising and falling response time, a lower PWM frequency is helpful to get better output accuracy. A 100Hz~500Hz PWM frequency is recommended. The resistor value of R_{FR} can be calculated as follows:

$$R_{FR} = \frac{2 \times 10^4}{f_{INTPWM}} \qquad (29)$$

Where, f_{INTPWM} is the desired internal PWM frequency in Hz and R_{FR} is in kΩ. If the PWMFR pin is either left floating or shorted to GND, the internal PWM generator will be disabled to get 100% output current.

With internal PWM generator, the IS32LT3958A can easily implement dual brightness outputs by controlling the PWMDC pin. As Figure 51. When the external MOSFET M_4 is off, the voltage on the PWMDC pin is determined by the resistor divider R_{DC1} and R_{DC2}. If the M_4 is turned on, the resistor R_{DC3} is connected in parallel with R_{DC2} and gets lower voltage on the PWMDC pin. The result is a lower brightness output.

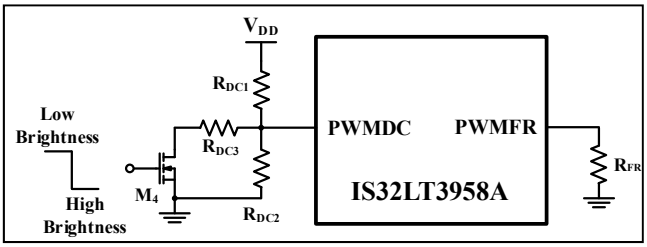


Figure 51 Dual Brightness Output with Internal PWM Dimming

The reference voltage of the internal PWM generator is derived from a reference voltage identical with the internal LDO of VDD. Therefore, in the applications, the voltage applied on the PWMDC pin should be derived from the VDD instead of an external voltage source to ensure better accuracy. 1% resistor type with good temperature-coefficient for R_{DC1}, R_{DC2} and R_{DC3} are recommended.

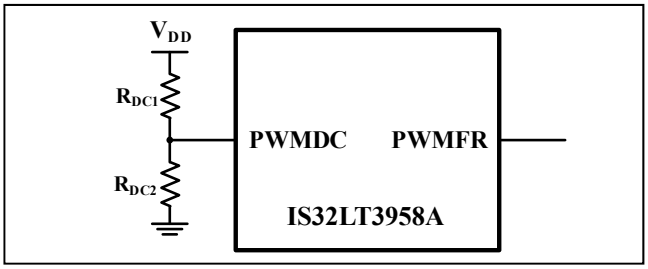


Figure 52 Internal PWM Dimming Unused

Never leave the PWMDC pin floating. If the internal PWM dimming function is not implemented, leave the PWMFR pin floating and connect the PWMDC pin to a voltage level within 3.5V to 5V. This voltage can be created with a resistor divider (R_{DC1}, R_{DC2}) from the VDD pin. As shown in Figure 52. The PWMDC pin cannot be connected directly to the VDD pin because the linear regulator VDD voltage (typical 6.6V) exceeds the maximum voltage rating of the PWMDC pin.

DIMMING MOSFET

A dimming NMOS (M_2) in series with the LED string is essential for PWM dimming application while in boost and SEPIC modes (refer to Figure 1, 2 and Figure 5, 6). The NMOS voltage rating should be as high as the power switching NMOS and its maximum continuous current rating should be higher than the maximum LED string current. Choose an NMOS with low total gate charge (Q_g) for high frequency turn on and off time for best PWM dimming contrast ratio. Another important NMOS selection parameter is low $R_{DS(ON)}$ for high operating efficiency and low power losses. If PWM dimming is not implemented, the dimming NMOS can be removed, the DIMOUT pin left floating, and the LED cathode connected directly to GND. However, please note the LED short protection feature will not be functional in boost mode. Therefore, it's recommended to use a dimming NMOS for most applications.

In buck-boost mode (refer to Figure 3 and 4), an additional PMOS (M_2), Zener (D_2), and resistors (R_{DIM1}, R_{DIM2}) are needed as a level shift to disconnect the output during PWM dimming operation. When the NMOS (M_3) connected to the DIMOUT pin turns on, the R_{DIM2} resistor will pull low the PMOS gate to turn it on. When the dimming NMOS turns off, R_{DIM1} resistor will pull high the PMOS gate to turn it off. A 7V Zener diode (D_2) is needed to clamp the V_{GS} voltage and protect the PMOS. The PMOS selection should follow the same guideline as the dimming NMOS regarding voltage and current ratings in boost mode. However, the dimming NMOS (M_3) in buck-boost mode can be a signal transistor which can be of low current capability, but the voltage rating should be the same as the power NMOS. If PWM dimming is not implemented, both dimming PMOS and NMOS can be removed with the DIMOUT pin left floating and LED anode connected directly to V_{OUT}. The recommended value of R_{DIM1} and R_{DIM2} are 2kΩ and 6.2kΩ. Too large value of R_{DIM1} and R_{DIM2} slows down the turn on/off speed of the M_2 that degrades the PWM dimming performance. While too low values discharge the output capacitor more quickly which extends the recovery time (when the PWM goes back high) and degrades the efficiency.

OUTPUT OVERVOLTAGE PROTECTION

The LED string open protection is achieved using overvoltage protection (OVP). The OVP is detected by the OV pin with a resistor divider network from the output to ground. When the OV pin voltage reaches the overvoltage protection threshold V_{OVP_TH}, the GATE and DIMOUT pins are immediately pulled low and the FAULTB pin is also pulled low to report the fault condition. They remain low until the OV pin voltage drops below the hysteresis voltage. To make sure the chip functions properly, the resistor divider (R_{O1}, R_{O2}) at the OV pin should be set to 1.2x greater than the LED string voltage, V_{LED}. For buck-boost applications, since the LED string is referenced to the input, the overvoltage protection should be sensed and translated to ground by using a PNP transistor Q_1 (a signal transistor type).

The OVP voltage (V_{OVP}) is calculated using following equations.

Boost and SEPIC:

$$V_{OVP} = \frac{V_{OVP\_TH} \times (R_{O1} + R_{O2})}{R_{O2}} \geq 1.2 \times V_{LED} \quad (30)$$

Buck-Boost:

$$V_{OVP} = \left(\frac{V_{OVP\_TH} \times R_{O1}}{R_{O2}} + 0.7 \right) \geq 1.2 \times V_{LED} \quad (31)$$

The OVP voltage hysteresis is determined by the R_{O1} resistor:

$$V_{OVP\_HY} = I_{OVP\_HY} \times R_{O1} \quad (32)$$

On the PCB layout, the resistor divider (R_{O1}, R_{O2}) must be placed as close to OV pin as possible. It is recommended to connect a 1nF ceramic capacitor from the OV pin to GND to avoid unexpected noise coupling into this pin when the sensing voltage comes from a long copper trace. This 1nF capacitor should be placed as close to the OV pin as possible.

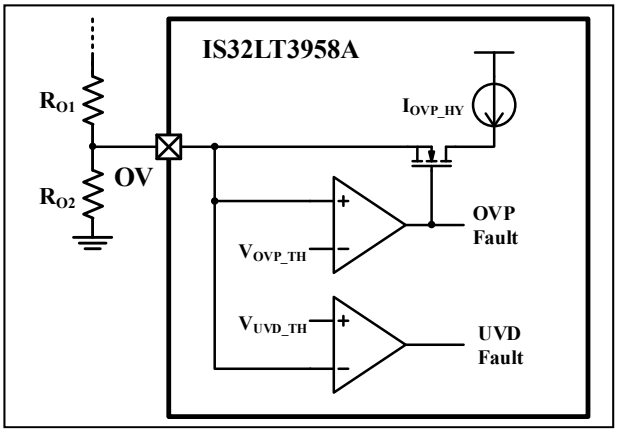


Figure 53 OVP and UVD Circuit

Note, the OVP voltage should not be set much higher than V_{LED}, otherwise the power NMOS, the dimming MOS, the recirculating diode and the output capacitor would require higher voltage ratings.

OUTPUT CURRENT MONITOR OUTPUT

the IMON pin voltage represents the output LED average current measured by the ISP and ISN pins connected to the output current sense resistor R_{IS}. It can be connected to an external host to implement output status tracking. The linear relationship between the IMON pin output voltage and the voltage across the current sense resistors is:

$$V_{IMON} = (V_{ISP} - V_{ISN}) \times 8 \quad (33)$$

The maximum output voltage of the IMON pin is internally clamped to V_{IMON_CLP} (Typical 3.35V). When a noise decoupling capacitor (C_{IMON}) is needed for the IMON pin, the recommended value is not greater than 1nF.

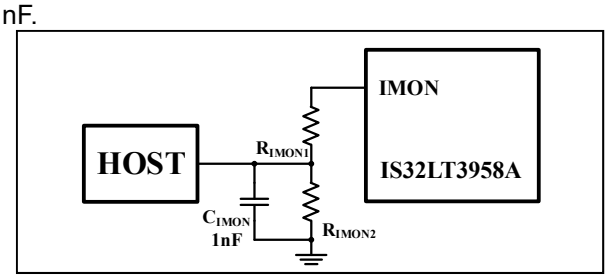


Figure 54 IMON Monitored by Host

If the current monitor function is not implemented, please leave the IMON pin floating.

Note that if analog dimming by the ICTRL pin is implemented then the IMON output is invalid.

OUTPUT SHORT PROTECTION

The output short fault condition is achieved using output undervoltage detection (UVD) and output overcurrent detection.

The UVD is detected by the OV pin with the resistor divider network from the output to ground. As shown in Figure 53. When the OV pin voltage falls below the undervoltage detection threshold V_{UVD_TH}, the device signals an output undervoltage fault condition. The UVD voltage (V_{UVD}) is calculated using following equations.

Boost and SEPIC:

$$V_{UVD} = \frac{V_{UVD\_TH} \times (R_{O1} + R_{O2})}{R_{O2}} \quad (34)$$

Buck-Boost:

$$V_{UVD} = \frac{V_{UVD\_TH} \times R_{O1}}{R_{O2}} + 0.7 \quad (35)$$

The output undervoltage detection is internally disable based on the SS pin voltage (<V_{SS_EN}) and internal PWM status. The fault blanking circuit is designed to prevent false undervoltage detection during the startup sequence and PWM dimming operation.

The device indicates the output undervoltage fault condition by pulling the FAULTB pin low but does not internally initiate any protection action and continue to operate. If the output undervoltage fault condition is cleared (the OV pin voltage rises above V_{UVD_TH}) or disabled by the SS pin, the FAULTB pin will go back to high impedance after t_{SKIP} duration.

The ISP and ISN pins have an output overcurrent threshold (V_{SENSE_OC}), which is higher than output current sense threshold (V_{SENSE}). The device signals an output overcurrent fault condition when the voltage across the current sense resistor R_{IS}, (V_{ISP}-V_{ISN}), exceeds overcurrent threshold V_{SENSE_OC}. When the common mode voltage of ISP and ISN pins is greater than 5V (Typ.), the device indicates the output overcurrent fault condition by pulling the FAULTB pin low but does not internally initiate any protection action and continue to operate. If the output overcurrent fault condition is cleared ((V_{ISP}-V_{ISN}) voltage drops below V_{SENSE_OC}), the FAULTB pin will go back to high impedance after t_{SKIP} duration.

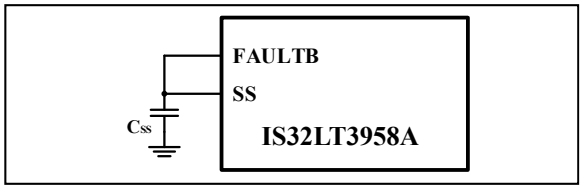


Figure 55 Enable Hiccup Mode Operation

No fault protection action might provide maximum design flexibility to enable user defined fault protection by using the fault reporting output, FAULTB, for some applications. If hiccup mode operation is desired under the output short fault condition, the FAULTB pin should be externally connected to the SS pin. On detection of output short fault condition, the FAULTB reporting forces the SS pin low (<V_{SS_RST}) and that stops the device from switching and the DIMOUT pin pulls the gate of dimming MOS M_2 to low. Upon t_{SKIP} expiration, the FAULTB pin is released, and the device attempts to restart with a new soft-start sequence. Under sustained fault conditions the device operates in hiccup mode, attempting to recover after every t_{SKIP} period.

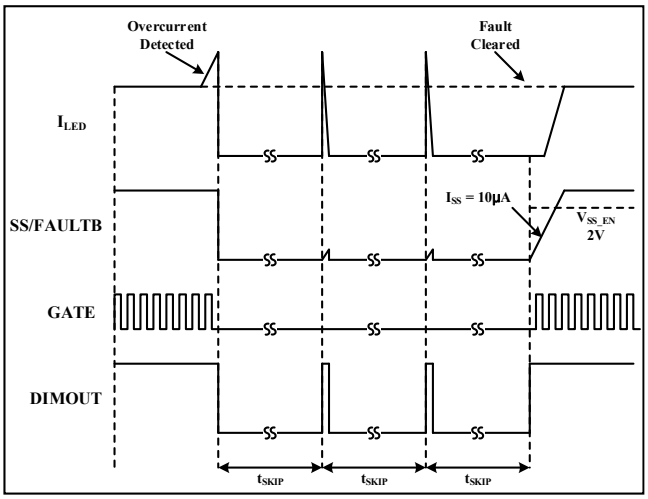


Figure 56 Output Overcurrent Hiccup Operation (FAULTB pin connected to SS pin)

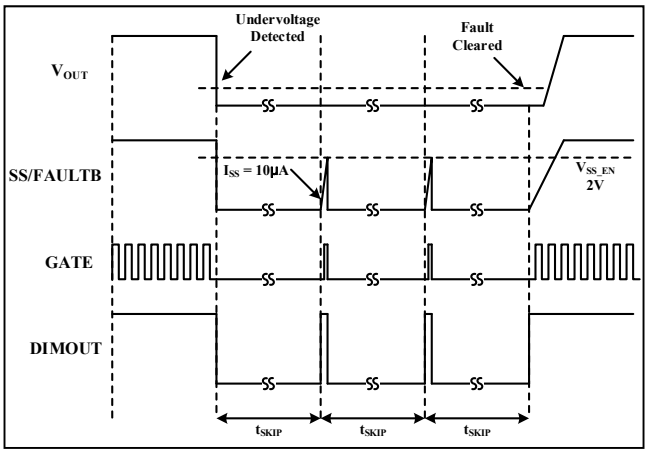


Figure 57 Output Undervoltage Hiccup Operation (FAULTB pin connected to SS pin)

In a boost configuration, if the LED string is completely shorted, there is a current path from V_{IN} through the inductor, recirculating diode, R_{IS} and dimming NMOS (M_2) to ground. If this fault occurs, the uncontrolled current of this path will rise rapidly. If the dimming NMOS M_2 does not disconnect this current path, the huge current may damage the components as well as the power source.

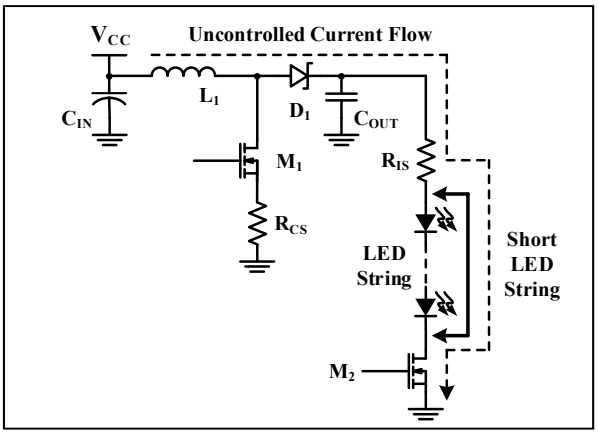


Figure 58 Boost LED String Short

In order to protect the circuit under this output short fault condition, once if the common mode voltage of ISP and ISN pins is lower than 5V (Typ.) and the voltage across the current sense resistor R_{IS}, (V_{ISP}-V_{ISN}), exceeds overcurrent threshold V_{SENSE_OC}, the device will immediately stop switching and pull low the DIMOUT and FAULTB pins for t_{SKIP} duration. When the timing is complete, the device attempts to restart and the FAULTB pin is released. If the fault condition still persists, the device shuts down and goes through the cycle again. The on/off cycling (hiccup mode operation) of the uncontrolled current flow will result in a low average value. If the fault condition is cleared (due to a momentary output short), the device will start regulating the output current normally. This prevents the circuitry and power supply from being damaged by an unwanted huge current. Note that the hiccup mode operation is enabled in this output overcurrent condition, even though the FAULTB pin is not externally connected to the SS pin.

In buck-boost and SEPIC configuration, when the LED string is shorted, there is no uncontrolled current path because the output current remains under control loop regulation. Therefore, an LED short circuit will not cause component damage.

THERMAL SHUTDOWN PROTECTION

To protect the IS32LT3958A from damage due to high power dissipation, the temperature of the die is monitored. If the die temperature exceeds the thermal shutdown temperature of 165°C (Typ.) the device will enter standby mode, and the FAULTB pin will be pulled low to report the fault. After a thermal shutdown event, the IS32LT3958A will not try to restart until its die temperature has reduced to less than 150°C (Typ.).

FAULT DETECTION AND REPORTING

For added system reliability, the IS32LT3958A integrates various fault detection and protection circuitry for LED string open/short circuit, VCC and VDD UVLO, power NMOS overcurrent, RT/SYNC and VDD pins short circuit and over temperature conditions. The open drain pin FAULTB can be used as a fault condition flag. When it's monitored by a host, a pull-up resistor from the FAULTB pin to the supply of the host is needed. It is pulled low to report the fault conditions. Table 2 briefly describes the typical protection trigger conditions and device behavior.

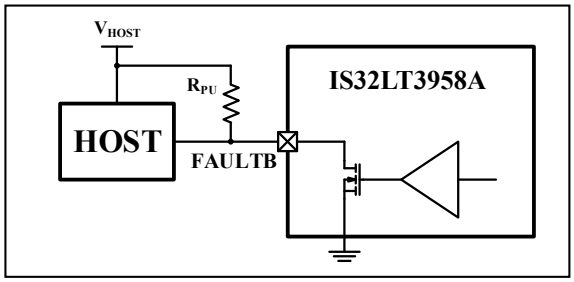


Figure 59 Host Monitors The Fault Reporting

The ideal value for the FAULTB R_{PU} range needs to take into account the number of IS32LT3958A devices connected to the same host. The resulting R_{PU} voltage level should not interfere with the V_{IH_HOST} and V_{IL_HOST} detection levels of the host. For no-fault detected operation, the sum of the leakage current(s) for the open drain (if more than one device interconnected) multiplied with the value of R_{PU} must be greater than V_{IH_HOST}. For fault detected operation, the pull-down voltage must be below V_{IL_HOST}. Then

$$R_{PU\_MAX} = \frac{V_{HOST} - V_{IH\_HOST}}{N \times I_{FAULTB\_LK}} \quad (36)$$

$$R_{PU\_MIN} = \frac{(V_{HOST} - V_{IL\_HOST}) \times V_{FAULTB\_LOW}}{V_{IL\_HOST} \times I_{OL}} \quad (37)$$

Where N is the number of IS32LT3958A devices connected to the same host. I_{OL} is the test condition of FAULTB pin pull down capability. It can be found in the EC table.

Table 2 Fault Actions

Fault Type	Fault Condition	Device Operation After Fault	FAULTB Pin	Fault Reset
VCC UVLO	$V_{CC}<V_{UVLO\_F}$	GATE and DIMOUT pull low immediately. IC enters standby mode. SS and COMP resets to zero.	High Impedance	$V_{CC}>V_{UVLO\_R}$
VDD UVLO	$V_{DD}<V_{UVLO\_F}$	GATE and DIMOUT pull low immediately. IC enters standby mode. SS and COMP resets to zero.	High Impedance	$V_{DD}>V_{UVLO\_R}$
VDD Pin Short	After startup and $V_{DD}<1.4V$	GATE and DIMOUT pulls low immediately. IC enters standby mode. SS and COMP resets to zero.	Pull Low	$V_{DD}>1.4V$
Output Overvoltage (LED Open)	$V_{OUT}\geq V_{OVP}$	GATE and DIMOUT pull low immediately. IC enters standby mode. SS and COMP resets to zero.	Pull Low	$V_{OUT}<(V_{OVP}-V_{OVP\_HY})$
Power NMOS Current Limit	$V_{CS}>V_{CS\_TH}$	GATE pulls low immediately until the next switching cycle.	High Impedance	$V_{CS}<V_{CS\_TH}$
Output Overcurrent (LED Short)	$V_{ISP}/V_{ISN}>5V$ and $(V_{ISP}-V_{ISN})>V_{SENSE\_OC}$	No internal protection action initiated, and device continue to operate. Only if the FAULTB pin is externally connect to SS pin, the device will operate in hiccup mode (restart every t_{SKIP} period).	Pull Low	$(V_{ISP}-V_{ISN})<V_{SENSE\_OC}$
	$V_{ISP}/V_{ISN}<5V$ and $(V_{ISP}-V_{ISN})>V_{SENSE\_OC}$	GATE and DIMOUT pulls low immediately. IC enters standby mode. SS and COMP resets to zero. The device will operate in hiccup mode (restart every t_{SKIP} period).	Pull Low	
Output Undervoltage (LED Short)	$V_{OV}<V_{UVD\_TH}$	No internal protection action initiated, and device continue to operate. Only if the FAULTB pin is externally connect to SS pin, the device will operate in hiccup mode (restart every t_{SKIP} period).	Pull Low	$V_{OV}>V_{UVD\_TH}$
RT/SYNC Pin Short	$f_{SW}>2.5MHz$	GATE pulls low immediately.	Pull Low	$f_{SW}<2.5MHz$
Thermal Shutdown	$T_J>165°C$	GATE and DIMOUT pulls low immediately. IC enters standby mode and SS and COMP resets to zero.	Pull Low	$T_J<150°C$

PCB LAYOUT CONSIDERATION

As with all switching power supplies, especially those providing high current and using high switching frequencies, layout is an important design step. If layout is not carefully done, the operation could show instability as well as EMI problems.

The high dV/dt surface and dI/dt loops are big noise emission sources. To optimize the EMI performance, keep the area size of all high switching frequency points with high voltage compact. Meantime, keep all traces carrying high current as short as possible to minimize the loops.

Please design the PCB layout according to following considerations.

(1) Wide and short traces should be used for connection of the high current paths that helps to achieve better efficiency and EMI performance. Such as the traces of power supply, inductor L_1, power NMOS M_1, recirculating diode D_1, LED load, ground.

(2) Keep the traces of the switching points shorter. The inductor L_1, power MOSFET M_1 and current recirculating diode D_1 should be placed as close to each other as possible and the traces of connection between them should be as short and wide as possible.

(3) To avoid the ground jitter, the components of parameter setting, especially the R_{IS}, R_{CS}, R_{RT}, R_{FR}, C_{SS}, C_{FSS}, C_{CP}, OV resistor divider, PWMDC resistor divider, and analog dimming resistor dividers should be placed close to the device with the trace length to the device pins as short as possible. On the other side, to prevent noise coupling, the traces of these components should either be far away or be isolated from high-current paths and high-speed switching nodes. These practices are essential for better accuracy and stability.

(4) The capacitor C_{VCC} and C_{VDD} should be placed as

close as possible to VCC and VDD pin for good filtering.

(5) For the boost/SEPIC application, the output capacitor C_{OUT} must be placed close to the cathode of D_1. For the buck-boost application, the C_{OUT} must be placed close to both anode of C_{IN} and the cathode of D_1, otherwise the output current performance will be degraded.

(6) All thermal pads on the back of IS32LT3958A, the recirculating diode and the power NMOS package must be soldered to a sufficient size of copper plane with sufficient vias to conduct the heat to opposite side of the PCB for adequate cooling.

(7) Flood all unused areas on all layers with copper that reduces the temperature rise of the power components. Connect the copper areas to GND.

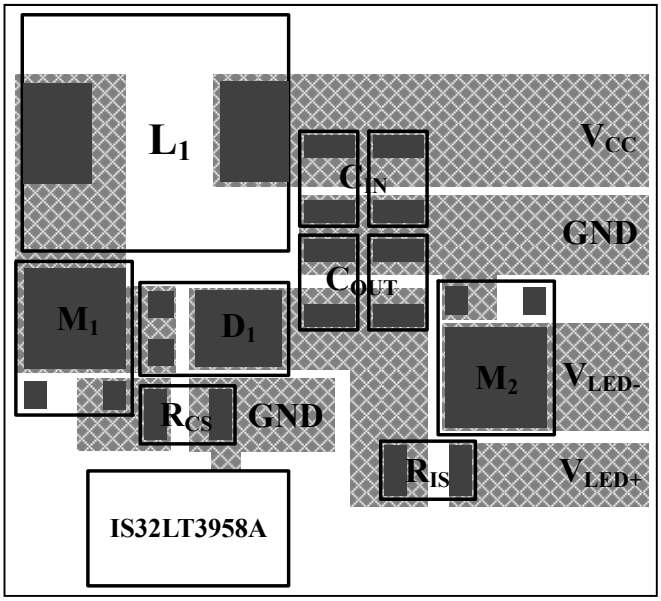


Figure 60 Boost PCB Layout Example

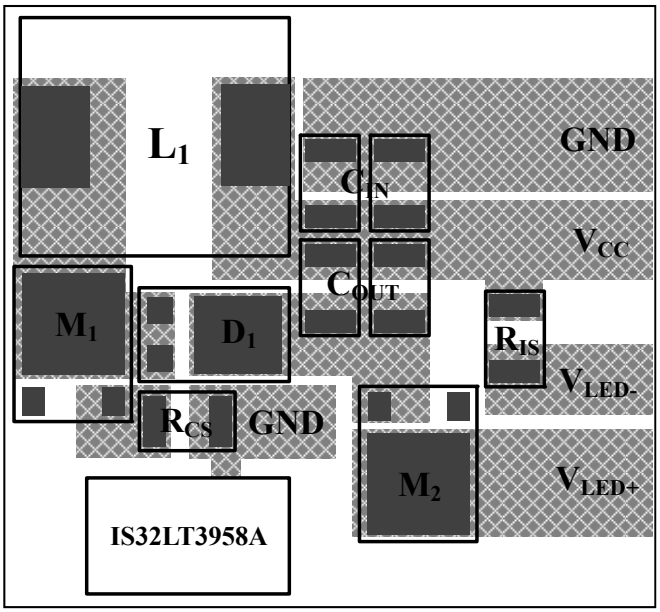


Figure 61 Buck-Boost PCB Layout Example

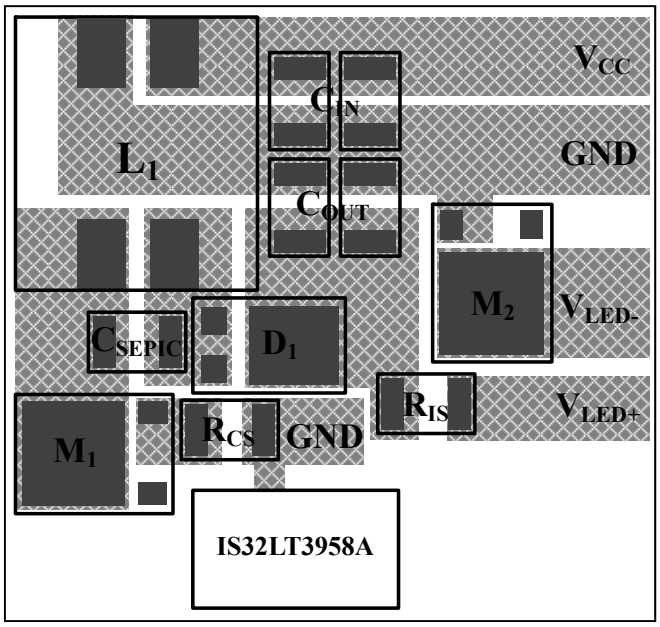


Figure 62 SEPIC PCB Layout Example

THERMAL CONSIDERATIONS

The package thermal resistance, θ_{JA}, determines the amount of heat that can pass from the silicon die to the surrounding ambient environment. The θ_{JA} is a measure of the temperature rise created by power dissipation and is usually measured in degree Celsius per watt (°C/W). The junction temperature, T_J, can be calculated by the rise of the silicon temperature, ΔT, the power dissipation, P_D, and the package thermal resistance, θ_{JA}, as in Equation (39):

$$P_D = V_{CC} \times (I_{CC} + f_{SW} \times Q_G) \quad (38)$$

and,

$$T_J = T_A + \Delta T = T_A + P_D \times \theta_{JA} \quad (39)$$

Where f_{SW} is operation frequency and Q_G is the total gate charge of power NMOS.

When operating the chip at high ambient temperatures, or when driving maximum load current, care must be taken to avoid exceeding the package power dissipation limits. The maximum power dissipation can be calculated using the following Equation (40):

$$P_{D(MAX)} = \frac{150°C - 25°C}{\theta_{JA}} \quad (40)$$

So,

$$P_{D(MAX)} = \frac{150°C - 25°C}{30.5°C/W} \approx 4.1W \quad (41)$$

for eTSSOP-20 package.

Figure 63, shows the power derating of the IS32LT3958A on a JEDEC boards (in accordance with JESD 51-5 and JESD 51-7) standing in still air.

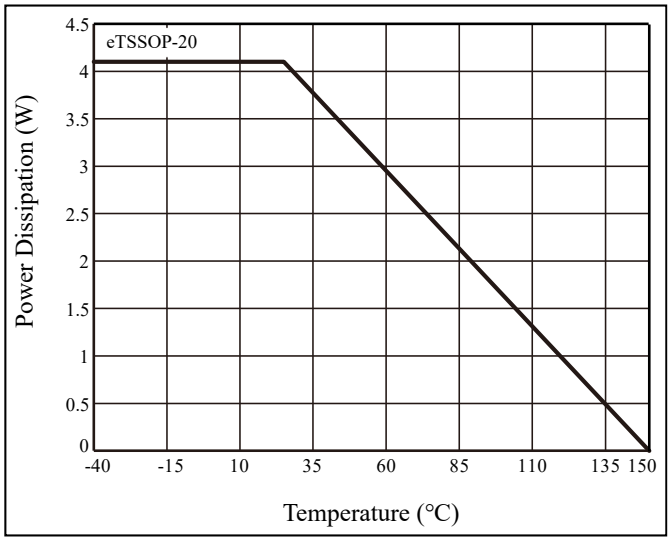


Figure 63 Dissipation Curve

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

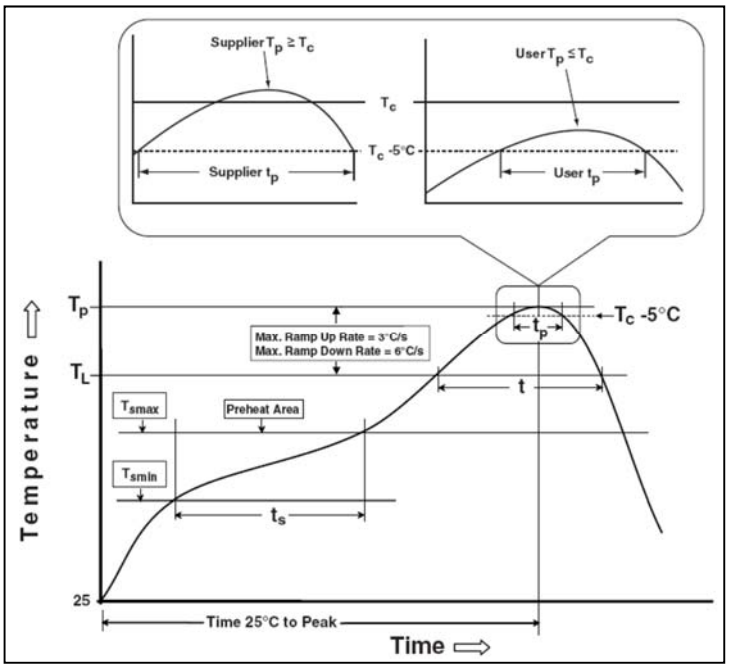
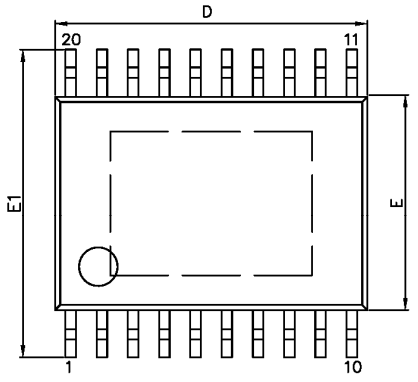


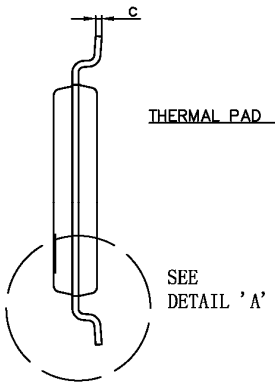
Figure 64 Classification Profile

PACKAGE INFORMATION

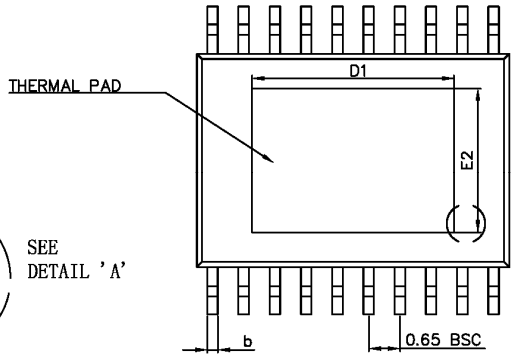
eTSSOP-20



TOP VIEW



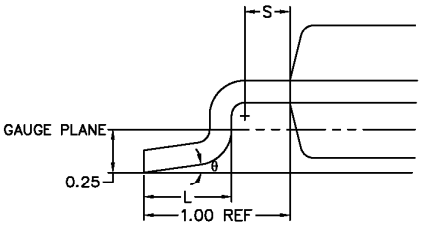
END VIEW



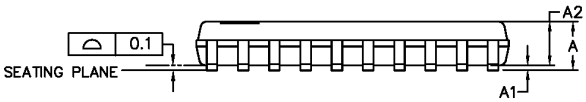
BOTTOM VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.02	—	0.15
A2	0.80	0.90	1.05
D	6.40	6.50	6.60
D1	3.79	—	4.40
E	4.30	4.40	4.50
E1	6.40BSC		
E2	2.60	—	3.20
L	0.45	0.60	0.75
b	0.19	—	0.30
S	0.20	—	—
c	0.09	—	0.20
θ	0°	—	8°

233-570-261 Rev. B



DETAIL 'A'

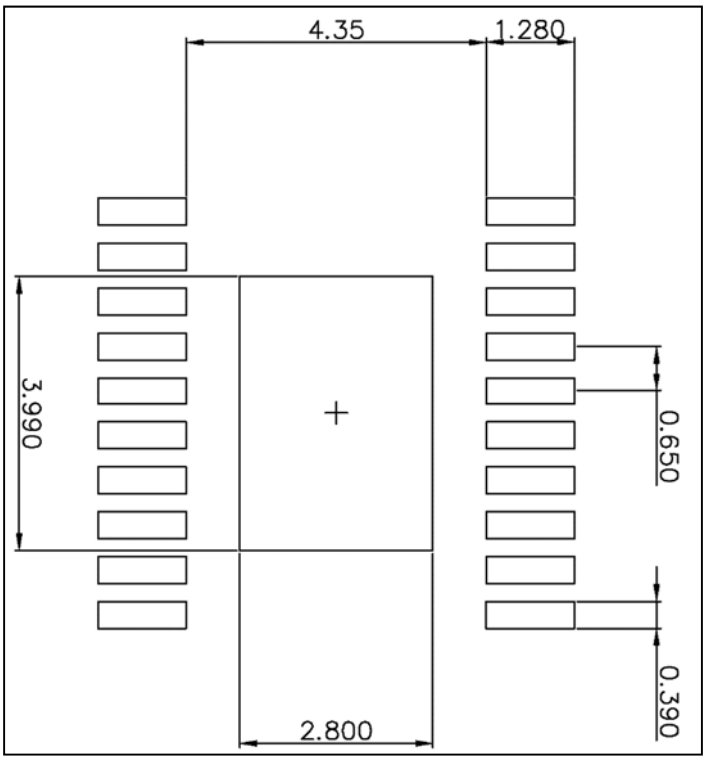


SIDE VIEW

NOTES:
1)The thermal pad shows different shape among different factories.
2)Controlling dimension:mm
3)Reference document:JEDEC MO-153

RECOMMENDED LAND PATTERN

eTSSOP-20



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. user's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
A	Initial release	2023.06.15