IS32LT3365A/B

HIGH-BRIGHTNESS LED DIMMER FOR AUTOMOTIVE LED ARRAY SYSTEMS

January 2025

1 GENERAL DESCRIPTION

The IS32LT3365 device is a compact, highly integrated solution with shunt dimming for large arrays of high-brightness LEDs in applications such as automotive matrix headlight system.

The IS32LT3365 device includes four groups of three switches in series array for bypassing individual LED(s) in the string. These four groups can either independently manage four LED strings or be connected in series to manage one LED strings, as well as paralleling up to four switches to bypass high current LEDs. Four on-board charge pump rails that can float up to 62V above GND provide the LED bypass switch gate drive. The low on-resistance ($R_{DS(ON)}$) of the bypass switch minimizes conduction loss and power dissipation.

The pulse width and phase shift of PWM control are programmable for each individual LED in the string. The PWM frequency is adjustable via an internal register, and multiple devices can be synchronized to the same frequency and phase. The programmable slew rate of switch transitions and spread spectrum in PWM dimming operation can optimize the EMI performance.

UART communication interface compatible with CAN PHY (IS32LT3365A) and CANLITE communication interface (IS32LT3365B) are used for control and management by a host MCU.

An integrated 10-bit ADC with two external multiplexed inputs can be used for either LED binning or temperature monitoring. The I^2C master interface can be used to read from or write to an external EEPROM to store system calibration data.

For additional system reliability, the IS32LT3365 device features LED open/short and single LED short detection, over temperature protection, as well as fault reporting via an open drain dedicated reporting pin (FAULTB) and the communication interface.

The eLQFP-48 package features a feed-through topology to enable easy routing of signals on single-layer aluminum LED load boards.

2 APPLICATIONS

- Automotive headlight systems
- Animation Daytime Running Light
- High-Brightness LED Matrix Systems

3 FEATURES

- Functional Safety-Capable
  - Developed according to ISO26262 with process complying to ASIL-B
- Embedded 12 LED bypass switches
  - Four groups of three series bypass switches
  - Maximum 20V across voltage on each switch
  - Maximum 55V from each switch to GND
  - Each switch up to 1.5A current capability
- Wide input voltage supply from 4.5V to 55V
- UART interface (IS32LT3365A) and CANLITE interface (IS32LT3365B) with Lumibus protocol
  - UART/CANLITE interfaces compatible with CAN physical layer, 100kbps~1Mbps baud rate
  - CRC to ensure robustness of communication
  - Support up to maximum 27 addressable devices
  - Watchdog timer to support fail-safe mode
- Individual PWM dimming to each switch
  - 10-bit PWM duty cycle setting
  - Individual phase shift setting
  - Spread spectrum to optimize EMI
  - Programmable slew rate control
  - Programmable PWM frequency up to 30kHz
  - Device-to-device synchronization
- I^2C master reading/writing EEPROM data for LED binning and calibration
- 10-bit ADC with two external MUXed inputs to support temperature monitor or LED binning
- Fault protection with flag and reporting
  - Programmable fail-safe mode
  - LED string open/short
  - Single LED short
  - CRC error
  - I^2C communication error
  - Internal LDO overvoltage
  - Programmable thermal alarm
  - Thermal shutdown
  - Dedicated fault reporting pin
- AEC-Q100 Qualified with Temperature Grade 1: -40°C to 125°C (IS32LT3365A/B-LQLA3-TR)
- AEC-Q100 qualification in process with Temperature Grade 1: -40°C to 125°C (IS32LT3365A/B-LQLCA3-TR)
- Operating junction temperature over -40°C ~ +150°C
- Thermally enhanced eLQFP-48 with exposed pad package
- RoHS & Halogen-Free Compliance
- TSCA Compliance

4 TYPICAL APPLICATION CIRCUIT

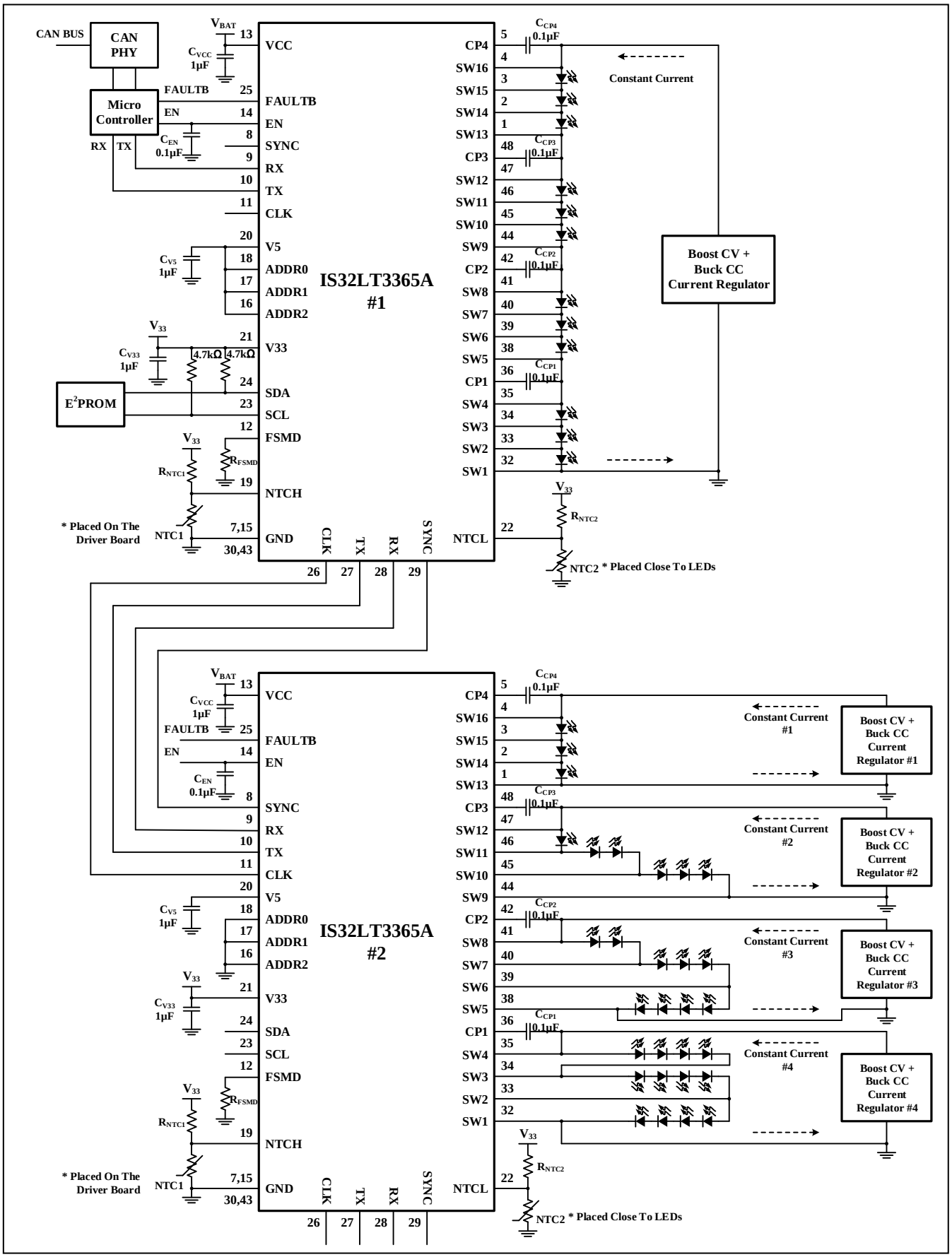

Figure 1 Typical Application Circuit of IS32LT3365A with UART Interface for On-board Communication

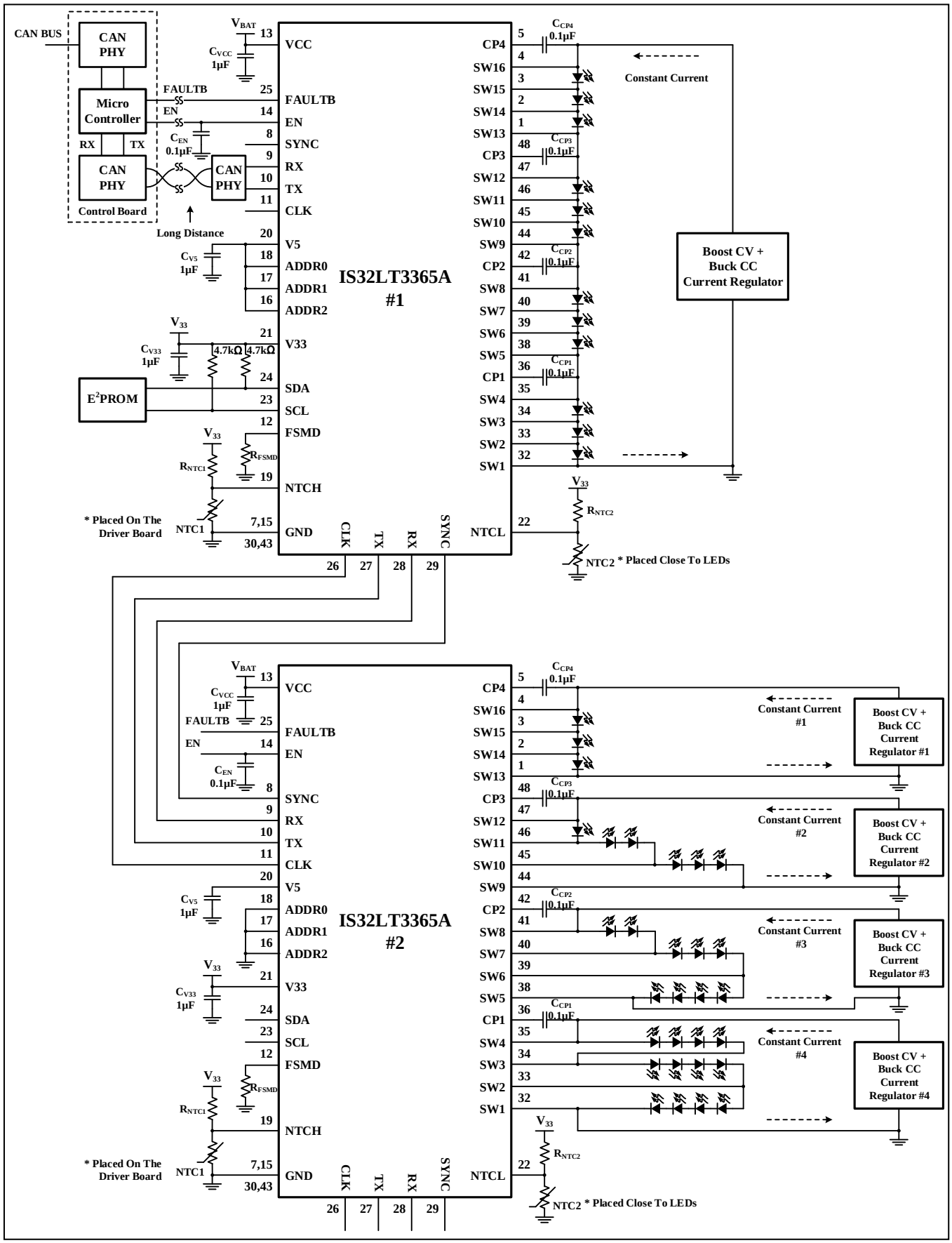

Figure 2 Typical Application Circuit of IS32LT3365A with External CAN PHY for Off-board Long Distance Communication

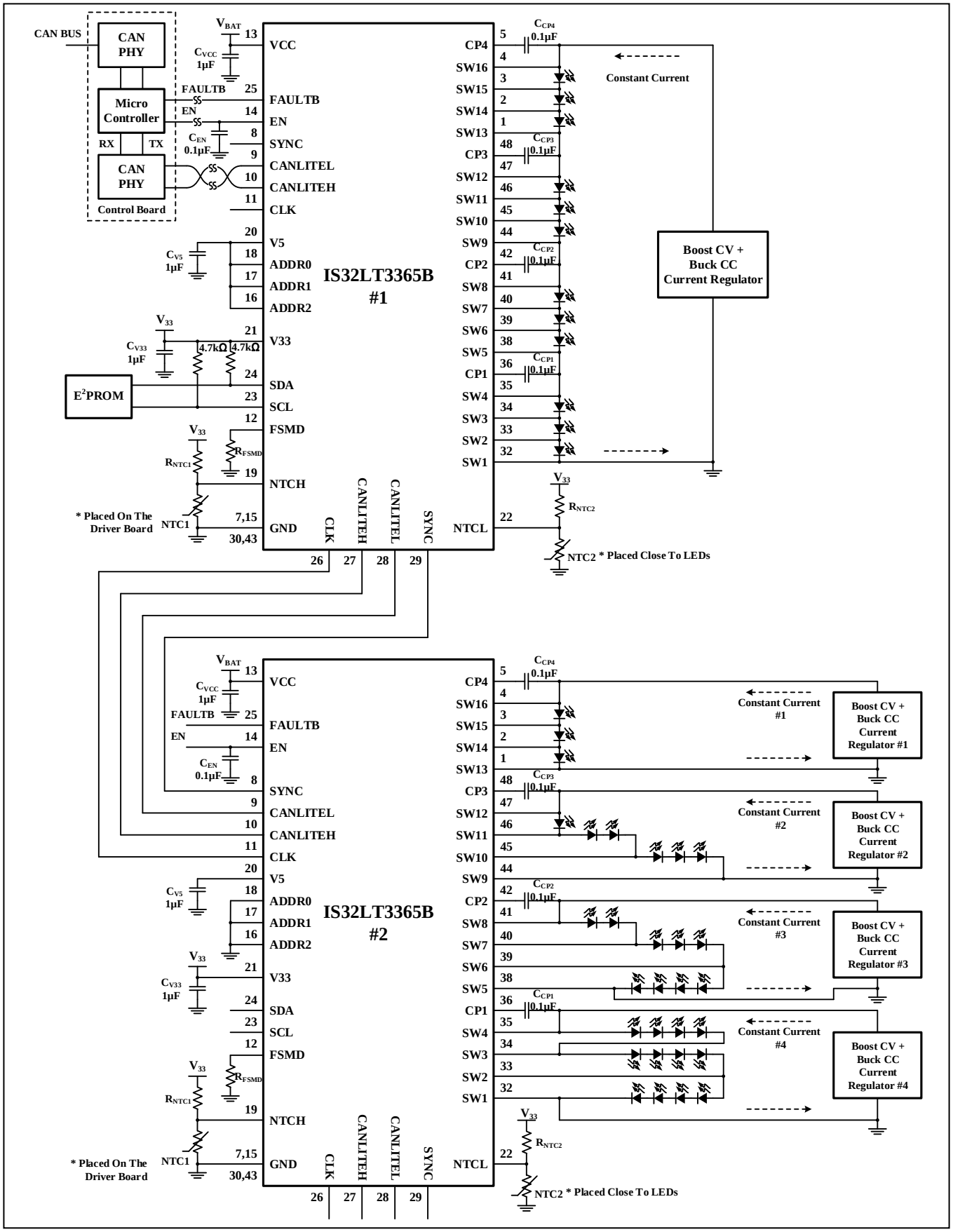

Figure 3 Typical Application Circuit of IS32LT3365B with CANLITE Interface for Off-board Long Distance Communication

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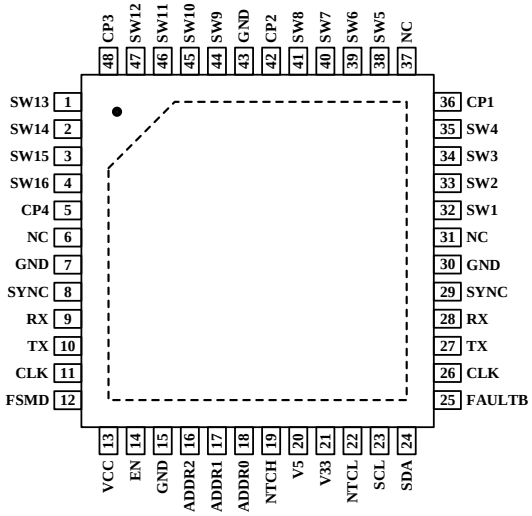
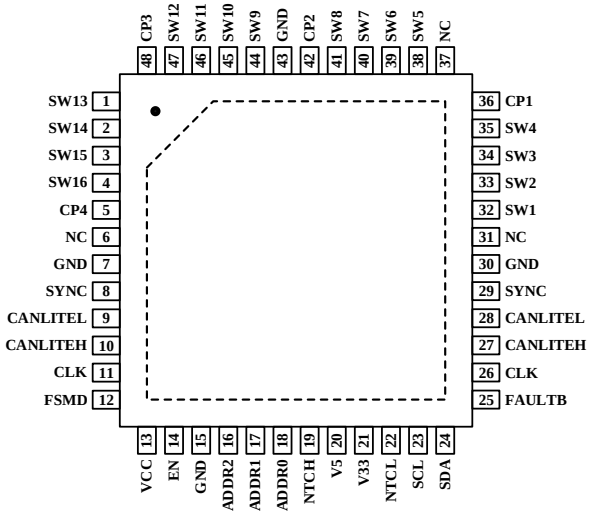
5 PIN CONFIGURATION

Package	Device	Pin Configuration (Top View)
eLQFP-48	IS32LT3365A	
	IS32LT3365B	

PIN DESCRIPTION (NOTE 1)

No.	Pin	Function
1~4	SW13~16	Group-S4 switches. SW16 connects to the anode of the first LED string. SW15 connects to the cathode of the first LED string and the anode of the second LED string. SW14 connects to the cathode of the second LED string and the anode of the third LED string. SW13 connects to the cathode of the third LED string and the anode of the next group of LEDs or GND.
5	CP4	Charge pump output for group-S4 switches. Bypass with a X7R ceramic capacitor with a value of 0.1μF to SW16. This capacitor must be placed as close to CP4 and SW16 pins as possible.
6,31,37	NC	No connection.
12	FSMD	Connect different value resistor to GND to set fail-safe mode.
7,15,30,43	GND	Device system ground. All these pins MUST be connected to GND for proper operation.
8,29	SYNC	Synchronization pins. Allows PWM synchronization of multiple IS32LT3365 devices on the same network. Left floating if not used.
9,28 (A)	RX	UART interface received data pin.
10,27 (A)	TX	UART interface transmitted data pin.
9,28 (B)	CANLITEL	CANLITE interface low-level.
10,27 (B)	CANLITEH	CANLITE interface high-level.
11,26	CLK	Master mode: internal PWM base clock output to the cascaded devices. Slave mode: external clock signal input for internal PWM base clock.
13	VCC	Power supply input for device. Bypass with a X7R ceramic capacitor with a minimum value of 1μF or greater. This capacitor must be placed as close to VCC pin as possible.
14	EN	Enable pin. The device is active when EN is high and reset when EN is low. Connect it to the microcontroller unit output or tie it to VCC via a 10kΩ resistor to enable it at power-up. When EN is low, all internal switches are in an off state, the LED string is turned on, and all registers are reset. It is recommended to use a 100nF X7R type capacitor close to this pin for noise decoupling. This capacitor should be placed as close to the EN pin as possible.
16~18	ADDR2 ~ ADDR0	Device address setting pins. Connected to V33, V5 or GND for different address.
19	NTCH	First ADC input. For example, externally connected to the NTC resistor and sample the voltage by the internal 10-bit ADC for temperature monitor of the driver board.
20	V5	Internal 5V LDO output. This pin requires an X7R ceramic output capacitor with a value of 1μF. This capacitor must be placed as close to the V5 pin as possible. It can be used for I^2C interface pull up, NTC voltage reference or device address set. DO NOT power high current external devices using the 5V LDO.

PIN DESCRIPTION (CONTINUED)

No.	Pin	Function
21	V33	Internal 3.3V LDO output. This pin requires an X7R ceramic output capacitor with a value of 1μF. This capacitor must be placed as close to the V33 pin as possible. It can be used for I²C interface pull up, NTC voltage reference or device address set. DO NOT power high current external devices using the 3.3V LDO.
22	NTCL	Second ADC input. For example, externally connected to the NTC resistor and sample the voltage by the internal 10-bit ADC for temperature monitor of the LED board.
23	SCL	I²C interface clock pin.
24	SDA	I²C interface data pin.
25	FAULTB	Open drain fault reporting pin. Active low to report fault conditions. It needs an external pull-up resistor.
32~35	SW1~SW4	Group-S1 switches. SW4 connects to the anode of the first LED string. SW3 connects to the cathode of the first LED string and the anode of the second LED string. SW2 connects to the cathode of the second LED string and the anode of the third LED string. SW1 connects to the cathode of the third LED string and GND.
36	CP1	Charge pump output for group-S1 switches. Bypass with an X7R ceramic capacitor with a value of 0.1μF to SW4. This capacitor must be placed as close to CP1 and SW4 pins as possible.
38~41	SW5~SW8	Group-S2 switches. SW8 connects to the anode of the first LED string. SW7 connects to the cathode of the first LED string and the anode of the second LED string. SW6 connects to the cathode of the second LED string and the anode of the third LED string. SW5 connects to the cathode of the third LED string and the anode of the next group LED or GND.
42	CP2	Charge pump output for group-S2 switches. Bypass with an X7R ceramic capacitor with a value of 0.1μF to SW8. This capacitor must be placed as close to CP2 and SW8 pins as possible.
44~47	SW9~SW12	Group-S3 switches. SW12 connects to the anode of the first LED string. SW11 connects to the cathode of the first LED string and the anode of the second LED string. SW10 connects to the cathode of the second LED string and the anode of the third LED string. SW9 connects to the cathode of the third LED string and the anode of the next group LED or GND.
48	CP3	Charge pump output for group-S3 switches. Bypass with an X7R ceramic capacitor with a value of 0.1μF to SW12. This capacitor must be placed as close to CP3 and SW12 pins as possible.
	Thermal Pad	MUST be connected to big size GND plane for better heatsink.

Note 1: (A) -- IS32LT3365A pin out; (B) -- IS32LT3365B pin out.

6 ORDERING INFORMATION

Automotive Range: -40°C to +125°C

Order Part No.	Package	QTY/Reel
IS32LT3365A-LQLA3-TR IS32LT3365A-LQLCA3-TR (Note 2) IS32LT3365B-LQLA3-TR IS32LT3365B-LQLCA3-TR (Note 2)	eLQFP-48, Lead-free	2500

Note 2: IS32LT3365A/B-LQLCA3-TR is with copper wire bonding.

7 SPECIFICATIONS

7.1 ABSOLUTE MAXIMUM RATINGS (NOTE 3)

Voltage at VCC, EN pins	-0.3V ~ +60V
Voltage at V5, V33, NTCL, NTCH, ADDR0~ADDR2, CLK, SYNC, FSMD, SDA, SCL, FAULTB pins	-0.3V ~ +6V
Voltage at RX, TX pins	-0.3V ~ (V_5 or V_{33}) +0.3V
Voltage at CANLITEH, CANLITEL pins	-20V ~ +20V
Differential voltage between CANLITEH and CANLITEL pins, ($V_{CANLITEH}$-$V_{CANLITEL}$)	-5V ~ +15V
CPx to GND voltage	-0.3V ~ +64V
CP1 to SW4, CP2 to SW8, CP3 to SW12, CP4 to SW6 voltage	-0.3V ~ +9V
SWx to GND voltage	-0.3V ~ +57V
SWx to SW(x-1) voltage in same switch group	-0.3V ~ +22V
Internal NMOS switch maximum continuous current	1.5A
Maximum power dissipation, $P_{D(MAX)}$	5.43W
Operating temperature range, T_A=T_J	-40°C ~ +150°C
Device storage temperature range, T_{STG}	-65°C ~ +150°C
Maximum operating junction temperature, T_{JMAX}	+150°C
Package thermal resistance, junction to ambient (4-layer standard test PCB based on JESD 51-2A), θ_{JA}	23°C/W
Package thermal resistance, junction to thermal PAD (4-layer standard test PCB based on JESD 51-2A), θ_{JP}	4.05°C/W
ESD (HBM) ESD (CDM)	±2kV ±750V

Note 3: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7.2 ELECTRONIC CHARACTERISTICS

Limits apply over operating junction temperature range -40°C≤ T_J ≤ +150°C. Typical values represent the most likely parametric norm at T_J= 25°C. Unless otherwise noted, V_{CC}= 12V.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
General						
I_{CC}	Quiescent current	82h=0x40		12	15	mA
I_{SD}	Shutdown current	V_{EN}=0V		15	25	μA
V_{CC_UVLOR}		VCC rising		4.3	4.49	V
V_{CC_UVLOF}		VCC falling	3.9	4.1		V
f_{OSC}	System clock frequency		30.11	30.72	31.33	MHz
V_{5_REG}	5V LDO regulated voltage	0< I_{OUT_V5}< 5mA	4.75	5	5.25	V
I_{AB_V5}	5V LDO current ability	V5 voltage drop ≤ 0.5V	50	90		mA
I_{CL_V5}	5V LDO current clamp	V5 shorted to ground	58	110		mA
V_{33_REG}	3.3V LDO regulated voltage	0< I_{OUT_V33}< 5mA	3.1	3.3	3.5	V
I_{AB_V33}	3.3V LDO current ability	V33 voltage drop ≤ 0.3V	15	20		mA
I_{CL_V33}	3.3V LDO current clamp	V33 shorted to ground	18	25		mA
V_{CPP}	Charge pump operating voltage	SW4/SW8/SW12/SW16= 0	5	7	8.5	V
		SW4/SW8/SW12/SW16= 7V	5	6	8.5	V
		SW4/SW8/SW12/SW16= 12V	4.5	5	7	V
		SW4/SW8/SW12/SW16= 55V	4.5	5	7	V

ELECTRONIC CHARACTERISTICS (CONTINUED)

Limits apply over operating junction temperature range -40°C≤ T_J ≤ +150°C. Typical values represent the most likely parametric norm at T_J= 25°C. Unless otherwise noted, V_{CC}= 12V.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{CPP}	Charge pump frequency	(Note 4)		2		MHz
T_{SD}	Thermal shutdown	(Note 4)		170		°C
T_{SD_HYS}	Thermal shutdown hysteresis	(Note 4)		20		°C
V_{PD_FAULTB}	FAULTB pull-down capability	I_{SINK}= 1mA		0.1	0.2	V
I_{LKG_FAULTB}	FAULTB leakage current	No Fault condition			2	μA
V_{TH1_AD}	ADDRx pins threshold-1		0.8	1	1.2	V
V_{TH2_AD}	ADDRx pins threshold-2		3.7	4	4.3	V
I_{FSMD}	FSMD pin source current			54		μA
V_{TH1_FS}	FSMD pin threshold-1		0.8	1	1.2	V
V_{TH2_FS}	FSMD pin threshold-2		1.8	2	2.2	V
V_{TH3_FS}	FSMD pin threshold-3		3.2	3.5	3.8	V
LED Matrix Switch						
R_{DSON_SW}	Switch on-resistance	Includes two internal bond wires		190		mΩ
R_{DSON_3SW}	3 switches in series on-resistance	Measured at (SW4-SW1), (SW8-SW5), (SW12-SW9), (SW16-SW13), Includes two internal bond wires		370	700	mΩ
I_{DS_LKG}	Off state switch leakage current	V_{DS}=20V		22	40	μA
V_{TH_SC}	LED short detection threshold voltage	0<SW<50V, related register setting: 0000 (default)	0.7	1	1.3	V
		0<SW<50V, related register setting: 0100	4.2	5	5.7	
		0<SW<50V, related register setting: 0111	7.2	8	8.8	
		0<SW<50V, related register setting: 1010	10	11	12	
V_{TH_OC}	LED open detection threshold voltage	0<SW<50V, related register setting: 00	4	5	6	V
		0<SW<50V, related register setting: 01	8.8	10	11.2	
		0<SW<50V, related register setting: 10	13.5	15	16.5	
		0<SW<50V, related register setting: 11 (default)	18	20	22	
t_{DELAY_OC}	LED open detection and correction delay	(Note 4)		50		ns

ELECTRONIC CHARACTERISTICS (CONTINUED)

Limits apply over operating junction temperature range -40°C≤ T_J ≤ +150°C. Typical values represent the most likely parametric norm at T_J= 25°C. Unless otherwise noted, V_{CC}= 12V.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{RISE}	Voltage rising time (V_{LED} = 3.3V)	I_{LED}= 0.4A, related register setting: 00		50		μs
		I_{LED}= 0.4A, related register setting: 01		25		
		I_{LED}= 0.4A, related register setting: 10		12		
		I_{LED}= 0.4A, related register setting: 11 (default)		2		
t_{FALL}	Voltage falling time (V_{LED} = 3.3V)	I_{LED}= 0.4A, related register setting: 00		50		μs
		I_{LED}= 0.4A, related register setting: 01		25		
		I_{LED}= 0.4A, related register setting: 10		12		
		I_{LED}= 0.4A, related register setting: 11 (default)		2		
EN, SYNC and CLK pins						
V_{IH}	High level input voltage	EN, SYNC and CLK pins	2			V
V_{IL}	Low level input voltage	EN, SYNC and CLK pins			0.8	V
V_{OH}	High level output voltage	SYNC and CLK pins, I_{SOURCE}= 10mA	4.7			V
V_{OL}	Low level output voltage	SYNC and CLK pins, I_{SINK}= 10mA			0.3	V
t_{R-DO1}	Rise time of digital output	SYNC and CLK pins, C_{LOAD}= 50pF (Note 4)		2		ns
t_{F-DO1}	Fall time of digital output	SYNC and CLK pins, C_{LOAD}= 50pF (Note 4)		2		ns
$I_{OS-SRC1}$	Output short source current	SYNC and CLK pins, PIN= 0V (Note 4)		100		mA
$I_{OS-SNK1}$	Output short sink current	SYNC and CLK pins, PIN= 5V (Note 4)		100		mA
R_{PASS1}	Resistance between SYNC pins, CLK pins			5		Ω
I²C Interface						
V_{IH_I2C}	High level input voltage	SDA, SCL pins (Note 4)	2			V
V_{IL_I2C}	Low level input voltage	SDA, SCL pins (Note 4)			0.8	V
V_{HY_I2C}	Input hysteresis voltage	SDA, SCL pins (Note 4)	0.25			V
V_{OL_I2C}	Low level output voltage	I_{SINK}= 2mA, SDA pin (Note 4)			0.3	V
$I_{OS-I2CSNK}$	Output short sink current	PIN= 5V, SDA, SCL pins (Note 4)		100		mA
ADC (10-Bit)						
V_{REFADC}	Reference voltage			1.8		V
DNL	Differential nonlinear	(Note 4)	-5		+5	LSB
INL	Integral nonlinear	(Note 4)	-8		+8	LSB
RESADC	Quantification steps	(Note 4)		1024		LSB
ADCERR	Quantification error	(Note 4)	-0.5		+0.5	LSB
t_{CONV}	Min. conversion time	(Note 4)		25		μs

ELECTRONIC CHARACTERISTICS (CONTINUED)

Limits apply over operating junction temperature range -40°C≤ T_J ≤ +150°C. Typical values represent the most likely parametric norm at T_J= 25°C. Unless otherwise noted, V_{CC}= 12V.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
CANLITE Interface (IS32LT3365B only)						
$V_{(O)DOM}$	Dominant output voltage	$V_{CANLITEH}$, R_{LOAD}= 60Ω	2.75	3.5	4.5	V
		$V_{CANLITEL}$, R_{LOAD}= 60Ω	0.5	1.5	2.25	V
$V_{(O)DIF}$	Differential output voltage ($V_{CANLITEH}$-$V_{CANLITEL}$)	Dominant, R_{LOAD}= 60Ω	1.5	2	3	V
		Recessive, R_{LOAD}= 60Ω	-50	0	50	mV
$V_{(O)RES}$	Recessive output voltage	$V_{CANLITEH}$ and $V_{CANLITEL}$, R_{LOAD}= open	2	0.5× V_5	3	V
V_{SYM}	Driver symmetry ($V_{CANLITEH}$+$V_{CANLITEL}$)/V_5	R_{LOAD}= 60Ω, operating frequency 1MHz	0.9	1.0	1.1	V/V
V_{SYM_DC}	DC output voltage symmetry (V_5-$V_{CANLITEH}$-$V_{CANLITEL}$)	Dominant or recessive, R_{LOAD}= 60Ω	-400		+400	mV
V_{CM}	Common mode voltage range		-10		12	V
V_{REC_IN}	Recessive state differential input voltage	($V_{CANLITEH}$-$V_{CANLITEL}$), -10V≤V_{CM}≤12V	-3		0.5	V
V_{TH_DIF}	Differential receiver threshold voltage	($V_{CANLITEH}$-$V_{CANLITEL}$), -10V≤V_{CM}≤12V	0.5	0.7	0.9	V
V_{HYS_DIF}	Differential receiver threshold voltage hysteresis	($V_{CANLITEH}$-$V_{CANLITEL}$), -10V≤V_{CM}≤12V		200		mV
V_{DOM_IN}	Dominate state differential input voltage	($V_{CANLITEH}$-$V_{CANLITEL}$), -10V≤V_{CM}≤12V	0.9		8	V
I_{O_DOM}	Dominant output current	CANLITEH pin	-115	-60		mA
		CANLITEL pin		60	115	mA
I_{O_RES}	Recessive output current	$V_{CANLITEH}$=$V_{CANLITEL}$ = -10V to 12V	-5		+5	mA
R_{IN_H}	Single ended input resistance (CANLITEH pin)	-2V≤ $V_{CANLITEH}$≤ 7V	6		50	kΩ
R_{IN_L}	Single ended input resistance (CANLITEL pin)	-2V≤ $V_{CANLITEL}$≤ 7V	6		50	kΩ
R_{ID}	Differential input resistance	-2V≤ $V_{CANLITEH}$≤ 7V, -2V≤ $V_{CANLITEL}$≤ 7V	12		100	kΩ
M_{RIN}	Input resistance matching 2×(R_{IN_H}-R_{IN_L})/(R_{IN_H}+R_{IN_L})	$V_{CANLITEH}$= $V_{CANLITEL}$= 5V	-3		3	%
I_{LKG_CAN}	Unpowered leakage current	$V_{CANLITEH}$=$V_{CANLITEL}$=5V, V_{CC}=0V	-10		10	μA
t_{DOM_TX}	Dominant time-out		1	2	3	ms
R_{PASS2}	Resistance between CANLITEH pins, CANLITEL pins			5		Ω

ELECTRONIC CHARACTERISTICS (CONTINUED)

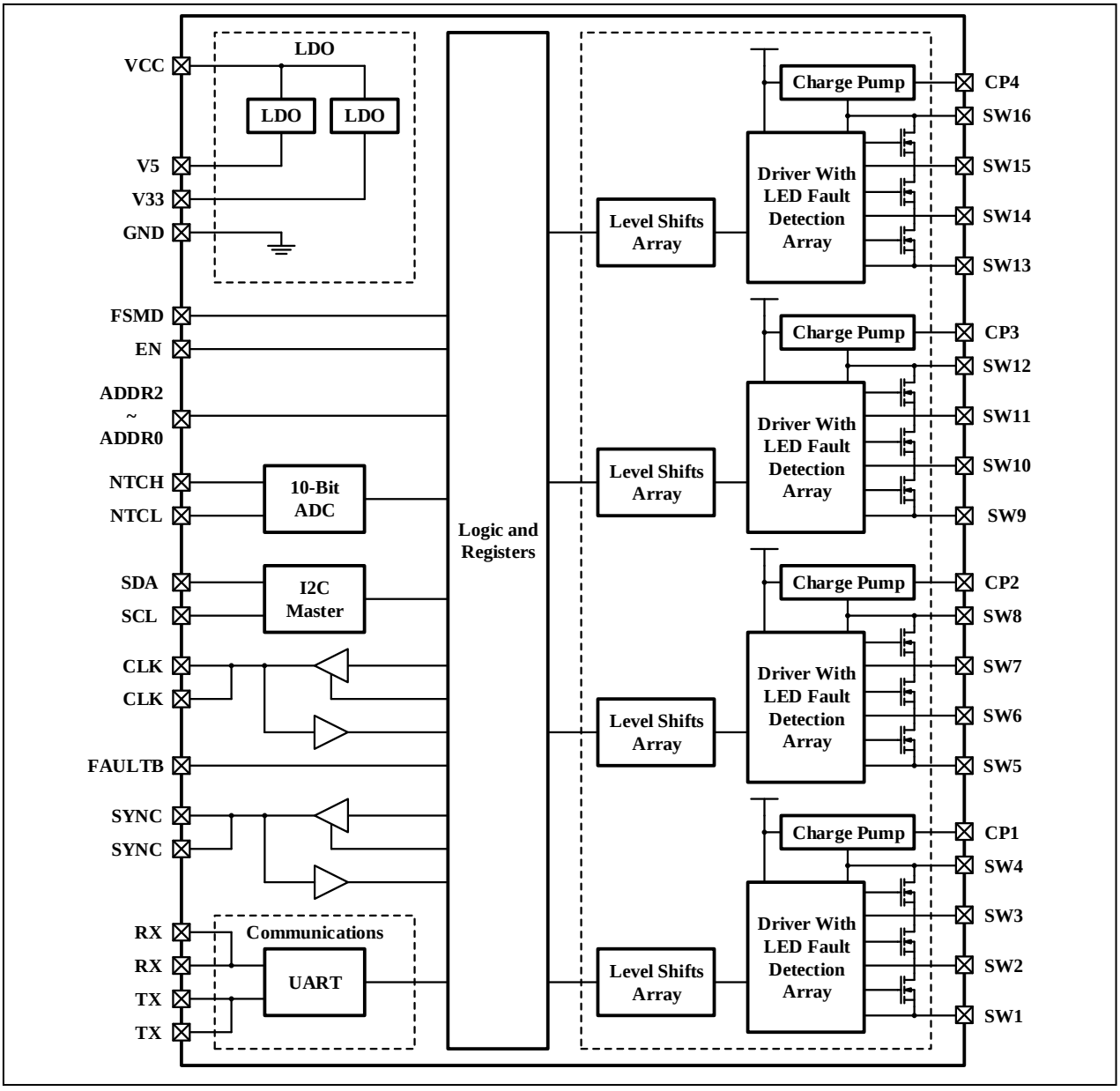
Limits apply over operating junction temperature range -40°C≤ T_J ≤ +150°C. Typical values represent the most likely parametric norm at T_J= 25°C. Unless otherwise noted, V_{CC}= 12V.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
UART Interface (IS32LT3365A only)						
V_{IH_RX}	RX logic “1” input voltage		2			V
V_{IL_RX}	RX logic “0” input voltage				0.7	V
V_{OL_TX}	TX low level output voltage	I_{SINK}=5mA	0		0.3	V
V_{OH_TX}	TX high level output voltage	I_{SOURCE}=-5mA	(V_5 or V_{33})-0.3V		V_5 or V_{33}	V
I_{LKG_UART}	TX, RX leakage current	TX high-z state	-1		1	μA
C_{IN_RX}	TX, RX input capacitance	TX high-z state (Note 4)		5	10	pF
$t_{R\text{-}DO2}$	Rise time of digital output	C_{LOAD}= 50pF, TX pin (Note 4)		2		ns
$t_{F\text{-}DO2}$	Fall time of digital output	C_{LOAD}= 50pF, TX pin (Note 4)		2		ns
$I_{OS\text{-}SRC2}$	Output short source current	TX pin, PIN= 0V (Note 4)		100		mA
$I_{OS\text{-}SNK2}$	Output short sink current	TX pin, PIN= 5V (Note 4)		100		mA
R_{PASS3}	Resistance between RX pins, TX pins			10		Ω

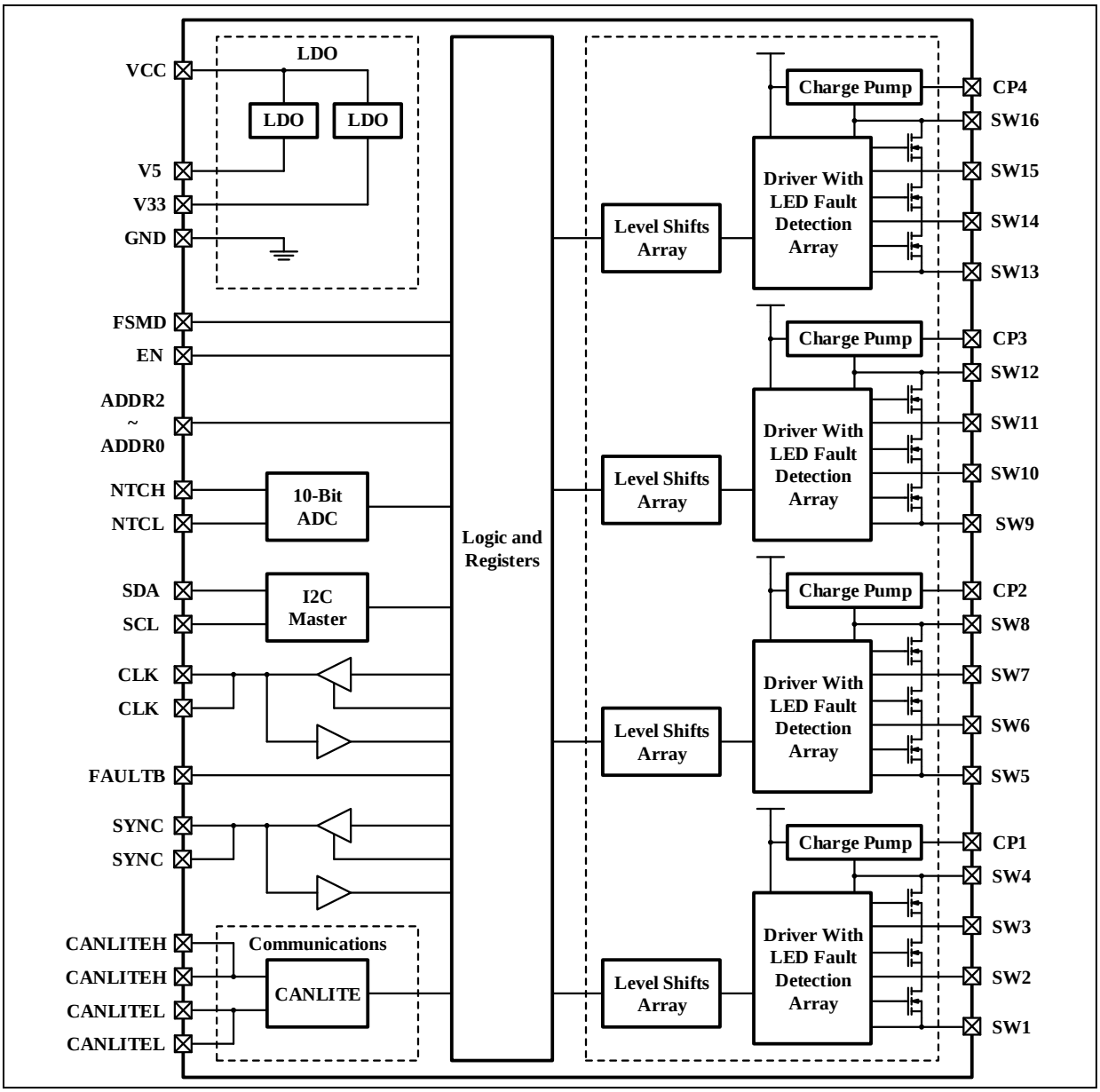
Note 4: Guarantee by design.

8 FUNCTIONAL BLOCK DIAGRAM

IS32LT3365A



IS32LT3365B



9 TYPICAL PERFORMANCE CHARACTERISTICS

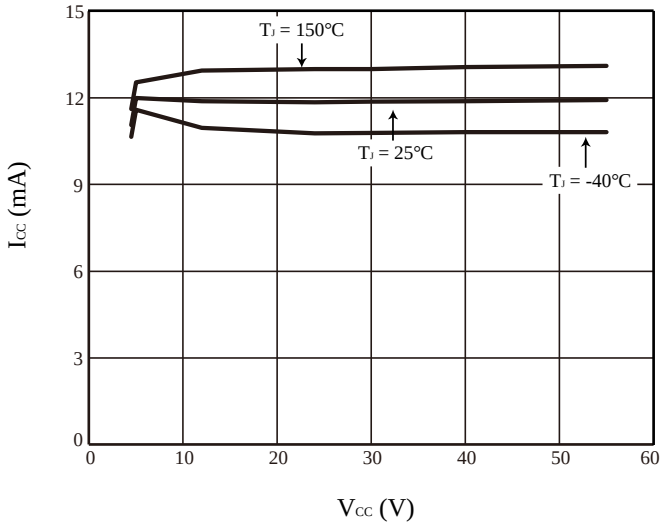


Figure 4 I_{CC} vs. V_{CC}

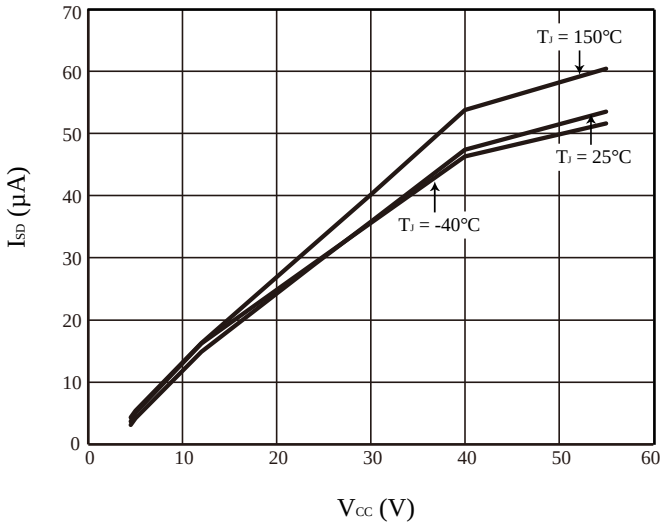


Figure 5 I_{SD} vs. V_{CC}

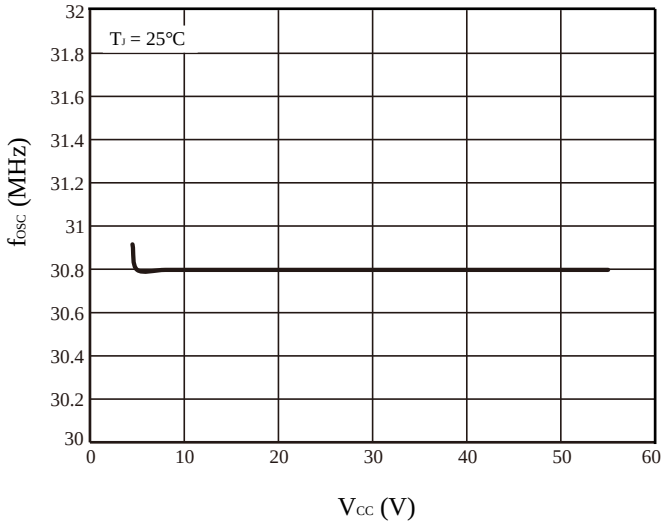


Figure 6 f_{OSC} vs. V_{CC}

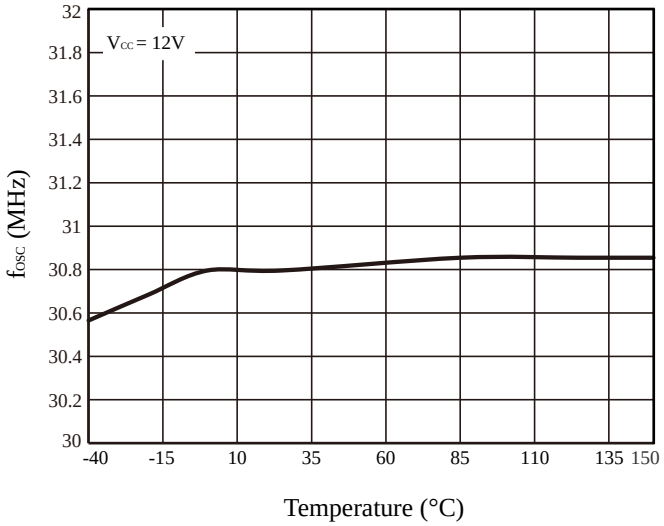


Figure 7 f_{OSC} vs. Temperature

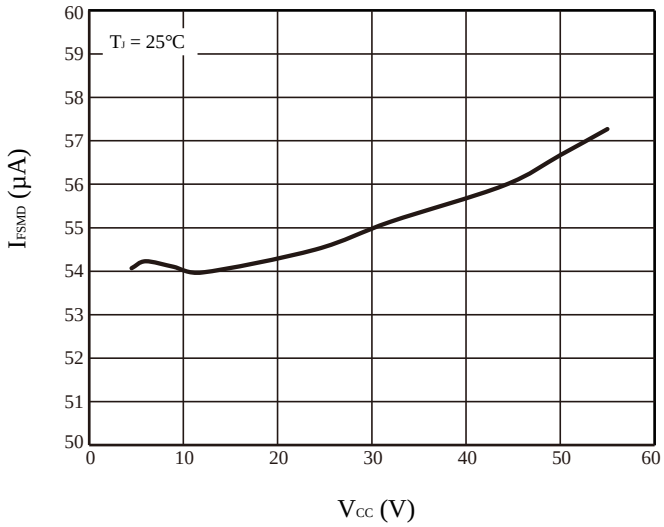


Figure 8 I_{FSMD} vs. V_{CC}

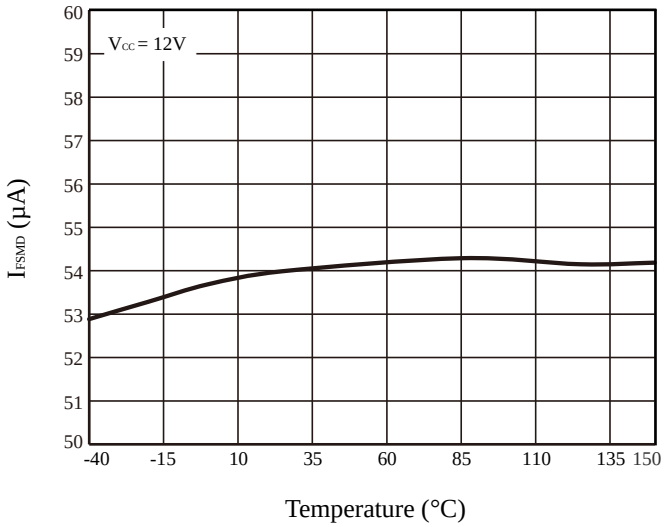


Figure 9 I_{FSMD} vs. Temperature

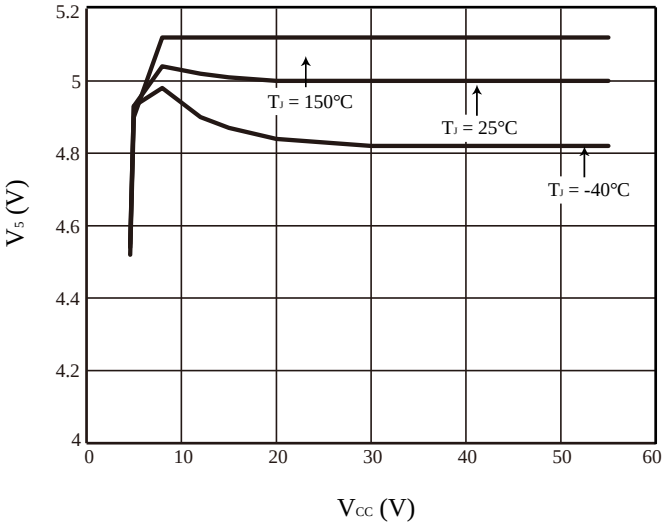


Figure 10 V_5 vs. V_{CC}

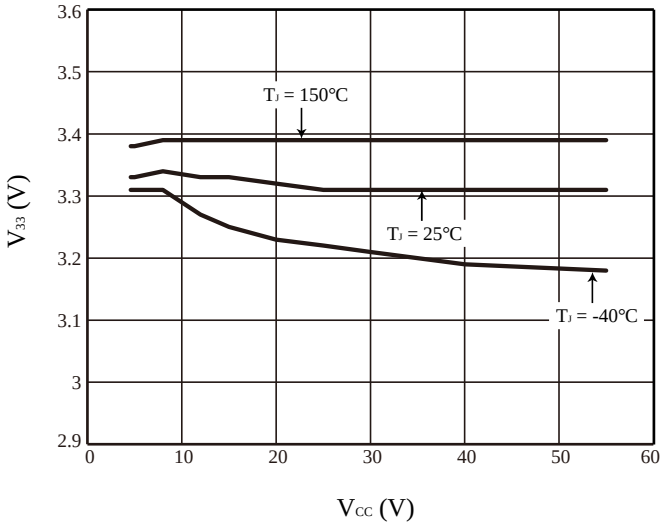


Figure 11 V_{33} vs. V_{CC}

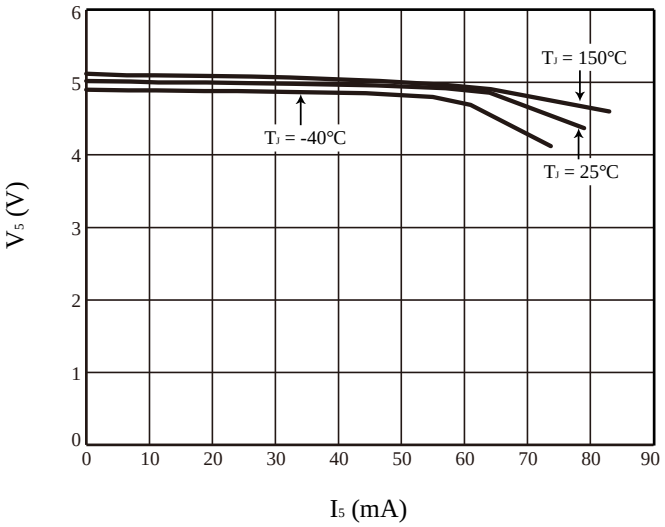


Figure 12 V_5 vs. I_5

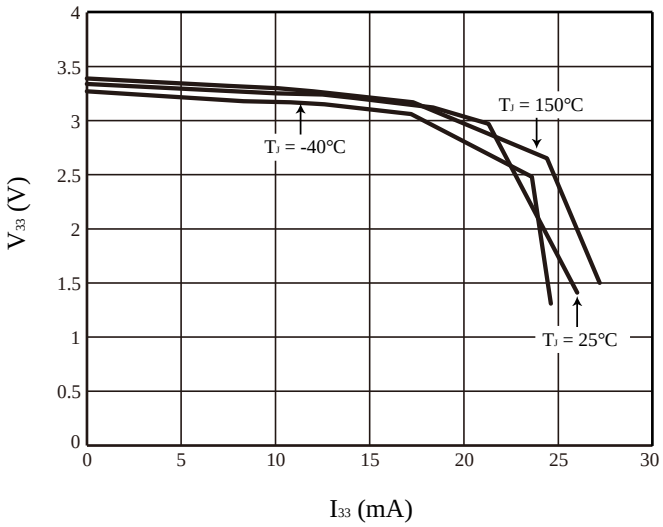


Figure 13 V_{33} vs. I_{33}

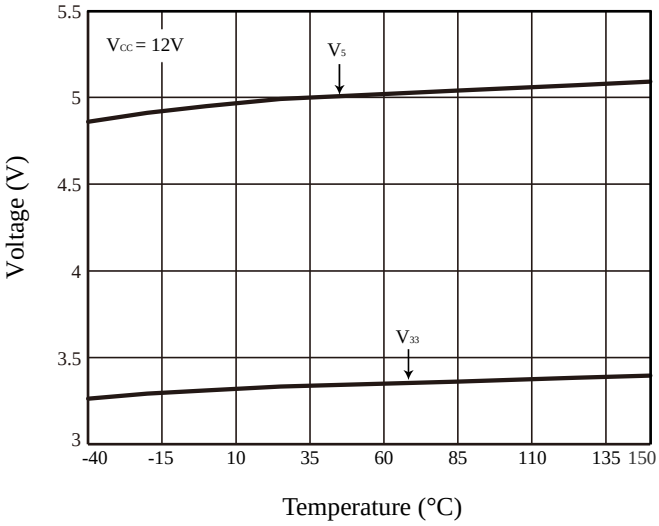


Figure 14 V_5&V_{33} vs. Temperature

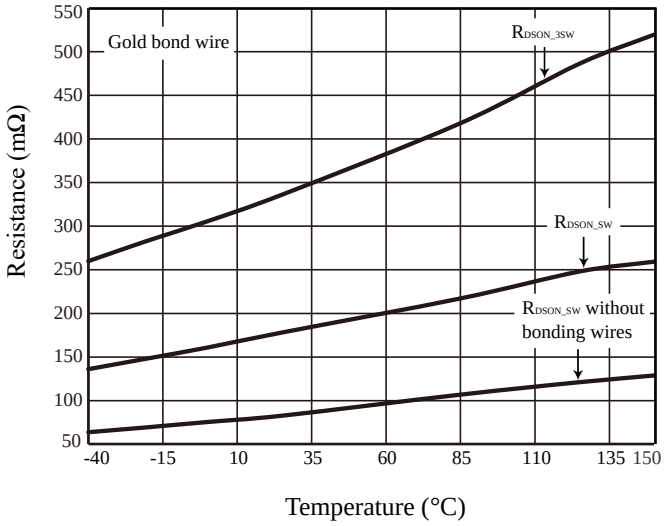


Figure 15 Resistance vs. Temperature

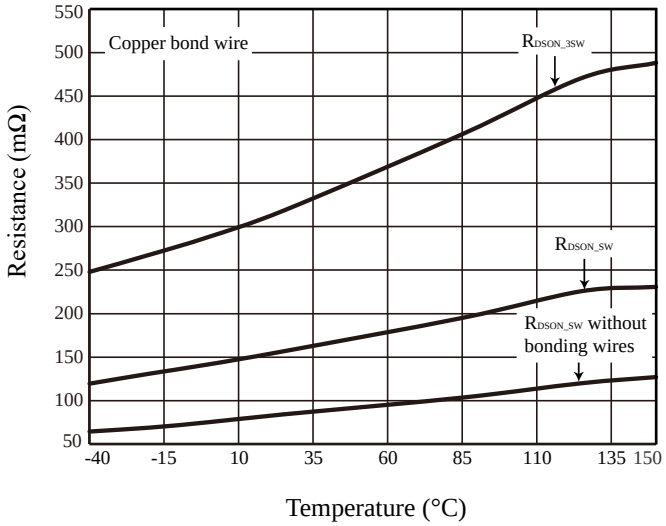


Figure 16 Resistance vs. Temperature

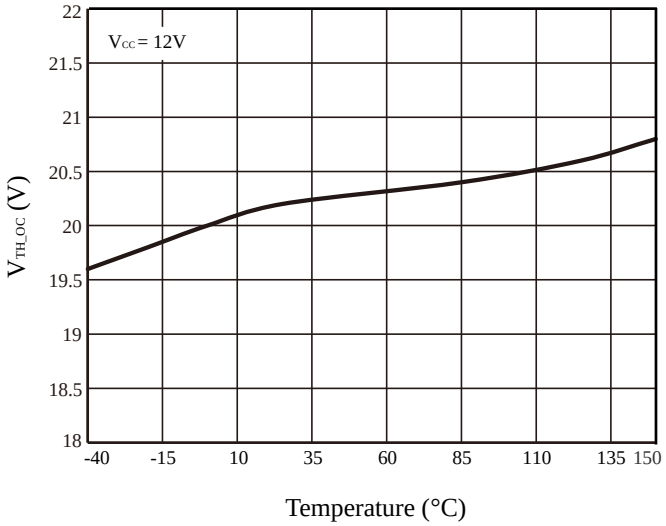


Figure 17 V_{TH_OC} vs. Temperature

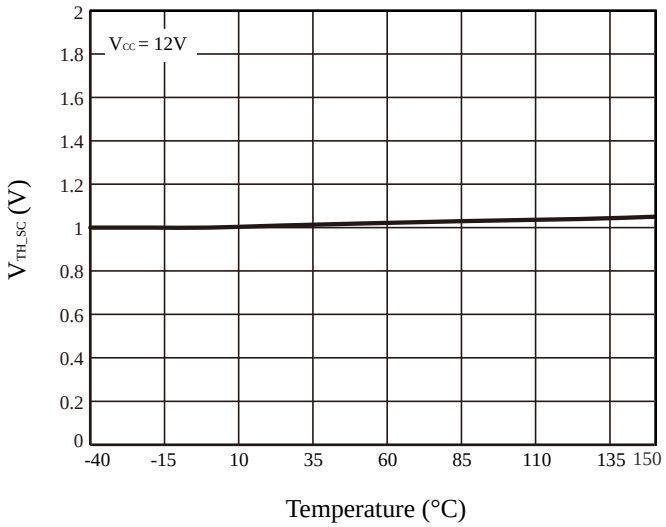


Figure 18 V_{TH_SC} vs. Temperature

10 APPLICATION INFORMATION

10.1 OVERVIEW

The IS32LT3365 device configures a total of 12 integrated NMOS switches, divided into four groups of three-series connections, to bypass individual LEDs for excellent dimming control. The series-connected internal NMOS switches can float up to 55V above ground, as long as the absolute maximum voltage across the Drain/Source of each switch does not exceed 20V. Each switch connects in parallel to one LED or multiple series connected LEDs, creating shunt paths across each LED(s). When the internal NMOS switches are turned off, the corresponding LED(s) light up, and when turned on they bypass the current to shut down the LED(s). All internal NMOS switches can be individually pulse width modulated (PWM) at a programmable frequency, phase shift and duty cycle to individually control the LED(s). In high-power LED array application scenarios, multiple internal switches of the IS32LT3365 device can be programmed to operate in a parallel configuration to bypass one LED string.

In conjunction with an up-steam boost constant voltage pre-regulator and one or multiple buck constant current drivers, the IS32LT3365 matrix LED manager device achieves a fully dynamic LED array solution with each LED individually dimming. The boost constant voltage regulator steps the variable battery voltage up to a stable DC voltage rail. The buck constant current driver(s) take this constant voltage rail to provide constant current to the LED array. This control topology of a LED array is ideally suited for high power LED dynamic lighting applications requires pixel level control. For the best performance, the IS32LT3365 device should be located on the LED board, as close as possible to the LEDs to which it directly connects. With closer proximity, the parasitic inductance and capacitance associated with the cable connection between IS32LT3365 and LEDs are minimized. When PWM dimming with the bypass switches is performed, the voltage and current ringing during each rising/falling transition will be significantly mitigated. For added system reliability, the IS32LT3365 features various fault protections, including LED string open, LED string shorted, single LED shorted (multiple series connected LEDs in parallel with one switch), over temperature, CRC error, LDO overvoltage, I^2C master communication failure, and watchdog timeout (fail-safe mode) conditions, for robust operation. Detection of these failures is reported by a dedicated fault reporting pin, FAULTB. There are dedicated flag bits in registers for each failure, which can be read back by the external host MCU through the interfaces. To optimize EMI performance, the device features spread spectrum on the internal PWM base clock and PWM base clock to spread the total electromagnetic emitting energy into a wider range that significantly degrades the peak energy of EMI. In addition, the NMOS switch ON/OFF transitions during PWM dimming has a programmable slew rate control to mitigate EMI and the current overshoot due to the output capacitor rapid discharging of the up-stream buck constant current driver.

The IS32LT3365 provides two types of interfaces, UART (IS32LT3365A) and CANLITE (IS32LT3365B), between a host MCU and multiple slave IS32LT3365 devices. The device address can be configured by the three address pins. The interfaces receive data to control all internal NMOS switches and transmit fault information back to the host MCU. The CANLITE interface allows long distance off-board communication between boards in the same lamp module (as shown in Figure 19). While the UART interface allows on-board communication. The UART interface along with an external industrial-standard CAN transceiver also allows long distance off-board communication with a host MCU placed outside of the lamp module (as shown in Figure 20). Based on the CAN physical layer, it can achieve excellent EMS and EMI performance. The embedded CRC correction ensures robust communication in automotive environments. These interfaces are easily supported by most MCUs available in the market.

To further increase robustness, the device will automatically switch to a fail-safe mode in case of communication loss, such as, host MCU failure or broken communication cables. The device supports programmable fail-safe mode which can be configured by the FSMD pin.

The IS32LT3365 device includes a 10-bit ADC with two external multiplexed general-purpose inputs, which can be used for system temperature compensation, binning/coding, etc. Additionally, the IS32LT3365 also contains an I^2C master that allows the host MCU to access an on-board EEPROM, which stores lighting module configuration data, through the UART or CANLITE interface.

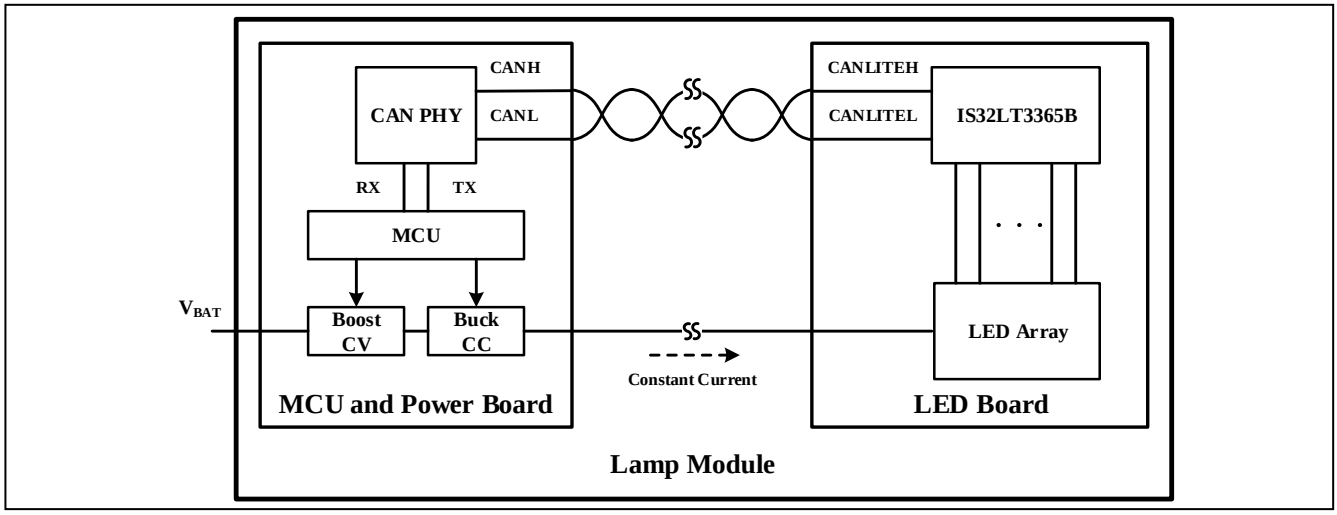


Figure 19 CANLITE Interface for Long Distance Intramodular Communication

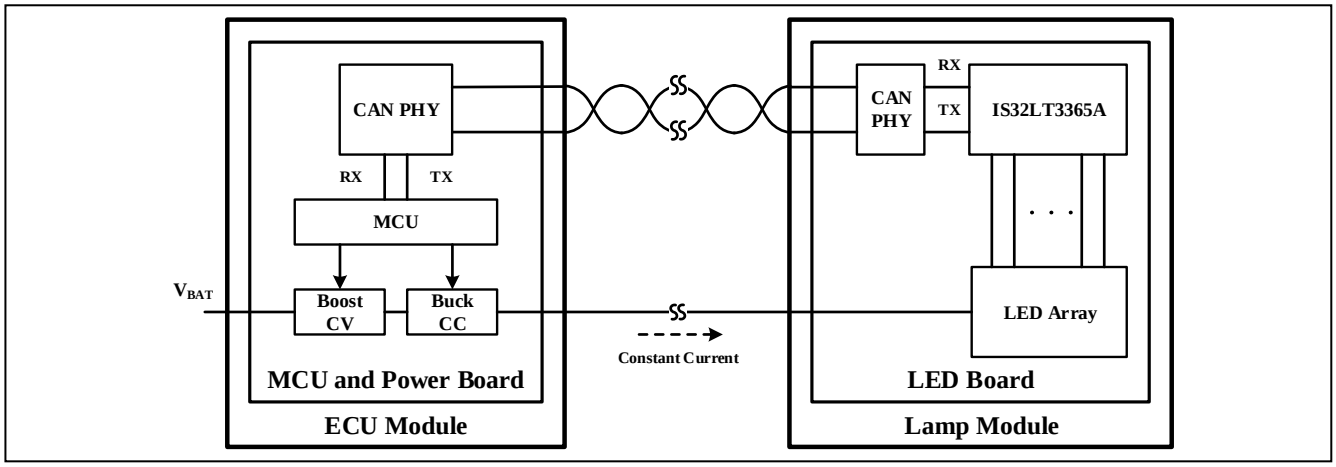


Figure 20 UART Interface with External CAN Transceiver for Long Distance Intermodular Communication

10.2 INTERNAL BYPASS SWITCHES

The IS32LT3365 device consists of four groups of three-series connected bypass NMOS switches. When each NMOS switch is driven to the off state, the current flows through the parallel-connected LED(s), turning the LED(s) on. Conversely, when each NMOS switch is driven to an on state, the current is shunted by the NMOS switch, turning the LED(s) off. Therefore, PWM controlling the gate of each NMOS switch can individually modulate the brightness of the parallel connected LED(s) by the duty cycle.

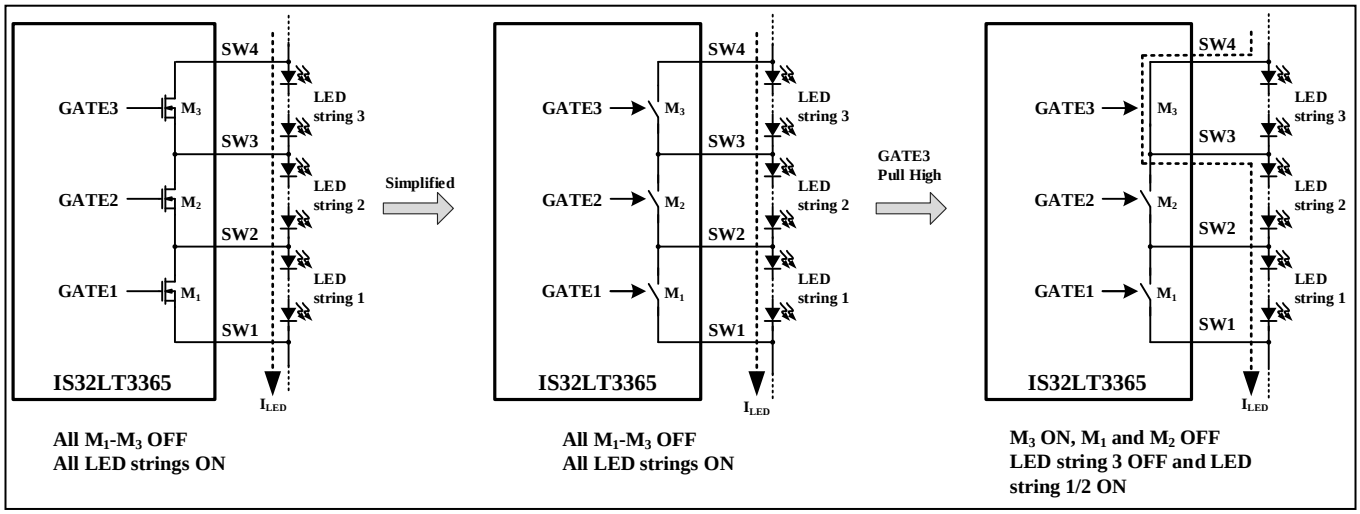
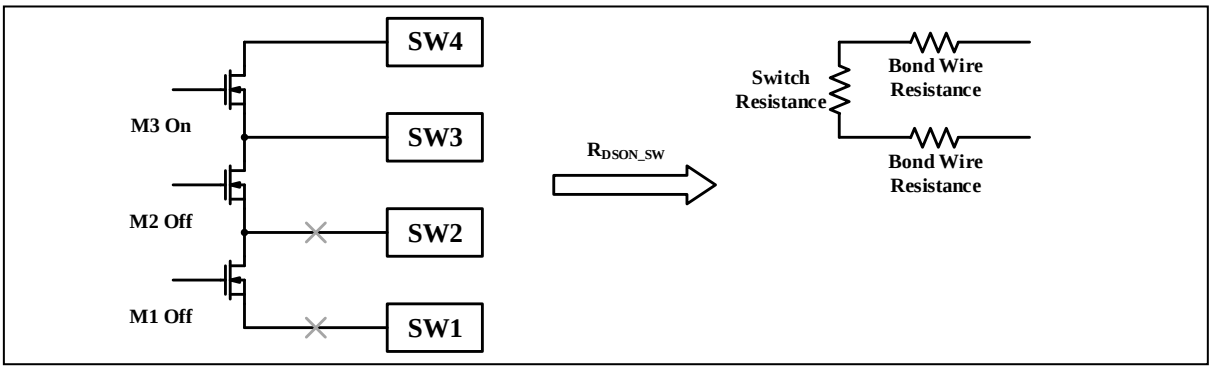


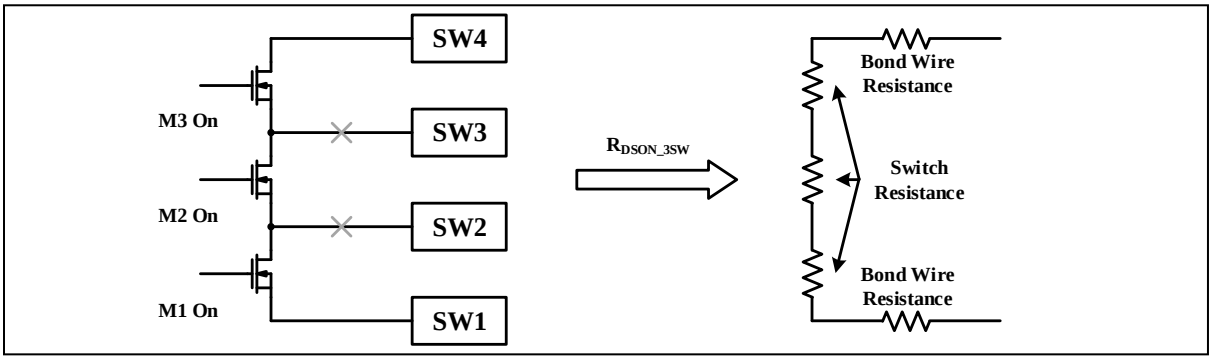
Figure 21 NMOS Shunt Dimming (Group-S1 switches as example)

Each single switch (connected between SWx and SWx+1) has a measurable typical R_{DSON_SW} value of 190mΩ. This

measurement includes the actual on-resistance of the switch and the resistance of the two internally connected bond wires. As shown in Figure 22(a). When multiple series switches are on, the effective resistance is not simply the number of channels multiplied by 190mΩ, due to the absence of two conducting bond wires for every series connected switch. The on-resistance of the 3×series-connected switches (R_{DSON_3SW}) is specified in the Electrical Characteristics table. This value includes three switches on-resistances and the resistance of the bond wires at each end of the series connected switches. As shown in Figure 22(b).



(a) R_{DSON_SW}



(b) R_{DSON_3SW}

Figure 22 Bypass Switch On-resistance

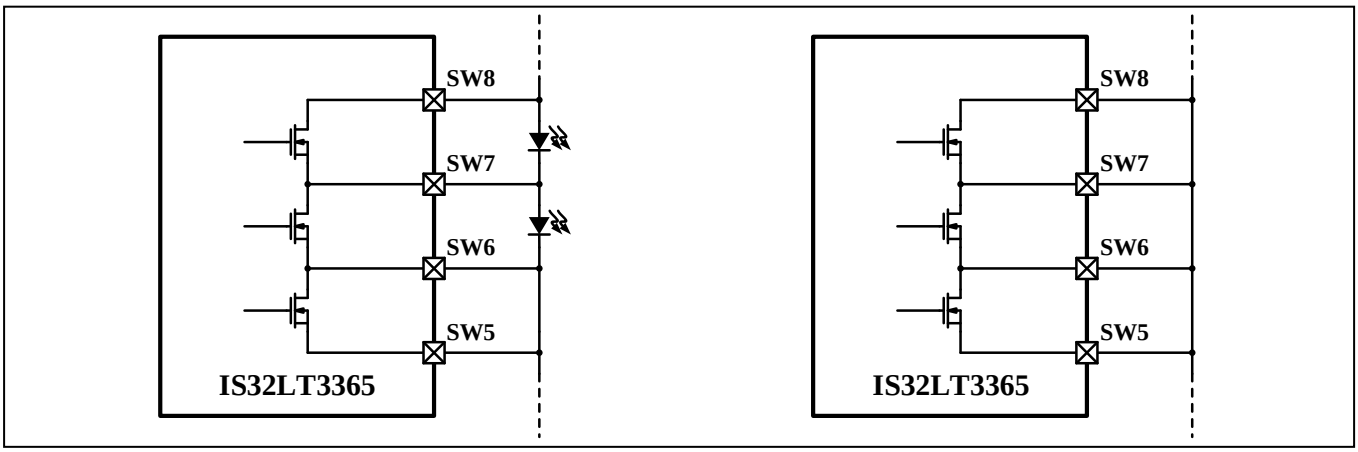
The dominant power loss mechanism in the IS32LT3365 device is the I^2R loss through the switches. Other power loss sources are typically less than 200mW. When calculating the power dissipation of the IS32LT3365 device switches, refer to the table below for the appropriate estimation of the power loss. It is important to note that the power dissipation depends on the PWM duty cycle. When PWM dimming is applied to the LEDs with duty cycle D, the effective switch resistance for power dissipation calculation is:

$$R_{DSon\_EFF} = (1 - D) \times R_{DSon} \qquad (1)$$

Table 1 Total R_{DSON} of The Switches

Switches in Series	Maximum Total R_{DSON} (mΩ)
1	R_{DSON_SW}
2	(R_{DSON_3SW} - R_{DSON_SW})/2 + R_{DSON_SW}
3	R_{DSON_3SW}
6	2×R_{DSON_3SW}
9	3×R_{DSON_3SW}
12	4×R_{DSON_3SW}

In practice, if any switch is unused, the corresponding bit in the ENPWM register (78h/79h) and/or the corresponding PWM WIDTH register must be set to “0” to disable the channel. And the switch should be shorted by an external physical connection on the PCB board.



(a) One Switch Unused (b) One Group Switches Unused

Figure 23 Switch Unused Example

10.3 PARALLEL SWITCHES

The IS32LT3365 device can be configured as switches connected in parallel to support high current LEDs and decrease power loss. The physical parallel connection must be performed externally to the IS32LT3365. The parallel configuration of the IS32LT3365 enables simultaneous PWM switching and fault handling of parallel switches. The IS32LT3365 device includes 4 groups of S1, S2, S3 and S4 with 3 series-connected switches. The combinations of LED strings that may be paralleled are:

• None (each group of bypass switches is independent from the others)

• One pair (S1 and S2 are connected in parallel, S3 and S4 are independent)

• Two pairs (S1 and S2 are connected in parallel, and S3 and S4 are connected in parallel)

• All (S1, S2, S3 and S4 are all connected in parallel)

Upon power-up, the default parallel configuration setting of all switches None; all switch groups are independent. The host MCU must program the PARLED register (71h) to set the parallel configuration to meet the physical parallel connection.

Parallel operation also affects fault management. When the switches are paralleled, there is a possibility that one switch senses an LED open condition and turns on before the other parallel switches do. If this situation were not addressed, the switch that clamps overvoltage condition continues to be the only switch conducting a potentially large current. Therefore, the programming of the PARLED register also configures the combinations of faults, that cause the gate drivers of all parallel switches to turn on in an LED open condition. There is a small delay due to synchronizing the incoming faults with the internal clock domain, after this, all parallel switches that have an LED open condition are immediately turned on to share the LED currents.

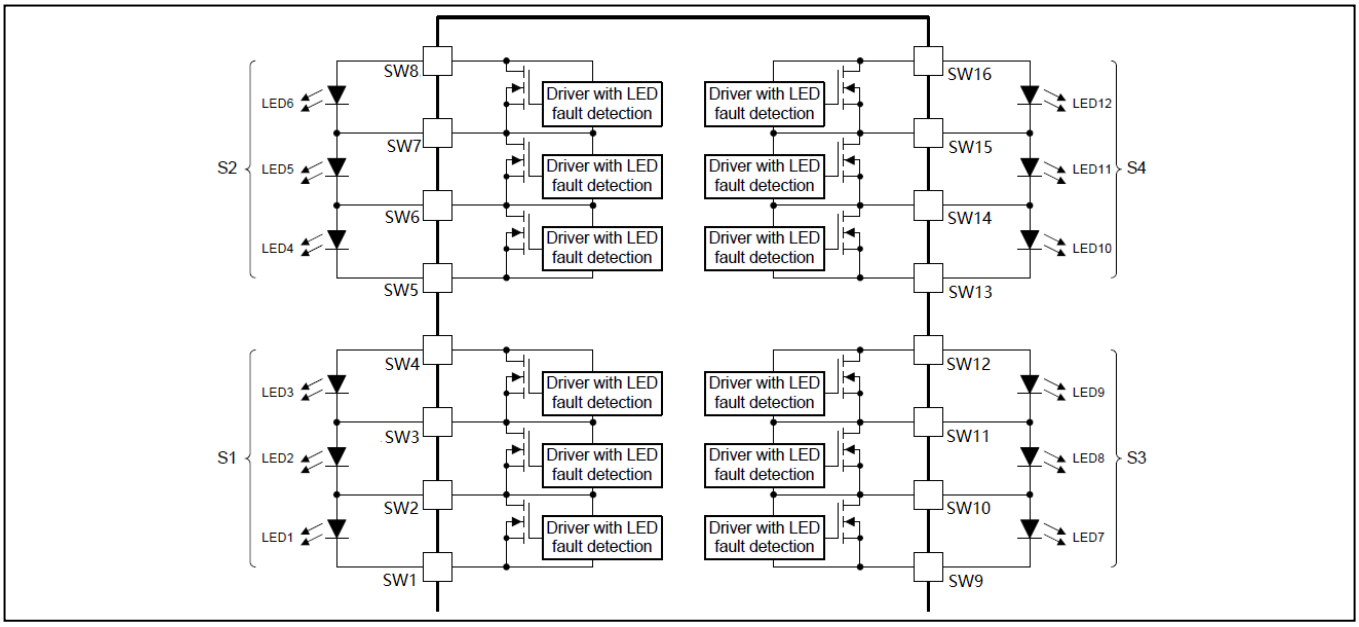


Figure 24 Bypass Switch Groups

10.4 PWM CONTROL

The IS32LT3365 device offers 10-bit phase shiftable PWM dimming for each LED. The PWM phase shift and PWM pulse width are respectively programmed by the PHASEx and WIDTHx registers (00h~6Fh). There is an internal 10-bit PWM period counter (TCNT), that counts continuously from 0 to 1023 and wraps back to 0 based on the PWM base clock pulse, to determine the PWM period, t_{PWM}. The PWM base clock can be either a divided-down signal from the integrated oscillator (SYSCLK, typical 30.72MHz) or a clock signal applied to the CLK pin, that can be selected by CLK_MSI register (7Ch). The PWM base clock divider is comprised of two dividers in series, that can be respectively programmed by PTBASE bits and PTCNT bits in PWMTICK register (82h).

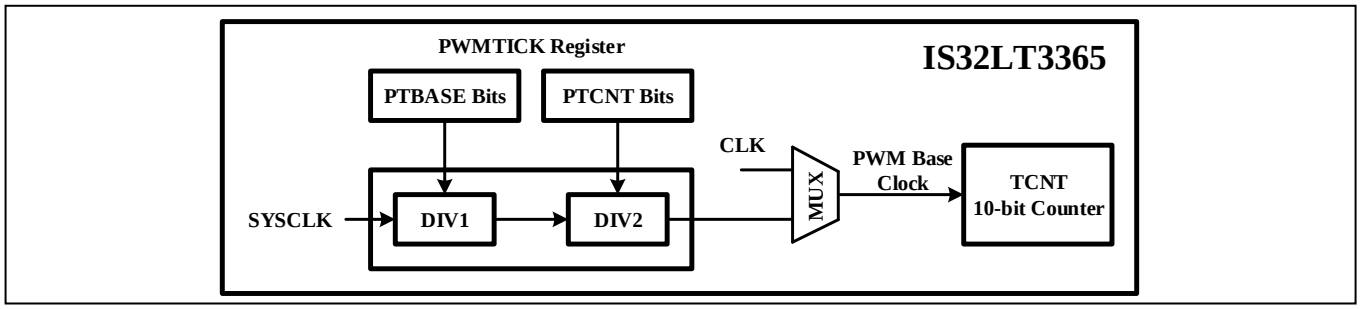


Figure 25 PWM Control and TCNT

There is an inherent PWM turn on/off delay time and PWM slew rate control during PWM dimming. A high frequency PWM has a shorter period of time that will degrade the PWM dimming linearity. Therefore, a low frequency PWM is good for achieving a better dimming contrast ratio. The recommended PWM frequency is in the range of 300Hz ~ 1kHz, and the default PWM frequency (about 468Hz) is a good choice for most applications.

10.4.1 PWM Width And Phase Shift

The PSON bit in the SYSCFG register (80h) is set to “1”:

The phase shift is applied to LED turn on times. When TCNT reaches the programmed PHASEx value for a given channel, the corresponding LED(s) turn on (the switch turns off). The LED(s) remain on until TCNT reaches the value of (PHASEx+WIDTHx), then the corresponding LED(s) turn off (the switch turns on). The PWM period t_{PWM} equals 1024 × PWM base clock period.

The figure below shows examples of PWM width and phase shift implementation as PSON= 1, using values of PHASEx= 0 and 360 with WIDTHx= 600. In both cases, the WIDTHx value determines the LED on time (the switch off time).

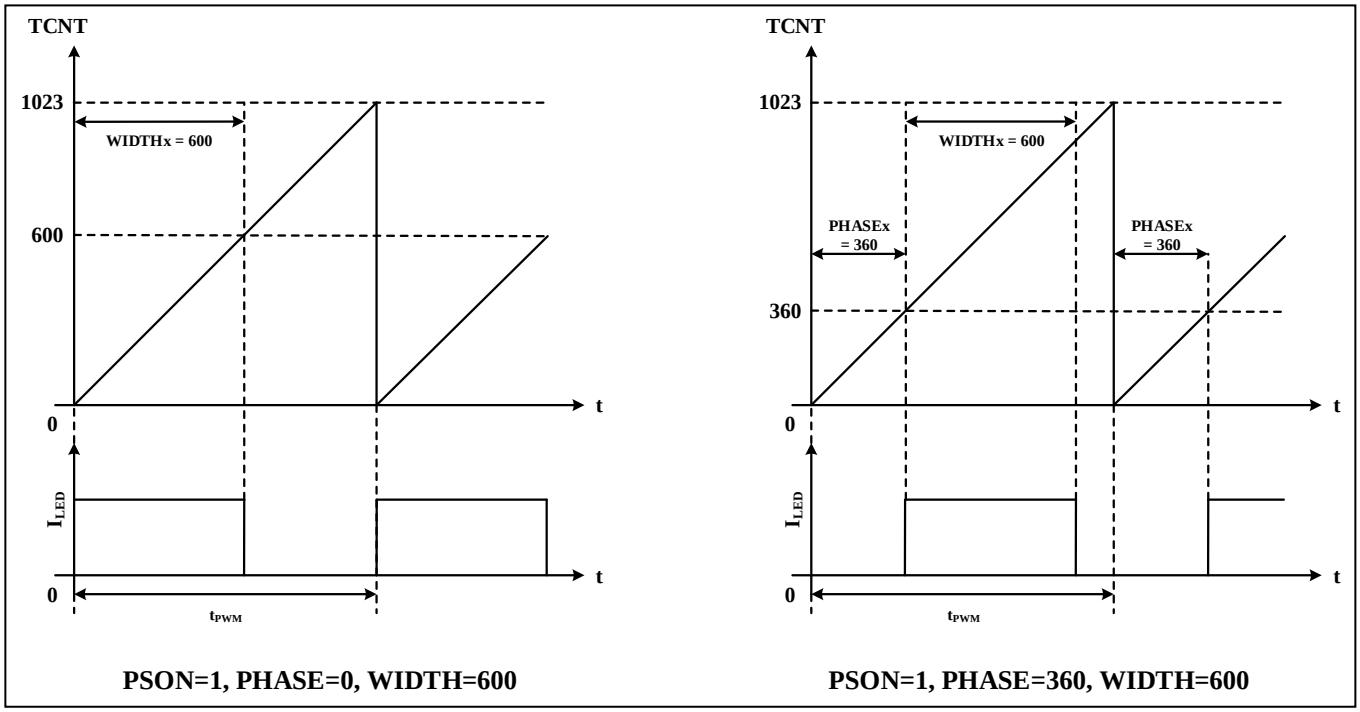


Figure 26 PWM Width and Phase Shift Implementation as PSON=1

The PSON bit in the SYSCFG register (80h) is set to “0”:

The phase shift is applied to LED turn off times. When TCNT reaches the programmed PHASEx value for a given channel, the corresponding LED(s) turn off (the switch turns on). The LED(s) remain off until TCNT reaches the value of (PHASEx+1023-WIDTHx), then the corresponding LED(s) turn on (the switch turns off). The PWM period t_{PWM} equals 1024 × PWM base clock period.

The figure below shows examples of PWM width and phase shift implementation PSON=0, using values of PHASEx = 0 and 360 with WIDTHx = 600. In both cases, the WIDTHx value determines the LED on time (the switch off time).

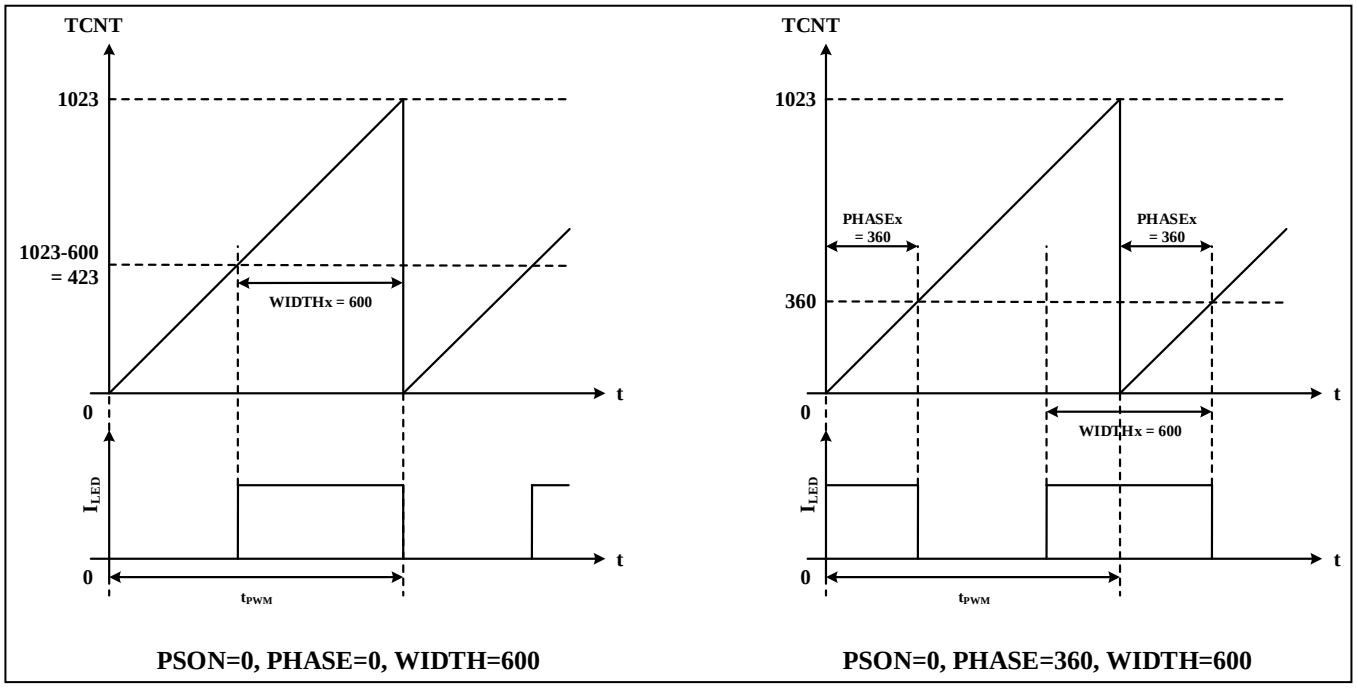


Figure 27 PWM Width and Phase Shift Implementation as PSON=0

The LED turns on (or turns off) time can independently be programmed for each LED via the PHASEx registers. The amount of phase shift between LED turn on (or turn off) times affects the instantaneous current drawn from the buck constant current driver. It is recommended to apply the phase shift to each switch such that the turn on (or turn

off) times of all the LEDs are evenly distributed in one PWM period. In the applications, the phase shift applied to the LED turn off time (PSON=0) can significantly reduce the LED current overshoot caused by the output capacitor (across the LED strings) of the buck constant current driver rapid discharging.

The PSON bit and PHASEx settings should be programmed at initialization and remain static during the PWM dimming operation.

To achieve a duty cycle of 0% (LED fully off), the register WIDTHx can be set to 0. When TCNT reaches the PHASEx register value, the corresponding LED turns off and remains off. Another easy way is to set the corresponding ENPWM bit in ENPWML and ENPWMH registers to “0”.

To achieve a duty cycle of 100% (LED fully on), the register WIDTHx must be set to 1023. As a result, the programmed brightness of 1023/1024 is not available.

Table 2 PWM Duty Cycle Mapping

PWM Duty Cycle (%)	WIDTHx [9:0]
0	0
0.1	1
…	…
99.7	1021
99.8	1022
99.9	Unavailable
100 (fully on)	1023

10.4.2 PWM Synchronization

Upon power-up, the TCNT counter is reset to 0. The TCNT counter is incremented by the PWM base clock, which is either a divided-down signal from the integrated oscillator (SYSCLK, typical 30.72MHz) or a clock signal applied on the CLK pin, which can be selected by the CLK_MSI register. To synchronize the PWM of multiple IS32LT3365 devices, the following condition must be met:

• All devices must be clocked by the same clock source from an IS32LT3365 master’s CLK pin.

The pairs of CLK pins on the IS32LT3365 device are feed-through pins (internally connected by low impedance metal), and either pin may be used to connect the IS32LT3365 device to the network. Feed-through pins enable the use of a metal core board with single layer routing. The CLK is a clock input/output pin with two register bits (INDEPEN and MS_SL) in the CLK_MSI register to configure it. If INDEPEN is set to “0”, the CLK pin’s input/output function is enabled. Otherwise, the CLK pin is disabled and IS32LT3365 device operates in independence mode (no PWM synchronization), which ignores the CLK pin’s clock signal and takes the internal system clock SYSCLK to generate the PWM base clock. In independence mode, the CLK pin is high impedance. If INDEPEN and MS_SL are set to “0”, the IS32LT3365 device is in master mode and drives the output buffer on the CLK pin, following its PWM base clock pulse. The resulting CLK output signal can be applied to the CLK pins of other IS32LT3365 devices in slave mode. If INDEPEN is set to “0” and MS_SL is set to “1”, the CLK pin is high impedance and operates as an input for slave mode. The IS32LT3365 device in slave mode will take the clock signal on the CLK pin as its PWM base clock. CLK is a feed-through signal that may be tied to the next IS32LT3365 devices in order to synchronize the PWM base clock of multiple devices with each other.

If synchronization is not implemented, INDEPEN should be set to “1”. Please note that the CLK_MSI register only supports single device write but not broadcast write.

It’s not allowed that more than one master mode devices to tie their CLK pins together, otherwise one push-pull state will be shorted by other push-pull states and the devices’ operation will be abnormal.

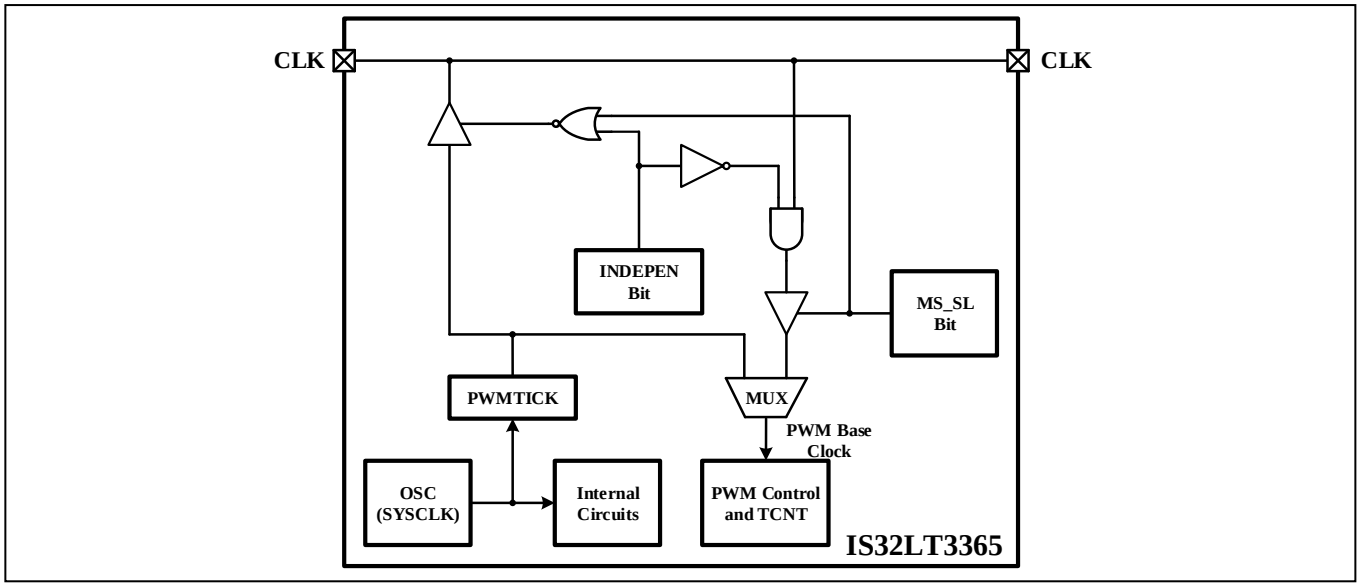


Figure 28 CLK Pin Control

Assuming the above conditions are met, the IS32LT3365 devices may be synchronized by either of two methods: Hardware Synchronization (SYNC pins cascading) or Software Synchronization (PWM Synchronization Command).

Hardware Synchronization:

The pairs of SYNC pins on the IS32LT3365 device are feed-through pins (internally connected by low impedance metal), and either pin may be used to connect the IS32LT3365 device to the network in order to synchronize multiple devices with each other. Feed-through pins enable the use of a metal core board with single layer routing. The SYNC is a synchronization input/output pin, and there are two synchronization register bits (SYNCOEN and SYNCPEN) in the SYSCFG register (80h) to configure it. If SYNCOEN is set to “1”, the IS32LT3365 drives the output buffer on the SYNC pin. Otherwise, the SYNC pin driver is tri-stated (high impedance) and operates as an input for slave mode. If SYNCOEN is set to “0”, a low-to-high transition on the SYNC pin for at least two PWM base clock periods resets both TCNT and the PWM base clock to 0. If SYNCOEN and SYNCPEN are both set to “1”, the IS32LT3365 device is in master mode and generates a high pulse that is one-half of a PWM period on the SYNC pin when TCNT and the PWM base clock are about to roll over to 0. The resulting SYNC signal can be applied to other IS32LT3365 devices in slave mode to achieve PWM hardware synchronization.

If hardware synchronization is not implemented, SYNCOEN should be set to "1" and SYNCPEN should be set to "0". This logic sets the SYNC pin low for independence mode to provide a strong pulldown on the SYNC line, preventing SYNC pin from experiencing EMI noise interference. Please note that the SYNCOEN and SYNCPEN bits only support single device write but not broadcast write.

It’s not allowed that a master mode device ties its SYNC pin to other master mode devices or independence mode devices, otherwise one push-pull state will be shorted by other push-pull states or strong pulldown states, and the devices’ operation will be abnormal.

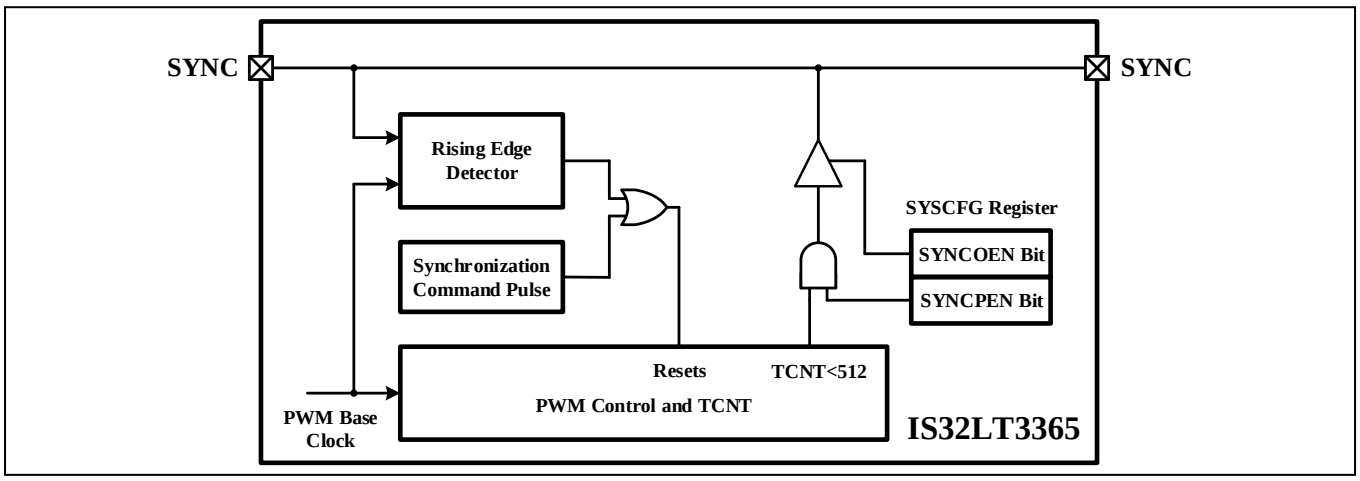


Figure 29 SYNC Pin Control

Table 3 PWM Hardware Synchronization Register Configuration

Operation Mode	CLK Pin Configuration		SYNC Pin Configuration	
	INDEPEN Bit	MS_SL Bit	SYNCOEN Bit	SYNCPEN Bit
Independence Mode (No PWM Synchronization)	1	0 or 1	1	0
Master Mode (PWM Synchronization)	0	0	1	1
Slave Mode (PWM Synchronization)	0	1	0	0 or 1

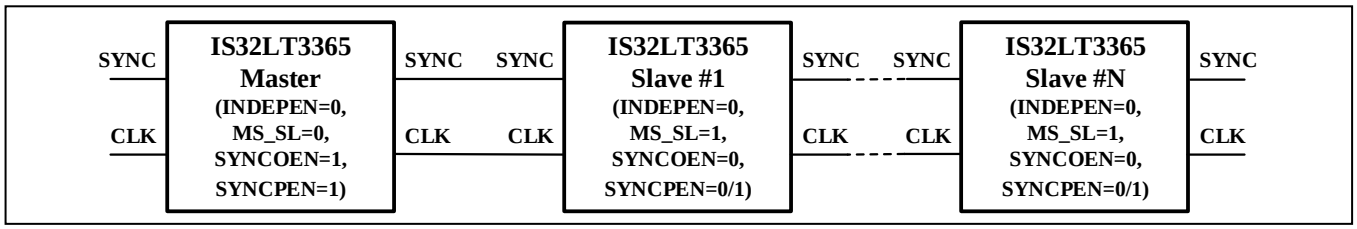


Figure 30 PWM Hardware Synchronization Connection

Software Synchronization:

The TCNT counter and the PWM base clock can both be reset to 0 at any time by issuing a broadcast PWM Synchronization Command frame (special command). Due to interface bit sampling variability, synchronization is achieved within 4 system clock cycles between IS32LT3365 devices.

Table 4 PWM Software Synchronization Register Configuration

Operation Mode	CLK Pin Configuration		SYNC Pin Configuration	
	INDEPEN Bit	MS_SL Bit	SYNCOEN Bit	SYNCPEN Bit
Independence Mode (No PWM Synchronization)	1	0 or 1	1	0
Master Mode (PWM Synchronization)	0	0	1	0
Slave Mode (PWM Synchronization)	0	1	1	0

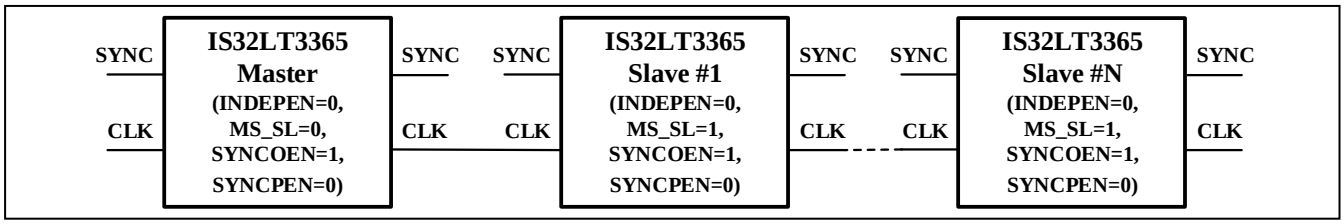


Figure 31 PWM Software Synchronization Connection

Both CLK and SYNC pins have tri-state, push-pull for master mode, strong pulldown for independence mode or high impedance input for slave mode. To prevent the push-pull state of one device is shorted by push-pull or strong pulldown of other devices, please follow the below steps to configure the PWM synchronization operation:

1) All devices are in independence mode in the initialization state.
2) Single device write command frames configure all devices to slave mode.
3) Single device write command frame configures one device to master mode.

Note that if the push-pull state is shorted by other push-pull or strong pulldown state, the device operation might be abnormal. For instance, when all devices are still in independence mode, the host MCU configures one device to master mode.

10.4.3 PWM Switch On/Off Slew Rate Control

The switching slew rate of each group of switches (three series connected switches) can be independently controlled and programmed via SLEWRATE register (70h). The slew rate of the switches is regulated by adjusting the gate driver strength. The slew rate of each group of switches (3 series connected switches) can be programmed through two bits, which provides four levels slew rate, typical 2μs, 12μs, 25μs and 50μs. A slow slew rate control significantly mitigates EMI and the current overshoot due to the output capacitor rapid discharging of the up-stream buck driver. However, the slow slew rate control degrades the PWM dimming linearity, especially the PWM frequency is high. Please carefully select a proper slew rate based on the measurement of the current overshoot in application. The recommended slew rate is either 12μs or 25μs for most applications.

10.4.4 Spread Spectrum

To optimize the EMI performance, the IS32LT3365 includes a spread spectrum feature on the PWM base clock. Spread spectrum can spread the total electromagnetic emitting energy into a wider range, significantly degrading the peak energy of EMI. With spread spectrum, the EMI test can be passed with a smaller size and lower cost filter circuit. Spread spectrum is enabled/disabled by the SSCEN bit and the frequency is selected by the SSC[1:0] bits in the SSCCFGA register (7Bh). When the spread spectrum function is enabled, the PWM frequency must be set to at least two times of the spread spectrum frequency to avoid flickering issue. Therefore, the default value of 125Hz (Typ.) is a good choice for most applications.

10.5 FAULT PROTECTION

10.5.1 Fault Reporting

For added system reliability, the IS32LT3365 integrates various fault detection for LED string open/short, single LED shorted, over temperature, LDO overvoltage, I²C master communication failure, CRC error, watchdog timeout, and PWM feedback duty cycle error conditions. The open drain pin FAULTB can be used to report fault conditions. If any fault occurs, the corresponding bit in the FAULT_TYPE register will be set to “1” and the FAULTB pin will go low to report the fault condition. When it is monitored by a host MCU, a pull-up resistor (47kΩ recommended) from the FAULTB pin to the supply of the host MCU is required.

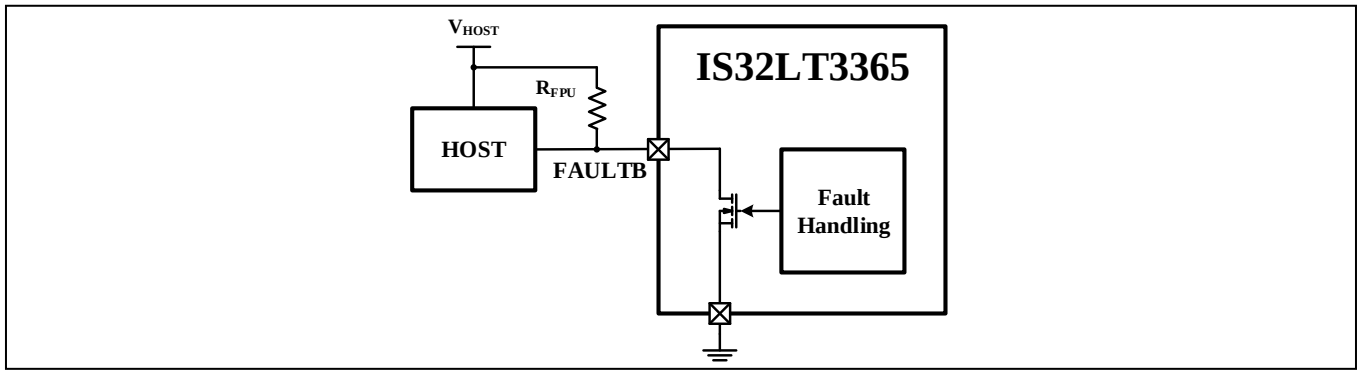


Figure 32 Host MCU Monitors The Fault Reporting

The IS32LT3365 provides fault masking capability using masking registers (96h and 97h). The device is capable of masking faults by fault type. The fault masking does not disable fault detection features but only prevents fault reporting to the FAULTB pin output. The table below lists the detailed description for each fault mask.

Table 5 Fault Masking

Fault Detected	Fault Flag Enable	Fault Flag State	FAULTB Pin Reporting Mask	FAULTB Pin State
LED string open	LEDx_OF_EN bit set to “1”	OPEN_FAULTx=1, OPENF=1	OPENFM bit set to “1”	Pulled low
			OPENFM bit set to “0”	No action
	LEDx_OF_EN bit set to “0”	OPEN_FAULTx=1, OPENF=0	OPENFM bit set to “1”	No action
			OPENFM bit set to “0”	No action
LED string short	LEDx_SF_EN bit set to “1”	SHORT_FAULTx=1, SHORTF=1	SHORTFM bit set to “1”	Pulled low
			SHORTFM bit set to “0”	No action
	LEDx_SF_EN bit set to “0”	SHORT_FAULTx=1, SHORTF=0	SHORTFM bit set to “1”	No action
			SHORTFM bit set to “0”	No action
V5 overvoltage	-	V5OVF=1	V5OVFM bit set to “1”	Pulled low
			V5OVFM bit set to “0”	No action
V33 overvoltage	-	V33OVF=1	V33OVFM bit set to “1”	Pulled low
			V33OVFM bit set to “0”	No action
Thermal shutdown	-	TSDF=1	TSDFM bit set to “1”	Pulled low
			TSDFM bit set to “0”	No action
Thermal alarm	-	OVTMPF=1	OVTMPFM bit set to “1”	Pulled low
			OVTMPFM bit set to “0”	No action
CRC error	-	CRCF=1	CRCFM bit set to “1”	Pulled low
			CRCFM bit set to “0”	No action
Communication loss	-	CMWF=1	CMWFM bit set to “1”	Pulled low
			CMWFM bit set to “0”	No action
I^2C communication failure	-	I2CF=1	I2CFM bit set to “1”	Pulled low
			I2CFM bit set to “0”	No action
Loopback verification	-	DUTYF=1	DUTYFM bit set to “1”	Pulled low
			DUTYFM bit set to “0”	No action

Table 6 Fault Action (Both Normal Mode and Fail-Safe Mode)

Fault Type	Detection	Conditions	Actions	Fault Flags	FAULTB Pin	Recovery
Supply UVLO	$V_{CC}<V_{CC\_UVLOF}$	-	Turn on all channels LEDs and reset all registers to default value	-	-	$V_{CC}>V_{CC\_UVLOR}$
LED string open	$V_{DS}> V_{TH\_OC}$	LEDx_OF_EN bit set to "1"	Turn on the corresponding bypass switch	92h/93h and OPENF bits	Pull low (OPENFM bit =1)	$V_{DS}<V_{TH\_OC}$ Write 92h/93h to "0"
LED string short (Single LED short)	$V_{DS}< V_{TH\_SC}$	LEDx_SF_EN bit set to "1"	-	90h/91h and SHORTF bits	Pull low (SHORTFM bit =1)	$V_{DS} >V_{TH\_SC}$ Write 90h/91h to "0"
V5 overvoltage	V_5>6.6V	-	-	V5OVF bit	Pull low (V5OVFM bit=1)	V_5<5.6V Write V5OVF bit to "0"
V33 overvoltage	V_{33}>6.6V	-	-	V33OVF bit	Pull low (V33OVFM bit=1)	V_{33}<5.6V Write V33OVF bit to "0"
Thermal shutdown	$T_J>T_{SD}$	-	All channels LEDs fully on	TSDF bit	Pull low (TSDFM bit =1)	$T_J<(T_{SD}-T_{SD\_HYS})$ Write TSDF bit to "0"
Thermal alarm	T_J> alarm threshold set by OVER_TEMP_TH [1:0] bits	-	-	OVTMPF bit	Pull low (OVTMPFM bit =1)	T_J< alarm threshold set by OVER_TEMP_TH[1:0] bits, Write OVTMPF bit to "0"
CRC error	Calculated CRC does not match CRC data	-	Increments CRC Error Count register (98h)	CRCF bit	Pull low (CRCFM bit =1)	Write CRCF bit to "0"
Communication loss	Watchdog times out	R_{FSMD}=10kΩ, 27kΩ or 51kΩ and no error-free communication	Enter fail-safe mode	CMWF bit	Pull low (CMWFM bit =1)	Send the update command then Write CMWF bit to "0"
I^2C communication failure	No ACK or transferred data does not match	-	-	I2CACKF/ I2CTXF and I2CF bits	Pull low (I2CFM bit =1)	Write I2CACKF/ I2CTXF/I2CF bits to "0"
Loopback verification	PWM duty cycle deviation exceeds preset tolerance	VFYEN bit = 1	-	C3h/C4h and DUTYF bits	Pull low (DUTYFM bit =1)	Deviation drops within preset tolerance

10.5.2 LED String Open/Short (Including Single LED Short) Fault Detection And Protection

Each NMOS switch is continuously monitored by a floating circuit and protected from LED open, LED shorted, and single LED short fault conditions.

The LED open fault is detected by an internal comparator monitoring the drain to source voltage (V_{DS}) of the internal NMOS switch. In the event of an LED open failure, the drain to source voltage exceeds the detection threshold voltage, V_{TH_OC}, causing the corresponding NMOS switch to be turned on momentarily. That maintains current flowing in the rest of the LED string in the presence of a faulty or damaged LED and protects the internal NMOS switch from overvoltage damage. The internal circuit holds the NMOS switch on state until the next PWM cycle. The protection circuit sets the corresponding fault flag bit to "1" in OPEN_FAULTL or OPEN_FAULTH registers (92h and 93h). When both the corresponding fault flag enable bit LEDx_OF_EN in LEDx_OS registers (84h~8Fh) and the OPENFM bit in fault mask register FAULT_MASKL (96h) are set to "1", the fault type flag OPENF bit in FAULT_TYPEL register (94h) will be set to "1" and the FAULTB pin will go low to report fault condition.

The LED open detection threshold voltage, V_{TH_OC}, can be programmed independently for each NMOS switch via LEDx_OPEN_TH bits in the LEDx_OS registers (84h~8Fh). The programmed value provides 5V, 10V, 15V and 20V typical threshold values. The programmability of the detection thresholds helps applications where multi-chip LEDs with higher forward voltage drops or multiple LEDs (2~4 pieces) in series are used. Furthermore, in applications where significant ringing occurs during switching events that may result in a false LED open triggering, a higher detection threshold voltage can help mitigate the problem. However, excessively high detection threshold could lead to large voltage bouncing during LED open transition that is not good for the normal operation of the device. Please refer to the table below for proper LED open detection threshold voltage selection according to the LED number connected in parallel to the corresponding switch.

Table 7 LED Open Detection Threshold Voltage Selection

LED Number	Recommended V_{TH_OC}
1	5V or 10V
2	10V or 15V
3	15V
4	20V

The LED short fault is detected by another internal comparator monitoring the drain to source voltage of the internal NMOS switch. In the event of LED shorted failure, if the drain to source voltage drops below the detection threshold voltage, V_{TH_SC}, by the end of the LED ON phase, the detection circuit sets the corresponding fault flag bit to "1" in SHORT_FAULTL or SHORT_FAULTH registers (90h and 91h). When both the corresponding fault flag enable bit LEDx_SF_EN in LEDx_OS registers (84h~8Fh) and the SHORTFM bit in fault mask register FAULT_MASKL (96h) are set to "1", the fault type flag SHORTF bit in FAULT_TYPEL register (94h) will be set to "1" and the FAULTB pin will go low to report fault condition.

The LED shorted detection threshold voltage, V_{TH_OC}, can be programmed independently for each NMOS switch via LEDx_SHORT_TH bits in the LEDx_OS registers (84h~8Fh). The programmed value provides 16 levels of threshold values, typical 1V, 2V, … 16V. The programmability of the detection thresholds helps applications where multiple LEDs (2~4 pieces) in series connection require single LED shorted fault detection.

To achieve proper single LED short detection and avoid false triggering, the V_{TH_SC} should be programmed according to the minimum and maximum of the LED forward voltage:

$$(N-1) \times V_{F\_MAX} < V_{TH\_SC} < N \times V_{F\_MIN} \qquad (27)$$

Where, N is the number of LEDs in the string. V_{F_MAX} and V_{F_MIN} are the maximum and minimum forward voltage of a single LED.

No matter which fault protection is used, the device recovers to normal operation once the fault condition is removed. However, the fault flag bits cannot automatically reset to "0" even when the fault conditions are removed. They can be cleared by the host MCU writing a "0" to the corresponding fault flag bit, and then the FAULTB pin will go back to high impedance, provided that the fault condition is no longer presented.

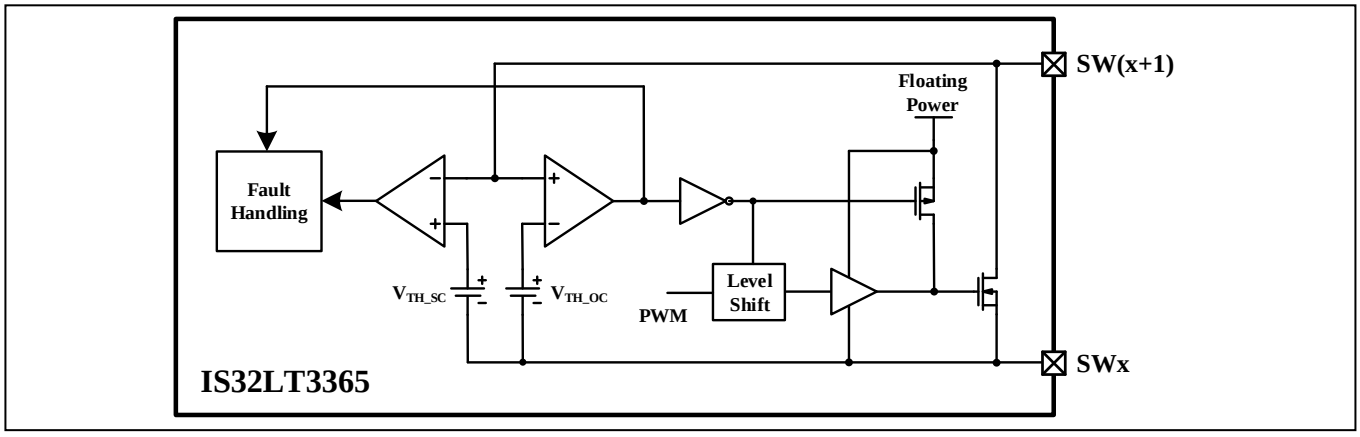


Figure 33 LED Open and Short Detection

10.5.3 Over Temperature Protection

The IS32LT3365 integrates thermal alarm and thermal shutdown protection to prevent the device from overheating. When the junction temperature rises above the thermal alarm threshold, which is preset by OVER_TEMP_TH[1:0] bits in the TEMP_TH register (7Ah), the OVTMPF bit in the FAULT_TYPEL register (94h) will be set to "1". When the OVTMPFM bit in the FAULT_MASKL register (96h) is set to "1", the FAULTB pin will go low to report fault condition. The OVTMPF bit in FLT_TYPEL register (94h) is latched, which means that it cannot automatically reset to "0" but must be cleared by the host MCU by writing it back to "0" after the device cools down. The FAULTB pin will recover to high impedance after OVTMPF bit is clear to "0".

In the event that the junction temperature exceeds T_{SD} (Typ. 170˚C), all internal NMOS switches will go to the OFF state (all LEDs will be turned on), and the TSDF bit in FLT_TYPE_L register (94h) will be set to "1". When the TSDFM bit in FAULT_MASKL register (96h) is set to "1", the FAULTB pin will go low to report fault condition. At this

point, the device presumably begins to cool off. Any attempt to toggle the internal NMOS switches back to the ON state before the device cools to below (T_{SD}-T_{SD_HYS}) (Typ. 150˚C) will be blocked, and the device will not be allowed to restart. The TSDF bit in FLT_TYPE_L register (94h) is latched, which means that it cannot automatically reset to "0" but must be cleared by the host MCU by writing it back to "0" after the device cools down. The FAULTB pin will recover to high impedance after the TSDF bit is cleared to "0".

10.6 ADC OPERATION

The IS32LT3365 device includes a 10-bit ADC with five multiplexed inputs, CH0~CH4. The CH0 and CH1 are connected to two general purpose external inputs (NTCH and NTCL pins), which can be used for system temperature compensation, binning (coding), etc. CH2 is connected to the internal PTAT for junction temperature measurement. The remaining two inputs, CH3 and CH4, are connected to the internal LDOs via corresponding resistor dividers (1/3 resistor divider for V5 and 1/2 resistor divider for V33) for voltage monitor.

Setting the ADCEN bit in ADCCFG register (9Ah) to "1" enables the ADC block. The ADCCH_SEL[4:0] in the ADCCHSEL register (99h) selects the desired input channels for ADC measurement. Writing "1" to the SADC bit in the ADCCTL register (9Bh) starts the ADC measurement and clears ADCCYC_F bit to "0". The selected inputs are periodically sampled in turn. As long as input measurements are completed and all ADC results are available, the ADCCYC_F bit will be set to "1". Their 10-bit results are independently stored in the ADC result registers. If the LOOP bit in the ADCCTL register (9Bh) is set to "0", all selected channels will only be measured once. If the LOOP bit is set to "1", the ADC will continuously measure all the selected channels all the time.

To get a more stable result, the ADC measures multiple times, which is programmed by the ADC_AVG[1:0] bits in the ADCCTL register (9Bh) and stores the average value into the corresponding result register.

The reference voltage for the ADC is V_{REFADC} = 1.8V (Typ.). The ADC operating frequency is programmed by the ADC_CLK[1:0] bits in ADCCFG register (9Ah).

It is recommended to add a 10nF ceramic capacitor from the NTCL/NTCH pin to GND to bypass any high frequency noise, especially if the analog voltage level comes from a long copper trace. This 10nF capacitor should be placed as close to the NTCL/NTCH pin as possible. If the NTCL and NTCH pins are unused, connect them to the ground.

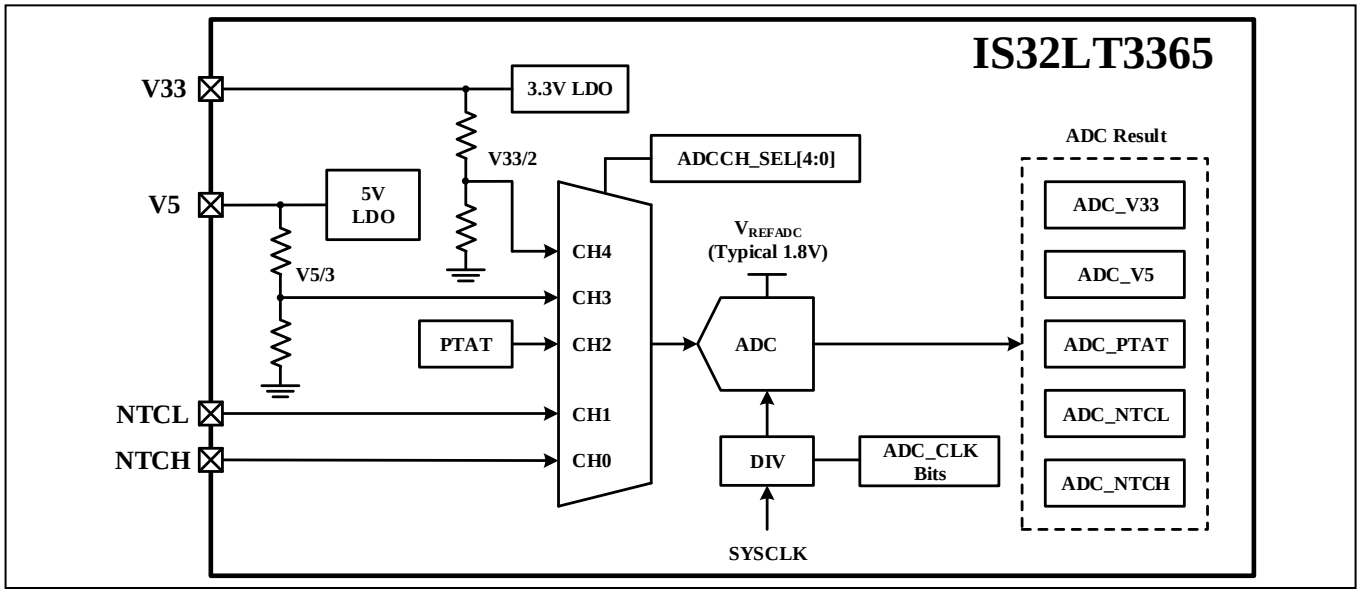


Figure 34 ADC Block

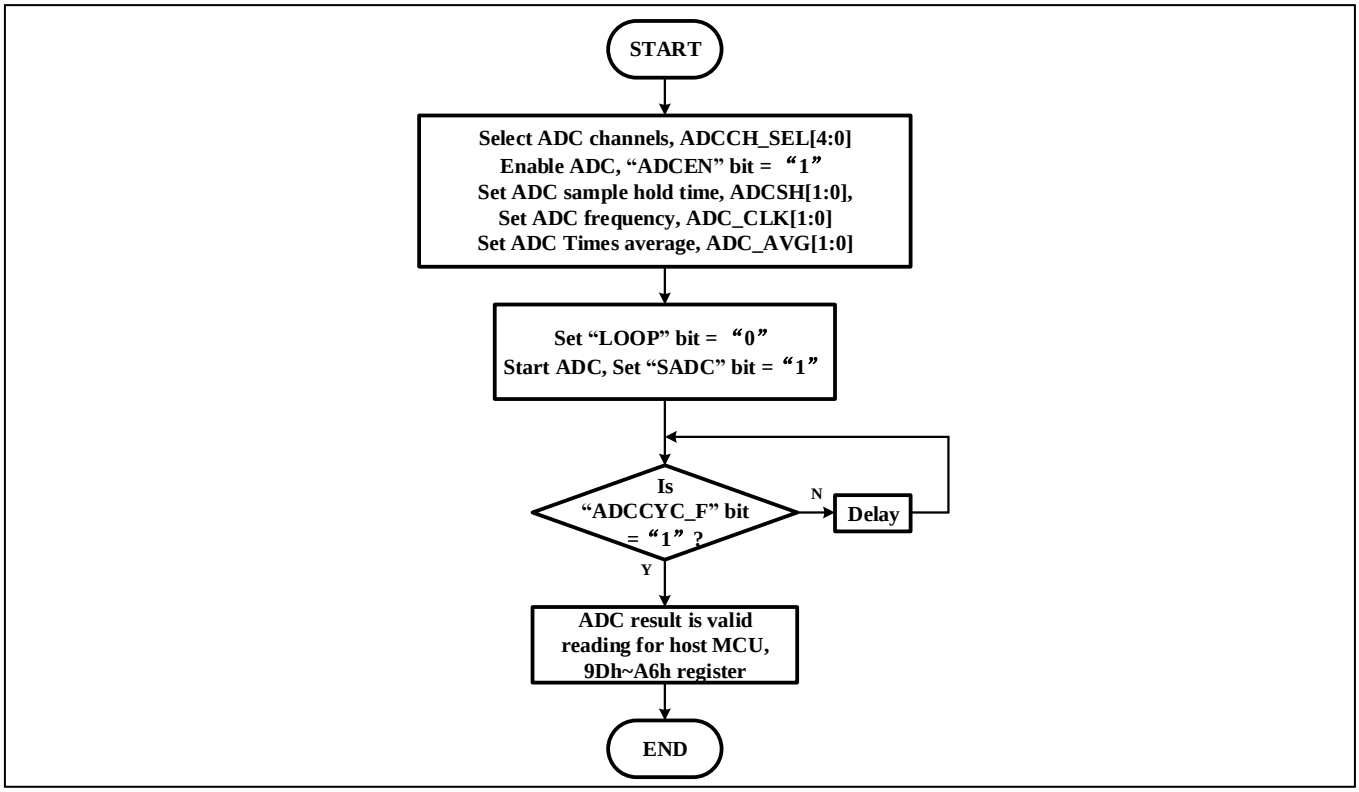


Figure 35 ADC Operation of Single Mode

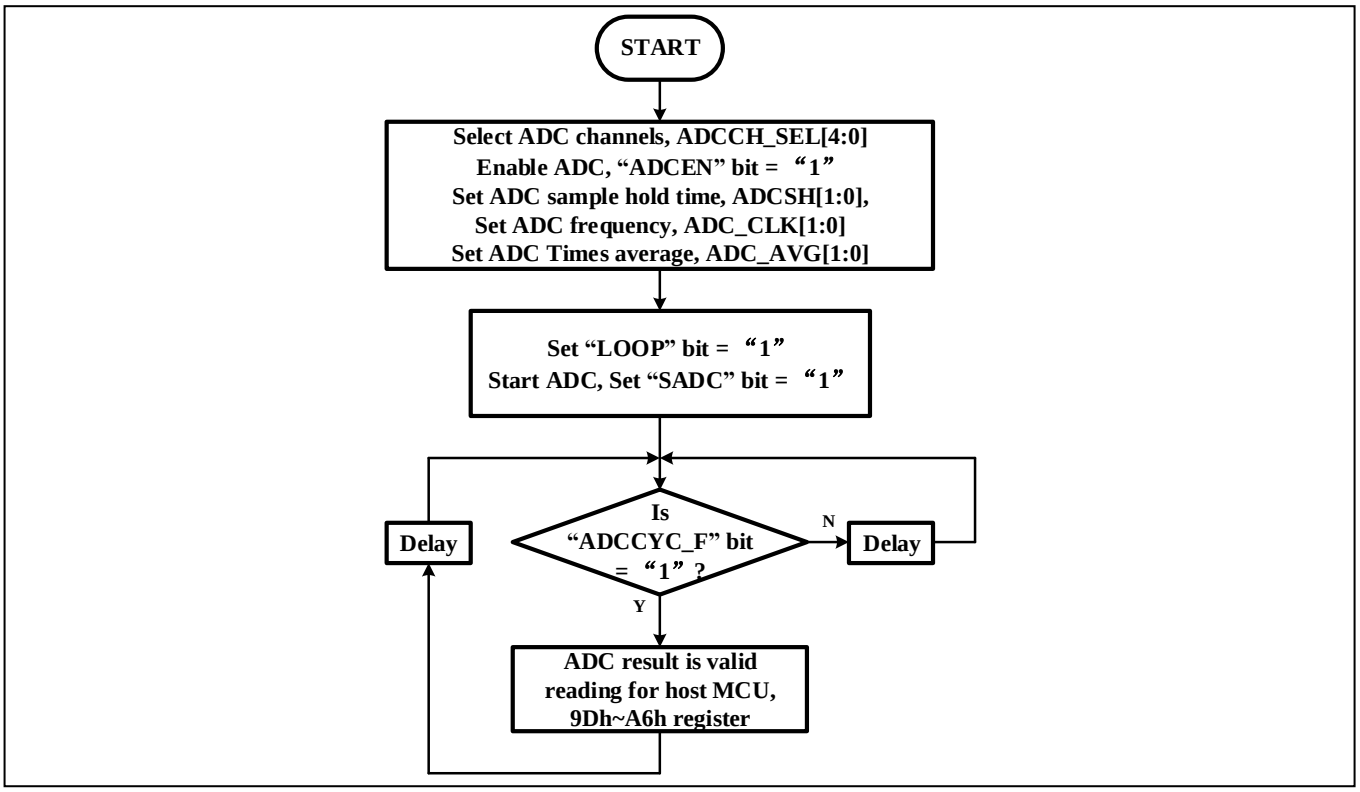


Figure 36 ADC Operation of Loop Mode

10.7 VCC UNDERVOLTAGE_LOCKOUT (UVLO)

The IS32LT3365 features an undervoltage-lockout (UVLO) function on the VCC pin to prevent unintended operation at too low input voltages. UVLO threshold is an internally fixed value and cannot be modified. Entering UVLO will reset all the registers to their default value. The device is disabled when the VCC voltage drops below V_{CC_UVLOF} and resumes normal operation when the VCC voltage rises above V_{CC_UVLOR}. Due to the LBIST (Logic Built-in Self-test) and device address detection, all registers are accessible 10ms after UVLO is released.

During system power up, VCC must be greater than V_{CC_UVLOR} prior to sourcing current through the LED string in order to ensure a controlled start-up.

10.8 INTERNAL VOLTAGE REGULATORS

The IS32LT3365 device integrates two LDOs, a 3.3V LDO and a 5V LDO. Their output pins, V33 and V5, must be bypassed by an X7R type 1μF ceramic capacitor to GND. These capacitors must be placed as close to V33 and V5 pins as possible with the shortest traces.

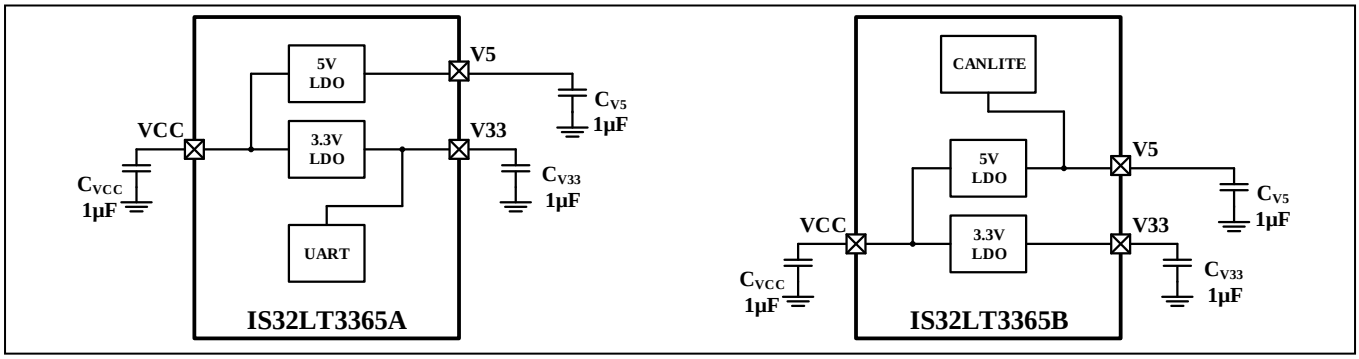


Figure 37 LDO Configuration for 3.3V Host MCU or CAN PHY Application

The positive voltage rail of the UART interface (IS32LT3365A) is supplied with the 3.3V LDO. If a 5V host MCU or CAN PHY is used for IS32LT3365A control, the V33 pin must be connected to the V5 pin, which overrides the internal 3.3V LDO and allows the UART interface to be applied with 5V level signals rather than 3.3V. As depicted in the below figure.

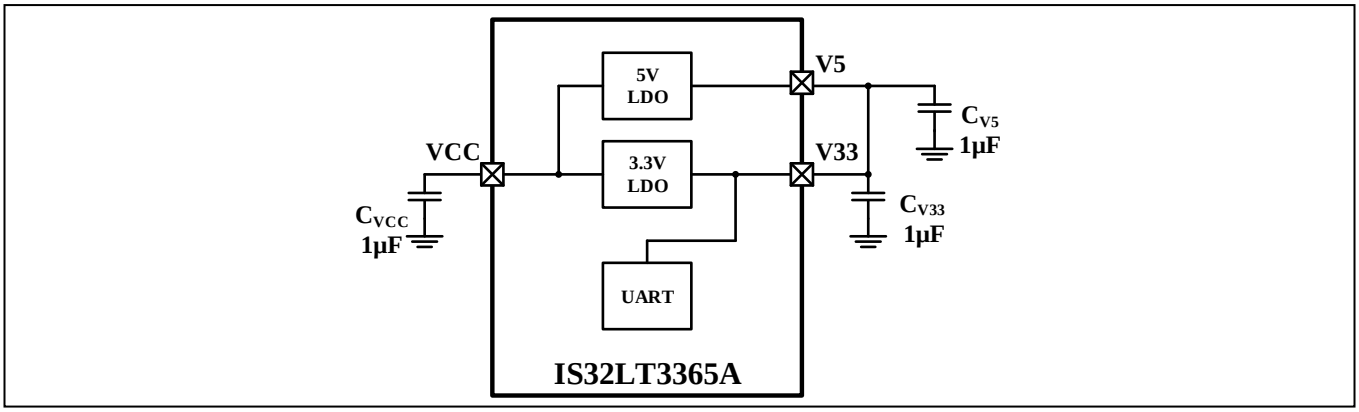


Figure 38 LDO Configuration for 5V Host MCU or CAN PHY Application

For IS32LT3365B, the internal transceiver of the CANLITE interface (IS32LT3365B) is always supplied with the 5V LDO.

Do not power high current external devices using the 5V and 3.3V LDOs.

If the power supply voltage is equivalent to or less than 5V, VCC pin can be connected to the V5 pin. This connection bypasses the internal 5V LDO, as shown in the below figure.

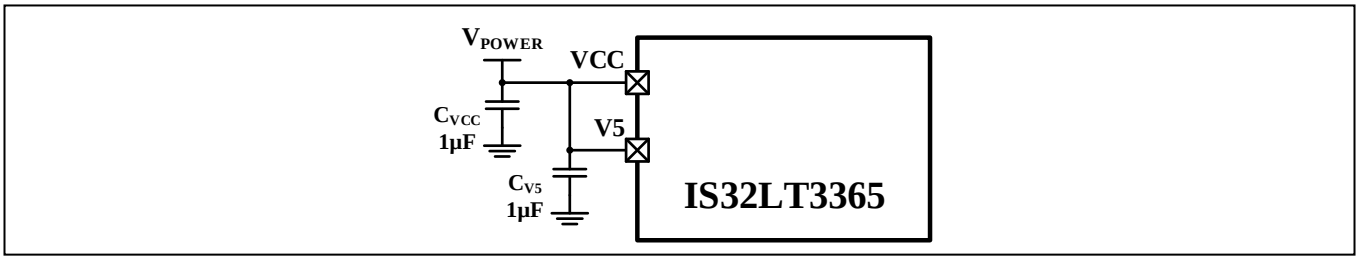


Figure 39 Power Supply Connection for V_{CC}≤5V

Both the V5 and V33 LDOs are monitored by overvoltage detection circuit. If the voltage exceeds the overvoltage detection threshold 6.6V (Typ.), the corresponding V5OVF and V33OVF fault flag bits in FAULT_TYPEH register (95h) will be set to “1”. When the V5OVFM or V33OVFM bit in FAULT_MASKH register (97h) is set to “1”, the FAULTB pin will go low to report fault condition. The V5OVF and V33OVF fault flag bits in FAULT_TYPEH register

(95h) are latched, which means that it cannot automatically reset to “0” but must be cleared by the host MCU writing it back to “0” after overvoltage condition has been removed. The FAULTB pin will return to a high impedance state once V5OVF and V33OVF bits are cleared to “0”.

10.9 COMMUNICATION INTERFACES

10.9.1 UART Interface (IS32LT3365A Only)

The host MCU can communicate with the IS32LT3365A device using a Universal Asynchronous Receiver and Transmitter (UART). The pairs of TX and RX pins on the IS32LT3365A device are feed-through pins (internally connected by low impedance metal), and either pin may be used to connect the IS32LT3365A device to the network. Feed-through pins enable the use of a metal core board with single layer routing. The UART communication process uses a command and response protocol (Lumibus protocol) mastered by the host MCU to write and read the registers to and from each IS32LT3365A device. The IS32LT3365A UART interface utilizes half-duplex communications (transmit and receive cannot overlap). A tri-state buffer drives the TX pin, so it is recommended to place an external pull-up resistor (R_{PU}, 10kΩ typical) on the RX input return line of the host MCU. This allows multiple IS32LT3365A devices to share a common pair of TX and RX signals by connecting all IS32LT3365A TX lines together and all IS32LT3365A RX lines together. The baud rate can support range from 100kbps~1Mbps.

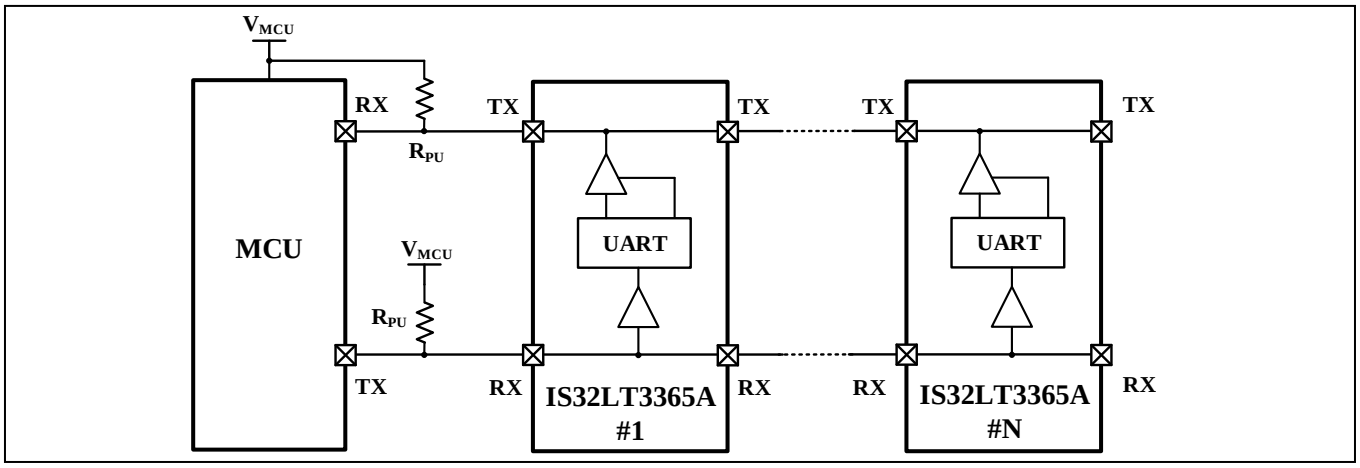


Figure 40 UART Interface Connection

Additionally, the physical TX and RX connections of IS32LT3365A can be joined together through an industrial-standard CAN transceiver (CAN PHY). This has the added advantage of protection from shorts to the battery and/or shorts to ground on the cables and/or harnesses between the MCU board and the IS32LT3365B board. The CAN physical layer has excellent EMI and EMS performance, making it suitable for long distance off-board connections.

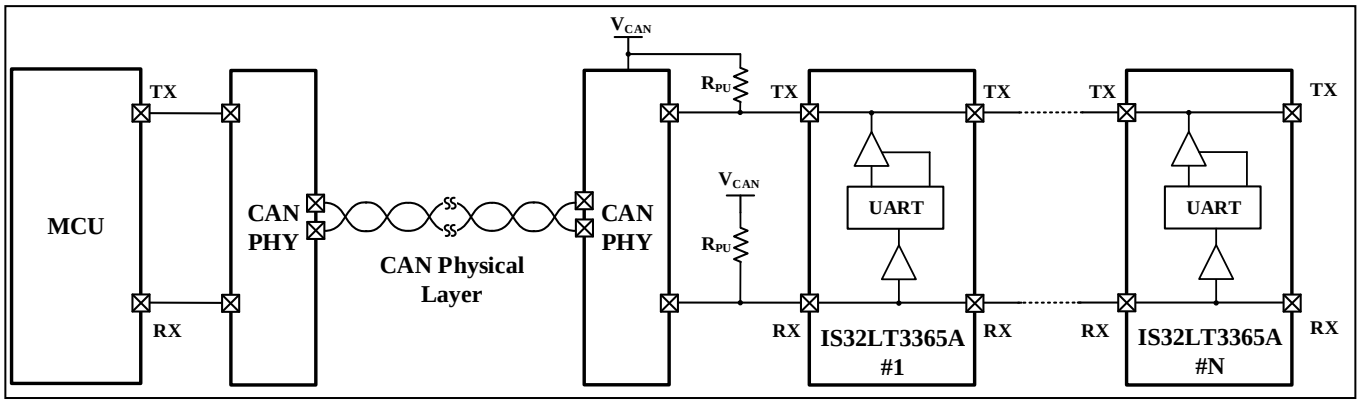


Figure 41 UART Interface with Industrial-Standard CAN Transceiver Connection

10.9.2 CANLITE Interface (IS32LT3365B Only)

The IS32LT3365B integrates CANLITE, which is compatible with an industrial-standard CAN transceiver (CAN PHY). The pairs of CANLITEH and CANLITEL pins on the IS32LT3365B device are feed-through pins (internally connected by low impedance metal), and either pin may be used to connect the IS32LT3365B device to the network. Feed-through pins enable the use of metal core board with single layer routing. The CANLITE interface can communicate with the industrial-standard CAN transceiver by connecting the CANLITEH and CANLITEL to the CAN bus. Therefore, the host MCU can control the IS32LT3365B devices via CANLITE interface through a CAN transceiver.

The integrated high-speed transceiver of CANLITE interface can support 100kbps~1 Mbps baud rate.

The internal CANLITE transceiver converts the single-ended input (TX) of an internal UART interface from internal Lumibus protocol handling circuitry to differential outputs for the BUS lines (CANLITEH and CANLITEL). The CANLITE transceiver reads differential inputs from the BUS lines (CANLITEH and CANLITEL) and transfers this data as the single-ended output (RX) of the internal UART interface to internal Lumibus protocol handling circuitry. The internal UART interface is identical to IS32LT3365A's UART interface, and both use the Lumibus protocol.

Like the industrial-standard CAN termination, resistors should be used to terminate both ends of the CANLITE bus. The termination may be on the cable or in a node. The recommended values of R_{TER1}, R_{TER2} and C_{TER} are 62Ω and 4.7nF, respectively.

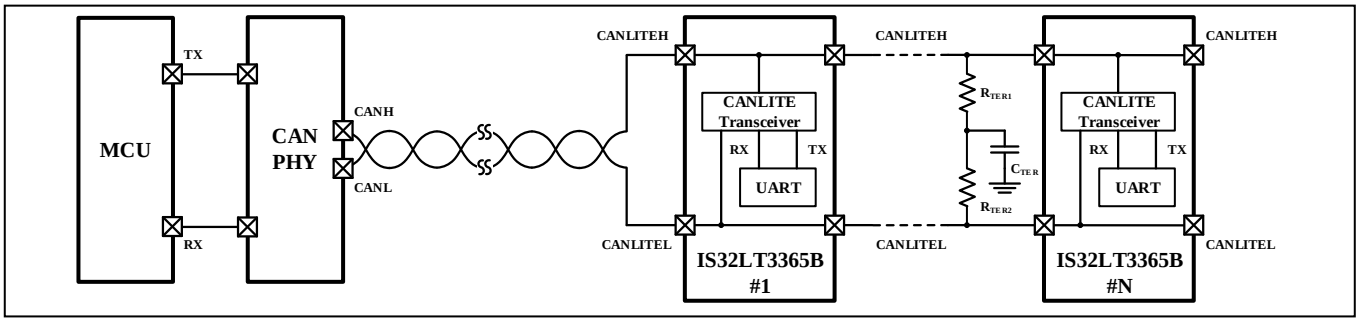


Figure 42 CANLITE Interface Connection

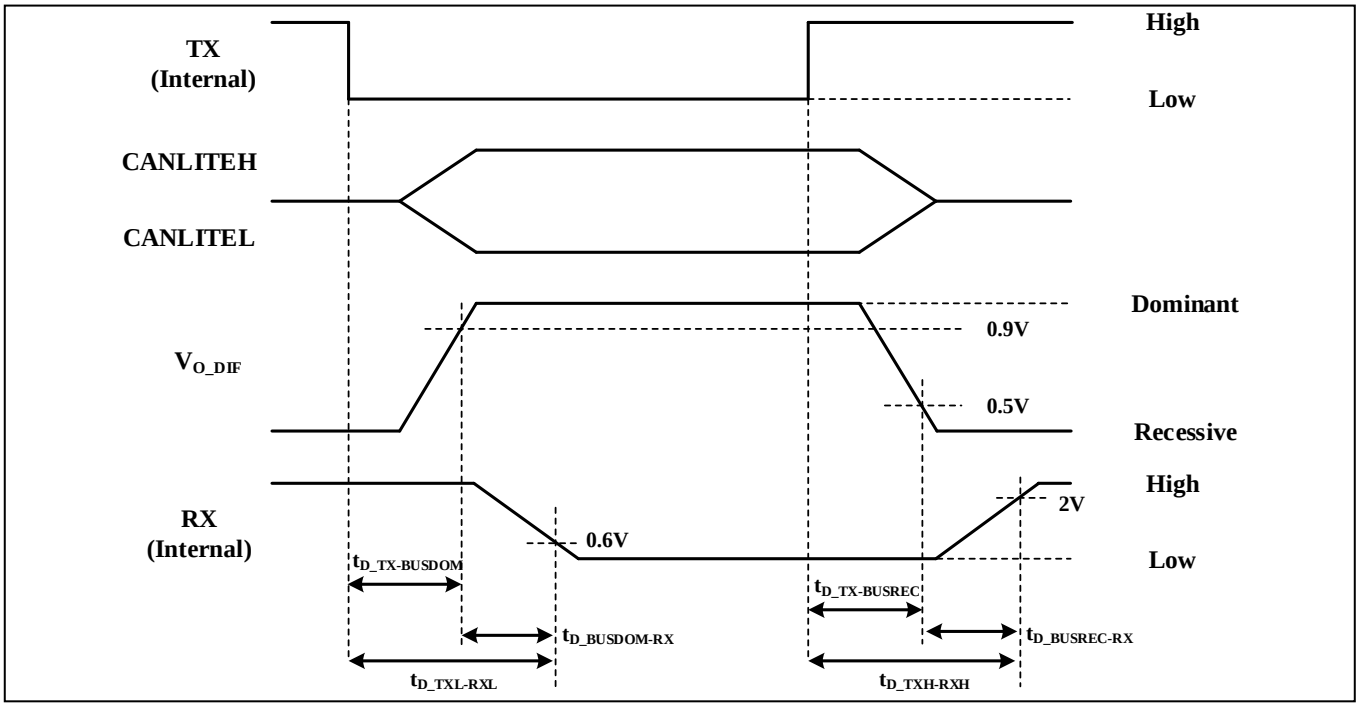


Figure 43 CANLITE Interface Timing

10.9.3 UART Data Format

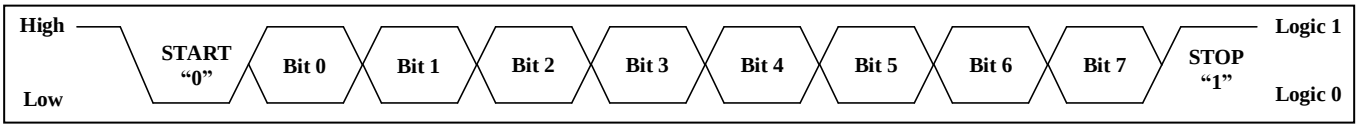


Figure 44 UART Data Byte Format

The UART operates with one start bit, eight data bits (LS bit first) and one stop bit. The above figure shows the waveform for an individual byte transfer on the UART. A logic "1" state occurs when the device drives the line to high voltage. A logic "0" state occurs when the device drives the line to the ground. Below figure shows actual data bytes with UART data format.

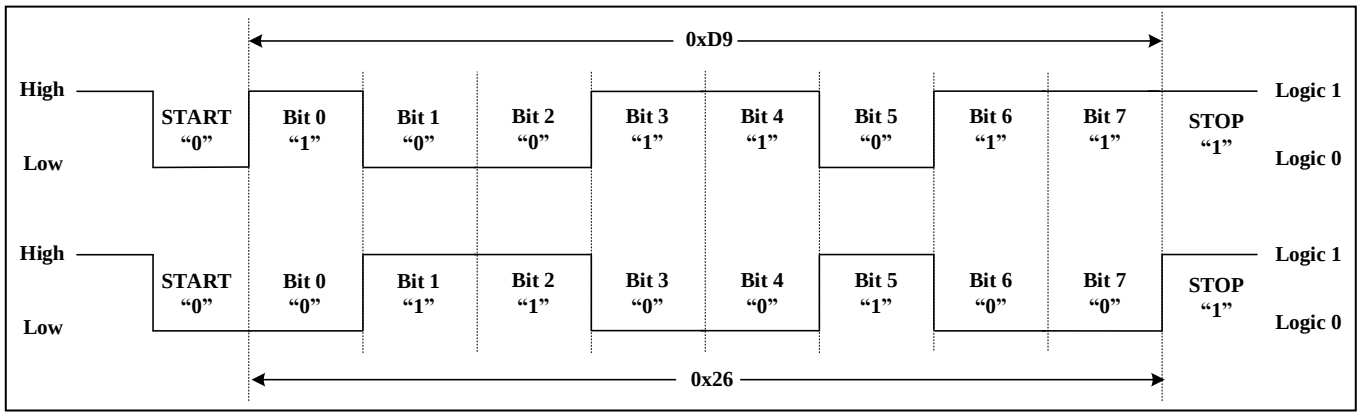


Figure 45 UART Data Transaction Example

The baud rate of UART communication can be 100kbps to 1Mbps, which is synchronized by the baud rate of the SYNC byte of the BUS Reset command. The UART uses 32x over-sampling on the incoming asynchronous RX signal. Between UART data bytes, at least one bit is required as STOP bit.

10.10 LUMIBUS PROTOCOL

The communication uses the Lumibus protocol, which is a UART-based protocol supported by most MCUs. The communication process of all two interfaces uses a command and response protocol mastered by the host MCU to write and read the registers to and from each IS32LT3365 device. This means that the IS32LT3365 device never initiates traffic onto the network. The Lumibus protocol maps the registers into an address space on each device. The host MCU uses the Lumibus protocol to initiate a communication transaction by sending a command frame. This command frame addresses either one IS32LT3365 device directly or broadcasts to all IS32LT3365 devices on the network. This addressing may cause a response frame to be sent back from the slave IS32LT3365 device, depending on the command type of the command frame. There are four types of commands:

1) BUS Reset Command: resets the UART/CANLITE BUS and synchronizes the baud rate
2) Write Command: writes data from host MCU to IS32LT3365 device(s)
3) Read Command: reads data from specific IS32LT3365 device to host MCU
4) Special Command: specifies IS32LT3365 device(s) to implement specific function.

There is no response frame following a broadcast write command frame. Therefore, only two types of response frames exist that an IS32LT3365 device sends back to the host MCU: Write Acknowledge (if enabled) and Read Response.

10.11 COMMAND FRAME TYPES

10.11.1 BUS Reset Command Frame

The host MCU can reset the device UART/CANLITE and Lumibus protocol state machine at any time by sending the BUS Reset command. The BUS Reset command consists of a reset signal and SYNC byte (0x55). The reset signal includes at least 150μs break low and a logic high break delimiter (2μs~100μs). Upon receiving the bus reset signal, the Lumibus protocol state machine of all IS32LT3365 devices on the bus will be reset to a known-good state. The bus reset signal must be followed by a SYNC byte with the desired baud rate (within 100kbps to 1Mbps) to synchronize the baud rate to all IS32LT3365 devices. Subsequent communication must use the identical baud rate. This synchronization approach saves the cost of the external crystal oscillator. To avoid clock drift over time and ambient temperature, it's recommended to send a BUS Reset Command to the IS32LT3365 devices periodically.

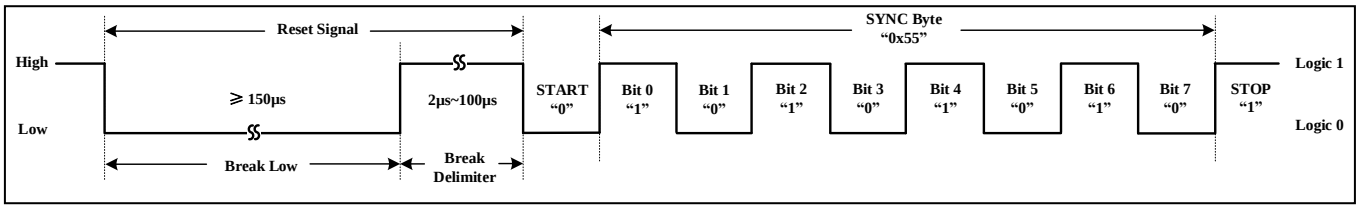


Figure 46 BUS Reset Command

Upon the system powering up, the host MCU must initialize the BUS by sending a BUS Reset command before communication. This BUS reset operation must be performed by the host MCU for several application scenarios:

(1) upon system power up, (2) host MCU watchdog time is expired, (3) communication fault is detected.

Note that the BUS Reset Command only resets the interface state machine (including stored communication baud rate). It does not reset the registers and does not halt normal LED PWM operation.

10.11.2 Write Command Frame

The Write Command Frame is comprised of the following sequence.

CMD Frame Header (One Byte)	Device ID (One Byte)	Start Register Address (One Byte)	Data 1 (One Byte)	…	Data N (One Byte)	CRC_L (One Byte)	CRC_H (One Byte)

10.11.3 Acknowledge Frame

If the ACKEN bit is set to “1” in the SYSCFG register (80h), the addressed device transmits an acknowledgment back to the host MCU upon a successful single device write. The Acknowledge Frame is comprised of a single byte (ACK=0x7F) as the following sequence.

ACK (0x7F)

10.11.4 Read Command Frame

The Read Command Frame (transferred by the host MCU) is comprised of the following sequence.

CMD Frame Header (One Byte)	Device ID (One Byte)	Start Register Address (One Byte)	CRC_L (One Byte)	CRC_H (One Byte)

A successfully-addressed IS32LT3365 device then transfers back the appropriate Read Response Frame.

The Read Response Frame is comprised of the following sequence.

RSP Frame Header (One Byte)	Device ID (One Byte)	Data 1 (One Byte)	…	Data N (One Byte)	CRC_L (One Byte)	CRC_H (One Byte)

10.11.5 Special Command Frame

The special command specifies the IS32LT3365 device to implement the specific function, which includes:

1) Update Command
   This special command is used for below scenarios:
   - Update the PWM WIDTH and PHASE register data (register 00h~6Fh) into output stages at the next PWM boundary after this command is issued.
   - Update the configuration of the PSON bit in the SYSCFG register (80h).
   - Update the configuration of the PARLED register (71h).
   - Quit from fail-safe mode to normal mode.
2) PWM Synchronization Command
   Resets the TCNT counter to 0. Issued by broadcast to realize PWM software synchronization.
3) Registers Reset Command
   Reset all registers to default value, excluding the PWR bit in the SYSCFG register (80h).

The Special Command Frame is comprised of the following sequence:

CMD Frame Header (One Byte)	Device ID (One Byte)	CRC_L (One Byte)	CRC_H (One Byte)

One complete command frame can be received successfully even if the bytes in the frame is not sent continuously.

10.12 TRANSACTION FRAME DESCRIPTION

The command frames include the following byte types:

1) Frame Header Byte
2) Device ID Byte
3) Start Register Address Byte

4) N Data Byte(s) (N = 1~16, 32)
5) CRC Bytes (CRC_L and CRC_H)
6) Acknowledge Byte (ACK)

10.12.1 Frame Header Byte

The Frame Header Byte identifies the transaction as either a write/read command frame or a response frame. In addition, the Frame Header Byte indicates how many data bytes are being written/read or responded. The number of data bytes to be written/read or responded can be 1~16 or 32.

Table 8 Frame Header Byte

Frame Header Type	D7	D6	D5	D4:D0
CMD Frame Header	FRM_TYPE	W/R	BCON	CMD
RSP Frame Header	FRM_TYPE	RSVD	RSVD	RSP

Table 9 The fields description of the Frame Header Byte

Name	Function	Value (BIN)	Description
FRM_TYPE (Bit 7)	Specify frame type	0	Read response frame sent back from the IS32LT3365 device to host MCU
		1	Command frame sent from host MCU to the IS32LT3365 device
W/R (Bit 6)	Specify write/read mode	0	Write mode command frame
		1	Read mode command frame
BCON (Bit 5)	Specify broadcast/single device mode	0	Single device write or read.
		1	Broadcast write. (Device ID Byte must be 0xBF. Broadcast only accepts write command)
CMD (Bit 4:0)	Specify transmit data length for write/read command frame	00000 ~ 01111	1 byte ~ 16 bytes of data length
		10000	32 bytes of data length
	Specify special command type (W/R bit must be set to “0”)	11000	Update Command. Valid for both single device and broadcast write
		11100	PWM Synchronization Command. Must be issued by broadcast write
		11110	Registers Reset Command. Valid for both single device and broadcast write
RSP (Bit 4:0)	Specify transmit data length for response frame	00000 ~ 01111	1 byte ~ 16 bytes of data length
		10000	32 bytes of data length

10.12.2 Device ID Byte

D7	D6	D5	D4	D3	D2	D1	D0
p[1]	p[0]	1	DEV_ID [4:0]				

IS32LT3365 supports maximum 27 slave devices. The Device ID Byte specifies the device of the destination. There are five DEV_ID bits, one reserved bit and two parity bits. The parity bits for the Device ID Byte are calculated with the equations below:

p[1] = ~(dev_id[1] ^ dev_id[3] ^ dev_id[4] ^ 1)

p[0] = dev_id[0] ^ dev_id[1] ^ dev_id[2] ^ dev_id[4]

The DEV_ID [4:0] of each IS32LT3365 device is determined by the three address pins of ADDR0, ADDR1 and ADDR2 as following mapping for the Device ID Byte.

For a broadcast command of UART and CANLITE interfaces, the DEV_ID[4:0] must be 0b 11111, otherwise, the broadcast command will be invalid.

Table 10 Device Address Decoded

ADDR2 Pin Voltage(V)	ADDR1 Pin Voltage(V)	ADDR0 Pin Voltage(V)	Bit [7:5] (BIN)	Bit [4:0] (BIN)	Device ID Byte (HEX)
0	0	0	001	00000	20
0	0	3.3	011	00001	61
0	0	5	111	00010	E2
0	3.3	0	101	00011	A3
0	3.3	3.3	011	00100	64
0	3.3	5	001	00101	25
0	5	0	101	00110	A6
0	5	3.3	111	00111	E7
0	5	5	101	01000	A8
3.3	0	0	111	01001	E9
3.3	0	3.3	011	01010	6A
3.3	0	5	001	01011	2B
3.3	3.3	0	111	01100	EC
3.3	3.3	3.3	101	01101	AD
3.3	3.3	5	001	01110	2E
3.3	5	0	011	01111	6F
3.3	5	3.3	111	10000	F0
3.3	5	5	101	10001	B1
5	0	0	001	10010	32
5	0	3.3	011	10011	73
5	0	5	101	10100	B4
5	3.3	0	111	10101	F5
5	3.3	3.3	011	10110	76
5	3.3	5	001	10111	37
5	5	0	011	11000	78
5	5	3.3	001	11001	39
5	5	5	101	11010	BA
-	-	-	101	11111	BF (For broadcast write command only)
-	-	-	111	11110	FE (Reserved)

10.12.3 Start Register Address Byte

The Lumibus protocol allows up to 32 successive register locations from the addressed register to be written or read by a single command frame. The Start Register Address Byte is a single byte which specifies the first register being written or read. It is only present in Write and Read Command transactions, not in Read Response and Special command transactions.

10.12.4 N Data Byte(s)

The Frame Header Byte specifies the number of data bytes to be included in the frame.

10.12.5 CRC Bytes (CRC_L and CRC_H)

The host MCU sends command to the IS32LT3365 using CRC-16-IBM standard for CRC checksum calculation, which will cover the whole frame bytes, e.g., Frame Header Byte, Device ID Byte, Start Register Address Byte, N Data Bytes. Lower byte first followed by higher byte. The CRC Bytes allow the detection of errors within the transaction frame. The device increments the CRC Error Count Register (98h) each time a CRC error occurs on an incoming command frame, and the CRCF bit in FAULT_TYPEL register (94h) will be set to “1”. When the CRCFM

bit in the FAULT_MASKL register (96h) is set to “1”, the FAULTB pin will go low to report fault condition.

The CRCF bit in FAULT_TYPEL register (94h) is latched, which means it cannot automatically reset to “0” when no RC error occurs but must be cleared by the host MCU writing it back to “0”. Once the CRCF bit is cleared, the FAULTB pin will go back to a high impedance.

The addressed device also calculates the CRC bytes during its Read Response.

The CRC bytes are then appended to the end of the read data, lower byte first followed by the higher byte. This allows the host MCU to check the read data coming from the IS32LT3365 device for any transmission errors. The following is a reference CRC checksum C code for transmission to the IS32LT3365 devices.

```
Uint16 crc_16_ibm (Uint8 *buf, Uint8 len)
{
        Uint16 crc = 0;
        Uint16 I;
        while (len--)
        {
                crc ^= *buf++;
                for (I = 0; I < 8; I++){
                crc = (crc >> 1) ^ ((crc & 1) ? 0xa001 : 0);
                }
        }
        return crc;
}
```

Upon reading data from the IS32LT3365 device, the host MCU should calculate and compare the CRC to determine whether valid data was received. When IS32LT3365 sends back CRC bytes to the host MCU, the calculated CRC bytes must be bit-reversed before comparison to the received CRC bytes. The following is a reference code to perform the received CRC bit reversal.

```
Uint8 reverse_byte(Uint8 byte)
{
        // First, swap the nibbles
        byte = (((byte & 0xF0) >> 4) | ((byte & 0x0F) << 4));
        // Then, swap bit pairs
        byte = (((byte & 0xCC) >> 2) | ((byte & 0x33) << 2));
        // Finally, swap adjacent bits
        byte = (((byte & 0xAA) >> 1) | ((byte & 0x55) << 1));
        // We should now be reversed (bit 0 <--> bit 7, bit 1 <--> bit 6, etc.)
        return byte;
}
```

The following is a reference code for checking the read data against received CRC bytes.

```
bool is_crc_valid(Uint8 *rx_buf, Uint8 crc_start)
{
        Uint16 crc_calc; // Calculated CRC
        Uint8 crc_msb, crc_lsb; // Individual bytes of calculated CRC
        // Calculate the CRC based on bytes received
        crc_calc = crc_16_ibm(rx_buf, crc_start);
        crc_lsb = (crc_calc & 0x00FF);
        crc_msb = ((crc_calc >> 8) & 0x00FF);
        // Perform the bit reversal within each byte
        crc_msb = reverse_byte(crc_msb);
        crc_lsb = reverse_byte(crc_lsb);
        // Do they match?
        if((*(rx_buf + crc_start) == crc_lsb) && (*(rx_buf + crc_start + 1) == crc_msb))
        {
                return TRUE;
        }
        else
        {
```

```
            return FALSE;
        }
}
```

10.12.6 Acknowledge Byte

The Acknowledge Byte (“ACK”) consists of a single byte (ACK=0x7F):

ACK is sent back by the addressed IS32LT3365 device only if the ACKEN bit is set in the SYSCFG register (80h) and only if the write is successful. A successful write yields no CRC checksum error or parity errors. Note that the acknowledge is only valid for single device write transaction of IS32LT3365 (broadcast write does not support acknowledge function).

10.12.7 Turnaround Time

When considering back-to-back data transfer, the turnaround time (additional time required between the end of the previous byte stop bit and the beginning of the next byte start bit) is required, which means a finite amount of dead time must be inserted between two bytes or two command frames as the requirement is shown in Figure 47~51. It’s recommended to use dual stop bits mode for the UART interface.

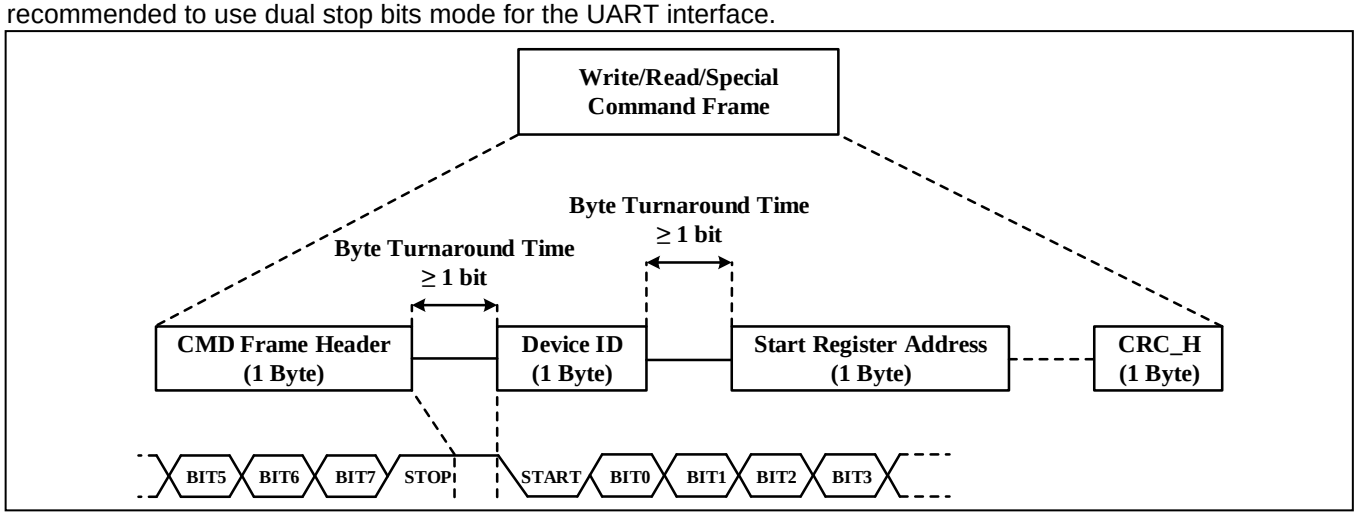


Figure 47 Turnaround Time Between Byte and Byte of Write/Read/Special Command Frame

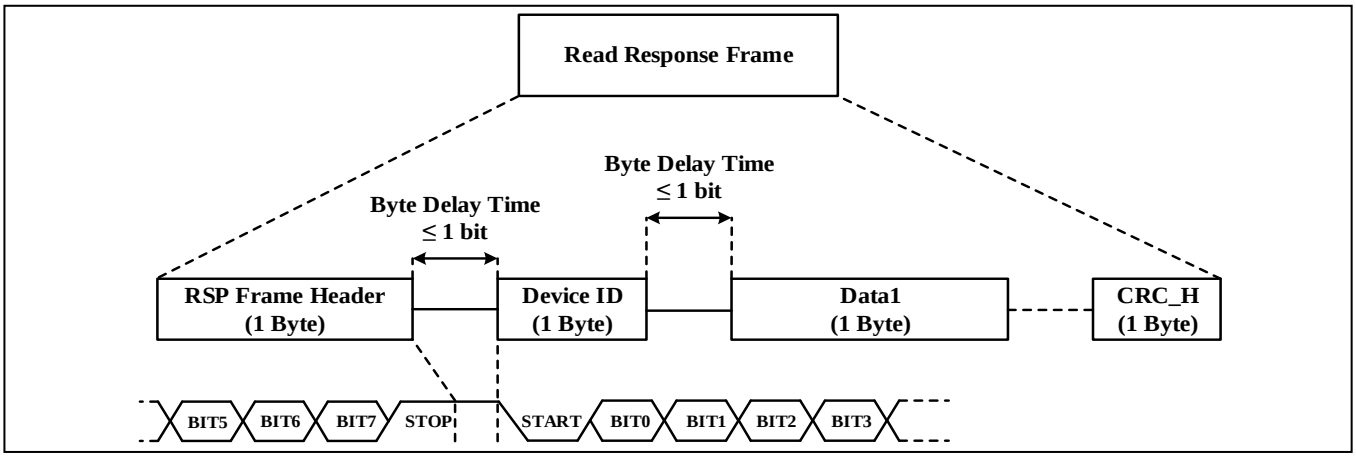


Figure 48 Delay Time Between Byte and Byte of Read Response Frame

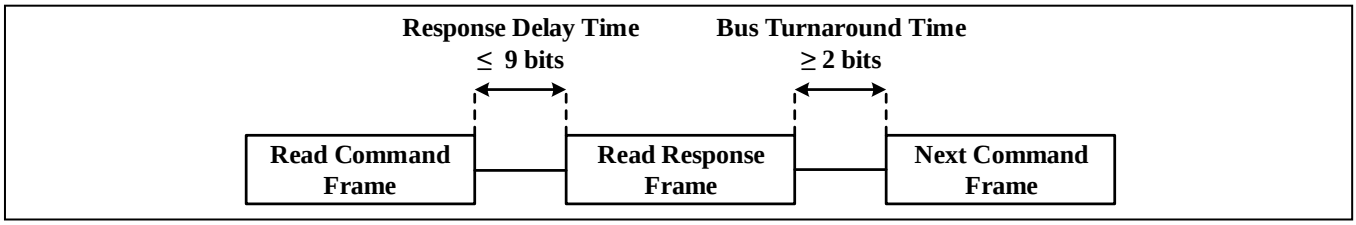


Figure 49 Turnaround Time Between Read Response Frame and Next Command Frame

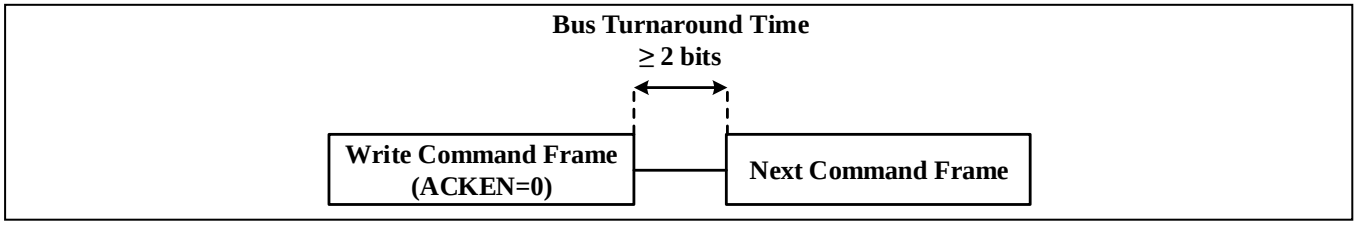


Figure 50 Turnaround Time Between Write Command Frame and Next Command Frame (ACK Disabled)

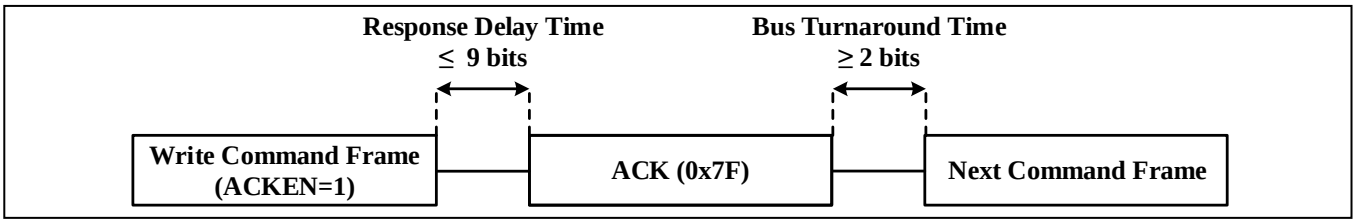


Figure 51 Turnaround Time Between ACK and Next Command Frame (ACK Enabled)

10.13 COMMUNICATIONS EXAMPLES

The total number of transmitted bytes depends on the specific task being performed. The examples below show the sequence of transmitted bytes for a given transaction.

Example 1: Single Device Write of 3 Bytes

Write to Device ID=0x25 (ADDR2=0V/ADDR1=3.3V/ADDR0=5V): beginning at register 00h, MG1_PHASE01L=0x1F, MG1_PHASE02L=0x2F, MG1_PHASE03L=0x3F

Byte Types	Number Of Bytes
CMD Frame Header Byte	1
Device ID Byte	1
Start Register Address Byte	1
Data Bytes	3
CRC Bytes	2
Total	8

Interface	Command Frame							
	CMD Frame Header	Device ID	Start Register Address	Data 1	Data 2	Data 3	CRC_L	CRC_H
UART/ CANLITE	0x82 (0b10000010)	0x25	0x00	0x1F	0x2F	0x3F	0x3E	0x03

Acknowledge from addressed device (if enabled ACKEN)

Acknowledge Frame
ACK
0x7F

Example 2: Single Device Read of 2 Bytes

Read from Device ID=0xA3 (ADDR2=0V/ADDR1=3.3V/ADDR0=0V): beginning at register 30h, read MG2_WIDTH01H and MG2_WIDTH02H

Byte Types	Number Of Bytes
CMD Frame Header Byte	1
Device ID Byte	1
Start Register Address Byte	1
CRC Bytes	2
Total	5

Interface	Command Frame				
	CMD Frame Header	Device ID	Start Register Address	CRC_L	CRC_H
UART/ CANLITE	0xC1 (0b11000001)	0xA3	0x30	0x29	0x18

Read Response: MG2_WIDTH01H = 0x00, MG2_WIDTH02H = 0x00

Byte Types	Number Of Bytes
RSP Frame Header Byte	1
Device ID Byte	1
Data Bytes	2
CRC Bytes	2
Total	6

Interface	Command Frame					
	RSP Frame Header	Device ID	Data 1	Data 2	CRC_L	CRC_H
UART/ CANLITE	0x01 (0b00000001)	0XA3	0x00	0x00	0x8F	0x7B

Example 3: Broadcast Write of 3 Bytes

Broadcast write to all devices (fixed Device ID with parity = 0xBF): beginning at register B0h, I2CDAT01=0x0F, I2CDAT02=0x1F, I2CDAT03=0x2F

Byte Types	Number Of Bytes
CMD Frame Header Byte	1
Device ID Byte	1
Start Register Address Byte	1
Data Bytes	3
CRC Bytes	2
Total	8

Interface	Command Frame							
	CMD Frame Header	Device ID	Start Register Address	Data 1	Data 2	Data 3	CRC_L	CRC_H
UART/ CANLITE	0xA2 (0b10100010)	0xBF	0xB0	0x0F	0x1F	0x2F	0x53	0xB6

Example 4: Broadcast PWM Synchronization Command (Special Command)

Broadcast PWM Synchronization Command to all devices (fixed Device ID with parity = 0xBF):

Byte Types	Number Of Bytes
CMD Frame Header Byte	1
Device ID Byte	1
CRC Bytes	2
Total	4

Interface	Command Frame			
	CMD Frame Header	Device ID	CRC_L	CRC_H
UART/ CANLITE	0xBC (0b10111100)	0xBF	0x31	0x70

Example 5: Broadcast Registers Reset Command (Special Command)

Broadcast Registers Reset Command to all devices (fixed Device ID with parity = 0xBF):

Byte Types	Number Of Bytes
CMD Frame Header Byte	1
Device ID Byte	1
CRC Bytes	2
Total	4

Interface	Command Frame			
	CMD Frame Header	Device ID	CRC_L	CRC_H
UART/ CANLITE	0xBE (0b10111110)	0xBF	0x30	0x10

Example 6: Broadcast Update Command (Special Command)

Broadcast Update Command to all devices (fixed Device ID with parity = 0xBF):

Byte Types	Number Of Bytes
CMD Frame Header Byte	1
Device ID Byte	1
CRC Bytes	2
Total	4

Interface	Command Frame			
	CMD Frame Header	Device ID	CRC_L	CRC_H
UART/ CANLITE	0xB8 (0b10111000)	0xBF	0x33	0xB0

10.14 DEVICE FUNCTIONAL MODES

The IS32LT3365 device operates in two modes, shown in below figure.

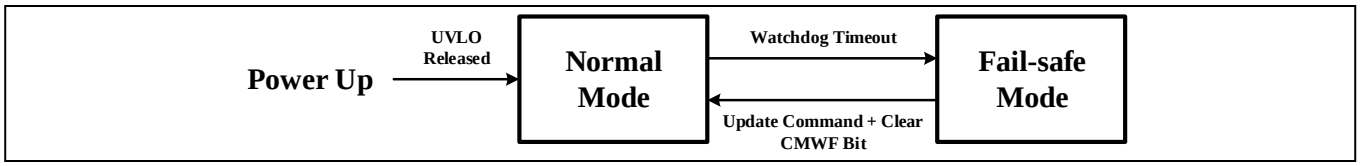


Figure 52 Operation Modes

10.14.1 Normal Mode

Upon power up and being released from UVLO, the IS32LT3365 operates in normal mode. The digital circuitry controls the IS32LT3365 outputs by accepting interface commands and by monitoring and responding to real-time events on the inputs associated with the analog and power circuitry. This allows the dimming of the LED outputs using the registers settings.

10.14.2 Fail-Safe Mode

This state allows the user to preset the outputs' state if the communication is broken. The device integrates a communication watchdog timer that operates based on the system clock pulse. The tap point, programmed via the CMWTAP register (81h), defines the timing of the communication watchdog timer (25-bit counter). By default, the tap point is set to bit 22, which means the device requires 2^22 system clock cycles for the communication watchdog timer to time out. If the communication watchdog times out (no error-free communication is successfully received for the programmed number of system clock cycles), the device will enter fail-safe mode.

The FSMD pin is used to configure the watchdog timer and the default value of the DEFAULT PULSE WIDTH registers (72h~77h). The resistor R_{FSMD} is connected to the FSMD pin. When the UVLO is released, the internal I_{FSMD} (typical 54μA) current source creates a voltage on the FSMD pin, V_{FSMD}. The device compares the V_{FSMD} with internal different reference voltage levels (V_{TH1_FS}, V_{TH2_FS} and V_{TH3_FS}) to determine watchdog action and the default value. Refer to the Fail-safe Mode Setting Table.

Note that the device only implements voltage comparison and default value setting once at power up or receiving a Registers Reset Command.

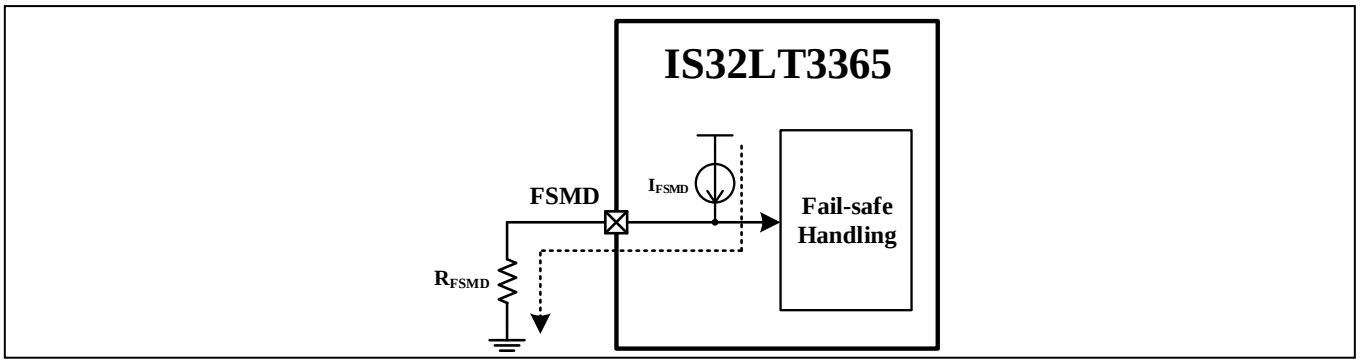


Figure 53 FSMD Pin Operation

When $V_{TH3\_FS}<V_{FSMD}<5.5V$ (recommend connecting the FSMD pin to the V5 pin via a 10kΩ resistor), the internal communication watchdog is invalid, and the fail-safe mode is disabled. The outputs are always controlled by the PHASE and WIDTH registers (00h~6Fh).

When $0V<V_{FSMD}<V_{TH3\_FS}$, or R_{FSMD}=10kΩ/27kΩ/51kΩ, the internal communication watchdog is active, and the fail-safe mode is enabled. If the watchdog times out, the device will enter fail-safe mode, and the outputs will be determined by the DEFAULT PULSE WIDTH registers (72h~77h). The CMWF bit in the FAULT_TYPEL register (94h) will be set to "1". When the CMWFM bit in the FAULT_MASKL register (96h) is set to "1", the FAULTB pin will go low to report the fault condition. In the fail-safe mode, the fault protections are also valid, including LED string open/short, single LED short, thermal shutdown, and thermal alarm, etc.

To switch from the fail-safe mode to normal mode, the host MCU must send an Update Command (special command) first and then write the CMWF bit in FAULT_TYPEL register (94h) to "0". The watchdog timer will be reset, and the FAULTB pin will return to a high impedance.

Note that the device must be re-initialized after quitting from the fail-safe mode to normal mode.

Table 11 Fail-safe Mode Setting

FSMD pin	Watchdog Timer	Default Value of DEFAULT PULSE WIDTH Registers (72h~77h)
$0V<V_{FSMD}<V_{TH1\_FS}$ or $R_{FSMD}=10k\Omega$	Active	0xFF
$V_{TH1\_FS}<V_{FSMD}<V_{TH2\_FS}$ or $R_{FSMD}=27k\Omega$		0x88
$V_{TH2\_FS}<V_{FSMD}<V_{TH3\_FS}$ or $R_{FSMD}=51k\Omega$		0x00
$V_{TH3\_FS}<V_{FSMD}<5.5V$ or connect FSMD to V5 via a 10kΩ resistor	Invalid	0x00

10.15 PWM DUTY CYCLE LOOPBACK VERIFICATION

To enhance its operation reliability, The IS32LT3365 integrates a loopback verification circuit with twelve multiplexed inputs to monitor the PWM duty cycle of internal switches. The twelve input channels are respectively connected to each output stage. The VFYCHSEL[3:0] bits in the VFYCTL register (C1h) selects the desired input channel for PWM duty cycle monitoring. Setting the VFYEN bit in the VFYCTL register (C1h) to "1" enables the loopback verification and clears VFYRDY bit in the VFYCFG register (C2h) to "0".

Once the verification is completed, the VFYRDY bit will be set to "1" and the PWM duty cycle measurement result is stored in the PWMDUTYH (C5h) and PWMDUTYL (C6h) registers. The loopback verification circuit compares the measurement result with the PWM duty cycle setting value in the PWM buffer. If the deviation is out of the tolerance, preset by the TOLERANCE[6:0] bits in the VFYCFG register (C2h), the corresponding loopback fault flag bit in DUTY_FAULTL or DUTY_FAULTH (C3h or C4h) and the DUTYF bit in FAULT_TYPEL (94h) will be set to "1". When the DUTYFM bit in the FAULT_MASKL register (96h) is set to "1", the FAULTB pin will go low to report the fault condition.

The corresponding loopback fault flag bit in DUTY_FAULTL or DUTY_FAULTH (C3h or C4h) and the DUTYF bit in FAULT_TYPEL register (94h) will reset to "0" once the deviation drops within the tolerance. Then the FAULTB pin will go back to a high impedance.

The tolerance, preset by the TOLERANCE[6:0] bits in the VFYCFG register (C2h), should not be set too low, especially in high PWM frequency applications. Otherwise, the loopback fault would be falsely triggered due to the accuracy of the PWM duty cycle measurement.

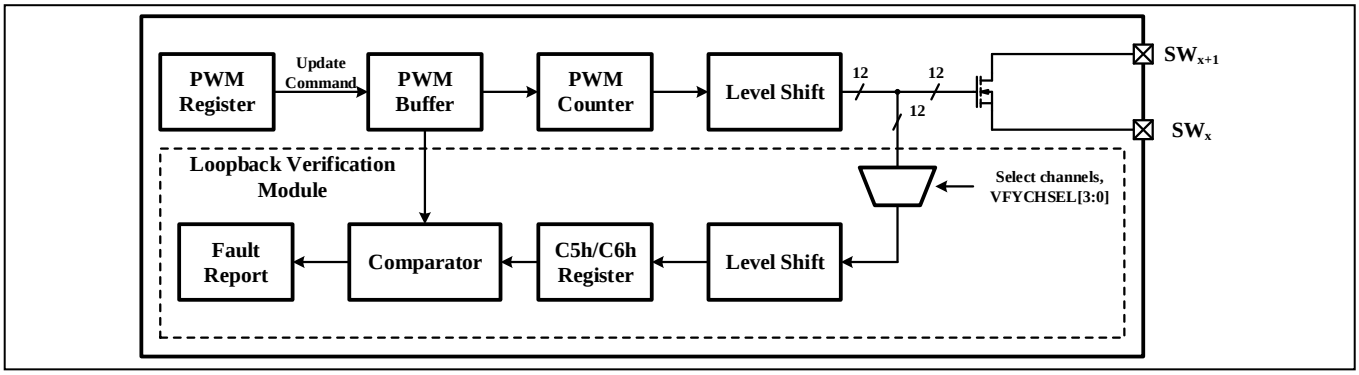


Figure 54 Loopback Verification Block

10.16 I²C MASTER FOR EXTERNAL EEPROM

The IS32LT3365 device includes an I²C master that allows the host MCU to access a local EEPROM via the UART or CANLITE interface. This feature allows the wiring harness between the ECU and the LED load board to have fewer connections and simplifies the hardware interconnect. The I²C master supports 7-bit addressing mode at SCL frequencies of 400kHz or less. It is intended primarily to communicate with an EEPROM device that stores lighting module configuration data.

In order for the I²C master to be used, external pull-up resistors (recommended value is 4.7kΩ) must be tied from SDA and SCL to either the V33 or V5 pin. The I2C_CLOCK register (A9h) must be programmed to attain the desired I²C bit-rate, and the I2CEN bit must be set to '1' in the SYSCFG register (80h). Once these two writes are performed, the I²C master logic is ready for read or write operation.

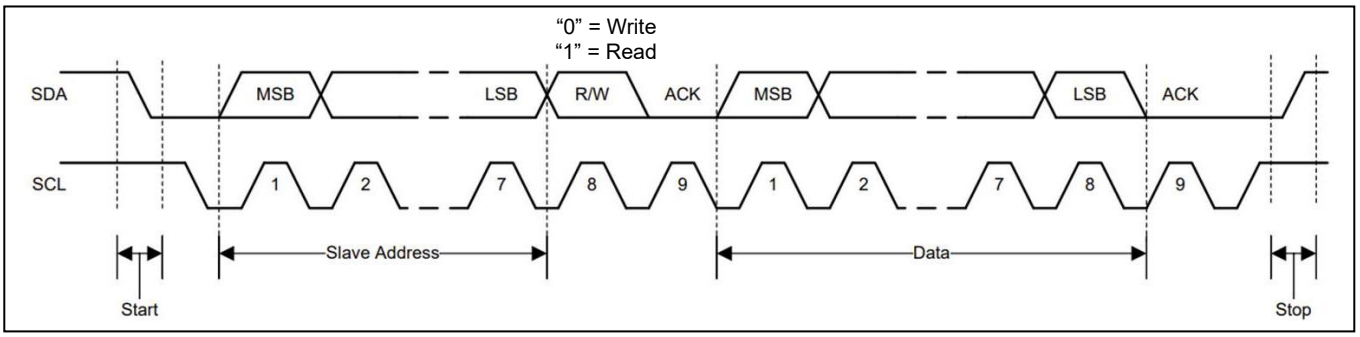


Figure 55 I²C Data Transfer

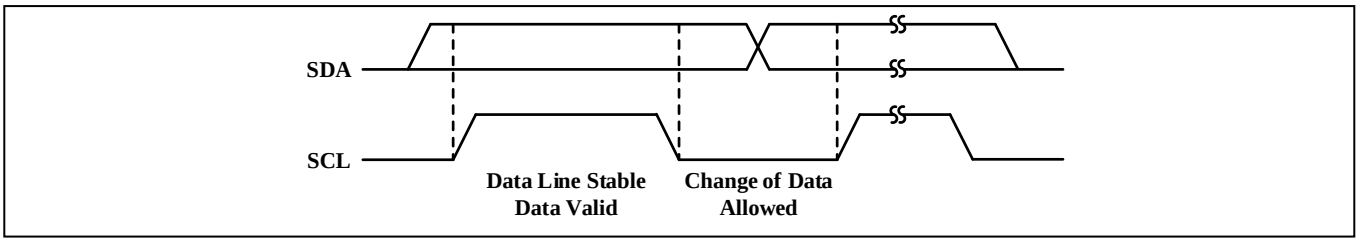


Figure 56 I²C Bit Transfer

IS32LT3365 I²C master uses command frame transmission mode. The I²C command frame type can be configured by I2CCMD[2:0] bits in I2C_CFG register (ACh). The command frame modes are listed in the table below.

Table 12 I²C Command Frame Mode Setting

I2CCMD [2:0]	Mode
111	One Byte Write
101	Burst Write
110	Set Start Address
001	Burst Read
011	Normal Read
010	One Times Polling EEPROM Ack
100	Auto Polling EEPROM Ack
Others	NA

The host MCU must program the slave ID (SLAVEID[6:0] bits in SLAVE_ID register (ADh)), the register address (I2C_REGADDRL and I2C_REGADDRH registers (AAh and ABh)) and the data bytes (I2CDAT01~I2CDAT16 registers (B0h~BFh)) to be sent to the EEPROM. Next, the host MCU issues the write command by writing the I2CRUN bit of the SLAVE_ID register (ADh) to a "1". Following an I²C command transaction, the host MCU may poll the I2C_STATE register (AEh) to check for the I2CBUSY bit to be cleared, indicating that the transaction is finished. After the I2CBUSY bit is cleared, the I2CTXF, and I2CACKF bits in the I2C_STATE register (AEh) must be checked. If any of these two bits are "1", the write command may be re-tried by writing the I2CRUN bit to "1" again.

10.16.1 One Byte Write

One Byte Write mode can implement single byte write to the external I²C EEPROM. The data sequence is shown in the figure below. It consists of a START condition, 7-bit EEPROM slave ID and the R/W bit ("0" for write), the register address and one data byte followed by a STOP condition. Each byte must be acknowledged by the EEPROM in order for the I²C master to continue to the next byte. Otherwise, the transfer is terminated prematurely with a STOP condition, and the appropriate error bit(s) are set in the I2C_STATE register (AEh). The I²C master supports either 8-bit or 16-bit register address, which can be configured by ESADRSEL bit in I2C_CFG register (ACh). The data byte to be sent is pre-stored in the I2CDAT01 register.

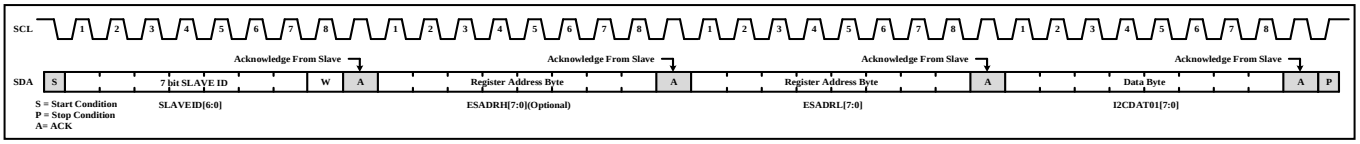


Figure 57 One Byte Write Sequence

10.16.2 Burst Write

Burst Write mode allows the I²C master to continuously write up to 16 bytes data in a single write cycle with the register address automatically incremented. The data length is specified by the DATLEN[3:0] value in I2C_CFG register (ACh). The data to be sent is stored in I2CDAT01-I2CDAT16 registers. The data sending sequence always starts from I2CDAT01. The I²C master sends from 1 to 16 byte of data, each of which must be acknowledged by the EEPROM in order for the I²C master to continue to the next byte. Otherwise, the transfer is terminated prematurely with a STOP condition, and the appropriate error bit(s) are set in the I2C_STATE register (AEh). For example, if the data length is 8, the data bytes to be sent will be I2CDAT01~I2CDAT08. The data sequence is shown in figure below. It consists of a START condition, 7-bit EEPROM slave ID and the R/W bit (“0” for write), and the start register address, N (1 to 16) bytes of data followed by a STOP condition. The start register address can be either 8-bit or 16-bit which can be configured by ESADRSEL bit in I2C_CFG register (ACh).

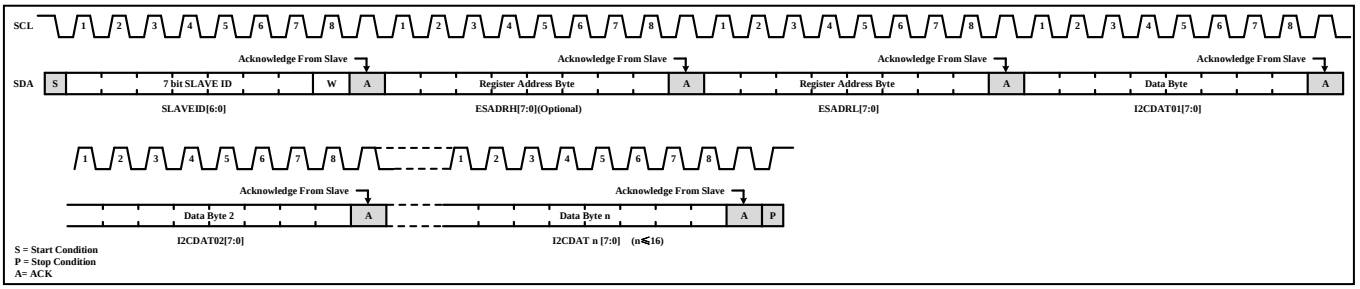


Figure 58 Burst Write Sequence

10.16.3 Set Start Address

The I²C master can write a start address to an external I²C EEPROM, which will be stored in the EEPROM and used for Burst Read. The data sequence is shown in the figure below. It consists of a START condition, 7-bit EEPROM slave ID and the R/W bit (“0” for write), and the start register address followed by a STOP condition. The start register address can be either 8-bit or 16-bit, which can be configured by ESADRSEL bit in I2C_CFG register (ACh). Each byte must be acknowledged by the EEPROM in order for the I²C master to continue to the next byte. Otherwise, the transfer is terminated prematurely with a STOP condition, and the appropriate error bit(s) are set in the I2C_STATE register (AEh).

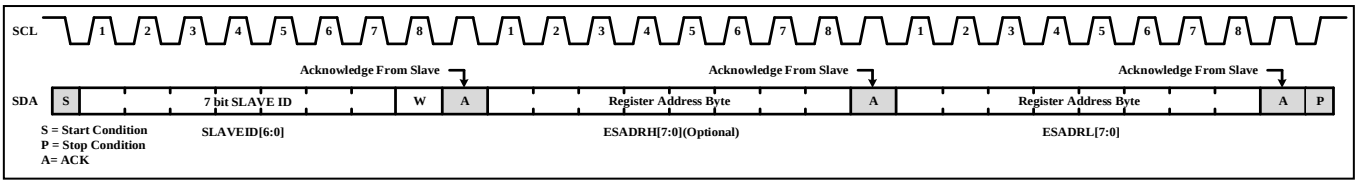


Figure 59 Set Start Address Sequence

10.16.4 Burst Read

Burst Read mode allows the I²C master to continuously read up to 16 bytes data in a single read cycle with the register address automatically incremented. This mode does not send the start register address, which must be specified by the Set Start Address in advance. The data sequence is shown in the figure below. The I²C master sends out a START condition, 7-bit EEPROM slave ID and the R/W bit (“1” for read), followed by an acknowledgement from the EEPROM. Then, the EEPROM continuously sends back 1 to 16 bytes of data, each of which will be followed by an acknowledgement from the I²C master. The read action is terminated by the last byte with no acknowledgment from the I²C master and a STOP condition. All read data is sequentially stored in I2CDAT01-I2CDAT16 registers (B0h~BFh).

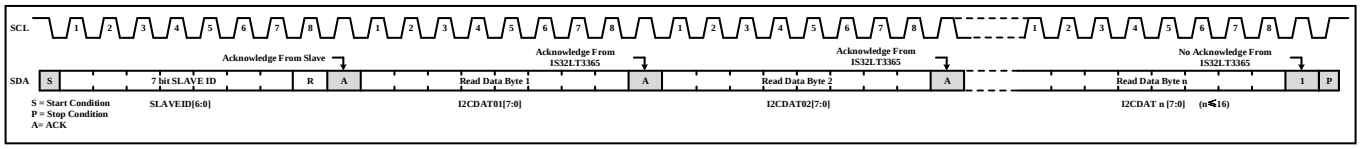


Figure 60 Burst Read Sequence

10.16.5 Normal Read

Normal Read mode also allows the I²C master to continuously read up to 16 bytes data with register address automatically incremented. However, compared to Burst Read mode, I²C master in this mode must send a start register address, which can be either 8-bit or 16-bit. The data sequence is shown in the figure below. The I2C master sends out a START condition, 7-bit EEPROM slave ID and the R/W bit (“0” for write), and the start register address followed by a STOP condition. Each byte must be followed by an acknowledge from the EEPROM in order for the I²C master to continue to the next byte, otherwise the transfer is terminated prematurely with a STOP condition, and the appropriate error bit(s) are set in the I2C_STATE register (AEh). Subsequently, The I²C master sends out a START condition, 7-bit EEPROM slave ID and the R/W bit (“1” for read), followed by an acknowledge from the EEPROM. Then the EEPROM continuously sends back 1 to 16 bytes of data, each of which will be followed by an acknowledgement from the I²C master. The read action is terminated by the last byte with no acknowledge from the I²C master and a STOP condition. All read data is sequentially stored in I2CDAT01-I2CDAT16 registers (B0h~BFh).

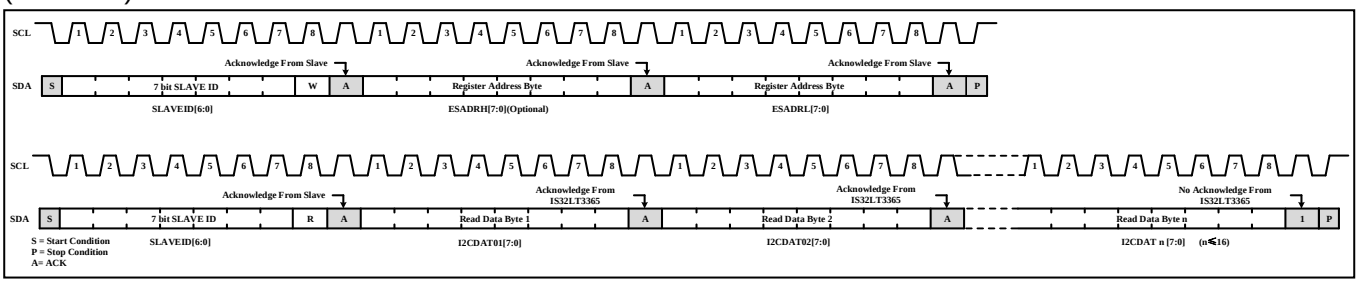


Figure 61 Normal Read Sequence

10.16.6 Auto Polling EEPROM ACK

Auto Polling EEPROM Ack mode is used to check the busy state of EEPROM. The data sequence is shown in the figure below. The I²C master only sends out a START bit, 7-bit EEPROM slave ID and the R/W bit (“0” for wirte). Then the I²C master waits for an acknowledgement from the EEPROM during the 9th bit time. If no acknowledgement is returned from the EEPROM, it means that the EEPROM is busy, so the EEPREADY bit in I2C_STATE register (AEh) will be set to “0”. The I2C master will repeat the polling in every five I²C clock cycles until get an acknowledgement. The EEPREADY bit will be set to “1”, indicating that the EEPROM is ready to receive next instruction.

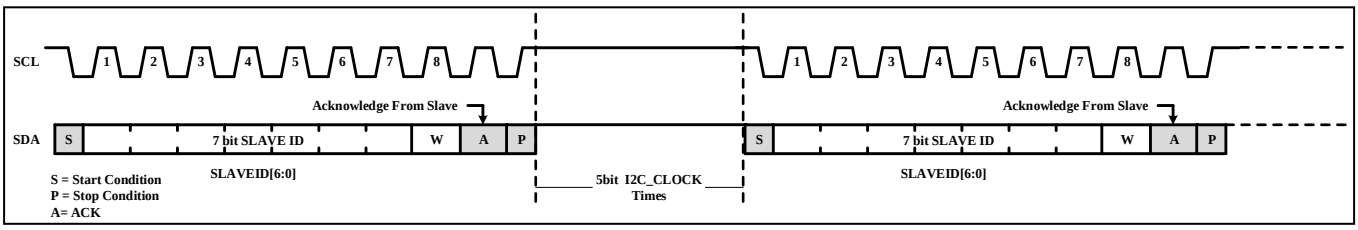


Figure 62 Auto Polling Sequence

10.16.7 One Times Polling EEPROM ACK

One Times Polling EEPROM Ack mode is used to check the busy state of EEPROM. The data sequence is shown in the figure below. The I²C master only sends out a START bit, 7-bit EEPROM slave ID and the R/W bit (“0” for write). Then the I2C master waits for an acknowledgement from the EEPROM during the 9th bit time. If an acknowledgement is returned from the EEPROM, the EEPREADY bit in I2C_STATE register (AEh) will be set to “1”, indicating that the EEPROM is ready to receive next instruction. Otherwise, it means that the EEPROM is busy so the EEPREADY bit will be set to “0”.

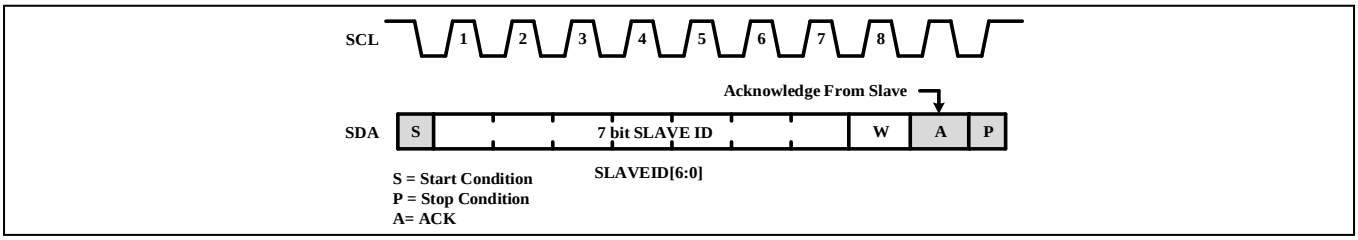


Figure 63 One Times Polling Sequence

10.16.8 EEPROM Operation Examples

Example 1: host MCU Writes 4 Bytes of Data to EEPROM Operation

IS32LT3365 Device ID with parity = 0x20, EEPROM slave ID = 50h, write 4 bytes data (0x55, 0x66, 0x77, 0x88) into 00h-03h registers of EEPROM

Registers configuration to I²C master:

Registers Setting	Function description
I2CEN bit = 1 in SYSCFG register (80h)	Enable I²C master
I2CDAT01 register (B0h) = 0x55	Fill in data 1
I2CDAT02 register (B1h) = 0x66	Fill in data 2
I2CDAT03 register (B2h) = 0x77	Fill in data 3
I2CDAT04 register (B3h) = 0x88	Fill in data 4
I2CCLK[5:0] bits = 0b011100 in I2C_CLOCK register (A9h)	Set I²C clock frequency to 46kHz
I2C_REGADDRL register (AAh) = 0x00	Configure Start Register Address low byte
I2C_REGADDRH register (ABh) = 0x00	Configure Start Register Address high byte
ESADRSEL bit = 0 in I2C_CFG register (ACh)	Select 8-bit EEPROM register address
I2CCMD[2:0] bits = 0b101 in I2C_CFG register (ACh)	Select Burst Write Mode
DATLEN[3:0] bits = 0b0011 in I2C_CFG register (ACh)	Select 4 bytes data length
SLAVEID[6:0] bits = 0x50 in SLAVE_ID register (ADh)	Configure 7-bit EEPROM slave ID
I2CRUN bit = 1 in SLAVE_ID register (ADh)	Starts I²C command transmission

Command frame 1: enable I²C master

Interface	Command Frame					
	CMD Frame Header	Device ID	Start Register Address	Data 1	CRC_L	CRC_H
UART/ CANLITE	0x80	0x20	0x80	0xC4	0x48	0x59

Command frame 2: write data to I2CDAT01- I2CDAT04 registers

Interface	Command Frame								
	CMD Frame Header	Device ID	Start Register Address	Data 1	Data 2	Data 3	Data 4	CRC_L	CRC_H
UART/ CANLITE	0x83	0x20	0xB0	0x55	0x66	0x77	0x88	0x22	0x37

Command frame 3: write I²C master configuration registers, then IS32LT3365 will write data into EEPROM

Interface	Command Frame									
	CMD Frame Header	Device ID	Start Register Address	Data 1	Data 2	Data 3	Data 4	Data 5	CRC_L	CRC_H
UART/ CANLITE	0x84	0x20	0xA9	0x1C	0x00	0x00	0x53	0xD0	0xDC	0XC6

Example 2: host MCU reads 4 Bytes of Data from EEPROM Operation

IS32LT3365 Device ID with parity = 0x20, EEPROM slave ID = 50h, read 4 bytes data (0x55, 0x66, 0x77, 0x88) from 00h-03h registers of EEPROM

Registers configuration to I²C master:

Registers Setting	Function Description
I2CEN bit = 1 in SYSCFG register (80h)	Enable I²C master
I2CCLK[5:0] bits = 0b011100 in I2C_CLOCK register (A9h)	Set I²C clock frequency to 46kHz
I2C_REGADDRL register (AAh) = 0x00	Configure Start Register Address low byte
I2C_REGADDRH register (ABh) = 0x00	Configure Start Register Address high byte
ESADRSEL bit = 0 in I2C_CFG register (ACh)	Select 8-bit EEPROM register address
I2CCMD[2:0] bits = 0b011 in I2C_CFG register (ACh)	Select Normal Read Mode
DATLEN[3:0] bits = 0b0011 in I2C_CFG register (ACh)	Select 4 bytes data length
SLAVEID[6:0] bits = 0x50 in SLAVE_ID register (ADh)	Configure 7-bit EEPROM slave ID
I2CRUN bit = 1 in SLAVE_ID register (ADh)	Starts I²C command transmission

Command frame 1: enable I²C master

Interface	Command Frame					
	CMD Frame Header	Device ID	Start Register Address	Data 1	CRC_L	CRC_H
UART/ CANLITE	0x80	0x20	0x80	0xC4	0x48	0x59

Command frame 2: write I²C master configuration registers. IS32LT3365 will read the data from EEPROM and store data in I2CDAT01-I2CDAT04 registers (address B0h-B3h).

Interface	Command Frame									
	CMD Frame Header	Device ID	Start Register Address	Data 1	Data 2	Data 3	Data 4	Data 5	CRC_L	CRC_H
UART/ CANLITE	0x84	0x20	0xA9	0x1C	0x00	0x00	0x33	0xD0	0xF4	0xC6

Command frame 3: Host MCU reads I2CDAT01-I2CDAT04 registers (address B0h-B3h) data from IS32LT3365

Interface	Command Frame				
	CMD Frame Header	Device ID	Start Register Address	CRC_L	CRC_H
UART/ CANLITE	0xC3	0x20	0xB0	0xE8	0x48

Command frame 4: IS32LT3365 responses to host MCU

Interface	Command Frame							
	RSP Frame Header	Device ID	Data 1	Data 2	Data 3	Data 4	CRC_L	CRC_H
UART/ CANLITE	0x03	0x20	0x55	0x66	0x77	0x88	0xEA	0x8D

I²C master checks whether the EEPROM is ready sequence flow-chart:

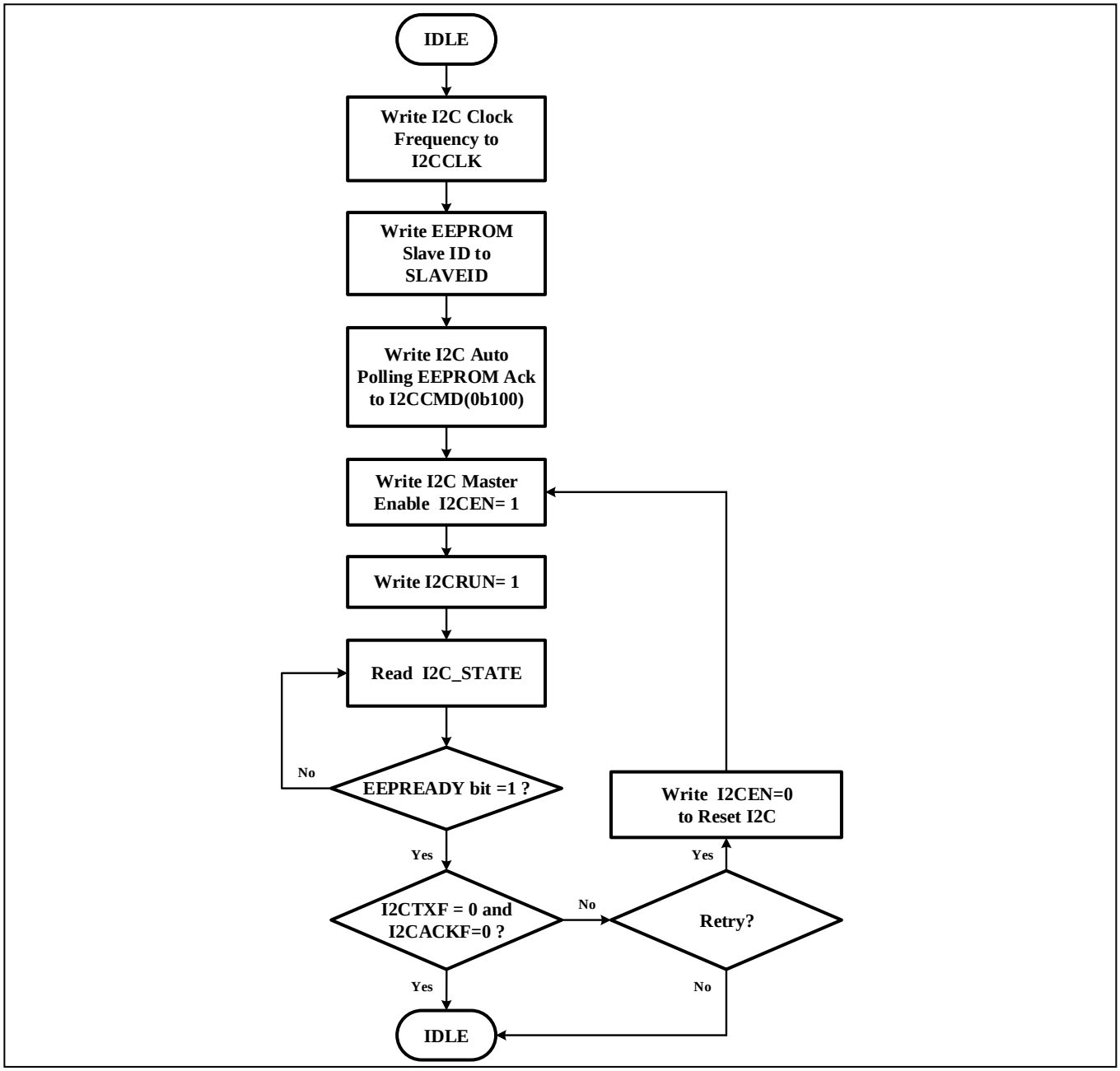


Figure 64 Check EEPROM Ready

I²C master writes N bytes of data to EEPROM sequence flow-chart:

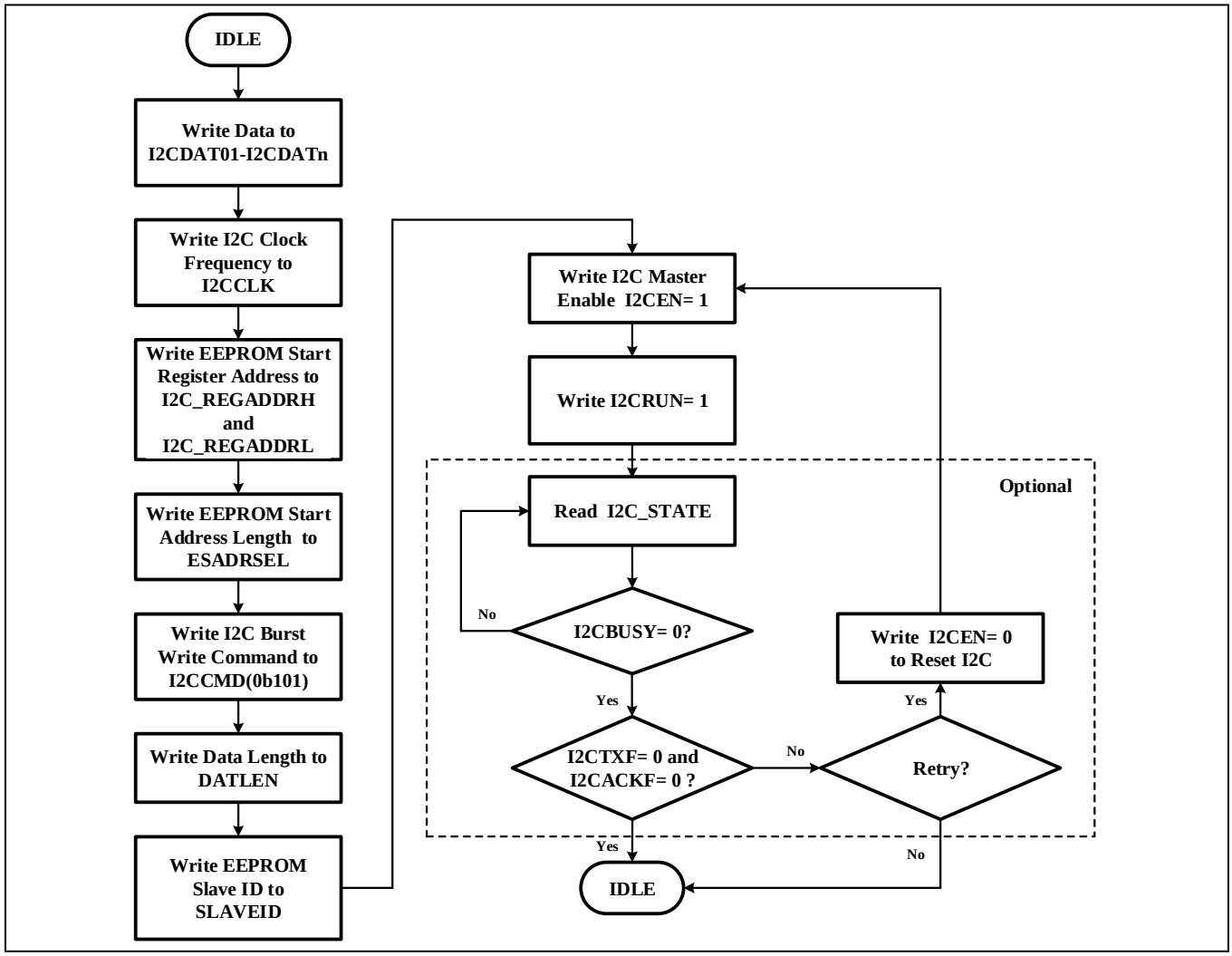


Figure 65 Write N Bytes Data

I²C master reads N bytes of data from EEPROM sequence flow-chart:

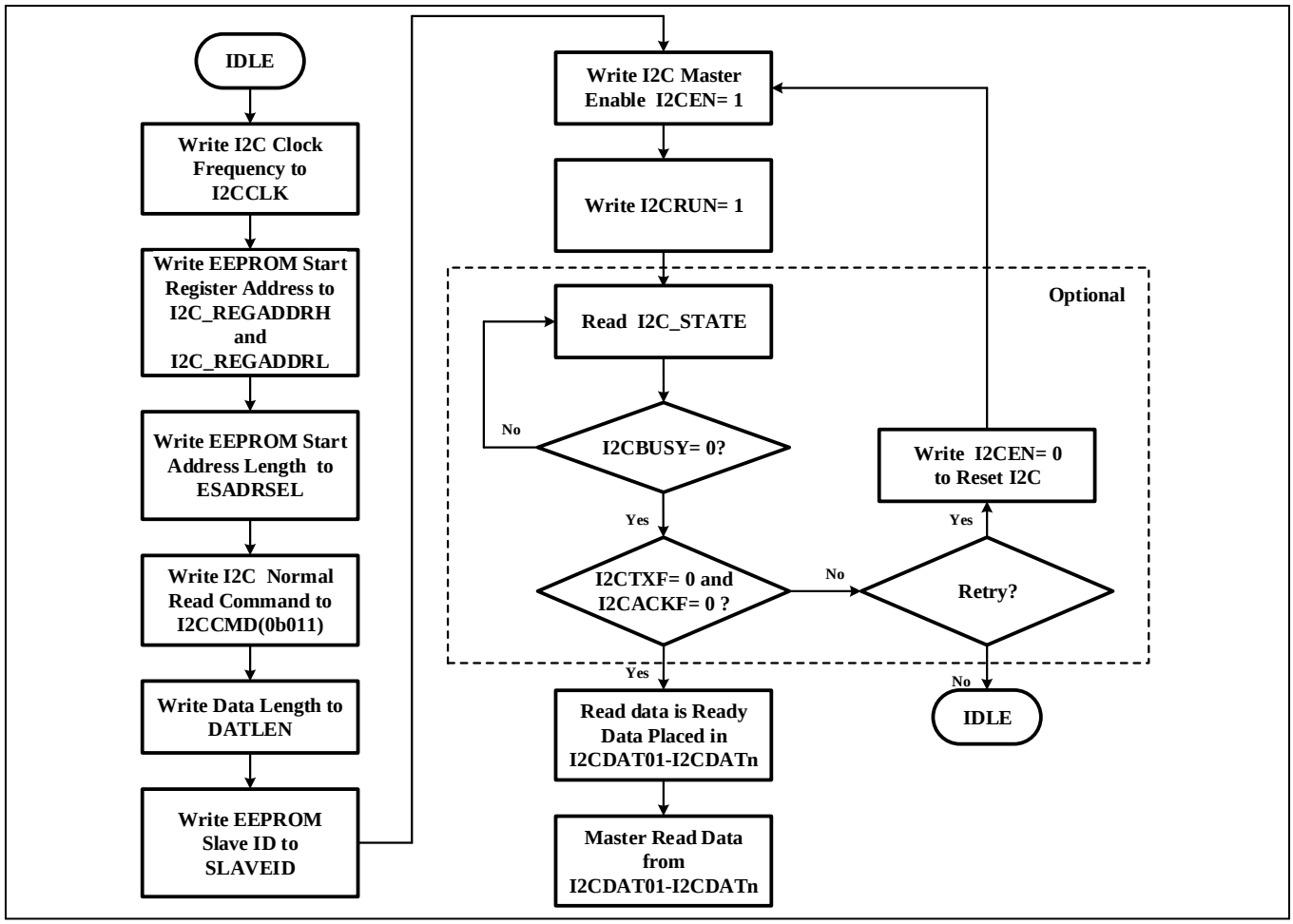


Figure 66 Read N Bytes Data

11 REGISTER

11.1 REGISTER MAP

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
LED Phase-Shift Registers and Width Registers Map Groups 1 (00h-1Fh)										
00h	MG1_PHASE01L	PHASE01[7:0]								0b 00000000
01h	MG1_PHASE02L	PHASE02[7:0]								0b 01010000
02h	MG1_PHASE03L	PHASE03[7:0]								0b 10100000
03h	MG1_PHASE03-01H	RSVD		PHASE03[9:8]		PHASE02[9:8]		PHASE01[9:8]		0b 00000000
04h	MG1_PHASE04L	PHASE04[7:0]								0b 11110000
05h	MG1_PHASE05L	PHASE05[7:0]								0b 01000000
06h	MG1_PHASE06L	PHASE06[7:0]								0b 10010000
07h	MG1_PHASE06-04H	RSVD		PHASE06[9:8]		PHASE05[9:8]		PHASE04[9:8]		0b 00010100
08h	MG1_PHASE07L	PHASE07[7:0]								0b 11100000
09h	MG1_PHASE08L	PHASE08[7:0]								0b 00110000
0Ah	MG1_PHASE09L	PHASE09[7:0]								0b 10000000
0Bh	MG1_PHASE09-07H	RSVD		PHASE09[9:8]		PHASE08[9:8]		PHASE07[9:8]		0b 00101001
0Ch	MG1_PHASE10L	PHASE10[7:0]								0b 11010000
0Dh	MG1_PHASE11L	PHASE11[7:0]								0b 00100000
0Eh	MG1_PHASE12L	PHASE12[7:0]								0b 01110000
0Fh	MG1_PHASE12-10H	RSVD		PHASE12[9:8]		PHASE11[9:8]		PHASE10[9:8]		0b 00111110
10h	MG1_WIDTH01L	WIDTH01[7:0]								0b 00000000
11h	MG1_WIDTH02L	WIDTH02[7:0]								0b 00000000
12h	MG1_WIDTH03L	WIDTH03[7:0]								0b 00000000
13h	MG1_WIDTH03-01H	RSVD		WIDTH03[9:8]		WIDTH02[9:8]		WIDTH01[9:8]		0b 00000000
14h	MG1_WIDTH04L	WIDTH04[7:0]								0b 00000000
15h	MG1_WIDTH05L	WIDTH05[7:0]								0b 00000000
16h	MG1_WIDTH06L	WIDTH06[7:0]								0b 00000000
17h	MG1_WIDTH06-04H	RSVD		WIDTH06[9:8]		WIDTH05[9:8]		WIDTH04[9:8]		0b 00000000
18h	MG1_WIDTH07L	WIDTH07[7:0]								0b 00000000
19h	MG1_WIDTH08L	WIDTH08[7:0]								0b 00000000
1Ah	MG1_WIDTH09L	WIDTH09[7:0]								0b 00000000
1Bh	MG1_WIDTH09-07H	RSVD		WIDTH09[9:8]		WIDTH08[9:8]		WIDTH07[9:8]		0b 00000000
1Ch	MG1_WIDTH10L	WIDTH10[7:0]								0b 00000000
1Dh	MG1_WIDTH11L	WIDTH11[7:0]								0b 00000000
1Eh	MG1_WIDTH12L	WIDTH12[7:0]								0b 00000000
1Fh	MG1_WIDTH12-10H	RSVD		WIDTH12[9:8]		WIDTH11[9:8]		WIDTH10[9:8]		0b 00000000

REGISTER MAP (CONTINUED)

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
LED Phase-Shift Registers and Width Registers Map Groups 2(20h-3Fh)										
20h	MG2_PHASE01H	PHASE01[9:2]								0b 00000000
21h	MG2_PHASE02H	PHASE02[9:2]								0b 00010100
22h	MG2_PHASE03H	PHASE03[9:2]								0b 00101000
23h	MG2_PHASE04H	PHASE04[9:2]								0b 00111100
24h	MG2_PHASE05H	PHASE05[9:2]								0b 01010000
25h	MG2_PHASE06H	PHASE06[9:2]								0b 01100100
26h	MG2_PHASE07H	PHASE07[9:2]								0b 01111000
27h	MG2_PHASE08H	PHASE08[9:2]								0b 10001100
28h	MG2_PHASE09H	PHASE09[9:2]								0b 10100000
29h	MG2_PHASE10H	PHASE10[9:2]								0b 10110100
2Ah	MG2_PHASE11H	PHASE11[9:2]								0b 11001000
2Bh	MG2_PHASE12H	PHASE12[9:2]								0b 11011100
2Ch	MG2_PHASE03_01L	RSVD		PHASE03[1:0]		PHASE02[1:0]		PHASE01[1:0]		0b 00000000
2Dh	MG2_PHASE06_04L	RSVD		PHASE06[1:0]		PHASE05[1:0]		PHASE04[1:0]		0b 00000000
2Eh	MG2_PHASE09_07L	RSVD		PHASE09[1:0]		PHASE08[1:0]		PHASE07[1:0]		0b 00000000
2Fh	MG2_PHASE12_10L	RSVD		PHASE12[1:0]		PHASE11[1:0]		PHASE10[1:0]		0b 00000000
30h	MG2_WIDTH01H	WIDTH01[9:2]								0b 00000000
31h	MG2_WIDTH02H	WIDTH02[9:2]								0b 00000000
32h	MG2_WIDTH03H	WIDTH03[9:2]								0b 00000000
33h	MG2_WIDTH04H	WIDTH04[9:2]								0b 00000000
34h	MG2_WIDTH05H	WIDTH05[9:2]								0b 00000000
35h	MG2_WIDTH06H	WIDTH06[9:2]								0b 00000000
36h	MG2_WIDTH07H	WIDTH07[9:2]								0b 00000000
37h	MG2_WIDTH08H	WIDTH08[9:2]								0b 00000000
38h	MG2_WIDTH09H	WIDTH09[9:2]								0b 00000000
39h	MG2_WIDTH10H	WIDTH10[9:2]								0b 00000000
3Ah	MG2_WIDTH11H	WIDTH11[9:2]								0b 00000000
3Bh	MG2_WIDTH12H	WIDTH12[9:2]								0b 00000000
3Ch	MG2_WIDTH03_01L	RSVD		WIDTH03[1:0]		WIDTH02[1:0]		WIDTH01[1:0]		0b 00000000
3Dh	MG2_WIDTH06_04L	RSVD		WIDTH06[1:0]		WIDTH05[1:0]		WIDTH04[1:0]		0b 00000000
3Eh	MG2_WIDTH09_07L	RSVD		WIDTH09[1:0]		WIDTH08[1:0]		WIDTH07[1:0]		0b 00000000
3Fh	MG2_WIDTH12_10L	RSVD		WIDTH12[1:0]		WIDTH11[1:0]		WIDTH10[1:0]		0b 00000000

REGISTER MAP (CONTINUED)

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
LED Phase-Shift Registers and Width Registers Map Groups 3 (40h-5Dh)										
40h	MG3_PHASE01L	PHASE01[7:0]								0b 00000000
41h	MG3_PHASE01H	RSVD						PHASE01[9:8]		0b 00000000
42h	MG3_WIDTH01L	WIDTH01[7:0]								0b 00000000
43h	MG3_WIDTH01H	RSVD						WIDTH01[9:8]		0b 00000000
44h	MG3_PHASE02L	PHASE02[7:0]								0b 01010000
45h	MG3_PHASE02H	RSVD						PHASE02[9:8]		0b 00000000
46h	MG3_WIDTH02L	WIDTH02[7:0]								0b 00000000
47h	MG3_WIDTH02H	RSVD						WIDTH02[9:8]		0b 00000000
48h	MG3_PHASE03L	PHASE03[7:0]								0b 10100000
49h	MG3_PHASE03H	RSVD						PHASE03[9:8]		0b 00000000
4Ah	MG3_WIDTH03L	WIDTH03[7:0]								0b 00000000
4Bh	MG3_WIDTH03H	RSVD						WIDTH03[9:8]		0b 00000000
4Ch	MG3_PHASE04L	PHASE04[7:0]								0b 11110000
4Dh	MG3_PHASE04H	RSVD						PHASE04[9:8]		0b 00000000
4Eh	MG3_WIDTH04L	WIDTH04[7:0]								0b 00000000
4Fh	MG3_WIDTH04H	RSVD						WIDTH04[9:8]		0b 00000000
50h	MG3_PHASE05L	PHASE05[7:0]								0b 01000000
51h	MG3_PHASE05H	RSVD						PHASE05[9:8]		0b 00000001
52h	MG3_WIDTH05L	WIDTH05[7:0]								0b 00000000
53h	MG3_WIDTH05H	RSVD						WIDTH05[9:8]		0b 00000000
54h	MG3_PHASE06L	PHASE06[7:0]								0b 10010000
55h	MG3_PHASE06H	RSVD						PHASE06[9:8]		0b 00000001
56h	MG3_WIDTH06L	WIDTH06[7:0]								0b 00000000
57h	MG3_WIDTH06H	RSVD						WIDTH06[9:8]		0b 00000000
58h	MG3_PHASE07L	PHASE07[7:0]								0b 11100000
59h	MG3_PHASE07H	RSVD						PHASE07[9:8]		0b 00000001
5Ah	MG3_WIDTH07L	WIDTH07[7:0]								0b 00000000
5Bh	MG3_WIDTH07H	RSVD						WIDTH07[9:8]		0b 00000000
5Ch	MG3_PHASE08L	PHASE08[7:0]								0b 00110000
5Dh	MG3_PHASE08H	RSVD						PHASE08[9:8]		0b 00000010

REGISTER MAP (CONTINUED)

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
LED Phase-Shift Registers and Width Registers Map Groups 3 (5Eh-6Fh)										
5Eh	MG3_WIDTH08L	WIDTH08[7:0]								0b 00000000
5Fh	MG3_WIDTH08H	RSVD						WIDTH08[9:8]		0b 00000000
60h	MG3_PHASE09L	PHASE09[7:0]								0b 10000000
61h	MG3_PHASE09H	RSVD						PHASE09[9:8]		0b 00000010
62h	MG3_WIDTH09L	WIDTH09[7:0]								0b 00000000
63h	MG3_WIDTH09H	RSVD						WIDTH09[9:8]		0b 00000000
64h	MG3_PHASE10L	PHASE10[7:0]								0b 11010000
65h	MG3_PHASE10H	RSVD						PHASE10[9:8]		0b 00000010
66h	MG3_WIDTH10L	WIDTH10[7:0]								0b 00000000
67h	MG3_WIDTH10H	RSVD						WIDTH10[9:8]		0b 00000000
68h	MG3_PHASE11L	PHASE11[7:0]								0b 00100000
69h	MG3_PHASE11H	RSVD						PHASE11[9:8]		0b 00000011
6Ah	MG3_WIDTH11L	WIDTH11[7:0]								0b 00000000
6Bh	MG3_WIDTH11H	RSVD						WIDTH11[9:8]		0b 00000000
6Ch	MG3_PHASE12L	PHASE12[7:0]								0b 01110000
6Dh	MG3_PHASE12H	RSVD						PHASE12[9:8]		0b 00000011
6Eh	MG3_WIDTH12L	WIDTH12[7:0]								0b 00000000
6Fh	MG3_WIDTH12H	RSVD						WIDTH12[9:8]		0b 00000000

REGISTER MAP (CONTINUED)

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
70h	SLEWRATE	SLEW_12_10[1:0]		SLEW_09_07[1:0]		SLEW_06_04[1:0]		SLEW_03_01[1:0]		0b 11111111
71h	PARLED	RSVD						PARLED[1:0]		0b 00000000
72h	DEFWIDTH02_01	DEFWIDTH02[3:0]				DEFWIDTH01[3:0]				0b xxxxxxxx
73h	DEFWIDTH04_03	DEFWIDTH04[3:0]				DEFWIDTH03[3:0]				0b xxxxxxxx
74h	DEFWIDTH06_05	DEFWIDTH06[3:0]				DEFWIDTH05[3:0]				0b xxxxxxxx
75h	DEFWIDTH08_07	DEFWIDTH08[3:0]				DEFWIDTH07[3:0]				0b xxxxxxxx
76h	DEFWIDTH10_09	DEFWIDTH10[3:0]				DEFWIDTH09[3:0]				0b xxxxxxxx
77h	DEFWIDTH12_11	DEFWIDTH12[3:0]				DEFWIDTH11[3:0]				0b xxxxxxxx
78h	ENPWML	ENPWM(8:1)								0b 11111111
79h	ENPWMH	RSVD				ENPWM(12:9)				0b 11111111
7Ah	TEMP_TH	RSVD						OVER_TEMP_TH[1:0]		0b 00000000
7Bh	SSCCFGA	SSCEN	RSVD					SSC[1:0]		0b 00000000
7Ch	CLK_MSI	RSVD						INDEPEN	MS_SL	0b 00000010
7Dh	TCNTL	TCNT[9:2]								0b xxxxxxxx
7Eh	TCNTH	RSVD						TCNT[1:0]		0b 000000xx
7Fh	RSVD	RSVD								0b xxxxxxxx
80h	SYSCFG	RSVD	I2CEN	ACKEN	PSON	RSVD	SYNCOEN	SYNCPEN	PWR	0b 10000100
81h	CMWTAP	RSVD					CMWTAP[2:0]			0b 00000100
82h	PWMTICK	PTBASE[1:0]		PTCNT[5:0]						0b 01000000
84h	LED01_OS	LED01_OF_EN	LED01_OPEN_TH[1:0]		LED01_SF_EN	LED01_SHORT_TH[3:0]				0b 11110000
85h	LED02_OS	LED02_OF_EN	LED02_OPEN_TH[1:0]		LED02_SF_EN	LED02_SHORT_TH[3:0]				0b 11110000
86h	LED03_OS	LED03_OF_EN	LED03_OPEN_TH[1:0]		LED03_SF_EN	LED03_SHORT_TH[3:0]				0b 11110000
87h	LED04_OS	LED04_OF_EN	LED04_OPEN_TH[1:0]		LED04_SF_EN	LED04_SHORT_TH[3:0]				0b 11110000
88h	LED05_OS	LED05_OF_EN	LED05_OPEN_TH[1:0]		LED05_SF_EN	LED05_SHORT_TH[3:0]				0b 11110000
89h	LED06_OS	LED06_OF_EN	LED06_OPEN_TH[1:0]		LED06_SF_EN	LED06_SHORT_TH[3:0]				0b 11110000
8Ah	LED07_OS	LED07_OF_EN	LED07_OPEN_TH[1:0]		LED07_SF_EN	LED07_SHORT_TH[3:0]				0b 11110000
8Bh	LED08_OS	LED08_OF_EN	LED08_OPEN_TH[1:0]		LED08_SF_EN	LED08_SHORT_TH[3:0]				0b 11110000
8Ch	LED09_OS	LED09_OF_EN	LED09_OPEN_TH[1:0]		LED09_SF_EN	LED09_SHORT_TH[3:0]				0b 11110000
8Dh	LED10_OS	LED10_OF_EN	LED10_OPEN_TH[1:0]		LED10_SF_EN	LED10_SHORT_TH[3:0]				0b 11110000
8Eh	LED11_OS	LED11_OF_EN	LED11_OPEN_TH[1:0]		LED11_SF_EN	LED11_SHORT_TH[3:0]				0b 11110000
8Fh	LED12_OS	LED12_OF_EN	LED12_OPEN_TH[1:0]		LED12_SF_EN	LED12_SHORT_TH[3:0]				0b 11110000

REGISTER MAP (CONTINUED)

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
90h	SHORT_FAULTL	SHORT_FAULT(8:1)								0b 00000000
91h	SHORT_FAULTH	RSVD				SHORT_FAULT(12:9)				0b 00000000
92h	OPEN_FAULTL	OPEN_FAULT(8:1)								0b 00000000
93h	OPEN_FAULTH	RSVD				OPEN_FAULT(12:9)				0b 00000000
94h	FAULT_TYPEL	I2CF	CRCF	TSDF	CMWF	DUTYF	OVTMPF	SHORTF	OPENF	0b 00000000
95h	FAULT_TYPEH	RSVD						V33OVF	V5OVF	0b 00000000
96h	FAULT_MASKL	I2CFM	CRCFM	TSDFM	CMWFM	DUTYFM	OVTMPFM	SHORTFM	OPENFM	0b 11111111
97h	FAULT_MASKH	RSVD						V33OVFM	V5OVFM	0b 00000011
98h	CERRCNT	CERRCNT[7:0]								0b 00000000
99h	ADCCHSEL	RSVD			ADCCH_SEL[4:0]					0b 00000000
9Ah	ADCCFG	RSVD			ADCEN	ADC_CLK[1:0]		ADCSH[1:0]		0b 00000000
9Bh	ADCCTL	ADCCYC_F	ADC_AVG[1:0]		LOOP	SADC	RSVD			0b 00000000
9Dh	ADC_NTCH_L	RSVD						ADC_NTCH[1:0]		0b 00000000
9Eh	ADC_NTCH_H	ADC_NTCH[9:2]								0b 00000000
9Fh	ADC_NTCL_L	RSVD						ADC_NTCL[1:0]		0b 00000000
A0h	ADC_NTCL_H	ADC_NTCL[9:2]								0b 00000000
A1h	ADC_VPTAT_L	RSVD						ADC_VPTAT[1:0]		0b 00000000
A2h	ADC_VPTAT_H	ADC_VPTAT[9:2]								0b 00000000
A3h	ADC_V5_L	RSVD						ADC_V5[1:0]		0b 00000000
A4h	ADC_V5_H	ADC_V5[9:2]								0b 00000000
A5h	ADC_V33_L	RSVD						ADC_V33[1:0]		0b 00000000
A6h	ADC_V33_H	ADC_V33[9:2]								0b 00000000
A9h	I2C_CLOCK	RSVD		I2CCLK[5:0]						0b 00011100
AAh	I2C_REGADDRL	ESADRL[7:0]								0b 00000000
ABh	I2C_REGADDRH	ESADRH[7:0]								0b 00000000
ACh	I2C_CFG	ESADRSEL	I2CCMD[2:0]			DATLEN[3:0]				0b 00000000
ADh	SLAVE_ID	I2CRUN	SLAVEID[6:0]							0b 00000000
AEh	I2C_STATE	EEPREADY	I2CBUSY	I2CTXF	I2CACKF	RSVD				0b 00000000
AFh	I2CBMON	RSVD						SCL	SDA	0b 000000xx
B0h	I2CDAT01	I2CDAT01[7:0]								0b 00000000
B1h	I2CDAT02	I2CDAT02[7:0]								0b 00000000
B2h	I2CDAT03	I2CDAT03[7:0]								0b 00000000
B3h	I2CDAT04	I2CDAT04[7:0]								0b 00000000

REGISTER MAP (CONTINUED)

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
B4h	I2CDAT05	I2CDAT05[7:0]								0b 00000000
B5h	I2CDAT06	I2CDAT06[7:0]								0b 00000000
B6h	I2CDAT07	I2CDAT07[7:0]								0b 00000000
B7h	I2CDAT08	I2CDAT08[7:0]								0b 00000000
B8h	I2CDAT09	I2CDAT09[7:0]								0b 00000000
B9h	I2CDAT10	I2CDAT10[7:0]								0b 00000000
BAh	I2CDAT11	I2CDAT11[7:0]								0b 00000000
BBh	I2CDAT12	I2CDAT12[7:0]								0b 00000000
BCh	I2CDAT13	I2CDAT13[7:0]								0b 00000000
BDh	I2CDAT14	I2CDAT14[7:0]								0b 00000000
BEh	I2CDAT15	I2CDAT15[7:0]								0b 00000000
BFh	I2CDAT16	I2CDAT16[7:0]								0b 00000000
C0h	BSTSTA	RSVD						FAIL	FINISH	0b 00000001
C1h	VFYCTL	VFYCHSEL[3:0]				FBTEN	INTDATA	AUTOLOOP	VFYEN	0b 00000000
C2h	VFYCFG	VFYRDY	TOLERANCE[6:0]							0b 00000010
C3h	DUTY_FAULT_L	DUTY_FAULT(8:1)								0b 00000000
C4h	DUTY_FAULT_H	RSVD				DUTY_FAULT(12:9)				0b 00000000
C5h	PWMDUTYH	PWMDUTY[9:2]								0b 00000000
C6h	PWMDUTYL	RSVD						PWMDUTY[1:0]		0b 00000000
C7h	ICID	ICID[7:0]								0b 10100001

Note 4: “RSVD” means “Reserved”.

11.2 REGISTERS DEFINITION

LED Phase-Shift Registers and Width Registers – Read/Write (00h-6Fh)

The PHASE and WIDTH register addresses are from 0x00 to 0x6F. There are 10-bit registers to control the phase shift and pulse width of the LEDs with respect to the PWM counter (TCNT). These registers are the PHASE and WIDTH registers, respectively. These registers may be written or read using three register map groups. These three map groups all communicate with a common set of registers internally. The data written into any map group will be synchronized into the other two map groups. The PHASE and WIDTH values are interpreted as follows:

PHASE[9:0] defines the count value within the 10-bit TCNT period when a start pulse is sent to a given PWM generator. Each adjacent channel has a phase delay with a default value of 80.

Table 13 Default Phase Delay Value

CHANNELS	PHASE
LED1	0
LED2	80
LED3	160
……	…..
LED12	880

WIDTH[9:0] defines the count value within the 10-bit of LED ON pulse width. 0% Duty Cycle: If WIDTH=0 for a given LED, that LED turns off and remains off (no PWM). 100% Duty Cycle: If WIDTH = 1023 for a given LED, that LED turns on and remains on (no PWM).

PHASE/WIDTH Registers Map Group 1 (MG1_PHASE and MG1_WIDTH) – Read/Write

The PHASE/WIDTH Register Map Groups 1 groups the most significant bits (MSBs) of the PHASE and WIDTH values together. This makes a total of 16 PHASE registers (at addresses 00h through 0Fh) and 16 WIDTH registers (at addresses 10h through 1Fh).

PHASE/WIDTH Registers Map Group 2 (MG2_PHASE and MG2_WIDTH) – Read/Write

The PHASE/WIDTH Register Map Groups 2 groups the two least significant bits (LSBs) of each LED PHASE and WIDTH value together and places these packed registers at the end of each register set. This makes a total of 16 PHASE registers (at addresses 20h through 2Fh) and 16 WIDTH registers (at addresses 30h through 3Fh).

PHASE/WIDTH Registers Map Group 3 (MG3_PHASE and MG2_WIDTH) – Read/Write

The PHASE/WIDTH Register Map Group 3 allows all twenty bits to be written or read for a single LED in one transaction without a need to write or read other LEDs' settings. This makes a total of 48 registers (at addresses 40h through 6Fh).

The configuration of these registers must be updated by the "Update Command".

Slew Rate Register – Read/Write

ADDR	REG NAME	D7:D6	D5:D4	D3:D2	D1:D0	DEFAULT
70h	SLEWRATE	SLEW_12_10[1:0]	SLEW_09_07[1:0]	SLEW_06_04[1:0]	SLEW_03_01[1:0]	0b 11111111

The LED bypass switch gate drivers have variable slew rates, one setting per LED sub-string. The SLEWRATE register controls them, and there are two bits for each LED sub-string.

SLEW_12_10[1:0]: Slew rate setting for LEDs 10-12.

SLEW_09_07[1:0]: Slew rate setting for LEDs 7-9.

SLEW_06_04[1:0]: Slew rate setting for LEDs 4-6.

SLEW_03_01[1:0]: Slew rate setting for LEDs 1-3.

SLEW_xx_xx[1:0]	Set LED bypass switch gate drivers slew rates
00	50μs
01	25μs

10 12µs
11 2µs (default)

Parallel LED String Register – Read/Write

ADDR	REG NAME	D7:D2	D1:D0	DEFAULT
71h	PARLED	RSVD	PARLED[1:0]	0b 00000000

The combinations of LED sub-strings that can be paralleled are as follows:

1. None (each string of bypass switches is independent of the others)
2. One Pair (sub-strings of S1 and S2 are connected in parallel, S3 and S4 are independent)
3. Two Pairs (sub-strings of S1 and S2 are connected in parallel, and S3 and S4 are connected in parallel)
4. All (sub-strings of S1, S2, S3 and S4 are all connected in parallel)

Table 14 PARLED Register Mapping

PARLED [1:0]	LED Strings Parallel Type	Used registers for Phase/Width/Slew Rate/Fault Detection/Default Pulse Width			
		S1: LED1-3	S2: LED4-6	S3: LED7-9	S1: LED10-12
0 (default)	None	LED1-3	LED4-6	LED7-9	LED10-12
1	S1||S2	LED1-3	LED1-3	LED7-9	LED10-12
2	S1||S2, S3||S4	LED1-3	LED1-3	LED7-9	LED7-9
3	S1||S2||S3||S4	LED1-3	LED1-3	LED1-3	LED1-3

Note that the physical parallel connection performed external to the IS32LT3365 must meet the PARLED register setting. The configuration of this register must be updated by the “Update Command”.

S1||S2 means LED1||LED4, LED2||LED5, LED3||LED6

S3||S4 means LED7||LED10, LED8||LED11, LED9||LED12

S1||S2||S3||S4 means LED1||LED4||LED7||LED10, LED2||LED5||LED8||LED11, LED3||LED6||LED9||LED12

As above table, there are 4 possible configurations, where the used PWM phase, width, slew rate, fault detection and default width register bits for each LED and sub-strings are specified.

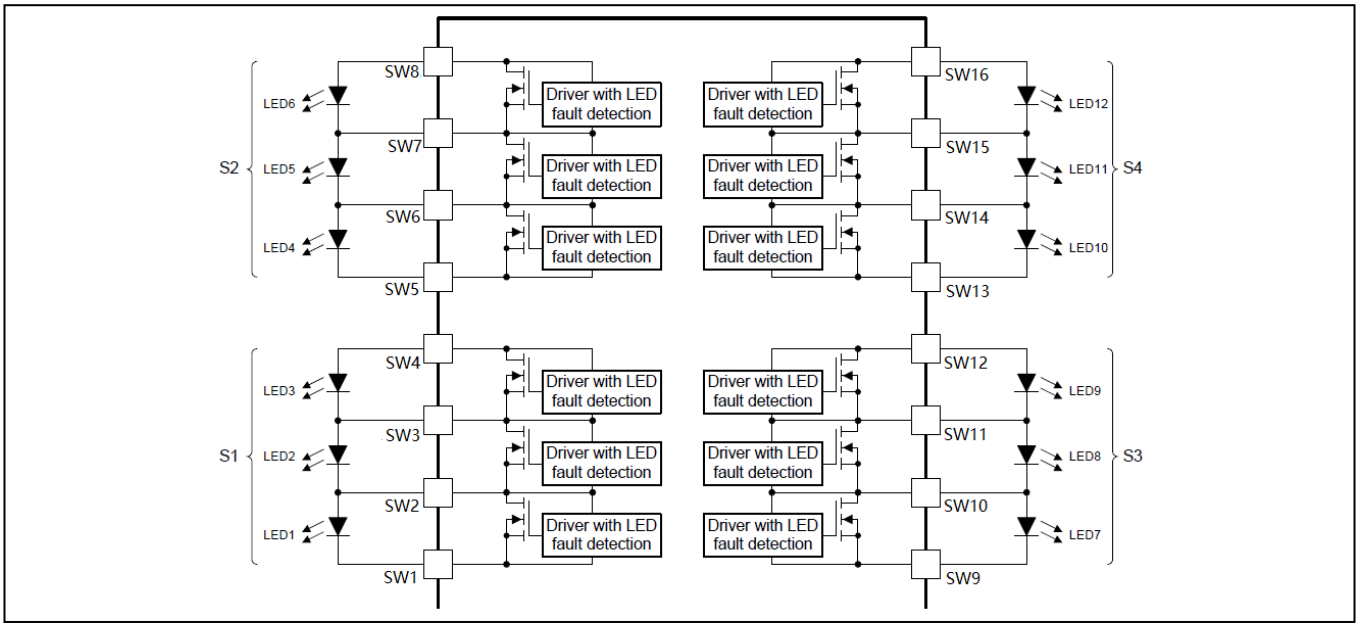


Figure 67 LED Sub-Strings

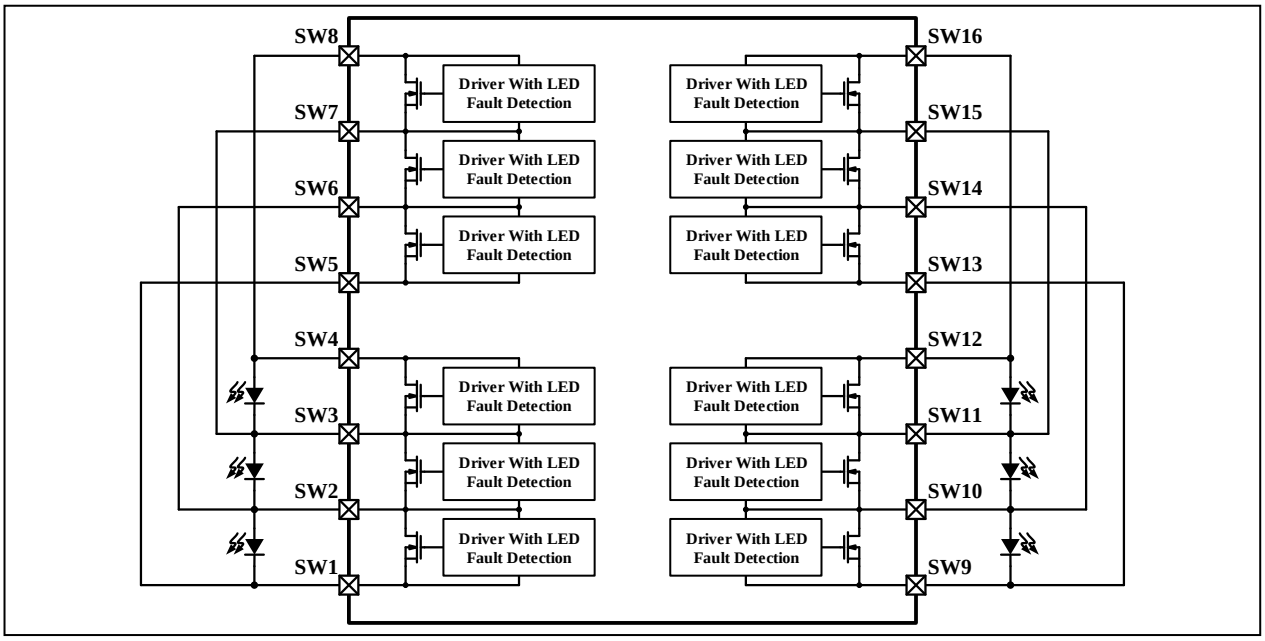


Figure 68 Physical Parallel Connection (S1||S2, S3||S4 as example)

Default Pulse Width Registers (DEFWIDTH) – Read/Write

ADDR	REG NAME	D7:D4	D3:D0	DEFAULT
72h	DEFWIDTH02_01	DEFWIDTH02[3:0]	DEFWIDTH01[3:0]	0b xxxxxxxx
73h	DEFWIDTH04_03	DEFWIDTH04[3:0]	DEFWIDTH03[3:0]	0b xxxxxxxx
74h	DEFWIDTH06_05	DEFWIDTH06[3:0]	DEFWIDTH05[3:0]	0b xxxxxxxx
75h	DEFWIDTH08_07	DEFWIDTH08[3:0]	DEFWIDTH07[3:0]	0b xxxxxxxx
76h	DEFWIDTH10_09	DEFWIDTH10[3:0]	DEFWIDTH09[3:0]	0b xxxxxxxx
77h	DEFWIDTH12_11	DEFWIDTH12[3:0]	DEFWIDTH11[3:0]	0b xxxxxxxx

The Default Pulse Width Registers are used for PWM dimming of each LED when communications watchdog timeout condition occurs (enter fail-safe mode).

DEFWIDTHx[3:0] Default Pulse Width. This 4-bit value determines the pulse width for LEDx when the communications watchdog timer times out (enter fail-safe mode). Note that a value of “0000” means fully OFF, and a value of “1111” means fully ON. In Default Pulse Width operating mode, the values in PHASE registers determine the phase shift, and the pulse widths are provided in the table below. This means in order for the Default Pulse Width mode to operate correctly, both the PHASE and the DEFWIDTH registers must be programmed.

The default value of Default Pulse Width registers depends on the FSMD pin setting. For more details, refer to the “FAIL-SAFE MODE” section.

Table 15 DEFWIDTHx Pulse Width Mapping

DEFWIDTHx[3:0]	LEDx PULSE WIDTH
0	0 (LED fully off)
1	64
2	128
3	192
4	256
5	320
6	384
7	448
8	512
9	576
10	640
11	704
12	768
13	832
14	896
15	1024 (LED fully on)

Note that the DEFWIDTHx pulse width mapping is modified by the PARLED register setting in the watchdog timeout condition.

Example 1:
PARLED[1:0] = 1
PHASE01 and DEFWIDTH01 control LED1 and LED4
PHASE02 and DEFWIDTH02 control LED2 and LED5
PHASE03 and DEFWIDTH03 control LED3 and LED6
PHASE07 and DEFWIDTH07 control LED7
PHASE08 and DEFWIDTH08 control LED8
PHASE09 and DEFWIDTH09 control LED9
PHASE10 and DEFWIDTH10 control LED10
PHASE11 and DEFWIDTH11 control LED11
PHASE12 and DEFWIDTH12 control LED12

Example 2:
PARLED[1:0] = 2
PHASE01 and DEFWIDTH01 control LED1 and LED4
PHASE02 and DEFWIDTH02 control LED2 and LED5
PHASE03 and DEFWIDTH03 control LED3 and LED6
PHASE07 and DEFWIDTH07 control LED7 and LED10
PHASE08 and DEFWIDTH08 control LED8 and LED11
PHASE09 and DEFWIDTH09 control LED9 and LED12

Example 3:
PARLED[1:0] = 3
PHASE01 and DEFWIDTH01 control LED1, LED4, LED7 and LED10
PHASE02 and DEFWIDTH02 control LED2, LED5, LED8 and LED11
PHASE03 and DEFWIDTH03 control LED3, LED6, LED9 and LED12

Enable Output PWM Registers (ENPWM) – Read/Write

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
78h	ENPWML	ENPWM(8:1)								0b 11111111
79h	ENPWMH	RSVD				ENPWM(12:9)				0b 11111111

The Enable Output PWM registers are used to enable the PWM control of each LED. The default state is PWM control.

ENPWM(12:1) Determine whether the device uses the corresponding WIDTH register to control the LED.
0 LED be fully off, un-controlled by WIDTH Register
1 LED dimming controlled by WIDTH Register (default)
If any channel is unused, please set the corresponding bit to “0” to disable it. In parallel switches configuration, if any parallel channel is unused, all corresponding bits must be set to “0”.

Over Temperature Threshold Register – Read/Write

ADDR	REG NAME	D7:D2	D1:D0	DEFAULT
7Ah	TEMP_TH	RSVD	OVER_TEMP_TH[1:0]	0b 00000000

OVER_TEMP_TH[1:0] Junction over temperature alarm threshold setting. When the junction temperature exceeds the threshold, the OVTMPF bit in the FAULT_TYPEL register (94h) is set to “1”, and the FAULTB pin goes low to report the fault condition (if set OVTMPFM bit=1).
00 130℃ (default)
01 140℃
10 150℃
11 160℃

Spread Spectrum Register – Read/Write

ADDR	REG NAME	D7	D6:D2	D1:D0	DEFAULT
7Bh	SSCCFGA	SSCEN	RSVD	SSC[1:0]	0b 00000000

SSCEN Spread spectrum function enable/disable
0 Disable (default)
1 Enable

SSC[1:0] Spread Spectrum Frequency
00 125Hz (default)
01 250Hz
10 500Hz
11 1kHz
When the spread spectrum function is enabled, the PWM frequency must be set to at least two times of the spread spectrum frequency to avoid flickering issue. Therefore, the default value of 125Hz (Typ.) is a good choice for most applications.

Master Slave Setting – Read/Write

ADDR	REG NAME	D7:D2	D1	D0	DEFAULT
7Ch	CLK_MSI	RSVD	INDEPEN	MS_SL	0b 00000010

The Master Slave Setting register is used to set the operating mode in the PWM synchronization operation of multiple IS32LT3365 devices. Please refer to the “PWM Synchronization” section for more details.

This register can only be configured by single device write command frame but not broadcast command frame.

INDEPEN External CLK pin enabled
0 External CLK pin enable as input (Slave) or output (Master) function for PWM synchronization
1 CLK pin high impedance (default, for independence mode to use internal clock)

MS_SL Master/Slave mode select
0 Master mode (default)
1 Slave mode

PWM Period Counter Register (TCNT) – Read Only

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
7Dh	TCNTH	TCNT[9:2]								0b xxxxxxxx
7Eh	TCNTL	RSVD						TCNT[1:0]		0b xxxxxxxx

TCNT[9:0] This is the PWM period count value. The TCNT register automatically counts from 0 to 1023 and wraps back to 0 again. It is provided here with read access for diagnostic purposes.

System Configuration Register – Read/Write

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
80h	SYSCFG	RSVD	I2CEN	ACKEN	PSON	RSVD	SYNCOEN	SYNCPEN	PWR	0b 10000100

I2CEN I^2C Master Enable
0 I^2C function disabled (default)
1 I^2C function enabled

ACKEN Acknowledge Enable
0 No acknowledge is transmitted following successfully received writes (default)
1 Acknowledge (0x7F) is transmitted following successfully received writes

PSON Phase Shift LED ON
0 LED phase shifts apply to LED turn-off times (default)
1 LED phase shifts apply to LED turn-on times
The configuration of this bit must be updated by the “Update Command”

SYNCOEN SYNC Output Enable
0 SYNC output disabled
1 SYNC output enabled (default)
This bit can only be configured by single device write command frame but not broadcast command frame.

SYNCPEN SYNC Pulse Enable
0 If SYNCOEN=0, the SYNC output is driven continuously low (default, no pulses)
1 If SYNCOEN=1, the SYNC output is driven with a 50% duty cycle pulse to synchronize other connected IS32LT3365 devices
This bit can only be configured by single device write command frame but not broadcast command frame.

PWR This bit is reset to 0 upon power-up or EN pin toggling (this bit cannot be written to '0' by MCU). It may be written to a “1” by the MCU. Reading this bit allows the MCU to detect whether there has been a power cycle happened
0 A power cycle has occurred since the last write to a “1”
1 No power cycle has occurred since the last write to a “1”

Communications Watchdog Timer Tap Point Register – Read/Write

ADDR	REG NAME	D7:D3	D2:D0	DEFAULT
81h	CMWTAP	RSVD	CMWTAP[2:0]	0b 00000100

CMWTAP[2:0] This 3-bit value selects the tap point (i.e., bit number, starting from 0) on the 25-bit communications watchdog timer to establish the timeout condition. The system clock frequency is 30.72Mhz (Typ.).

Table16 Communication watchdog overflow time is set as follows

CMWTAP [2:0]	TimeOut
111	2^25 SYSCLK (Typical 1092.3ms)
110	2^24 SYSCLK (Typical 546.1ms)
101	2^23 SYSCLK (Typical 273.1ms)
100 (default)	2^22 SYSCLK (Typical 136.5ms)
011	2^21 SYSCLK (Typical 68.3ms)
010	2^20 SYSCLK (Typical 34.1ms)
001	2^19 SYSCLK (Typical 17.1ms)
000	2^18 SYSCLK (Typical 8.5ms)

If the fail-safe mode is active ($0V<V_{FSMD}<V_{TH3\_FS}$, or R_{FSMD}=10kΩ/27kΩ/51kΩ), the host MCU must send out the first command within 2^22 SYSCLK upon power up. Otherwise, the device will enter fail-safe mode.

PWM Tick Period Register – Read/Write

ADDR	REG NAME	D7:D6	D5:D0	DEFAULT
82h	PWMTICK	PTBASE[1:0]	PTCNT[5:0]	0b 01000000

This register determines the divisor value applied to the SYSCLK clock, which generates the PWM base clock. PWMTICK register comprises of two fields: PTBASE and PTCNT. These two fields program the two divider blocks in series, which generates the PWM base clock.

The recommended PWM frequency is in a range of 300Hz ~ 1kHz and the default PWM frequency (about 468Hz) is good choice for most applications.

PTBASE[1:0] First division on the SYSCLK
00 SYSCLK divide by 1 (DIV1)
01 SYSCLK divide by 64 (DIV1)
10 SYSCLK divide by 128 (DIV1)
11 SYSCLK divide by 256 (DIV1)

PTCNT[5:0] Second division on the SYSCLK
Second division on the SYSCLK value is 1 ~ 64.
Division factor DIV2 = PTCNT[5:0]+1.

Example 1:
Default mode
PWMTICK[7:0] = '01000000'
PTBASE[1:0] = 1 → DIV1 = 64
PTCNT[5:0] = 0 → DIV2 = 1
PWM base clock frequency = SYSCLK ÷ DIV1 ÷ DIV2 = 30.72MHz÷64÷1= 0.48MHz
PWM frequency = PWM base clock frequency÷1024=468.75Hz

Example 2:
PWMTICK[7:0] = '00011101'
PTBASE[1:0] = 0 → DIV1 = 1
PTCNT[5:0] = 29 → DIV2 = 30
PWM base clock frequency = SYSCLK ÷ DIV1 ÷ DIV2 = 30.72MHz÷1÷30 = 1.024MHz
PWM frequency = PWM base clock frequency÷1024=1kHz

LED Open and Short Control Register (LED_OS) – Read/Write

ADDR	REG NAME	D7	D6:D5	D4	D3:D0	DEFAULT
84h	LED01_OS	LED01_OF_EN	LED01_OPEN_TH [1:0]	LED01_SF_EN	LED01_SHORT_TH [3:0]	0b 11110000
85h	LED02_OS	LED02_OF_EN	LED02_OPEN_TH [1:0]	LED02_SF_EN	LED02_SHORT_TH [3:0]	0b 11110000
86h	LED03_OS	LED03_OF_EN	LED03_OPEN_TH [1:0]	LED03_SF_EN	LED03_SHORT_TH [3:0]	0b 11110000
87h	LED04_OS	LED04_OF_EN	LED04_OPEN_TH [1:0]	LED04_SF_EN	LED04_SHORT_TH [3:0]	0b 11110000
88h	LED05_OS	LED05_OF_EN	LED05_OPEN_TH [1:0]	LED05_SF_EN	LED05_SHORT_TH [3:0]	0b 11110000
89h	LED06_OS	LED06_OF_EN	LED06_OPEN_TH [1:0]	LED06_SF_EN	LED06_SHORT_TH [3:0]	0b 11110000
8Ah	LED07_OS	LED07_OF_EN	LED07_OPEN_TH [1:0]	LED07_SF_EN	LED07_SHORT_TH [3:0]	0b 11110000
8Bh	LED08_OS	LED08_OF_EN	LED08_OPEN_TH [1:0]	LED08_SF_EN	LED08_SHORT_TH [3:0]	0b 11110000
8Ch	LED09_OS	LED09_OF_EN	LED09_OPEN_TH [1:0]	LED09_SF_EN	LED09_SHORT_TH [3:0]	0b 11110000
8Dh	LED10_OS	LED10_OF_EN	LED10_OPEN_TH [1:0]	LED10_SF_EN	LED10_SHORT_TH [3:0]	0b 11110000
8Eh	LED11_OS	LED11_OF_EN	LED11_OPEN_TH [1:0]	LED11_SF_EN	LED11_SHORT_TH [3:0]	0b 11110000
8Fh	LED12_OS	LED12_OF_EN	LED12_OPEN_TH [1:0]	LED12_SF_EN	LED12_SHORT_TH [3:0]	0b 11110000

These registers enable the LED open/LED short fault reporting (OPENF bit/SHORTF bit in FAULT_TYPEL register (94h)) and program the threshold voltage of LED open/LED short detection for each switch.

LEDx_OF_EN LEDx open fault reporting enable

0 When LEDx voltage exceeds LEDx_OPEN_TH[1:0], only OPEN_FAULT register (92h/93h) bits set by “1”, OPENF bit in FAULT_TYPEL register (94h) not set by “1”.

1 When LEDx voltage exceeds LEDx_OPEN_TH[1:0], OPEN_FAULT register (92h/93h) bits set by “1” and OPENF bit in FAULT_TYPEL register (94h) also set by “1”, FAULTB pin goes low to report fault condition (if OPENFM bit = “1” in FAULT_MASKL register (96h)).

LEDx_OPEN_TH[1:0] LEDx open fault detection threshold voltage

00 5V

01 10V

10 15V

11 20V (default)

LEDx_SF_EN LEDx short fault reporting enable

0 When LEDx voltage drops below LEDx_SHORT_TH[1:0], only SHORT_FAULT register (90h/91h) bits set by “1”, SHORTF bit in FAULT_TYPEL register (94h) not set by “1”.

1 When LEDx voltage drops below LEDx_SHORT_TH[1:0], SHORT_FAULT register (90h/91h) bits set by “1” and SHORTF bit in FAULT_TYPEL register (94h) also set by “1”, FAULTB pin goes low to report fault condition (if SHORTFM bit = “1” in FAULT_MASKL register (96h)).

LEDx_SHORT_TH[3:0] LEDx short fault detection threshold voltage

0000 1V (default)

0001 2V

0010	3V
0011	4V
0100	5V
0101	6V
0110	7V
0111	8V
1000	9V
1001	10V
1010	11V
1011	12V
1100	13V
1101	14V
1110	15V
1111	16V

LED Short Fault Flag Registers (SHORT_FAULT) – Read/Write

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
90h	SHORT_FAULTL	SHORT_FAULT(8:1)								0b 00000000
91h	SHORT_FAULTH	RSVD				SHORT_FAULT(12:9)				0b 00000000

SHORT_FAULT(12:1) Individual short fault flag of each switch.

0	An LED short fault has not occurred on LEDx
1	An LED short fault has occurred on LEDx

LED Open Fault Report Registers (OPEN_FAULT) – Read/Write

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
92h	OPEN_FAULTL	OPEN_FAULT(8:1)								0b 00000000
93h	OPEN_FAULTH	RSVD				OPEN_FAULT(12:9)				0b 00000000

OPEN_FAULT(12:1) Individual open fault flag of each switch

0	An LED open fault has not occurred on LEDx
1	An LED open fault has occurred on LEDx

Fault Status Flag Registers (FAULT_TYPE) – Read/Write (DUTYF, SHORTF and OPENF bit CANNOT be written)

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
94h	FAULT_TYPEL	I2CF	CRCF	TSDF	CMWF	DUTYF	OVTMPF	SHORTF	OPENF	0b 00000000
95h	FAULT_TYPEH	RSVD						V33OVF	V5OVF	0b 00000000

Fault flags to indicate the various fault types.

I2CF	Mater I^2C communication fault flag
CRCF	CRC checksum fault flag
TSDF	Thermal shutdown fault flag
CMWF	Communication watchdog timeout flag
DUTYF	Loopback verification result fault flag
OVTMPF	Over temperature alarm fault flag
SHORTF	LED short fault flag. If any switch (LED) occurs short fault, this bit will be set to “1”.
OPENF	LED open fault flag. If any switch (LED) occurs open fault, this bit will be set to “1”.
V33OVF	3.3V LDO output overvoltage fault flag
V5OVF	5V LDO output overvoltage fault flag

0	Fault has not occurred (default)
1	Fault has occurred

Note: All 90h~95h fault flag bits are latched. Even though the fault conditions are removed, they cannot automatically reset to “0” but must be cleared by the host MCU writing them back to “0”. If a fault condition still exists, the corresponding FAULT flag is immediately set back to a “1”. To clear OPENF, SHORTF, or DUTYF bit, the corresponding registers of OPEN_FAULT (92h/93h), SHORT_FAULT (90h/91h) or DUTY_FAULT (C3h/C4h) should be cleared.

Hardware Fault Reporting Setting Registers (FAULT_MASK) – Read/Write

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
96h	FAULT_MASKL	I2CFM	CRCFM	TSDFM	CMWFM	DUTYFM	OVTMPFM	SHORTFM	OPENFM	0b 11111111
97h	FAULT_MASKH	RSVD						V33OVFM	V5OVFM	0b 00000011

These register bits determine whether to pull the FAULTB pin to low when corresponding fault condition happens.

I2CFM Mater I²C communication fault reporting mask
CRCFM CRC checksum fault reporting mask
TSDFM Thermal shutdown fault reporting mask
CMWFM Communication watchdog timeout reporting mask
DUTYFM Loopback verification result fault reporting mask
OVTMPFM Over temperature alarm fault reporting mask
SHORTFM LED short fault reporting mask. If any switch (LED) occurs short fault, this bit will be set to “1”.
OPENFM LED open fault reporting mask. If any switch (LED) occurs open fault, this bit will be set to “1”.
V33OVFM 3.3V LDO output overvoltage fault reporting mask
V5OVFM 5V LDO output overvoltage fault reporting mask

0 No action
1 Pull FAULTB pin to low (default)

Note: In order to enable the function of OPENFM or SHORTFM, the LED open or LED short fault detection reporting needs to be enabled first in LED_OS registers (84h~8Fh).

CRC Error Count Register – Read/Write

ADDR	REG NAME	D7:D0	DEFAULT
98h	CERRCNT	CERRCNT[7:0]	0b 00000000

CERRCNT[7:0] CRC error count register

This register value is incremented each time a CRC error is received. This register may be read by the host MCU and then written back to 0 to clear the count. The CERRCNT value saturates at 0xFF; it does not wrap back to 0 when it reaches 0xFF. The CERRCNT register is not automatically cleared when a communications reset is received. It must be cleared manually by writing it back to 0. Note that the CERRCNT register can be written to any 8-bit value. This is intended for diagnostic purposes.

ADC Registers (99h-A6h)

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
99h	ADCCHSEL	RSVD			ADCCH_SEL[4:0]					0b 00000000
9Ah	ADCCFG	RSVD			ADCEN	ADC_CLK [1:0]		ADCSH[1:0]		0b 00000000
9Bh	ADCCTL	ADCCYC_F	ADC_AVG [1:0]		LOOP	SADC	RSVD			0b 00000000
9Dh	ADC_NTCH_L	RSVD						ADC_NTCH[1:0]		0b 00000000
9Eh	ADC_NTCH_H	ADC_NTCH[9:2]								0b 00000000
9Fh	ADC_NTCL_L	RSVD						ADC_NTCL[1:0]		0b 00000000
A0h	ADC_NTCL_H	ADC_NTCL[9:2]								0b 00000000
A1h	ADC_VPTAT_L	RSVD						ADC_VPTAT[1:0]		0b 00000000
A2h	ADC_VPTAT_H	ADC_VPTAT[9:2]								0b 00000000
A3h	ADC_V5_L	RSVD						ADC_V5[1:0]		0b 00000000
A4h	ADC_V5_H	ADC_V5[9:2]								0b 00000000
A5h	ADC_V33_L	RSVD						ADC_V33[1:0]		0b 00000000
A6h	ADC_V33_H	ADC_V33[9:2]								0b 00000000

ADC Channel Selection Registers – Read/Write

ADDR	REG NAME	D7:D5	D4:D0	DEFAULT
99h	ADCCHSEL	RSVD	ADCCH_SEL[4:0]	0b 00000000

ADCCH_SEL[4:0] The ADC has five multiplexed input channels (CH0~CH4), which can be individually selected by the ADCCH_SEL[4:0] bits. Multiple channels can be selected which will be periodically measured in turn. ADC channel selections are shown in the table below.

Table17 ADC Channels Selection

Bit	Channel	Description	Bit=0 (default)	Bit=1
ADCCH_SEL[4]	CH4	Pin V33 voltage sampling	Not Selected	Selected
ADCCH_SEL[3]	CH3	Pin V5 voltage sampling	Not Selected	Selected
ADCCH_SEL[2]	CH2	Chip temperature sensor voltage sampling	Not Selected	Selected
ADCCH_SEL[1]	CH1	Pin NTCL voltage sampling	Not Selected	Selected
ADCCH_SEL[0]	CH0	Pin NTCH voltage sampling	Not Selected	Selected

ADC Configuration Registers – Read/Write

ADDR	REG NAME	D7:D5	D4	D3:D2	D1:D0	DEFAULT
9Ah	ADCCFG	RSVD	ADCEN	ADC_CLK[1:0]	ADCSH[1:0]	0b 00000000

ADCEN ADC enable
0 Disable (default)
1 Enable

ADC_CLK[1:0] ADC frequency setting
00 ADC CLK=SYSCLK/16 (default)
01 ADC CLK=SYSCLK/32

10 ADC CLK=SYSCLK/64
11 ADC CLK=SYSCLK/128

ADCSH[1:0] ADC sampling/hold set
00 ADC always sampling on (default)
01 ADC sample time = 2 ADC CLK
10 ADC sample time = 4 ADC CLK
11 ADC sample time = 8 ADC CLK

ADC control Registers – Read/Write

ADDR	REG NAME	D7	D6:D5	D4	D3	D2:D0	DEFAULT
9Bh	ADCCTL	ADCCYC_F	ADC_AVG[1:0]	LOOP	SADC	RSVD	0b 00000000

ADCCYC_F Effective reading flag
0 ADC sampling in progress, ADC Result Registers(9Dh-A6h) are not valid (default)
1 ADC sampling finished, ADC Result Registers(9Dh-A6h) are valid reading for host MCU

ADC_AVG ADC times average
00 2 times average (default)
01 4 times average
10 8 times average
11 16 times average
For a more stable and precise result, each voltage is always sampled for multiple times to calculate the average value.

LOOP ADC sampling mode
0 ADC single conversion (default)
1 Enable continue ADC conversion
If the LOOP bit is set to “0”, all selected channels will be only measured once. If the LOOP bit is set to “1”, the ADC will repeat the measurement of all selected channels all the time.

SADC Start ADC measurement
0 ADC measurement stops (default)
1 ADC measurement starts

Please set the ADCEN bit first, then set the SADC bit. Otherwise ADC cannot measure voltage.

NTCH Channel ADC Result Registers (ADC_NTCH) – Read Only

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
9Dh	ADC_NTCH_L	RSVD						ADC_NTCH[1:0]		0b 00000000
9Eh	ADC_NTCH_H	ADC_NTCH[9:2]								0b 00000000

ADC_NTCH[9:0] The ADC result of the NTCH pin voltage measurement

This pin can be used for LED binning or temperature monitoring in conjunction with an external NTC resistor. Its voltage measurement can be calculated by:

$$V_{NTCH}(V) = \frac{\sum_{n=0}^{9} D[n] \cdot 2^n}{1024} \times V_{REFADC} \qquad (2)$$

Where, V_{REFADC} is the reference voltage of the ADC, typical 1.8V.

NTCL Channel ADC Result Registers (ADC_NTCL) – Read Only

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
9Fh	ADC_NTCL_L	RSVD						ADC_NTCL[1:0]		0b 00000000
A0h	ADC_NTCL_H	ADC_NTCL[9:2]								0b 00000000

ADC_NTCL[9:0] The ADC result of the NTCL pin voltage measurement

This pin can be used for LED binning or temperature monitoring in conjunction with an external NTC resistor. Its voltage measurement can be calculated by:

$$V_{NTCL}(V) = \frac{\sum_{n=0}^{9} D[n] \cdot 2^n}{1024} \times V_{REFADC} \qquad (3)$$

VPTAT Channel ADC Result Registers (ADC_VPTAT) – Read Only

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
A1h	ADC_VPTAT_L	RSVD						ADC_VPTAT[1:0]		0b 00000000
A2h	ADC_VPTAT_H	ADC_VPTAT[9:2]								0b 00000000

ADC_ VPTAT[9:0] The ADC result of the chip temperature sensor voltage measurement

This result can be used to estimate the device junction temperature by following equation:

$$T_J(°C) = \frac{(\frac{\sum_{n=0}^{9} D[n] \cdot 2^n}{1024} \times V_{REFADC} - 0.608)}{0.0021} + 25 \qquad (4)$$

V5 Channel ADC Result Registers (ADC_V5) – Read Only

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
A3h	ADC_V5_L	RSVD						ADC_V5[1:0]		0b 00000000
A4h	ADC_V5_H	ADC_V5[9:2]								0b 00000000

ADC_ V5[9:0] The ADC result of the V5 pin voltage measurement

This result can be used to calculate the 5V LDO voltage measurement by following equation:

$$V_{V5}(V) = \frac{\sum_{n=0}^{9} D[n] \cdot 2^n}{1024} \times V_{REFADC} \times 3 \qquad (5)$$

V33 Channel ADC Result Registers (ADC_V33) – Read Only

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
A5h	ADC_V33_L	RSVD						ADC_V33[1:0]		0b 00000000
A6h	ADC_V33_H	ADC_V33[9:2]								0b 00000000

ADC_ V33[9:0] The ADC result of the V33 pin voltage measurement

This result can be used to calculate the 3.3V LDO voltage measurement by following equation:

$$V_{V33}(V) = \frac{\sum_{n=0}^{9} D[n] \cdot 2^n}{1024} \times V_{REFADC} \times 2 \qquad (6)$$

I²C Registers (A9h-BFh)

The I²C master controller provides the interface to I²C slave devices. It can be programmed to operate with a built-in command set for external EEPROM access.

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
A9h	I2C_CLOCK	RSVD		I2CCLK[5:0]						0b 00011100
AAh	I2C_REGADDRL	ESADRL[7:0]								0b 00000000
ABh	I2C_REGADDRH	ESADRH[7:0]								0b 00000000
ACh	I2C_CFG	ESADR SEL	I2CCMD[2:0]			DATLEN[3:0]				0b 00000000
ADh	SLAVE_ID	I2CRU N	SLAVEID[6:0]							0b 00000000
AEh	I2C_STATE	EEPRE ADY	I2CBU SY	I2CTXF	I2CAC KF	RSVD				0b 00000000
AFh	I2CBMON	RSVD						SCL	SDA	0b 000000xx
B0h	I2CDAT01	I2CDAT01[7:0]								0b 00000000
B1h	I2CDAT02	I2CDAT02[7:0]								0b 00000000
B2h	I2CDAT03	I2CDAT03[7:0]								0b 00000000
B3h	I2CDAT04	I2CDAT04[7:0]								0b 00000000
B4h	I2CDAT05	I2CDAT05[7:0]								0b 00000000
B5h	I2CDAT06	I2CDAT06[7:0]								0b 00000000
B6h	I2CDAT07	I2CDAT07[7:0]								0b 00000000
B7h	I2CDAT08	I2CDAT08[7:0]								0b 00000000
B8h	I2CDAT09	I2CDAT09[7:0]								0b 00000000
B9h	I2CDAT10	I2CDAT10[7:0]								0b 00000000
BAh	I2CDAT11	I2CDAT11[7:0]								0b 00000000
BBh	I2CDAT12	I2CDAT12[7:0]								0b 00000000
BCh	I2CDAT13	I2CDAT13[7:0]								0b 00000000
BDh	I2CDAT14	I2CDAT14[7:0]								0b 00000000
BEh	I2CDAT15	I2CDAT15[7:0]								0b 00000000
BFh	I2CDAT16	I2CDAT16[7:0]								0b 00000000

I²C Clock Setting Register – Read/Write

ADDR	REG NAME	D7:D6	D5:D0	DEFAULT
A9h	I2C_CLOCK	RSVD	I2CCLK[5:0]	0b 00011100

I2CCLK[5:0] I²C master clock frequency setting

SCL clock frequency = 8MHz/(I2CCLK[5:0]+1)/6. The default SCL clock frequency = 8MHz/(28+1)/6 = 46kHz. The maximum SCL clock must not exceed 400kHz.

EEPROM Start Address Register – Read/Write

ADDR	REG NAME	D7:D0	DEFAULT
AAh	I2C_REGADDRL	ESADRL[7:0]	0b 00000000
ABh	I2C_REGADDRH	ESADRH[7:0]	0b 00000000

ESADRL[7:0] EEPROM Start Address low byte
ESADRH[7:0] EEPROM Start Address high byte (optional for 16-bit register address)

I²C Configuration Register – Read/Write

ADDR	REG NAME	D7	D6:D4	D3:D0	DEFAULT
ACh	I2C_CFG	ESADRSEL	I2CCMD[2:0]	DATLEN[3:0]	0b 00000000

ESADRSEL EEPROM register address length selection
0 8-bit EEPROM register address (default)
1 16-bit EEPROM register address

If ESADRSEL=0, only the lower 8-bit address of I²C command frame is valid.

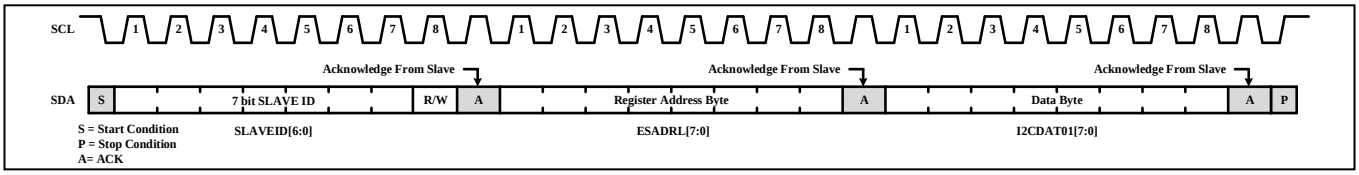


Figure 69 8-bit Address Frame

If ESADRSEL=1, all 16-bit address is valid.

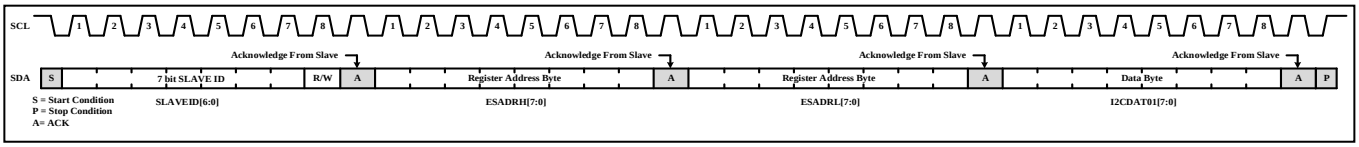


Figure 70 16-bit Address Frame

I2CCMD[2:0] I²C executed frame command mode set

DATLEN[3:0] Define burst access data length (DATLEN+1) bytes

I2C Slave ID Register – Read/Write

ADDR	REG NAME	D7	D6:D0	DEFAULT
ADh	SLAVE_ID	I2CRUN	SLAVEID[6:0]	0b 00000000

I2CRUN Set this bit to "1" starts the I²C command transmission. It is cleared to "0" when the transmission is done.

SLAVEID[6:0] 7-bit slave ID of external EEPROM. This does not contain I²C read/write bit.

I²C Communication Status Register – Read/Write

ADDR	REG NAME	D7	D6	D5	D4	D3:D0	DEFAULT
AEh	I2C_STATE	EEPREADY	I2CBUSY	I2CTXF	I2CACKF	RSVD	0b 00000000

EEPREADY External EEPROM ready flag
With either One Times Polling EEPROM Ack mode or Auto Polling EEPROM Ack mode, if IS32LT3365 does not get the acknowledge signal from EEPROM, this bit will be set to "0". Once the EEPROM returns acknowledgment, this bit will be set to "1".

I2CBUSY I²C bus busy flag
When I²C bus is in transmission, the START signal sets this bit to “1” and the STOP signal clears this bit to “0”.

I2CTXF I²C transmit fault flag
The I²C master monitors the transferred data on the I²C bus. If the data transferred on the bus does not match the data in the data buffer, this bit will set to “1”. No acknowledge from the EEPROM also will set this bit to “1”. This bit is cleared to “0” by either an error-free I²C communication or the host MCU writing it back to “0”.

I2CACKF I²C ACK fault flag
During an I²C data transaction, no acknowledgment on I²C BUS will set this bit to “1”. This bit is cleared to “0” by either an error-free I²C communication or the host MCU writing it back to “0”.

If any bit of I2CTXF and I2CACKF is set to “1”, the I2CF bit in the FAULT_TYPEL register (94h) will be set to “1”, and the FAULTB pin goes low to report fault condition (if I2CFM bit = “1” in the FAULT_MASKL register (96h)). The I2CF bit in the FAULT_TYPEL register (94h) is latched, it cannot automatically reset to “0” but must be cleared by the host MCU writing it back to “0”.

I²C Bus Monitor Register – Read Only

ADDR	REG NAME	D7:D2	D1	D0	DEFAULT
AFh	I2CBMON	RSVD	SCL	SDA	0b 000000xx

This register is used to monitor the SCL and SDA pins’ status, no matter I²C master is enabled or not.

SCL I²C SCL Line Status
0 The I²C SCL signal is low
1 The I²C SCL signal is high

SDA I²C SDA Line Status
0 The I²C SDA signal is low
1 The I²C SDA signal is high

I²C 16 Bytes Data Buffer Registers – Read/Write (B0h-BFh)

ADDR	REG NAME	D7:D0	DEFAULT
B0h	I2CDAT01	I2CDAT01[7:0]	0b 00000000
B1h	I2CDAT02	I2CDAT02[7:0]	0b 00000000
B2h	I2CDAT03	I2CDAT03[7:0]	0b 00000000
B3h	I2CDAT04	I2CDAT04[7:0]	0b 00000000
B4h	I2CDAT05	I2CDAT05[7:0]	0b 00000000
B5h	I2CDAT06	I2CDAT06[7:0]	0b 00000000
B6h	I2CDAT07	I2CDAT07[7:0]	0b 00000000
B7h	I2CDAT08	I2CDAT08[7:0]	0b 00000000
B8h	I2CDAT09	I2CDAT09[7:0]	0b 00000000
B9h	I2CDAT10	I2CDAT10[7:0]	0b 00000000
BAh	I2CDAT11	I2CDAT11[7:0]	0b 00000000
BBh	I2CDAT12	I2CDAT12[7:0]	0b 00000000
BCh	I2CDAT13	I2CDAT13[7:0]	0b 00000000
BDh	I2CDAT14	I2CDAT14[7:0]	0b 00000000
BEh	I2CDAT15	I2CDAT15[7:0]	0b 00000000
BFh	I2CDAT16	I2CDAT16[7:0]	0b 00000000

I2CDATAx[7:0] These registers contains the data to be transmitted when in the Master Transmit state and the data received when in the Master Receive state.

PWM Loopback Function Registers (C0h-C6h)

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
C0h	BSTSTA	RSVD						FAIL	FINISH	0b 00000001
C1h	VFYCTL	VFYCHSEL[3:0]				FBTEN	INTDATA	AUTOLOOP	VFYEN	0b 00000000
C2h	VFYCFG	VFYRDY	TOLERANCE[6:0]							0b 00000010
C3h	DUTY_FAULT_L	DUTY_FAULT(8:1)								0b 00000000
C4h	DUTY_FAULT_H	RSVD				DUTY_FAULT(12:9)				0b 00000000
C5h	PWMDUTYH	PWMDUTY[9:2]								0b 00000000
C6h	PWMDUTYL	RSVD						PWMDUTY[1:0]		0b 00000000

LBIST State Register – Read Only

ADDR	REG NAME	D7:D2	D1	D0	DEFAULT
C0h	BSTSTA	RSVD	FAIL	FINISH	0b 00000001

FINISH LBIST state flag
0 LBIST in progress
1 LBIST finished
The device will perform a Logic Built-in Self-test (LBIST) upon UVLO being released. When it is finished, this flag will be set to “1”.

FAIL LBIST result
0 Pass
1 Failure
This result is only available after LBIST is finished, with the FINISH bit set to “1”. If the LBIST result fails, the device is defective and cannot be used.

Loopback Control Register – Read/Write

ADDR	REG NAME	D7:D4	D3	D2	D1	D0	DEFAULT
C1h	VFYCTL	VFYCHSEL[3:0]	FBTEN	INTDATA	AUTOLOOP	VFYEN	0b 00000000

VFYEN Loopback verification function enable
0 Disabled
1 Enabled

FBTEN Loopback verification function select
0 Self-test
1 Loopback test

INTDATA Data for self-test
0 0x00
1 0xFF

AUTOLOOP Loopback verification mode select
0 Keep verification on selected channel (selected by VFYCHSEL[3:0] register)
1 Autoloop verification all channels in turn

VFYCHSEL[3:0] Loopback verification channel select
The PWM duty cycle loopback verification circuit has twelve multiplexed inputs to monitor the PWM duty cycle of output channels. The twelve input channels (LPBCH1~LPBCH12) are respectively connected to each output stage, as shown in the table below. Only one channel can be verified at a time.

Table 18 Loopback Verification Channels Selection

VFYCHSEL[3:0]	Input Channel Selected	Input Signal
0	LPBCH1	PWM signal from output stage of channel 1
1	LPBCH2	PWM signal from output stage of channel 2
2	LPBCH3	PWM signal from output stage of channel 3
…	…	…
11	LPBCH12	PWM signal from output stage of channel 12
12~15	Invalid	-

Loopback Configuration Register – (D7 - Read only, D0~D6 - Read/Write)

ADDR	REG NAME	D7	D6:D0	DEFAULT
C2h	VFYCFG	VFYRDY	TOLERANCE[6:0]	0b 00000010

VFYRDY Loopback verification state flag
0 Verification in progress
1 Verification finished

TOLERANCE[6:0] Loopback comparison tolerance setting
Preset PWM duty cycle deviation tolerance between the measurement result and the PWM duty cycle setting value in the PWM buffer.

Loopback Fault Flag Registers (DUTY_FAULT) – Read only

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
C3h	DUTY_FAULT_L	DUTY_FAULT(8:1)								0b 00000000
C4h	DUTY_FAULT_H	RSVD				DUTY_FAULT(12:9)				0b 00000000

DUTY_FAULT(12:1) Loopback fault flag for each channel
0 No loopback failure
1 Loopback failure
Any bit in these two registers set to “1”, the DUTYF bit in FAULT_TYPEL register (94h) will be set to “1”, and the FAULTB pin goes low to report fault condition (if DUTYFM bit = “1” in FAULT_MASKL register (96h)).
Note that these bits cannot be cleared to “0” by MCU, but only the loopback verification test can clear them to “0”. When all bits in these two registers are cleared to “0”, the DUTYF bit in the FAULT_TYPEL register (94h) will be automatically clear to “0”.

Loopback PWM Duty Cycle Registers (PWMDUTY) – Read only

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
C5h	PWMDUTYH	PWMDUTY[9:2]								0b 00000000
C6h	PWMDUTYL	RSVD						PWMDUTY[1:0]		0b 00000000

PWMDUTY[9:0] The PWM duty cycle measure result of the selected channel.

IC Identification Register – Read Only

ADDR	REG NAME	D7:D0	DEFAULT
C7h	ICID	ICID[7:0]	0b 10100001

ICID[7:0] Reads to this register address return the value 0xA1. This is intended to be used to identify an IS32LT3365 device. Writing to this register has no effect.

12 INITIALIZATION SETUP

Th below flow-chart outlines the recommended steps to begin communication with the IS32LT3365 device and PWM dimming the LEDs.

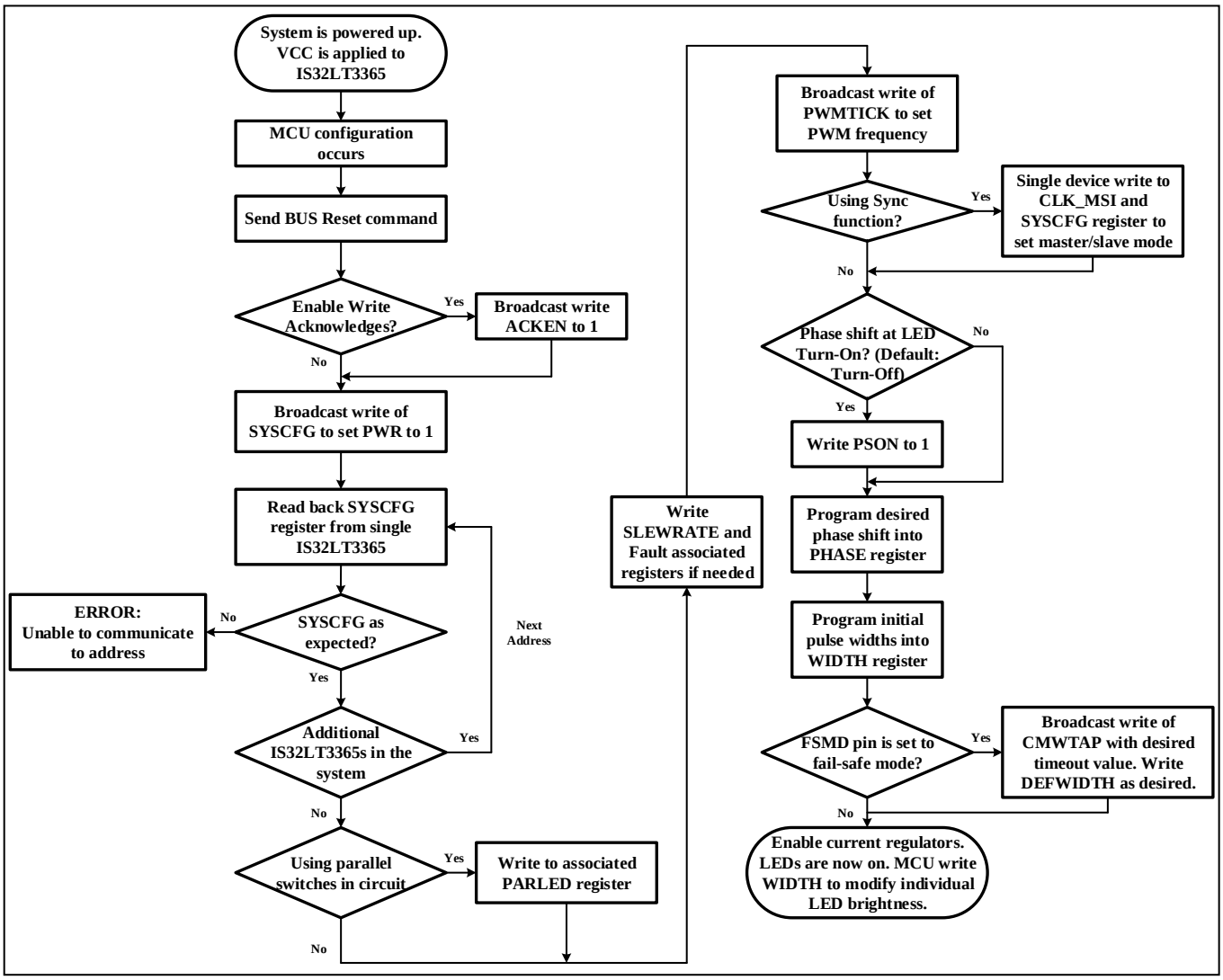


Figure 71 Recommended Initialization Flow-chart

13 THERMAL AND PCB LAYOUT CONSIDERATIONS

The package thermal resistance, θ_{JA}, determines the amount of heat that can pass from the silicon die to the surrounding ambient environment. The θ_{JA} is a measure of the temperature rise created by power dissipation and is usually measured in degrees Celsius per watt (°C/W). The junction temperature, T_J, can be calculated by the rise of the silicon temperature, ΔT, the power dissipation on IS32LT3365, P_{3365}, and the package thermal resistance, θ_{JA}, as in Equation (7):

$$T_J = T_A + \Delta T = T_A + P_{3365} \times \theta_{JA} = T_A + (V_{CC} \times I_{CC} + R_{DSon\_EFF} \times {I_{LED}}^2) \times \theta_{JA} \qquad (7)$$

Where, the I_{LED} is the LED string current. The R_{DSON_EFF} is the effective switch resistance described in the "INTERNAL BYPASS SWITCHES" section.

When operating the chip at high ambient temperatures or when the supply voltage is high, care must be taken to avoid exceeding the package power dissipation limits. The maximum power dissipation at T_A=25˚C can be calculated using the following Equation (8):

$$P_{D(MAX)} = \frac{150°C - 25°C}{\theta_{JA}} \qquad (8)$$

So,

$$P_{D(MAX)} = \frac{150°C - 25°C}{23°C/W} \approx 5.43W$$

for eLQFP-48 package.

Below figure shows the power derating of the IS32LT3365 on a JEDEC board (in accordance with JESD 51-5 and JESD 51-7) standing in still air.

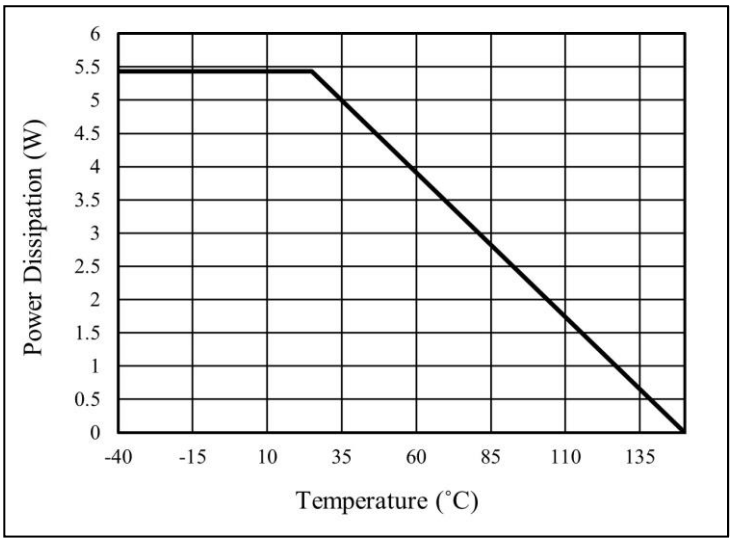


Figure 72 Dissipation Curve

Layout considerations for passive components follow below guidelines:

1. Place the VCC, V5 and V33 decoupling capacitors close to the corresponding pin with a short trace connection.
2. Make the traces between the CPx pins and their associated bypass capacitors short.
3. The R_{FSMD} resistor must be placed as close to the FSMD pin as possible.
4. Add a 10nF ceramic capacitor from the NTCL/NTCH pin to GND to bypass any high frequency noise, especially if the analog voltage level comes from a long copper trace.
5. For the best performance, the IS32LT3365 device shall be located on the LED board where it is as close as possible to the LEDs to which it directly connects. The connection traces between IS32LT3365 SWx pins to the LED strings should be as short as possible to minimize the parasitic inductance and capacitance.
6. The communication pins and CLK/SYNC pins are designed for ease of routing on a single-sided, metal core board. Each pin has a duplicate pin on the opposite side of the device, allowing multiple devices to use a daisy chain configuration.

When designing the Printed Circuit Board (PCB) layout, multiple layers or metal core PCB board type should be

used for better thermal dissipation. That will help to conduct heat from the exposed pad of the IS32LT3365 to the PCB board and additional heatsink. To avoid heat buildup, the IS32LT3365 devices should be placed on the PCB board at some distance from the LEDs. When multiple IS32LT3365 devices are used, they should be spread out on the PCB board at some distance.

Please carefully check the IS32LT3365 case and junction temperature during and after prototyping the solution.

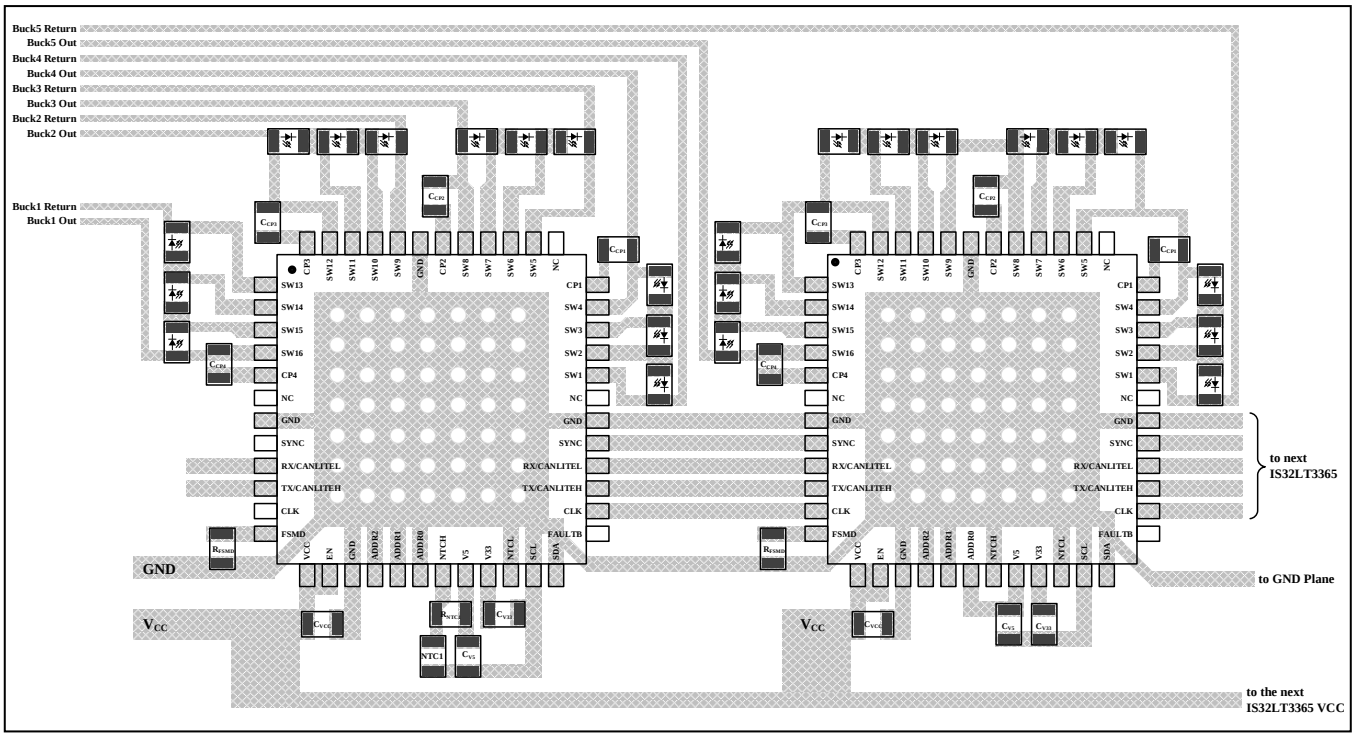


Figure 73 Recommended PCB Layout

14 CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

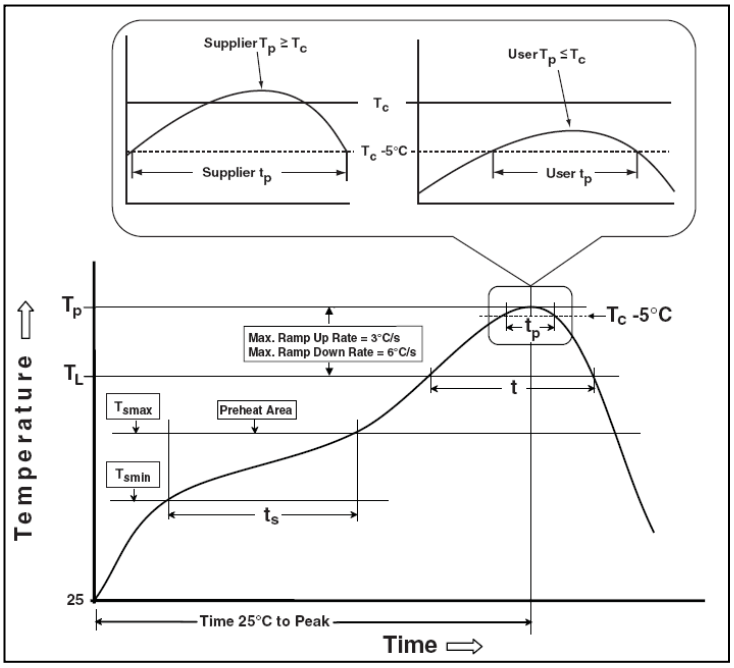
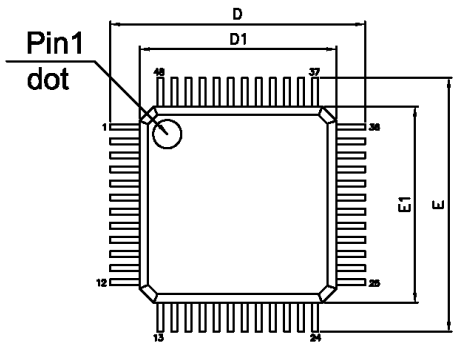


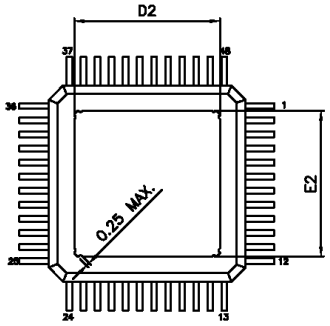
Figure 74 Classification Profile

15 PACKAGE INFORMATION

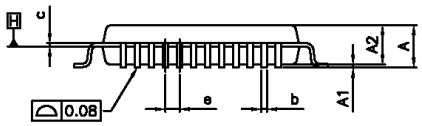
eLQFP-48



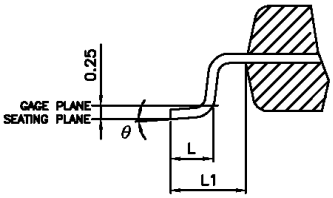
TOP VIEW



BOTTOM VIEW



SIDE VIEW



NOTE:

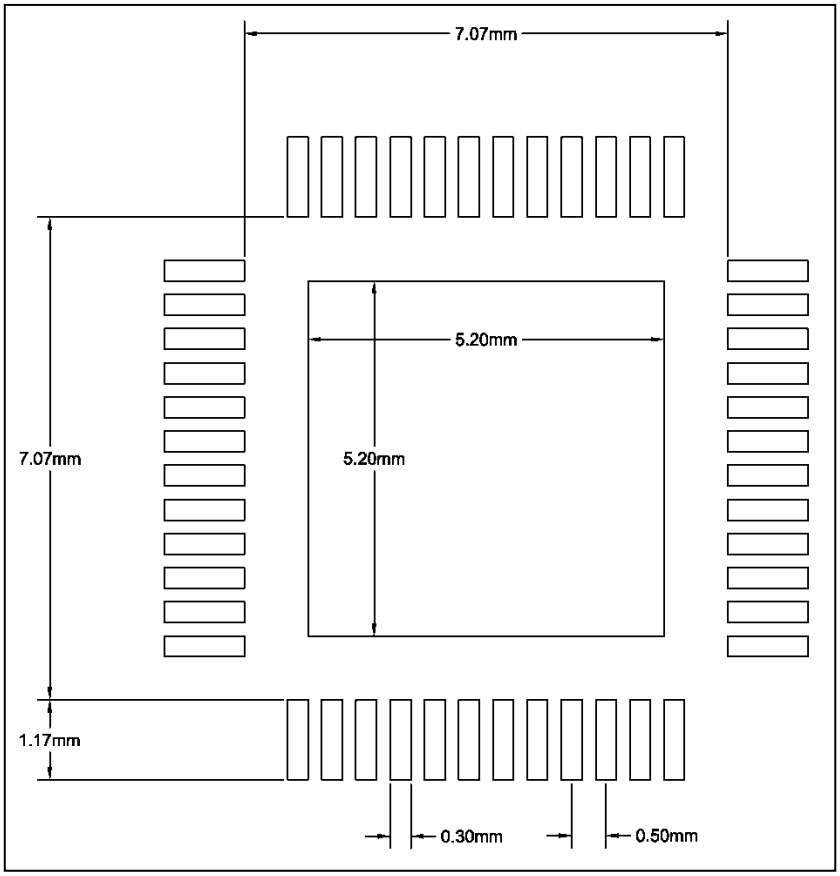
1. CONTROLLING DIMENSION : MM
2. REFERENCE DOCUMENT: JEDEC MO-026D

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
D		9.0BSC	
E		9.0BSC	
E1		7.0BSC	
D1		7.0BSC	
D2	2.00	—	—
E2	2.00	—	—
L1		1.0REF	
L	0.45	0.60	0.75
c	0.09	—	0.20
e		0.50BSC	
b	0.17	0.22	0.27
θ	0°	3.5°	7°

233-570-310 Rev. A

16 RECOMMENDED LAND PATTERN

eLQFP-48



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. user's board manufacturing specs), user must determine suitability for use.

17 REVISION HISTORY

Revision	Detail Information	Date
0B	Update pin out definition and functions.	2023.11.27
0C	Update EC and application description.	2023.12.04
0D	Update EC and application description.	2024.03.15
0E	Update EC.	2024.04.12
0F	Update pinout and EC.	2024.05.30
0G	Update EC and others.	2024.07.04
0H	Format updated.	2024.08.28
0I	Add table of contents and copper wire part number.	2024.11.01
A	Update to final version	2024.12.31