IS32LT3365A HIGH-BRIGHTNESS LED DIMMER FOR AUTOMOTIVE LED ARRAY SYSTEM EVALUATION BOARD GUIDE

GENERAL DESCRIPTION

The IS32LT3365A device is a compact, highly integrated solution with shunt dimming for large arrays of high-brightness LEDs in applications such as automotive matrix headlight system.

The IS32LT3365A device includes four groups of three switches in a series array for bypassing individual LED(s) in the string. These four groups can either independently manage four LED strings or be connected in series to manage one LED string, as well as paralleling up to four switches to bypass high current LEDs. Four on-board charge pump rails that can float up to 62V above GND provide the LED bypass switch gate drive. The low on-resistance (RDS(ON)) of the bypass switch minimizes conduction loss and power dissipation.

The pulse width and phase shift of PWM control are programmable for each individual LED in the string. The PWM frequency is adjustable via an internal register, and multiple devices can be synchronized to the same frequency and phase. The programmable slew rate of switch transitions and spread spectrum in PWM dimming operation can optimize the EMI performance.

UART communication interface compatible with CAN PHY (IS32LT3365A) are used for control and management by a host MCU.

For additional system reliability, the IS32LT3365A device features LED open/short and single LED short detection, over temperature protection, as well as fault reporting via an open drain dedicated reporting pin (FAULTB) and the communication interface.

The eLQFP-48 package features a feed-through topology to enable easy routing of signals on single-layer aluminum LED load boards.

QUICK START

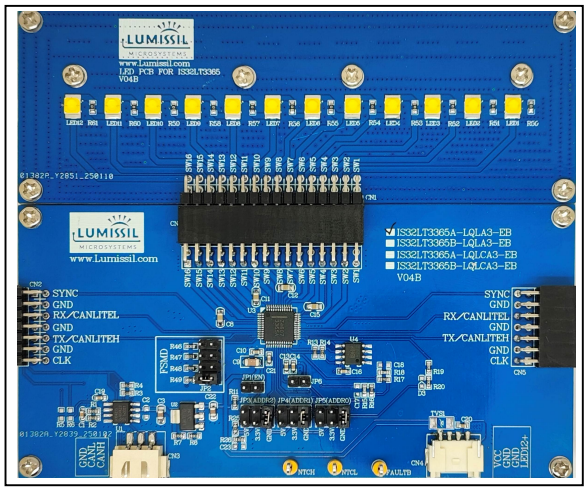

Figure 1 IS32LT3365A Evaluation Board Photo

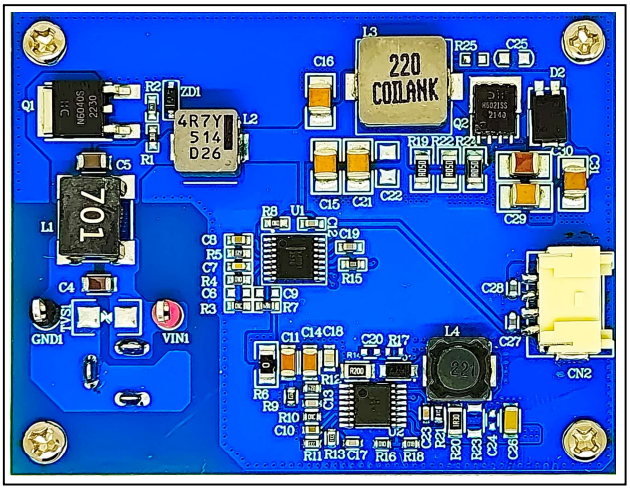

Figure 2 Power Board for IS32LT3365A

FEATURES

- Wide input voltage supply from 4.5V to 55V
- Functional Safety-Capable
  - Developed according to ISO26262 with process complying to ASIL-B
- UART interface
  - UART interface compatible with CAN physical layer, 100kbps~1Mbps baud rate
  - CRC to ensure robustness of communication
  - Support up to maximum 27 addressable devices
  - Watchdog timer to support fail-safe mode
- Embedded 12 LED bypass switches
  - Four groups of three series bypass switches
  - Maximum 20V across voltage on each switch
  - Maximum 55V from each switch to GND
  - Each switch up to 1.5A current capability
- Individual PWM dimming for each switch
  - 10-bit PWM duty cycle setting
  - Individual phase shift setting
  - Spread spectrum to optimize EMI
  - Programmable slew rate control
  - Programmable PWM frequency up to 30kHz
  - Device-to-device synchronization
- I²C master reading/writing EEPROM data for LED binning and calibration
- 10-bit ADC with two external MUXed inputs to support temperature monitor or LED binning
- Fault protection with flag and reporting
  - Programmable fail-safe modes
  - LED string open/short detection
  - Single LED short detection
  - I²C communication error
  - Internal LDO overvoltage

- CRC error
- Programmable thermal alarm
- Thermal shutdown
- Dedicated fault reporting pin

- Operating junction temperature range (-40°C ~ +150°C)
- AEC-Q100 Qualified with Temperature Grade 1: -40°C to 125°C (IS32LT3365A-LQLA3-TR)
- AEC-Q100 qualification in process with Temperature Grade 1: -40°C to 125°C (IS32LT3365A-LQLCA3-TR)
- RoHS & Halogen-Free Compliance
- TSCA Compliance
- Thermally enhanced eLQFP-48 with exposed pad package

RECOMMENDED EQUIPMENT

- 12V, 2A DC power supply

ABSOLUTE MAXIMUM RATINGS

- ≤ 40V power supply

ORDERING INFORMATION

Part No.	Temperature Range	Package
IS32LT3365A-LQLA3-EB	-40°C ~ +125°C (Automotive)	eLQFP-48, Lead-free
IS32LT3365A-LQLCA3-EB	-40°C ~ +125°C (Automotive)	eLQFP-48, Lead-free

Table 1 Ordering Information

For pricing, delivery, and ordering information, please contact Lumissil's analog marketing team at analog@Lumissil.com or (408) 969-6600.

PROCEDURE

The IS32LT3365A evaluation board is fully assembled and tested. Follow the steps listed below to verify board operation.

Caution: Do not turn on the power supply until all connections are completed.

Hardware Setup

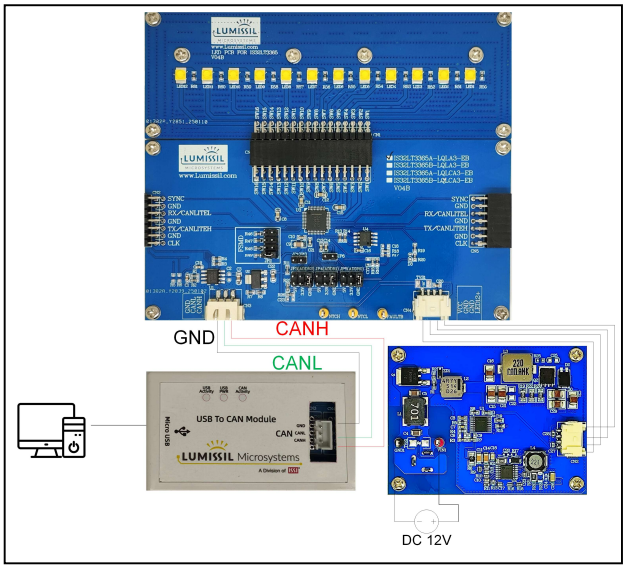

Figure 3 Hardware Connection

1. Connect a 12V power supply to VIN1 and GND1 or connect 12V adapter to CN1 connector.
2. Connect the CN2 to CN4.
3. Connect the USB TO CAN Module to PC through the USB cable.
4. Connect the USB TO CAN Module to the CN3 connector through the XH2.54mm 3P wire.
5. Open JP1 to enable device IS32LT3365A.
6. Open JP6. Note that if a 5V host MCU is used for IS32LT3365A control, you should short JP6.
7. Fail-safe mode Setting
   Fail-safe mode can be set by JP2 (See Table 2 jumper settings).

Resistor	Jumper Setting	Watchdog Timer	LED State
R49(10kΩ)	Closed	Invalid	-
R48(51kΩ)	Closed	Active	All LED Completely Off
R47(27kΩ)	Closed	Active	All LED on with 50% PWM duty cycle
R46(10kΩ)	Closed	Active	All LED on with fully brightness

Table 2 Fail-safe Mode Setting

8. Device address Setting
   Device ID can be set by JP3(ADDR2), JP4(ADDR1) and JP5(ADDR0) using Table 3 jumper settings.

ADDR2 voltage	ADDR1 voltage	ADDR0 voltage	Device ID Byte (HEX)
0	0	0	20
0	0	3.3V	61
0	0	5V	E2
0	3.3V	0	A3
0	3.3V	3.3V	64
0	3.3V	5V	25
0	5V	0	A6
0	5V	3.3V	E7
0	5V	5V	A8
3.3V	0	0	E9
3.3V	0	3.3V	6A
3.3V	0	5V	2B
3.3V	3.3V	0	EC
3.3V	3.3V	3.3V	AD
3.3V	3.3V	5V	2E
3.3V	5V	0	6F
3.3V	5V	3.3V	F0
3.3V	5V	5V	B1
5V	0	0	32
5V	0	3.3	73
5V	0	5V	B4
5V	3.3V	0	F5
5V	3.3V	3.3V	76
5V	3.3V	5V	37
5V	5V	0	78
5V	5V	3.3V	39
5V	5V	5V	BA

Table 3 Device ID Setting

9. Fault Reporting

   The fault protections include LED string open/short, single LED short, fail-safe mode, thermal alarm, thermal shutdown, CRC error, LDO overvoltage, I^2C communication failure, Loopback verification failure, and so on. The FAULTB pin will go low when the device detects a fault condition. When FAULTB pin goes low, LED D3 will light up. Once the fault condition is removed and the corresponding fault bit is cleared, the FAULTB pin goes back to high impedance, and LED D3 will turn off.

   Note: R19, R20 and D3 are not necessary for actual application.

10. Turn on the power supply and open the IS32LT3365 GUI on PC to control LED strings.

INSTRUCTIONS FOR IS32LT3365 GUI

1. INTRODUCTION

This chapter introduces how to use IS32LT3365 GUI tool to demonstrate/control IS32LT3365A evaluation boards.

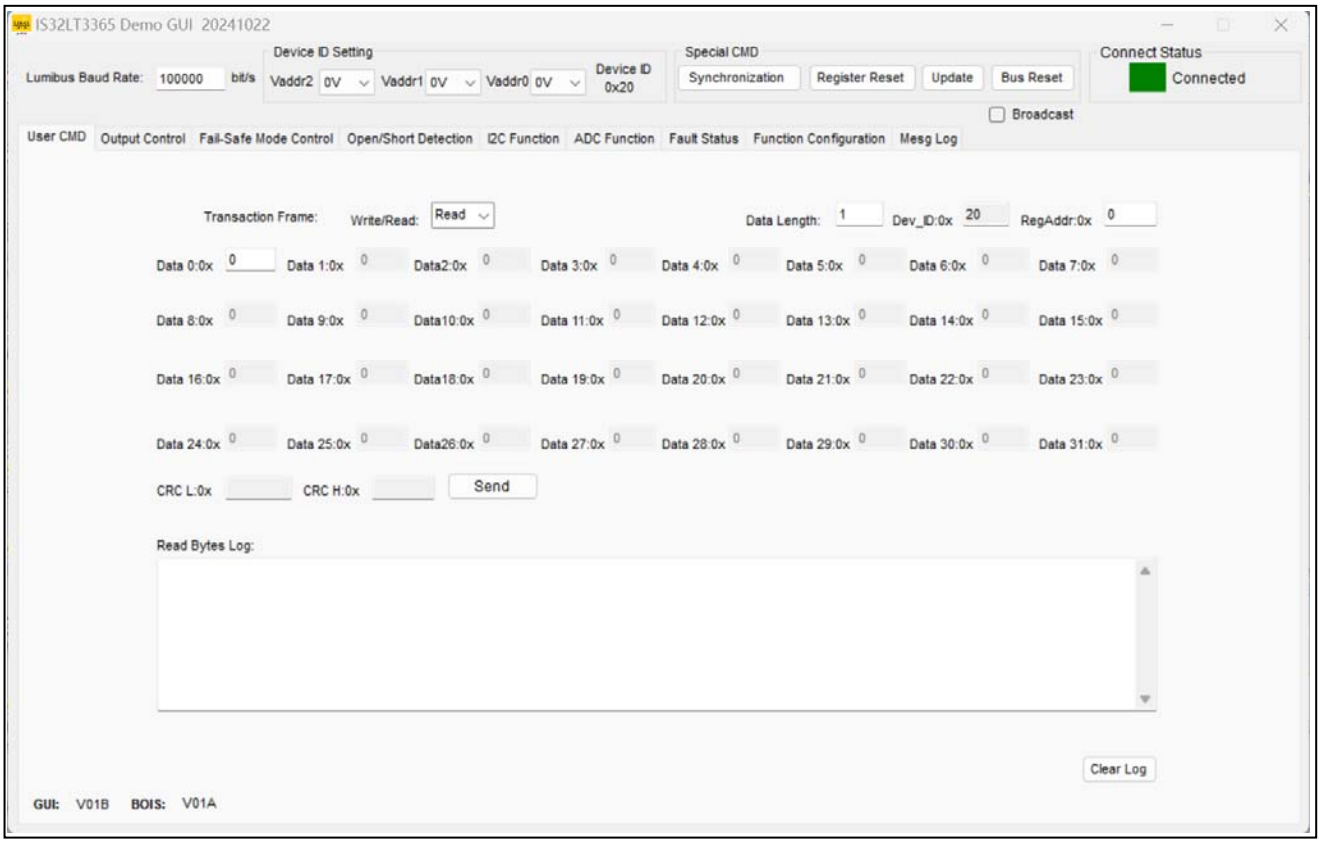

Figure 4 User Command Page

2. CONNECTION

USB to CAN Module supports micro-USB port, a micro-USB line can connect the Module to a computer for power supply and GUI support.

USB to CAN Module and IS32LT3365A evaluation board are connected via CAN bus.

The power supply for the power board is 12V.

Figure 5 Micro-USB

Step 1: Connect evaluation board to the USB to CAN Module via CAN bus (CANH, CANL, GND).

Step 2: Connect input voltage connector to 12V.

Step 3: Connect the USB to CAN Module to the computer. At this time, the demo board LED starts to run mode.

Step 4: Open the GUI tool. The GUI tool will change the connection status from red to green. At this time, on the

evaluation board, all LEDs will be turned off.

Red: Evaluation board has no connection to the computer (refer to Figure 6).

Green: Evaluation board is already connected to the computer (refer to Figure 6).

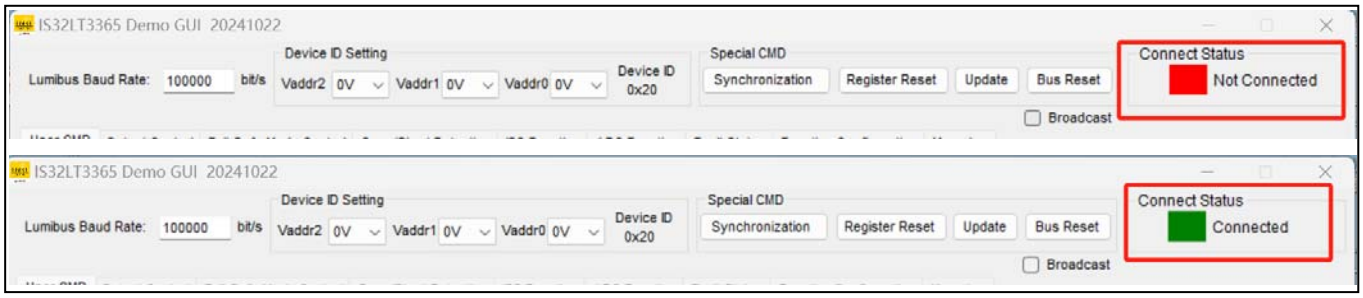

Figure 6 GUI Tool Setting

3. GUI INTERFACE INTRODUCTION

3.1 Baud Rate Frequency Setting

Set Baud rate to 100000bps for IS32LT3365A (Refer to Figure 7, can support Baud rate range: 100kbps~1Mbps).

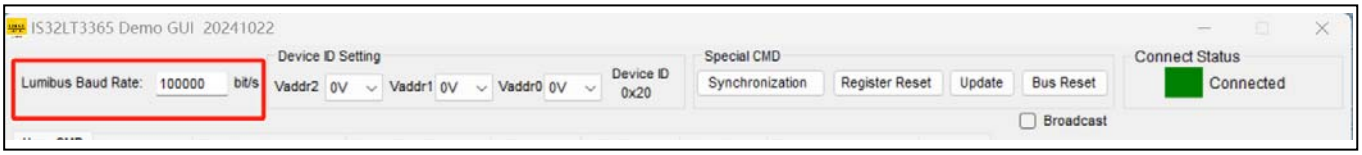

Figure 7 Baud Rate Frequency Setting

3.2 Device ID Setting

Set the corresponding Vaddr2/Vaddr1/Vaddr0 according to the evaluation board setting (Refer to Figure 8, default setting Vaddr2=Vaddr1=Vaddr0=0V).

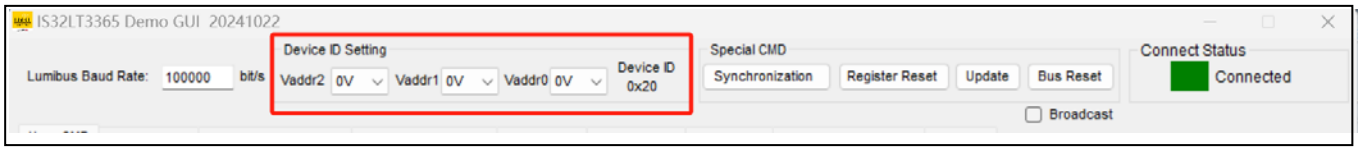

Figure 8 Device ID setting

3.3 Special Command (Refer to Figure 9)

Synchronization: Reset the TCNT counter to 0. Issued by broadcast to realize PWM software synchronization.

Register Reset: Resets all registers to default value, excluding the PWR bit in register 80h.

Update: Update the PWM WIDTH and PHASE register data into output stages at the next PWM boundary after this command is issued. Update the configuration of the PSON bit in 80h. Update the configuration of PARLED register in 71h. Quit from fail-safe mode to normal mode.

Bus Reset: Upon system power up, the host MCU must initialize the BUS by sending a BUS Reset Command before communication.

Broadcast: Broadcast to all IS32LT3365A devices. Broadcast only applies to writing commands.

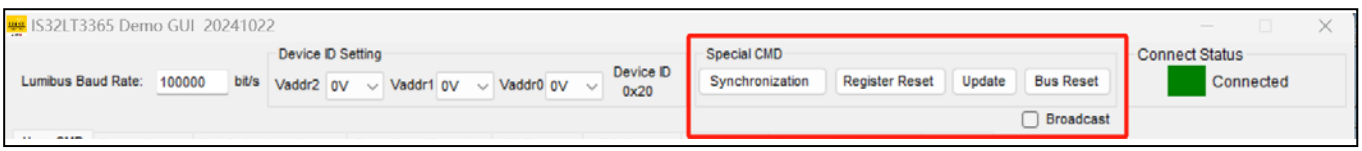

Figure 9 Special Command

3.4 User Command Page

This page provides direct read and write operations of registers (refer to Figure 10).

3.4.1 Write or Read Select

3.4.2 Device Address: Control by Device Setting

3.4.3 Write or Read Data Length (1~16 or 32)

3.4.4 Write or Read Start Register Address

3.4.5 Write Data0~Datan (Prohibit Use During Read Operation)

3.4.6 CRC Data

3.4.7 Click the “Send” button to Send command

3.4.8 Record the data when using Read mode

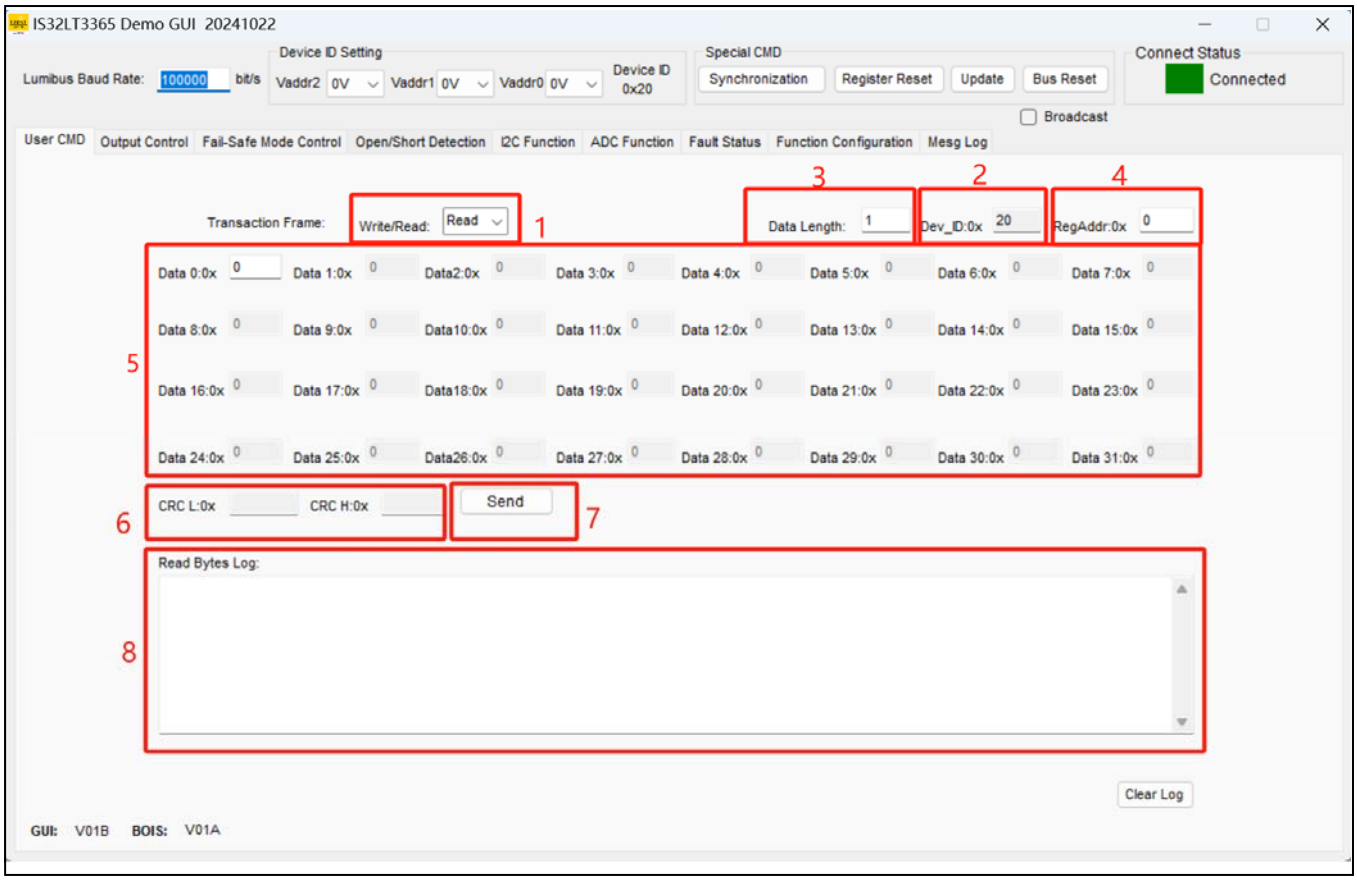

Figure 10 User Command Page

3.5 Output Control Page (Refer to Figure 11)

3.5.1 Group Select (Group1:00h~1Fh, Group2:20h~3Fh, Group3:40h~6Fh)

The PHASE and WIDTH register addresses are from 0x00 to 0x6F. There are 10-bit registers to control the phase shift and pulse width of the LEDs with respect to the PWM counter (TCNT). These registers are the PHASE and WIDTH registers, respectively. These registers may be written or read using three register map groups. These three map groups all communicate with a common set of registers internally. The data written into any map group will be synchronized into the other two map groups.

3.5.2 Slew rate control (70h)

The LED bypass switch gate drivers have variable slew rates, one setting per LED sub-string.

They are controlled via the SLEWRATE register, with a default value of 2us per channel.

SLEW_12_10: Slew rate setting for LEDs 10~12.

SLEW_09_07: Slew rate setting for LEDs 7~9.

SLEW_06_04: Slew rate setting for LEDs 4~6.

SLEW_03_01: Slew rate setting for LEDs 1~3.

3.5.3 PWM Frequency Setting (82h)

The recommended PWM frequency is in a range of 300Hz ~ 1kHz and the default PWM frequency (about 468Hz) is a good choice for most applications.

3.5.4 Channel Enable (78h~79h)

If any channel is unused, please set the corresponding bit to “0” to disable it. In a parallel switches configuration, if any parallel channel is unused, all corresponding bits must be set to “0”.

3.5.5 WIDTH Control

The IS32LT3365A device offers 10-bit phase shiftable PWM dimming for each LED. The pulse width can be programmable for each individual LED in the string. For example, 1023=LED fully on (100% PWM duty cycle), 512=50% PWM duty cycle, 0=LED off.

3.5.6 PHASE Shift Control

The phase shift of PWM control is programmable for each individual LED in the string. The phase shift is applied to LED turn off times. The figure below shows examples of PWM width and phase shift implementation PSON=0, using values of PHASEx = 0 and 360 with WIDTHx = 600. In both cases, the WIDTHx value determines the LED on time (the switch off time).

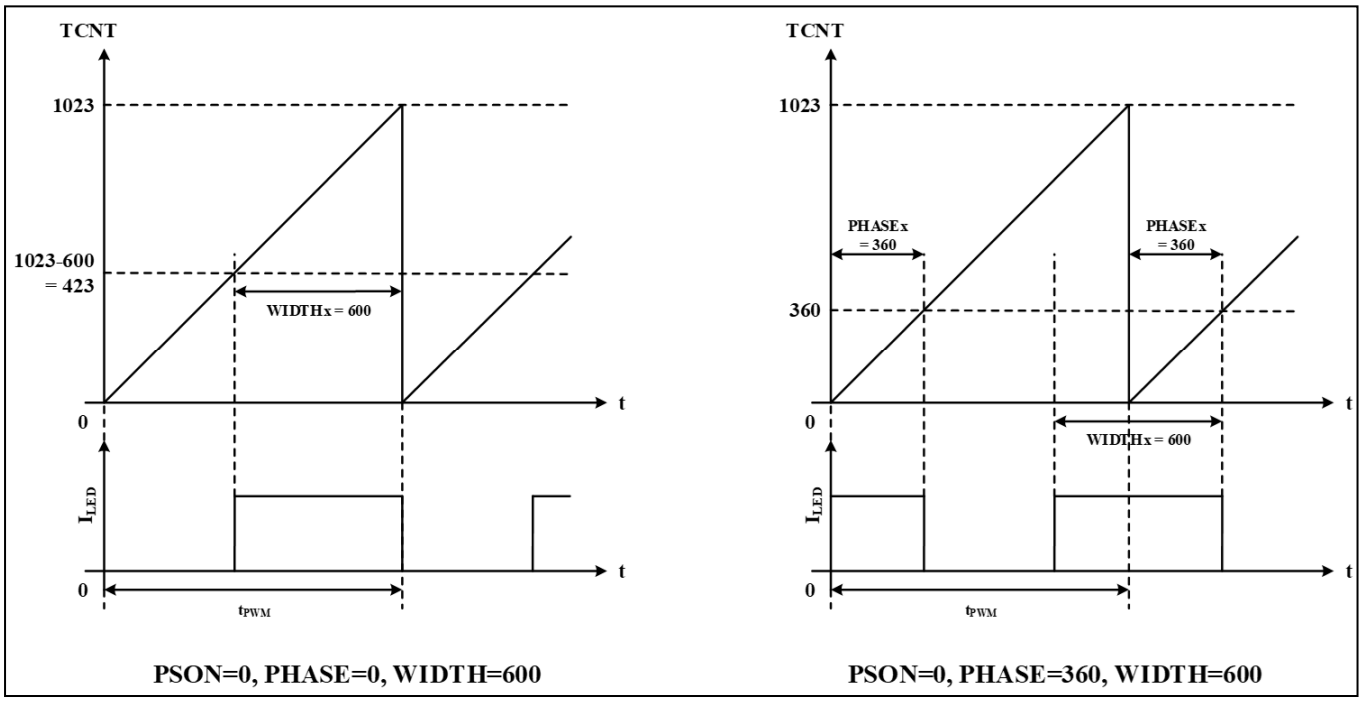

Figure 11 PWM Width and Phase Shift implementation as PSON=0

3.5.7 Quick operation

“Enable All Width”: if it is enabled, slide the slider on the right to set all channel’s WIDTH value.

“Auto Send Update CMD”: if enabled, and then click the “Write” button, it will send an update command automatically after the send write command, otherwise, you should send an update command every time after sending the write command.

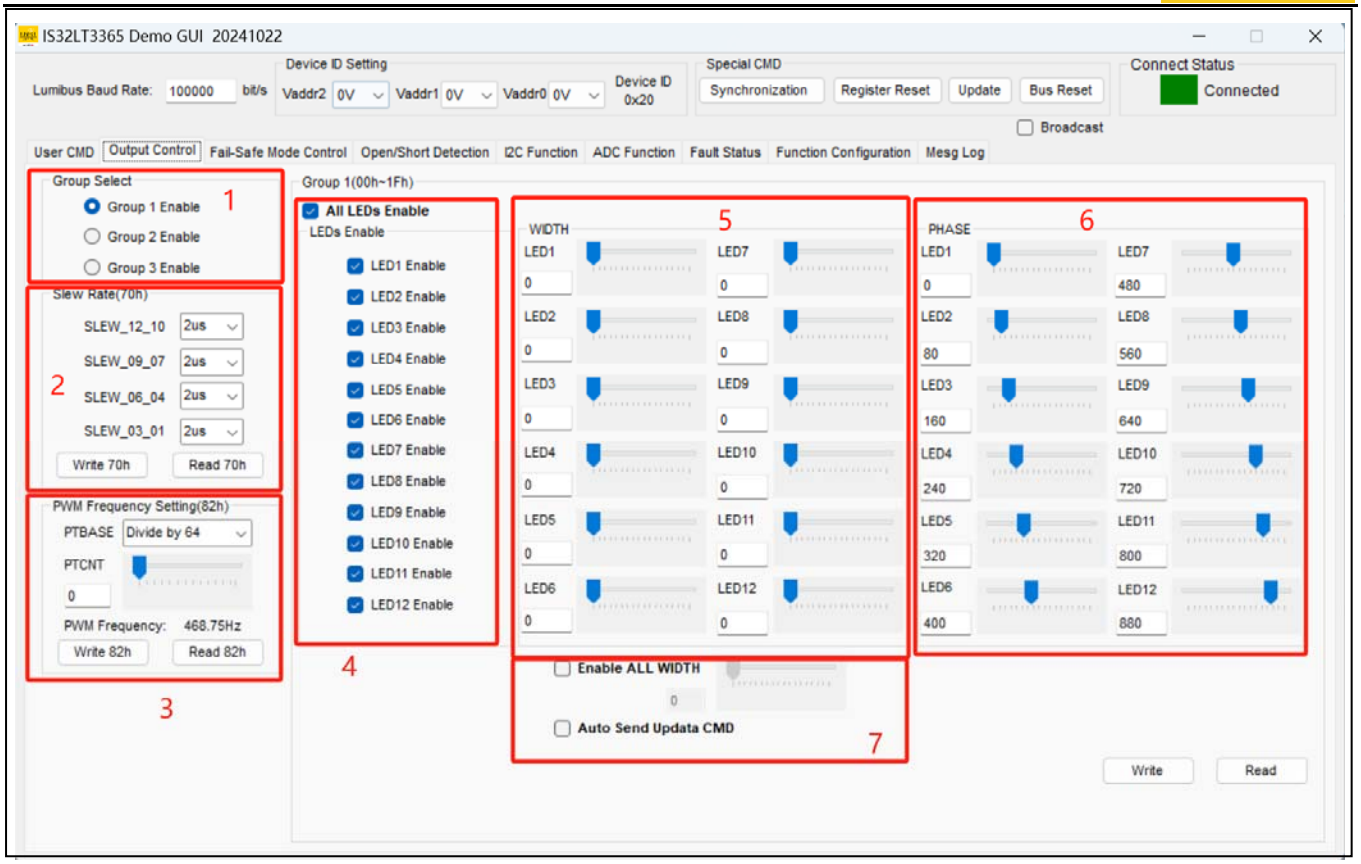

Figure 12 Output Control Page

3.6 Fail-Safe Mode Page (Refer to Figure 13)

This state allows the user to preset the outputs' state if the communication is broken. The device integrates a communication watchdog timer that operates based on the system clock pulse. The tap point, programmed via the CMWTAP register (81h), defines the timing of the communication watchdog timer (25-bit counter). By default, the tap point is set to bit 22, which means the device requires 2^22 system clock cycles for the communication watchdog timer to time out. If the communication watchdog times out (no error-free communication is successfully received for the programmed number of system clock cycles), the device will enter fail-safe mode.

When 0V<VFSMD<VTH3_FS, or RFSMD=10kΩ/27kΩ/51kΩ, the internal communication watchdog is active, and the fail-safe mode is enabled. If the watchdog times out, the device will enter fail-safe mode, and the outputs will be determined by the DEFAULT PULSE WIDTH registers (72h~77h).

To switch from the fail-safe mode to normal mode, the host MCU must send an Update Command (special command) first and then write the CMWF bit in FAULT_TYPEL register (94h) to "0". The watchdog timer will be reset, and the FAULTB pin will return to a high impedance.

Note that the device must be re-initialized after quitting from the fail-safe mode to normal mode. Below table is the default value of 72h~77h when FSMD pin in different settings.

FSMD pin	Watchdog Timer	Default Value of DEFAULT PULSE WIDTH Registers (72h~77h)
$0V<V_{FSMD}<V_{TH1\_FS}$ or $R_{FSMD}=10k\Omega$	Active	0xFF
$V_{TH1\_FS}<V_{FSMD}<V_{TH2\_FS}$ or $R_{FSMD}=27k\Omega$		0x88
$V_{TH2\_FS}<V_{FSMD}<V_{TH3\_FS}$ or $R_{FSMD}=51k\Omega$		0x00
$V_{TH3\_FS}<V_{FSMD}<5.5V$ or connect FSMD to V5 via a 10kΩ resistor	Invalid	0x00

Table 4 Fail-safe mode Setting

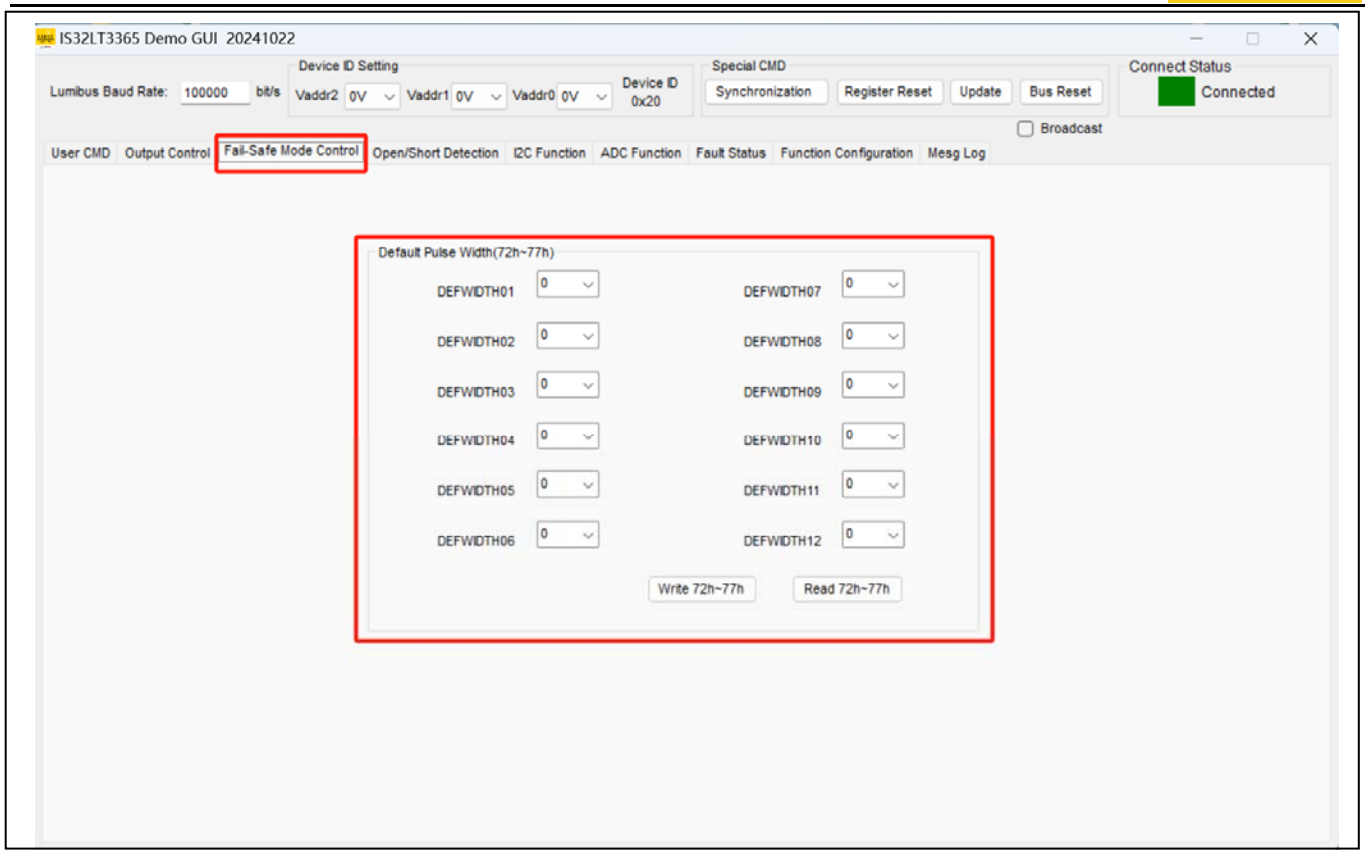

Figure 13 Fail-Safe Mode Control Page

3.7 Open/Short Detection Page (Refer to Figure 14)

3.7.1 LED Open/Short Detect enable and detect threshold Setting (84h~8Fh)

a) “LEDx_OF_EN”: LEDx Open Fault Detect Enable.

b) “LEDx_SF_EN”: LEDx Short Fault Detect Enable.

c) LED Open Detect threshold can be set to 5V/10V/15V/20V, default is 20V.

d) LED Short Detect threshold can be set to 1V~16V, default is 1V.

e) The LED open fault is detected by an internal comparator monitoring the drain to source voltage (VDS) of the internal NMOS switch. In the event of an LED open failure, the drain to source voltage exceeds the detection threshold voltage, causing the corresponding NMOS switch to be turned on momentarily and sets the corresponding fault flag bit to “1”.

f) The LED short fault is detected by another internal comparator monitoring the drain to source voltage of the internal NMOS switch. In the event of LED shorted failure, if the drain to source voltage drops below the detection threshold voltage, by the end of the LED ON phase, the detection circuit sets the corresponding fault flag bit to “1”

3.7.2 LED Open/Short Fault flag (90h~93h)

When there is an LED open or short fault event happened at any channel, the corresponding fault bit will be set to “1”. Note that all these fault flag bits are latched. Even though the fault conditions are removed, they cannot automatically reset to “0” but must be cleared by the host MCU, writing them back to “0”.

3.7.3 Fault Status Flag (94h)

a) “LED Short”: If any switch (LED) occurs short fault, this bit will be set to “1”.

b) “LED Open”: If any switch (LED) occurs open fault, this bit will be set to “1”.

c) To clear these two bits, you should clear 90h~93h first.

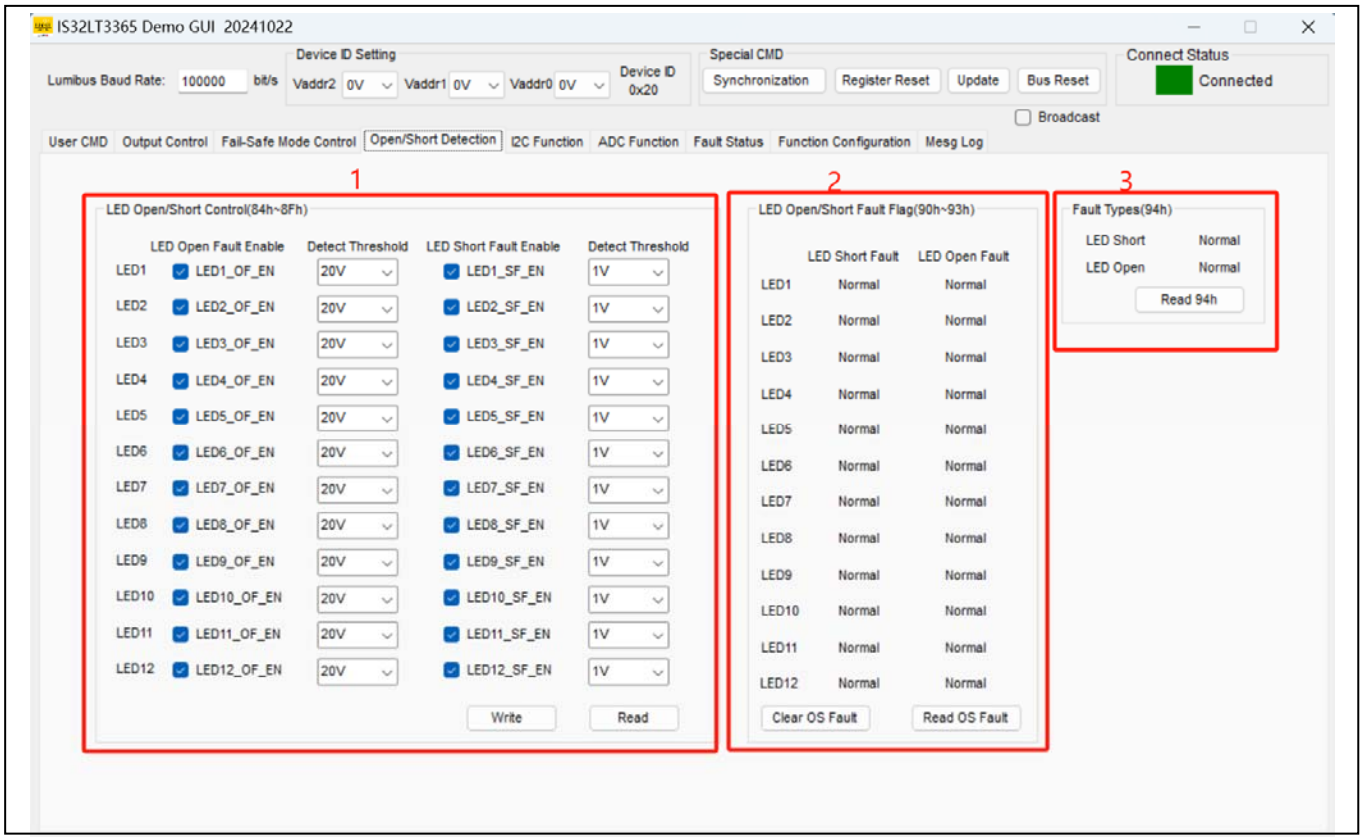

Figure 14 Open/Short Detection Page

3.8 I²C Function Page (Refer to Figure 15)

3.8.1 I²C Setting

a) I²C enable: Enable I²C master.

b) I2CCLK: Set I²C master clock frequency, default is 46kHz.

c) EEPROM Start Addr: EEPROM Start Address

d) I2C Config: I²C Configuration including I²C command and data length setting.

e) I2C Slave ID: 7-bit slave ID of external EEPROM. This does not contain I²C read/write bit.

f) I2C Communication Status: Flag bit used to indicate fault happened, see detail in datasheet.

g) I2C BUS Monitor: used to monitor the SCL and SDA pins' status.

3.8.2 I2C Data (B0h~BFh)

These registers contain the data to be transmitted when in the Master Transmit state and the data received when in the Master Receive state.

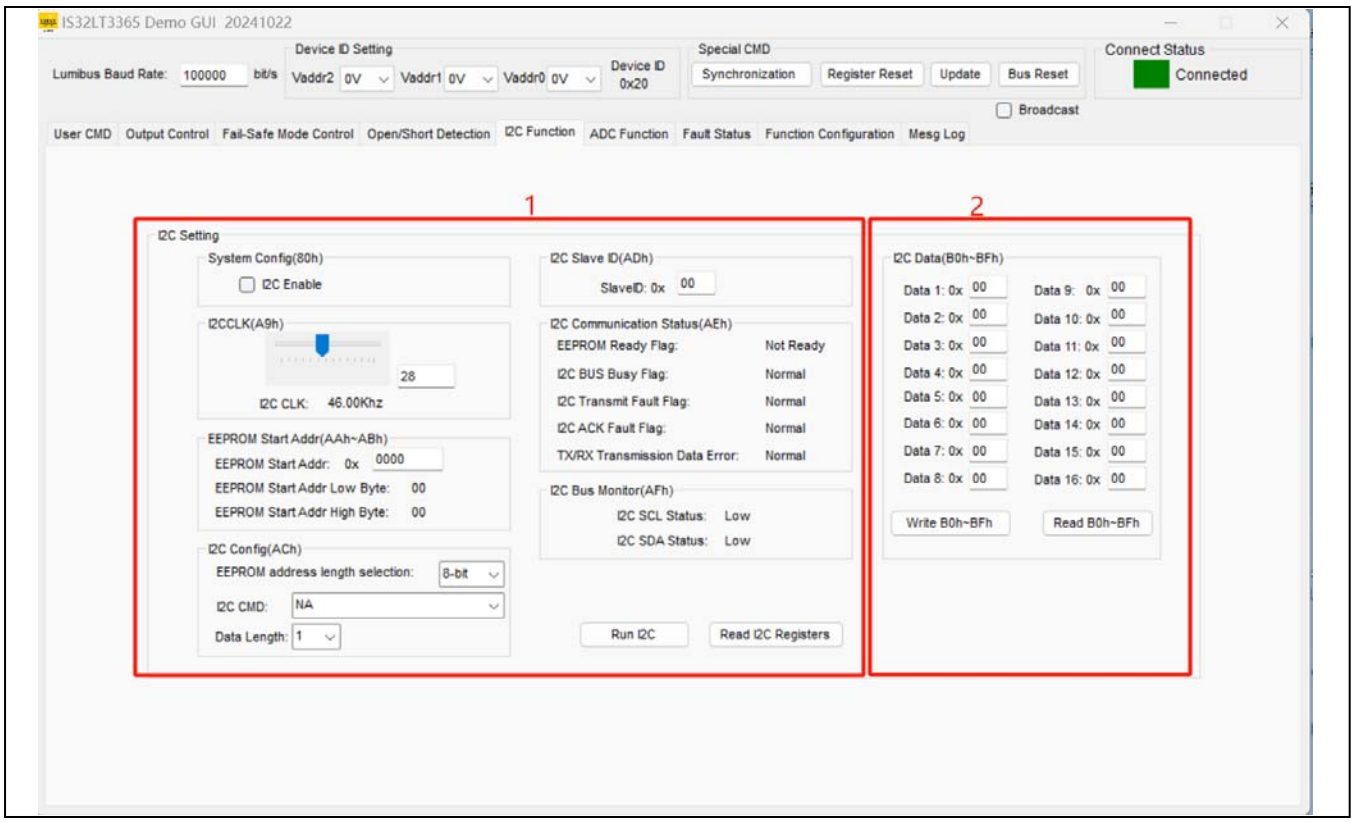

Figure 15 I²C Function Page

3.9 ADC Function Page (Refer to Figure 16)

3.9.1 ADC Configuration (99h~9Bh)

a) ADC Channel Enable: selects the desired input channels for ADC measurement.

b) ADC_EN: ADC Enable.

c) ADC CLK: ADC frequency setting.

d) ADC Sample: ADC sampling/hold time setting.

e) ADC Start: Start ADC measurement.

f) ADC Sampling Mode: If select the Single mode, all selected channels will be only measured once. If select the cycle mode, the ADC will repeat the measurement of all selected channels all the time.

g) ADC Times Average: For a more stable and precise result, each voltage is always sampled multiple times to calculate the average value.

3.9.2 ADC value (9Dh~A6h)

a) ADC_NTCH Value: The ADC result of NTCH pin.

b) ADC_NTCL Value: The ADC result of NTCL pin.

c) ADC_VPTAT Value: The ADC result of internal PTAT voltage. This result can be used to estimate the device junction temperature.

d) ADC_V5 Value: The ADC result of internal 5V LDO.

e) ADC_V33 Value: The ADC result of internal 3.3V LDO.

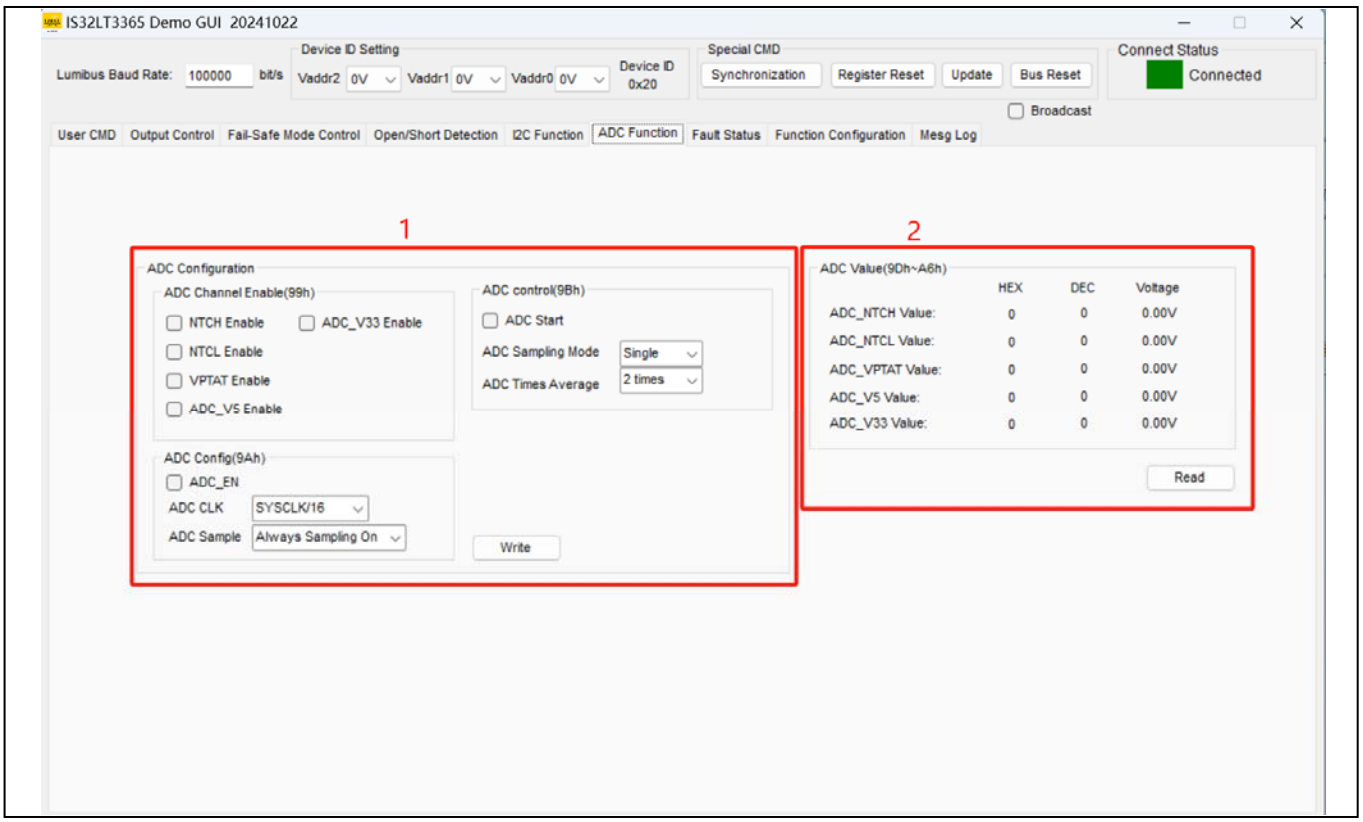

Figure 16 ADC Function Page

3.10 Fault Status Page (Refer to Figure 17)

3.10.1 Fault Types (94h~95h). Fault flag to indicate the various fault types.

3.10.2 Hardware Fault reporting setting (96h~97h). These registers determine whether to pull the FAULTB pin to low when the corresponding fault condition happens.

3.10.3 CRC Error counter (98h). This register value is incremented each time a CRC error is received.

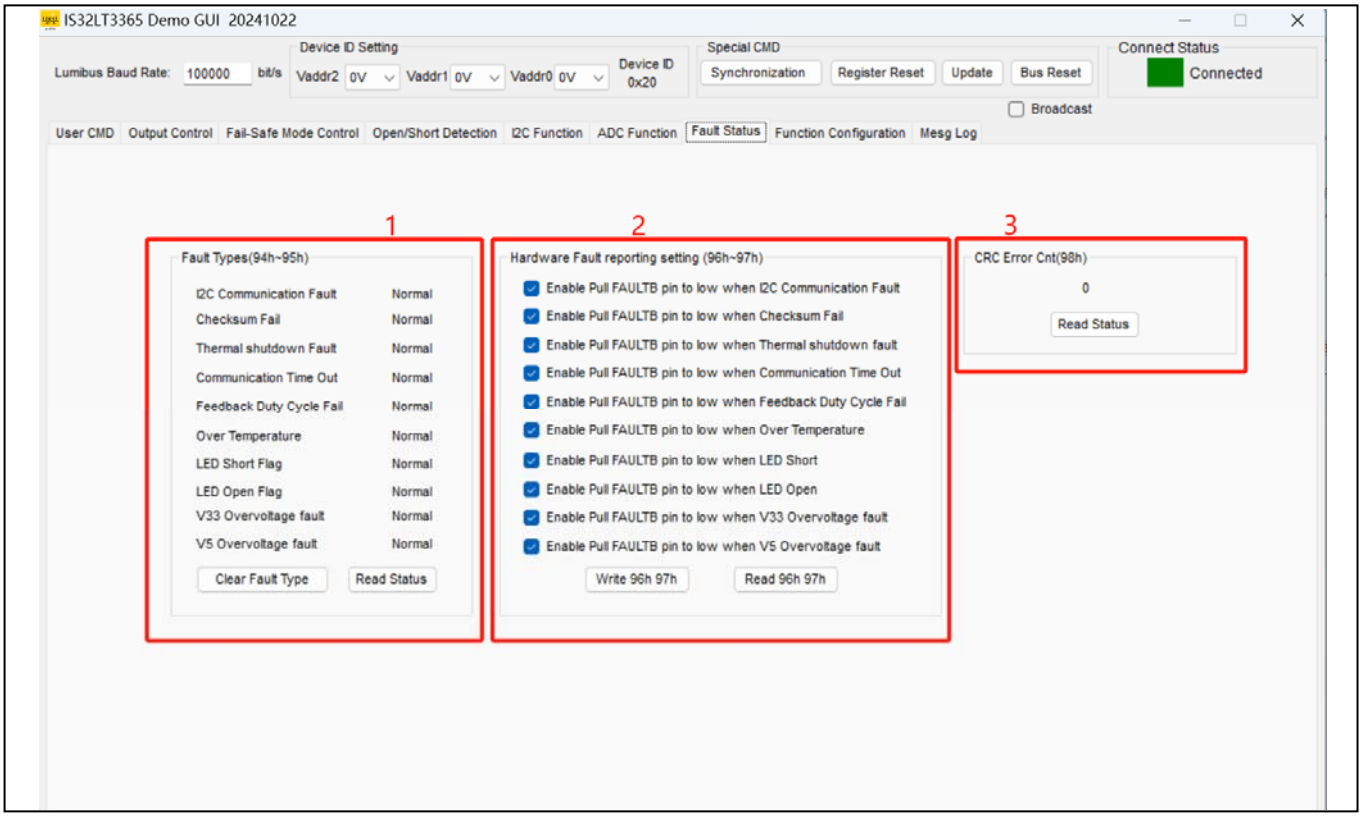

Figure 17 Fault Status Page

3.11 Function Configuration Page (Refer to Figure 18)

3.11.1 PARLED (71h)

a) None: each string of bypass switches is independent of the others.

b) S1//S2: sub-strings of S1 and S2 are connected in parallel, S3 and S4 are independent.

c) S1//S2, S3//S4: sub-strings of S1 and S2 are connected in parallel, and S3 and S4 are connected in parallel

d) S1//S2//S3//S4: sub-strings of S1, S2, S3, and S4 are all connected in parallel

3.11.2 OVER TEMP Threshold (7Ah)

Junction over temperature alarm threshold setting.

3.11.3 Spread Spectrum Config (7Bh)

When the spread spectrum function is enabled, the PWM frequency must be set to at least two times of the spread spectrum frequency to avoid flickering issue. Therefore, the default value of 125Hz (Typ.) is a good choice for most applications.

3.11.4 Master Slave Setting (7Ch)

The Master Slave Setting register is used to set the operating mode in the PWM synchronization operation of multiple IS32LT3365A devices. Disable external CLK pin when the device working at independent mode, enable external CLK pin when the device working at master or slave mode. To prevent the push-pull state of one device is shorted by push-pull or strong pulldown of other devices, please configure all devices to slave mode before one device to master mode.

3.11.5 System Config (80h)

a) I2C Enable: I^2C Master Enable.

b) ACK Enable: if select ACK enables, acknowledge (0x7F) is transmitted following successfully received writes.

c) Phase Shift LED ON Enable: If select this, the LED phase shift apply to LED turn-on times. The configuration of this bit must be updated by the “Update Command”.

d) SYNC Output Enable: This bit can only be configured by a single device write command frame but not a broadcast command frame.

e) SYNC Pulse Enable:

Selecting this setting enables the SYNC output to be powered with a 50% duty cycle pulse to synchronize with other IS32LT3365A device.

f) Power Cycle Flag: This bit is reset to 0 upon power-up or EN pin toggling.

3.11.6 Communications Watchdog Time Out (81h)

3.11.7 LBIST state (C0h)

This device will perform a Logic Built-in Self-test upon UVLO being released.

3.11.8 IC Identification (C7h)

Read to this register address return the value 0xA1. This is intended to be used to identify an IS32LT3365A device.

3.11.9 Loopback Control (C1h~C4h)

a) Loopback Channel select: Select the channel for loopback verification.

b) Loopback verification function select：Select self-test mode or loopback test mode.

c) Loopback one channel mode: Keep verification on selected channel.

d) Loopback auto loop mode: Autoloop verification of all channels in turn.

e) Tolerance: Loopback comparison tolerance setting

f) Loopback Fault Flag: Loopback fault flag for each channel, when the comparison error exceeds the preset tolerance value, the corresponding fault flag bit will be set to 1.

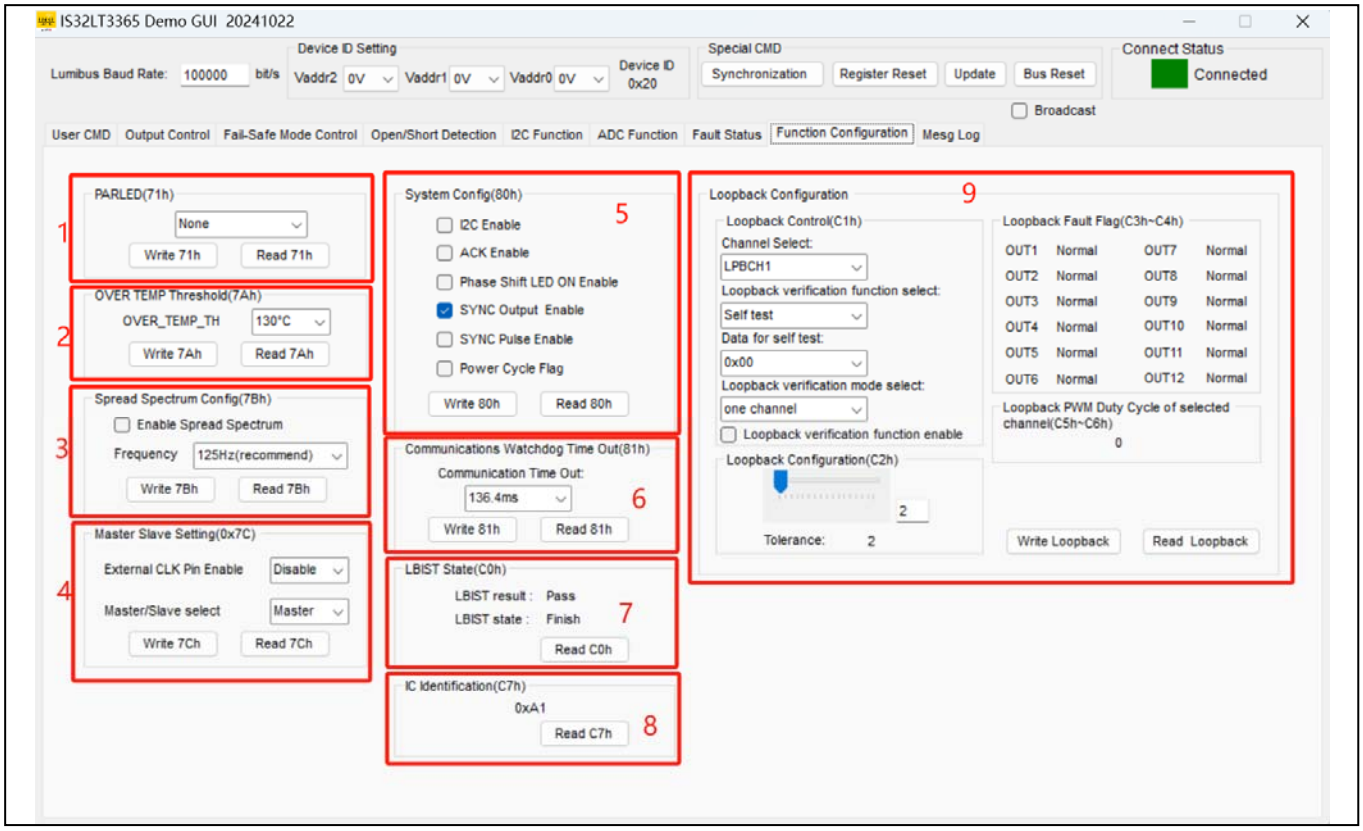

Figure 18 Function Configuration Page

3.12 Message Log Page (Refer to Figure 19)

3.12.1 Communication Command Message Log

3.12.2 Clear Log: Clear Message Log

3.12.3 Save Log: Save Message Log to Excel

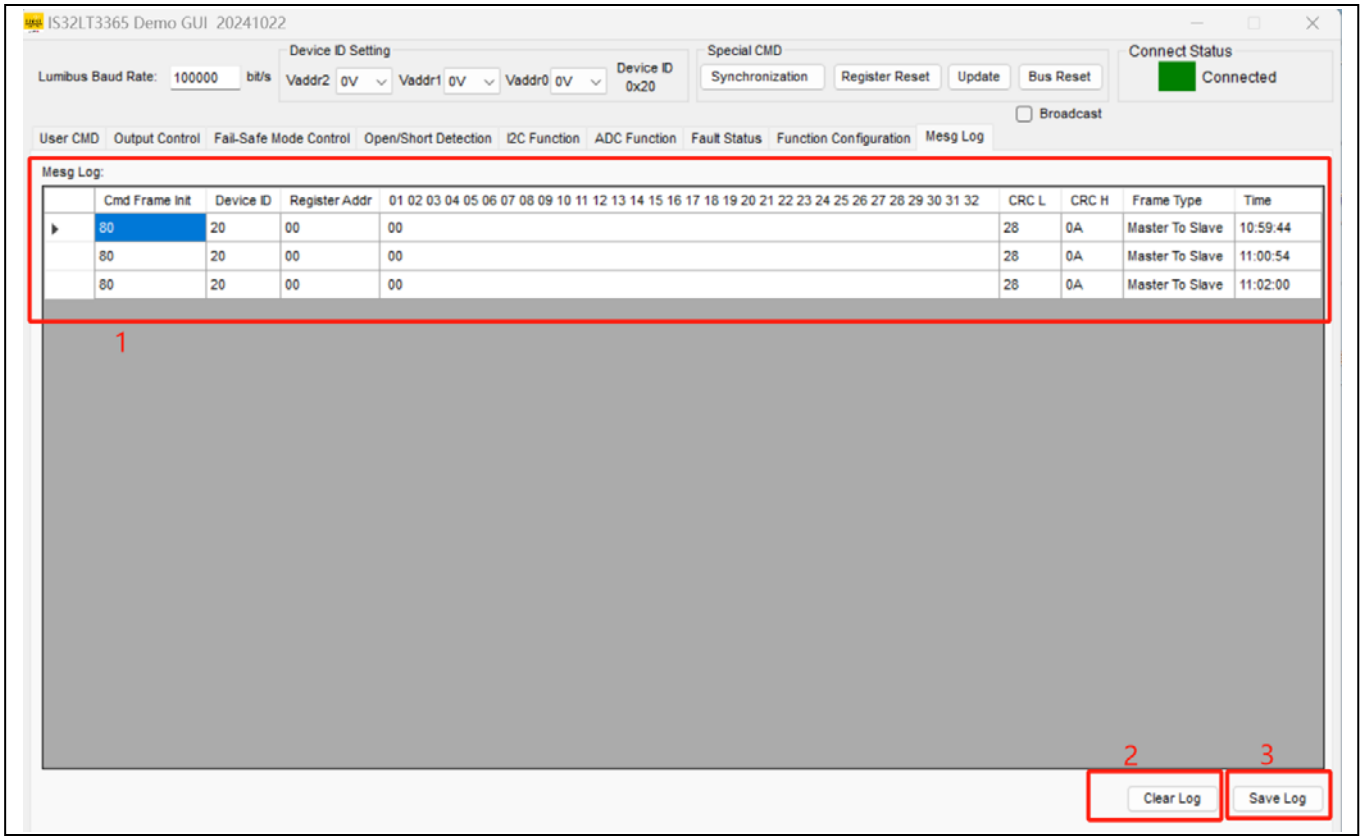

Figure 19 Message Log Page

4. EXAMPLE

Example 1: How to light up output channels 1/2/3 (PWM Duty cycle=50%)? Refer to Figure 20~21.

STEP 1: Check the connect status, green is OK, red is unconnected.

STEP 2: Setting Device ID.

STEP 3: Setting Baud rate (100kbps~1Mbps).

STEP 4: Send Bus Reset command.

STEP 5: Turn to the output control page and set PWM to 512 of output channels 1/2/3, then send the frame.

STEP 6: Send update command, then you can find LED channels 1/2/3 are light up with duty cycle=50%.

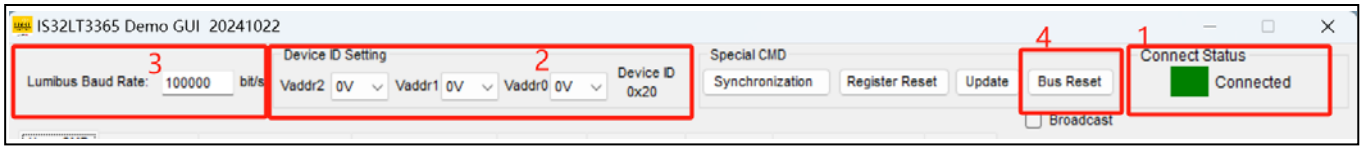

Figure 20 GUI Setting Page

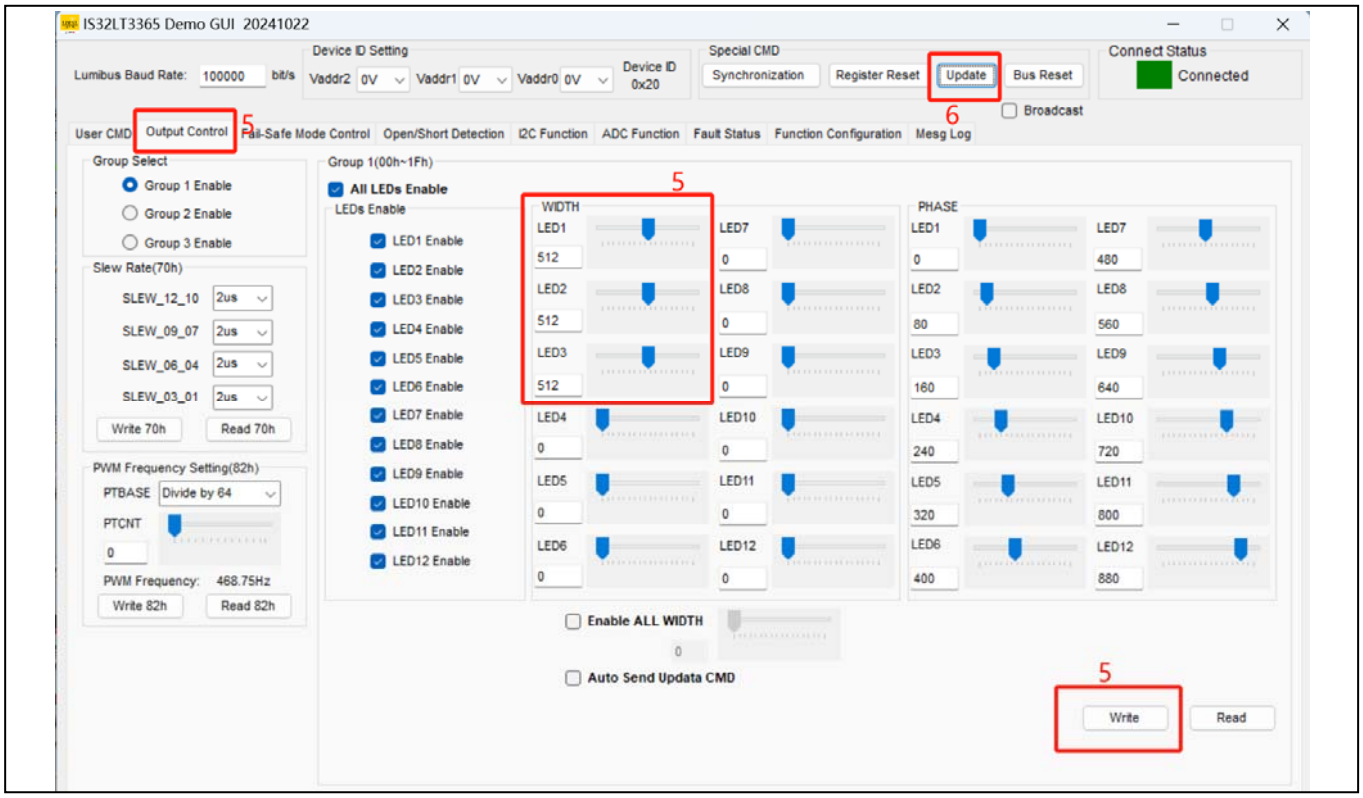

Figure 21 Output Control Page

Example 2: How to read 01h register of IS32LT3365A? Refer to Figure 22~23.

STEP 1: Check the connect status, green is ok, red is unconnected.

STEP 2: Setting Device ID.

STEP 3: Setting Baud rate (100kbps~1Mbps).

STEP 4: Send Bus Reset command.

STEP 5: Turn to User command page and select READ mode then input the value “01” to Register Address.

STEP 6: Send the frame and you can find data “50” is returned by IS32LT3365A.

Figure 22 GUI Setting Page

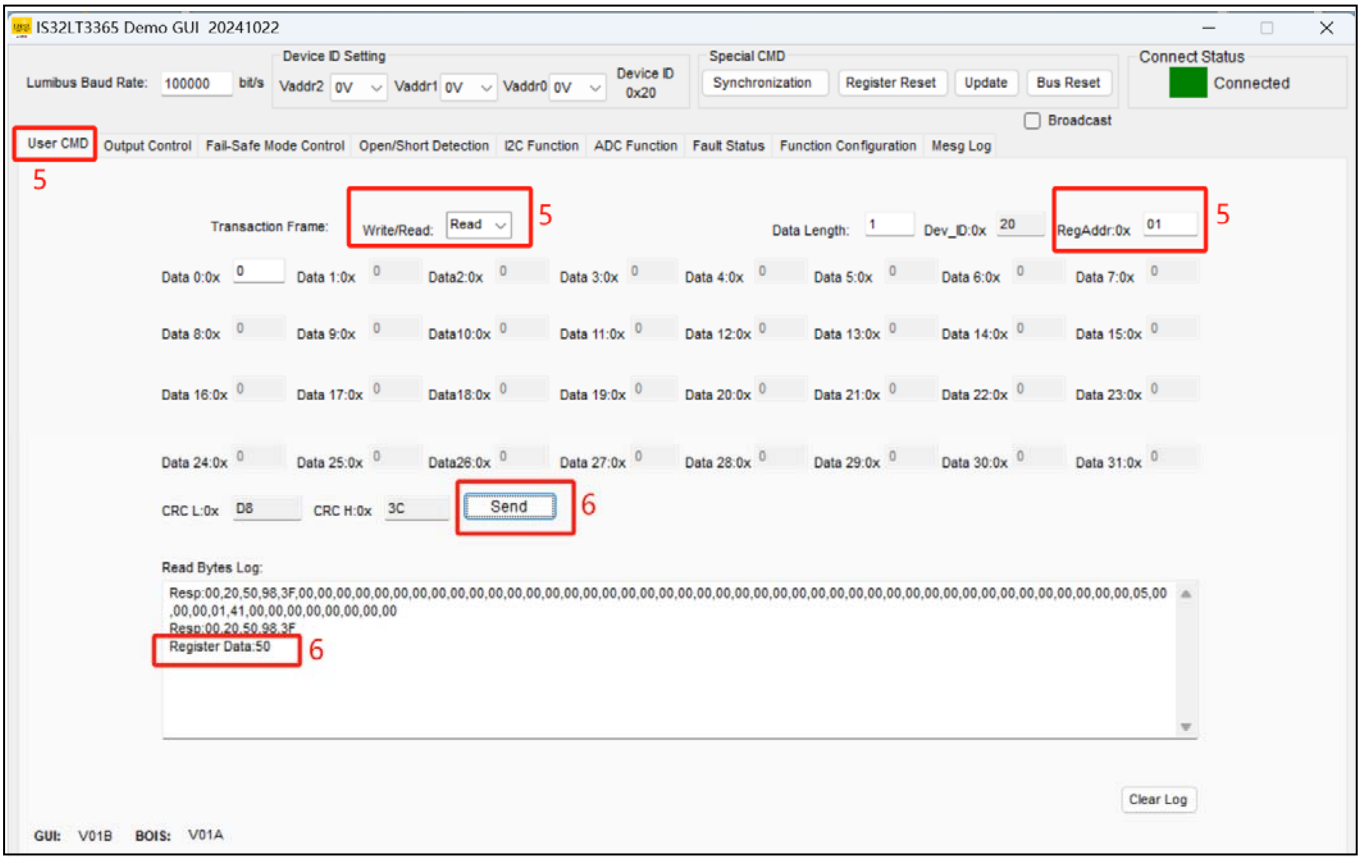

Figure 23 User Command Page

SCHEMATIC OF LED BOARD

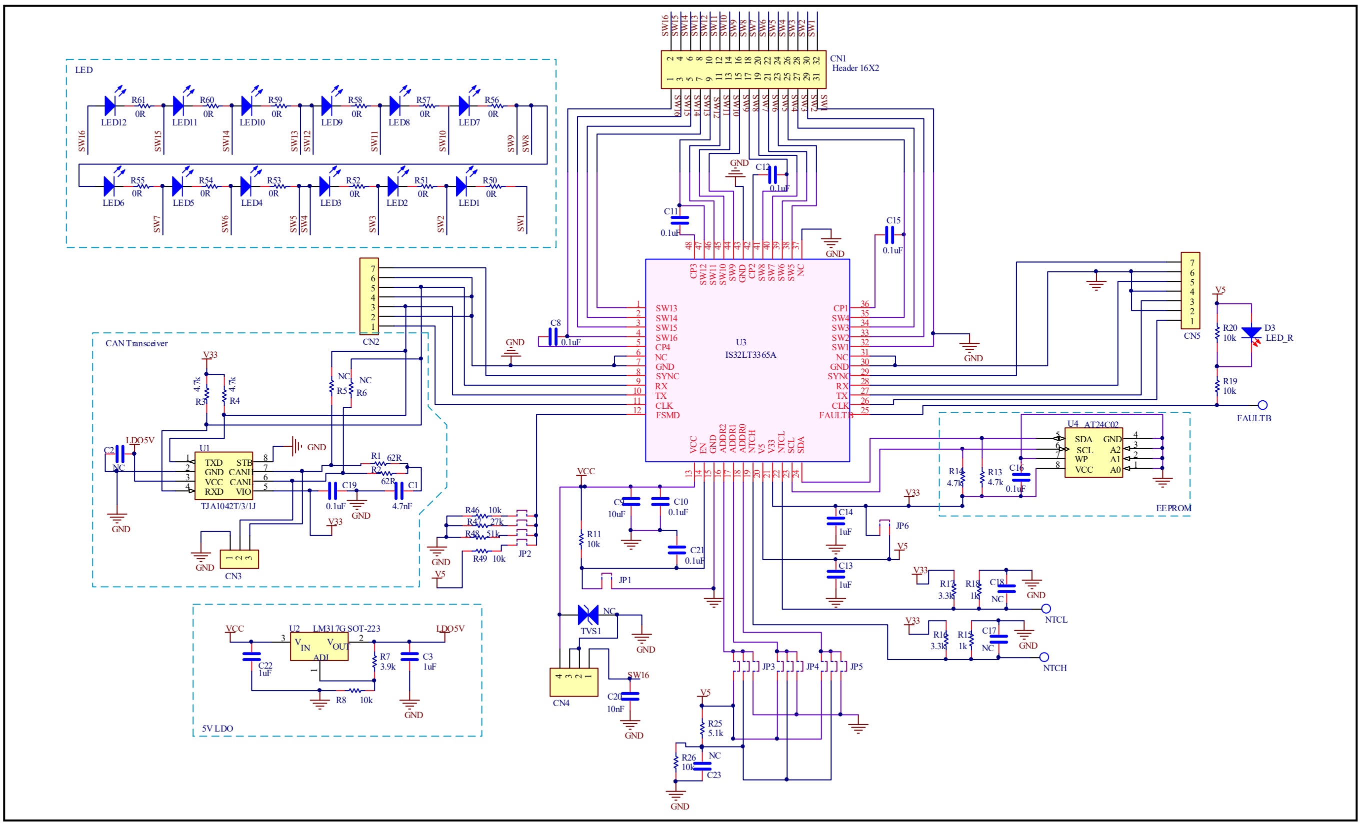

Figure 24 Schematic of IS32LT3365A LED Board

BILL OF LED BOARD

Name	Symbol	Description	Qty	Supplier	Part No.
-	TVS1, C18, C17, C3, C23, R5, R6, C2	NC	0		-
PCB	-	116mm × 63mm, FR-4, 4 layers, 1oz copper	1	-	-
LED Dimmer	U3	LED DIMMER	1	Lumissil	IS32LT3365A-LQLA3
Capacitor	C10, C16, C19, C21	CAP, 0.1μF, 0603, 50V, ±10%, SMD	4	Yageo	AC0603KKX7R9BB104
Capacitor	C9	CAP,10μF, 1206, 50V, ±10%, SMD	1	Yageo	AC1206KKX7R9BB106
Capacitor	C13, C14	CAP,1μF,50V, 0603, ±10%, SMD	3	Yageo	AC0603KKX7R9BB105
Capacitor	C1	CAP,4.7nF,0603,50V, ±10%, SMD	1	Yageo	AC0603KKX7R9BB472
Capacitor	C20	CAP,10nF,0603,50V, ±10%, SMD	1	Yageo	AC0603KKX7R9BB103
Capacitor	C3, C22	CAP, 1μF,0805,50V, ±10%, SMD	2	Yageo	AC0805KKX7R9BB105
Capacitor	C8, C11, C12, C15	CAP,0.1μF,0805,50V, ±10%, SMD	4	Yageo	AC0805KKX7R9BB104
Resistor	R18, R15	RES,1k, 0603, ±5%, SMD	2	Yageo	AC0603JR-071KL
Resistor	R16, R17	RES,3.3k, 0603, ±5%, SMD	2	Yageo	AC0603JR-073K3L
Resistor	R7	RES,3.9k, 0603, ±5%, SMD	1	Yageo	AC0603JR-073K9L
Resistor	R25	RES,5.1k, 0603, ±5%, SMD	1	Yageo	AC0603JR-075K1L
Resistor	R49, R11, R26, R46, R20, R19, R8	RES,10k, 0603, ±5%, SMD	7	Yageo	AC0603JR-0710KL
Resistor	R47	RES,27k, 0603, ±5%, SMD	1	Yageo	AC0603JR-0727KL
Resistor	R48	RES,51k, 0603, ±5%, SMD	1	Yageo	AC0603JR-0751KL
Resistor	R50, R51, R52, R53, R54, R55, R56, R57, R58, R59, R60, R61	RES,0R, 0603, ±5%, SMD	12	Yageo	AC0603JR-070RL
Resistor	R1, R2	RES,62R, 0603, ±5%, SMD	2	Yageo	AC0603JR-0762RL
Resistor	R3, R4, R13, R14	RES,4.7k, 0603, ±5%, SMD	4	Yageo	AC0603JR-074K7L
EEPROM	U4	I^2C-Compatible (2-wire) Serial EEPROM	1	ATMEL	AT24C02C-SSHM-T
CAN Transceiver	U1	High-speed CAN transceiver	1	NXP	TJA1042T/3/1J
LDO	U2	HIGH CURRENT 1.3V TO 37V ADJUSTABLE VOLTAGE REGULATOR	1	MSKSEMI	LM317G-MS
LED	D3	RED LED, 0603, VF=3V	1	OSRAM	LS Q976-NR-1
LED	LED1~LED12	White LED, VF=3.3V, IF=700mA	12	HUAYI	C35W60-120

Bill of Materials, refer to Figure 24 above.

PCB LAYOUT OF LED BOARD

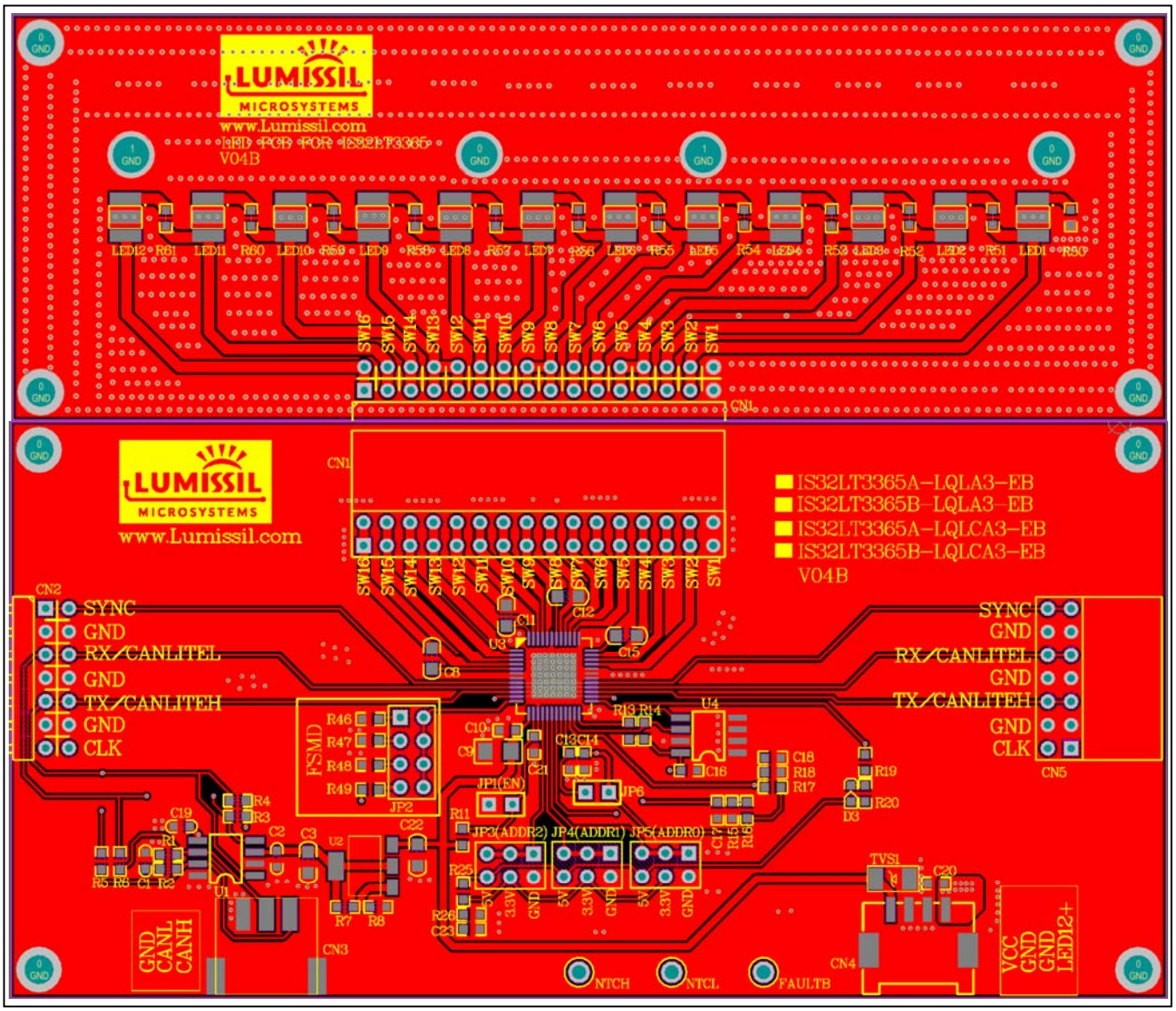

Figure 25 Top Layer

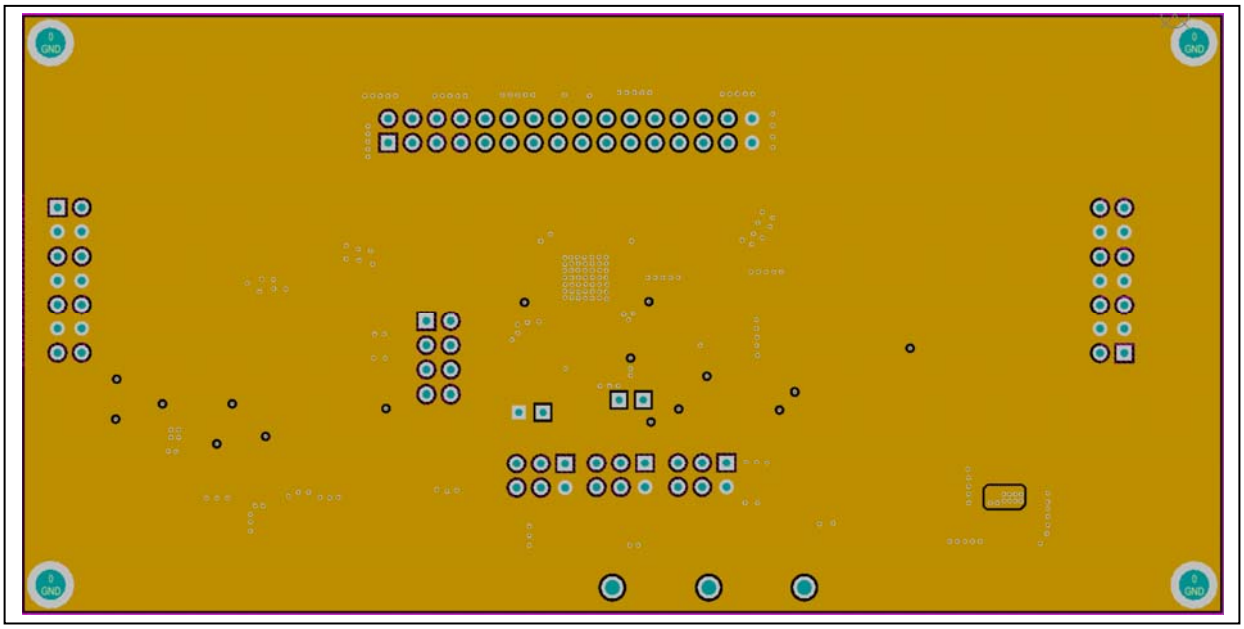

Figure 26 Second Layer

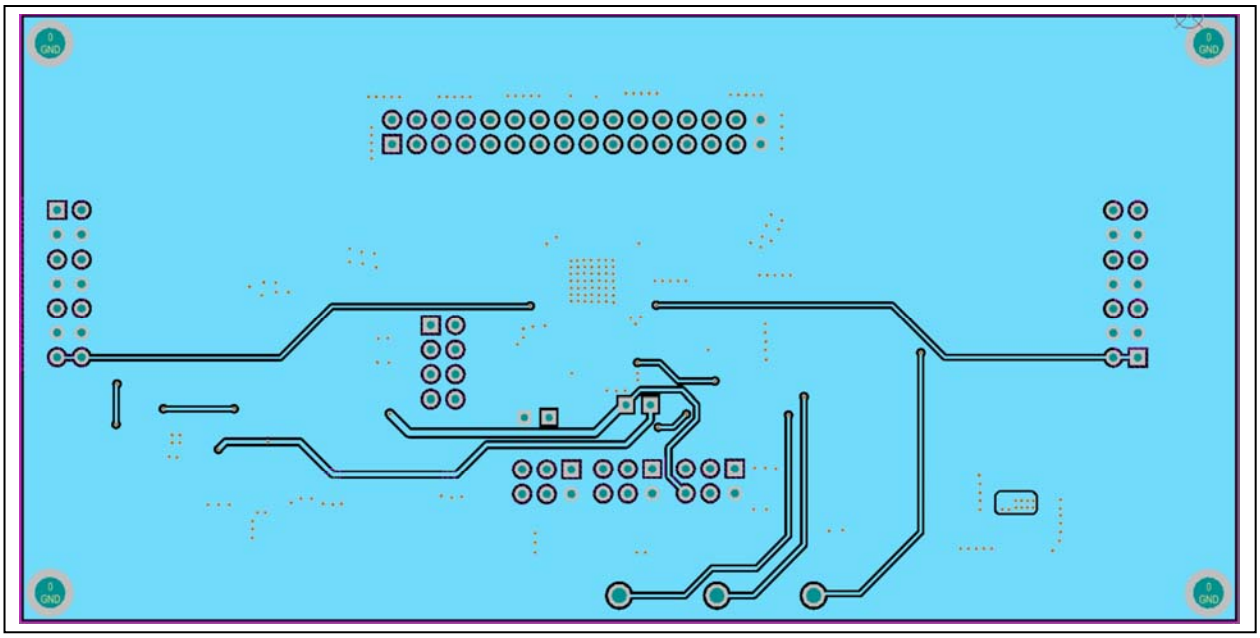

Figure 27 Third Layer

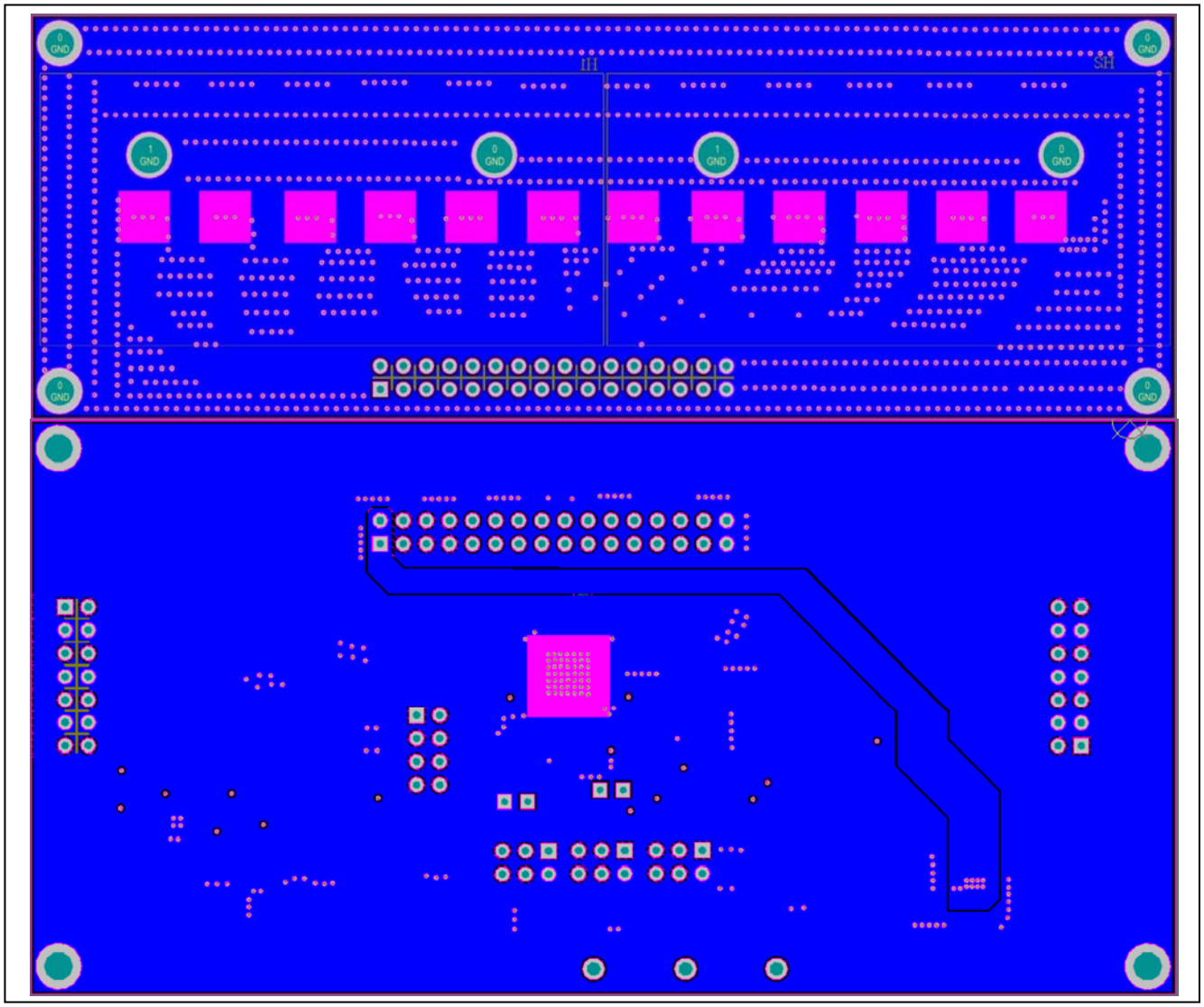

Figure 28 Bottom Layer

SCHEMATIC OF POWER BOARD

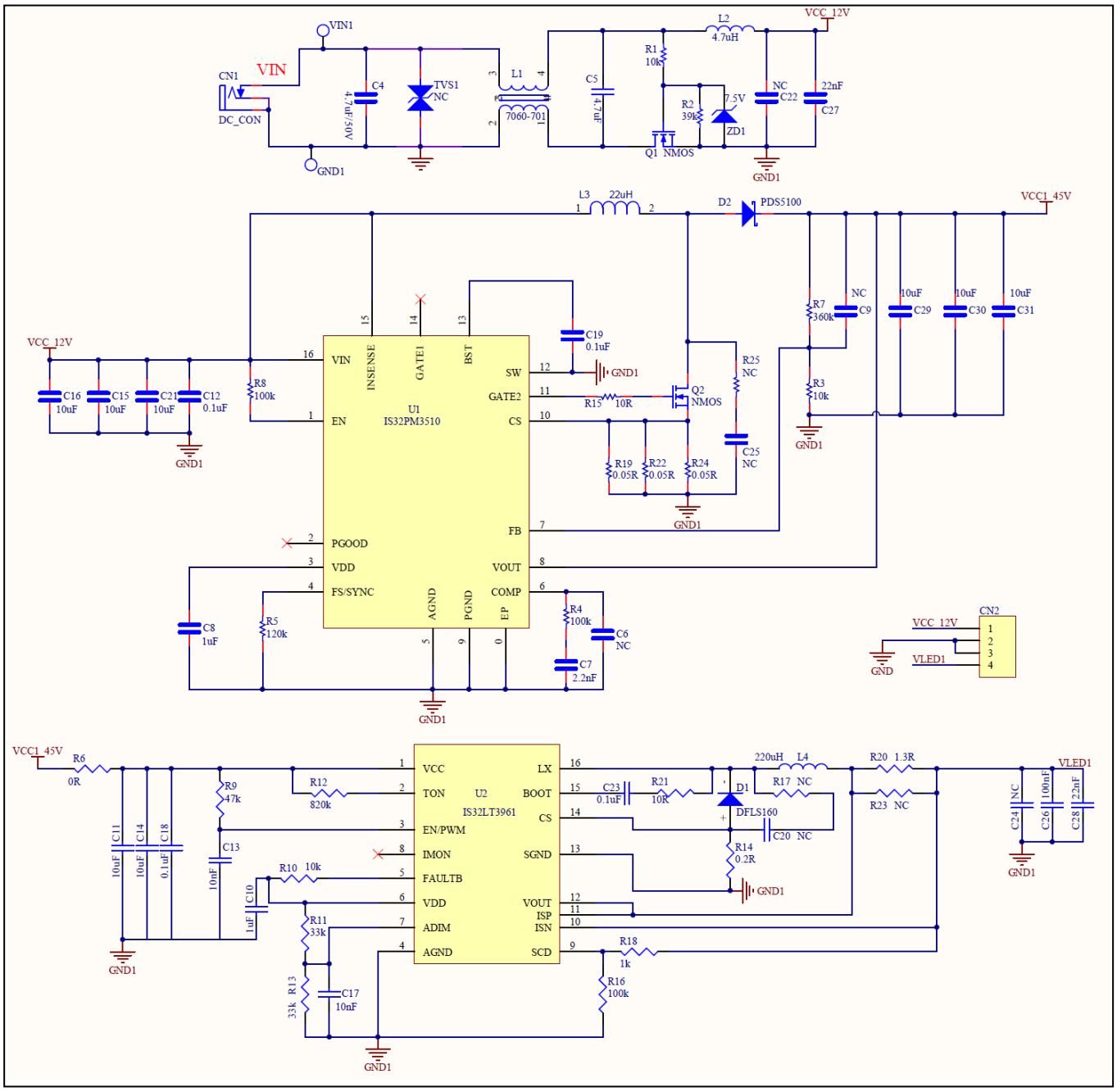

Figure 29 Schematic of Power Board

BILL OF LED BOARD

Name	Symbol	Description	Qty	Supplier	Part No.
IC	U1	ASYNCHRONOUS BOOST AND BUCK-BOOST VOLTAGE REGULATOR	1	Lumissil	IS32PM3510-ZLA3
IC	U2	CONSTANT-CURRENT LED DRIVER	1	Lumissil	IS32LT3961-ZLA3
DC power outlet	CN1	DC-005, 12V	1	CIKI	DC-005-A
Capacitor	C16, C15, C21, C29, C30, C31	CAP,10μF, 1210, 50V, ±10%, SMD	6	TAIYO YUDEN	UMK325AB7106KMHP
Capacitor	C12, C18, C19, C23	CAP,0.1μF,0603, 50V, ±10%, SMD	2	Yageo	AC0603KKX7R9BB104
Capacitor	C11, C14	CAP,10μF,1206, 50V, ±10%, SMD	2	Yageo	AC1206KKX7R9BB106
Capacitor	C10, C8	CAP,1μF,16V, 0603, ±10%, SMD	2	Yageo	AC0603KKX7R7BB105
Capacitor	C26	CAP,0.1μF,50V, 0805, ±10%, SMD	1	Yageo	AC0805KKX7R9BB104
Capacitor	C4, C5	CAP,4.7μF,50V, 0805, ±10%, SMD	2	Yageo	AC0805KKX7R9BB475
Capacitor	C7, C27, C28	CAP,22nF, 0603, 50V, ±10%, SMD	1	Yageo	AC0603KKX7R9BB223
Capacitor	C13, C17	CAP,10nF, 0603, 50V, ±10%, SMD	1	Yageo	AC0603KKX7R9BB103
PCB	-	70mm × 54mm, FR-4, 4 layers, 1oz copper	1		-
-	TVS1, C24, R23, R17, C20, C6, C9, R25, C25, C22	NC			-
Resistor	R19, R22, R24	RES,0.05R,1206, ±1%, SMD	3	Yageo	PE1206FRF7W0R05L
Resistor	R14	RES,0.2R,1206, ±1%, SMD	1	Yageo	PT1206FR-070R2L
Resistor	R20	RES,1.3R,1206, ±1%, SMD	1	Yageo	AC1206FR-071R3L
Resistor	R6	RES,0R, 0603, ±5%, SMD	1	Yageo	AC0603JR-070RL
Resistor	R5	RES,120kR,0603, ±5%, SMD	1	Yageo	AC0603JR-07120KL
Resistor	R4, R9, R10, R11, R13, R1, R3	RES,10kR,0603, ±5%, SMD	7	Yageo	AC0603JR-0710KL
Resistor	R8, R16	RES,100kR, 0603, ±5%, SMD	2	Yageo	AC0603JR-07100KL
Resistor	R7	RES,390kR, 0603, ±5%, SMD	1	Yageo	AC0603JR-07390KL
Resistor	R18	RES,1kR, 0603, ±5%, SMD	1	Yageo	AC0603JR-071KL
Resistor	R15, R21	RES,10R, 0603, ±5%, SMD	2	Yageo	AC0603JR-0710RL
Resistor	R12	RES,680kR, 0603, ±5%, SMD	1	Yageo	AC0603JR-07680KL
Resistor	R2	RES,39kR, 0603, ±5%, SMD	1	Yageo	AC0603JR-0739KL
MOSFET	Q1	20A, 60V, NMOS	1	DIODES	DMN6040SK3-13
MOSFET	Q2	55A, 60V, NMOS	1	DIODES	DMNH6021SPSQ-13
Inductor	L3	22μH±20%, Isat≥5.55A, SMD	1	COILANK	AAPS10A40M220
Inductor	L4	220μH±20%, Isat≥1A, SMD	1	COILANK	AAPW07A45M221
Inductor	L2	4.7μH±20%, I_R=6.3A	1	Panasonic	ETQP5M4R7YFM
Inductor	L1	700Ω@100MHz, I_R=5A	1	TDK	ACM90V-701-2PL-TL00
Diode	D2	5A, 100V, Shottky diodes	1	DIODES	PDS5100H-13
Diode	D1	1A, 60V, Shottky diodes	1	DIODES	DFLS160-7
Diode	ZD1	DIODE ZENER 7.5V	1	DIODES	BZT52HC7V5WF-7

Bill of Materials, refer to Figure 28 above.

PCB LAYOUT OF POWER BOARD

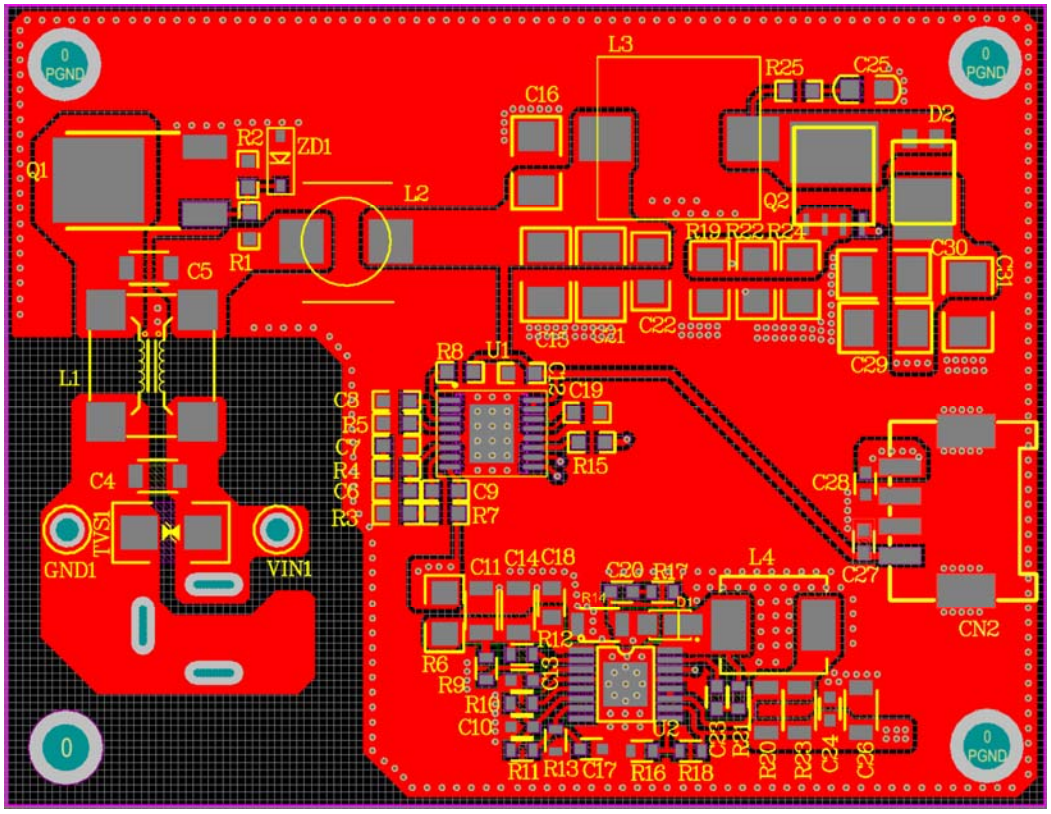

Figure 30 Top Layer

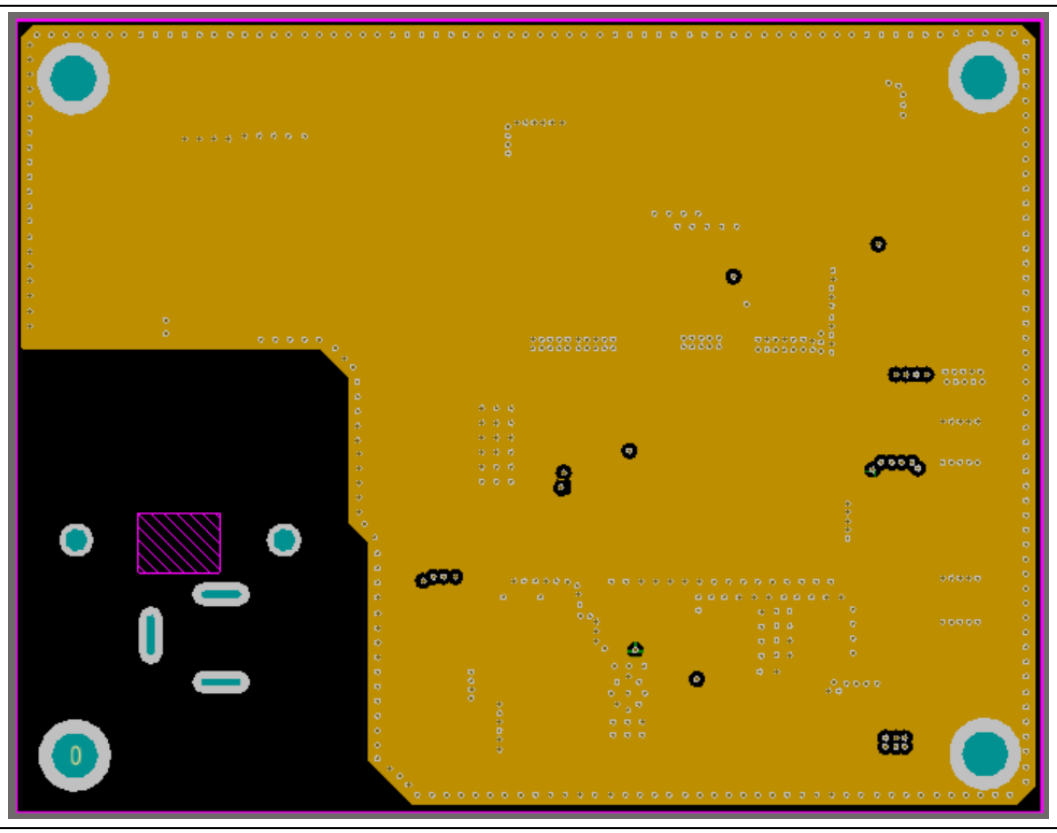

Figure 31 Second Layer

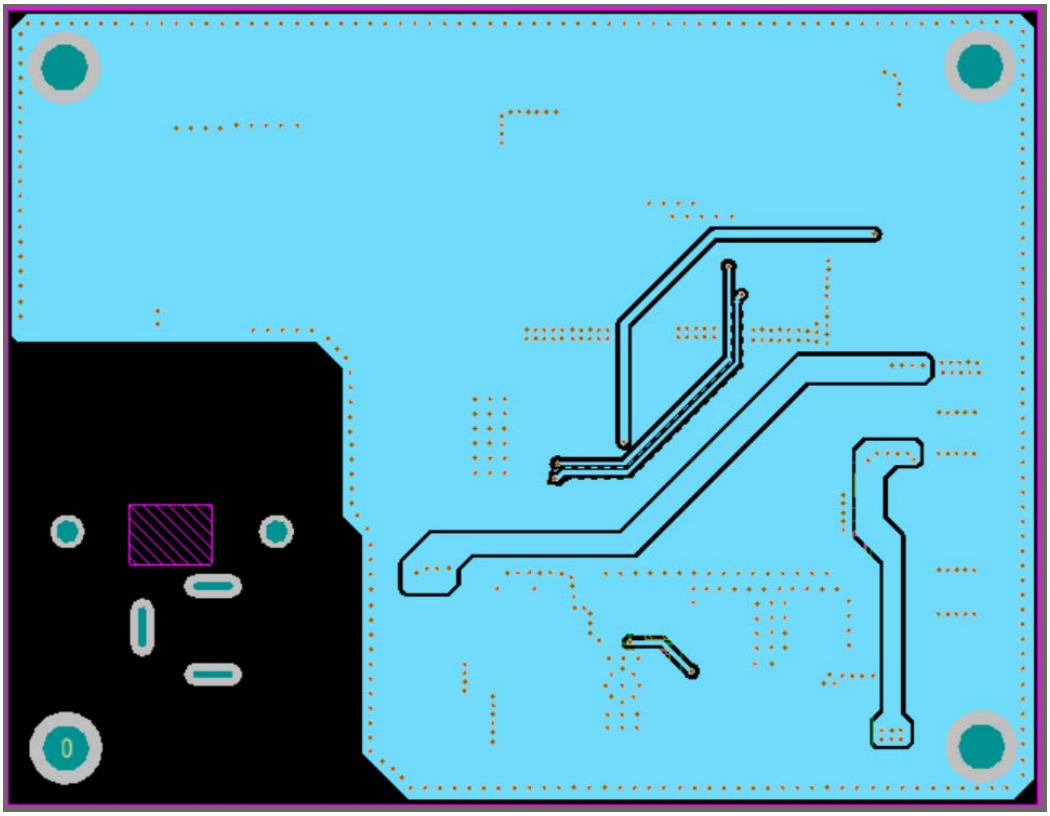

Figure 32 Third Layer

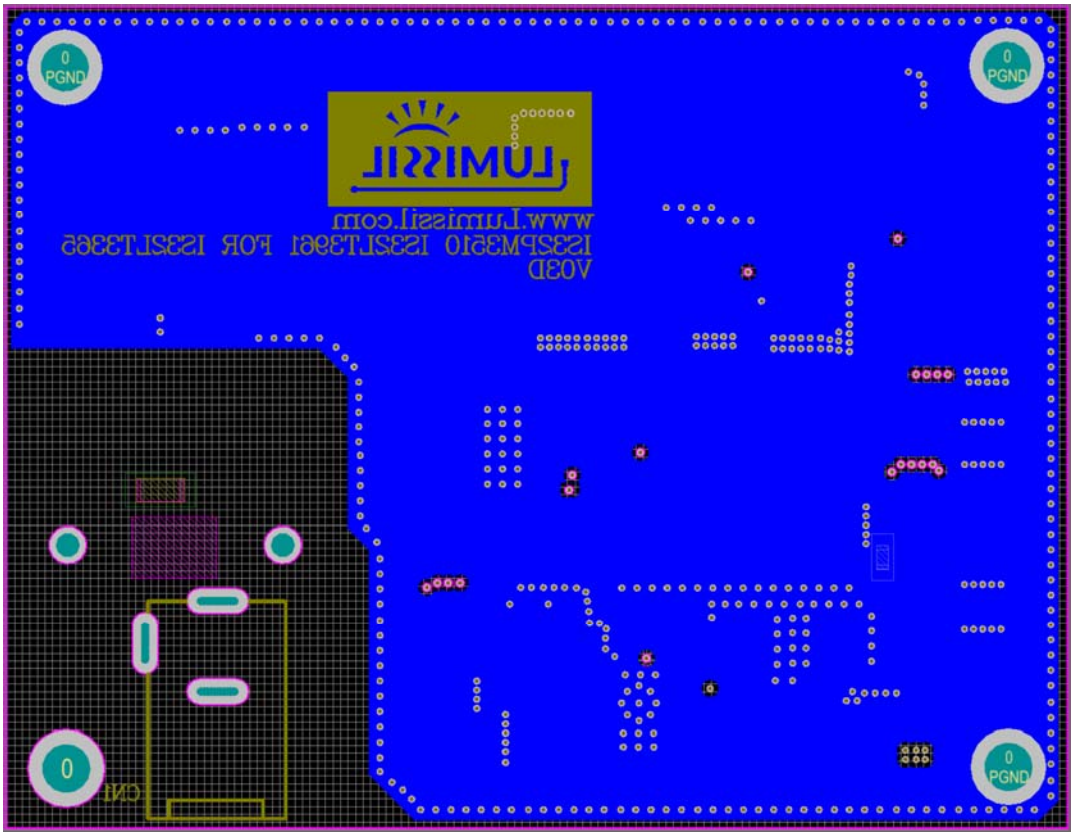

Figure 33 Bottom Layer

CONDUCTED EMI PERFORMANCE

Test Conditions: V_{IN}= 12V, V_{LED}= 36V, I_{LED}= 0.15A, ALL LED WIDTH= 512 (PWM DUTY CYCLE= 50%).

Test standard: CISPR-25 Class 5 conducted EMI (Blue: Peak scanning, Red: Average scanning).

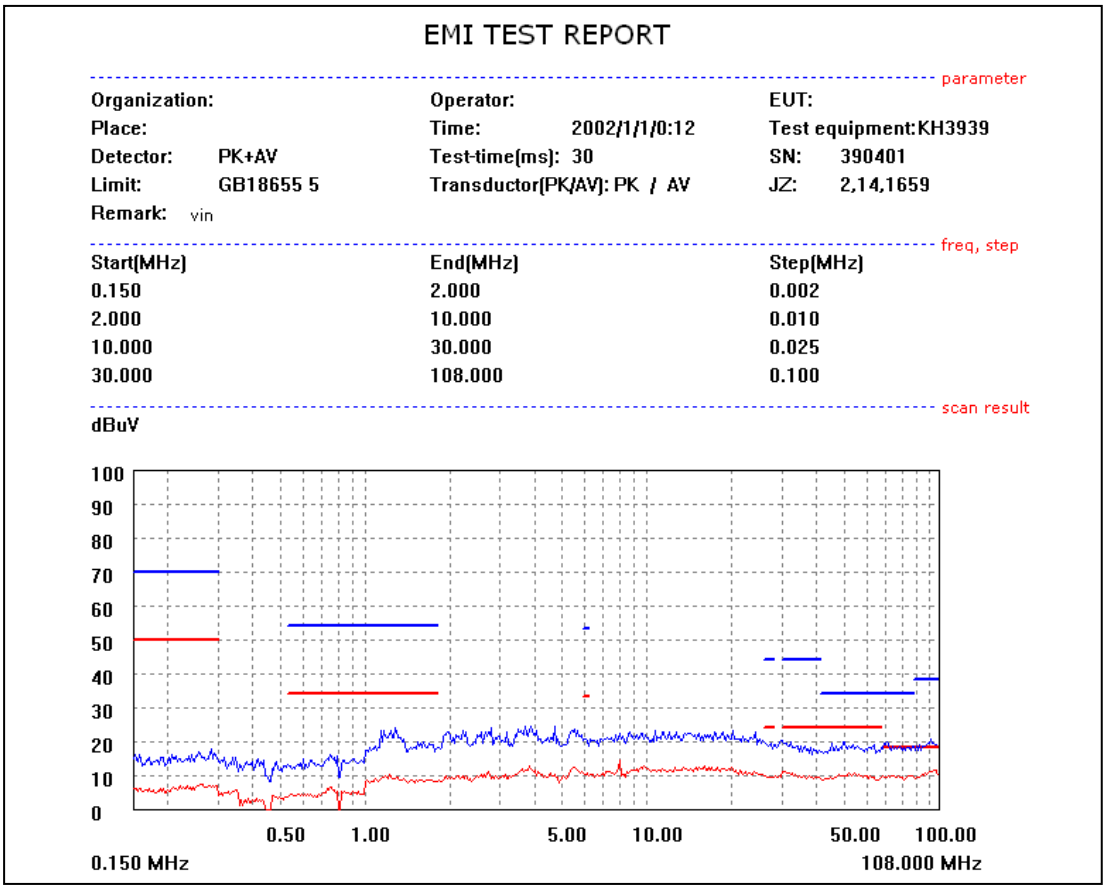

Figure 34 CISPR-25 Class 5 Conducted EMI Scan VIN Line

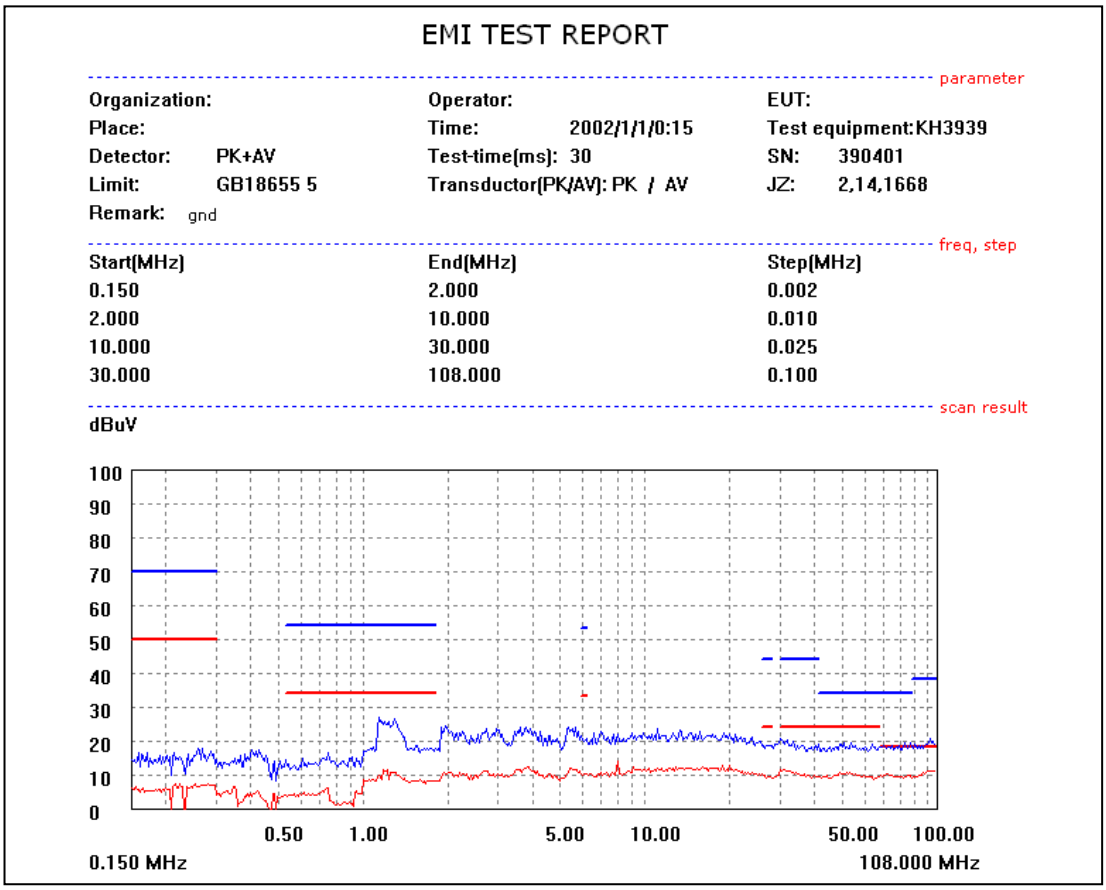

Figure 35 CISPR-25 Class 5 Conducted EMI Scan GND Line

REVISION HISTORY

Revision	Detail Information	Date
A	Initial release	2025.01.21