IS32LT3136

32-CHANNEL LINEAR LED DRIVER WITH UART INTERFACE

May 2026

1 GENERAL DESCRIPTION

The IS32LT3136 is a high-side output linear programmable current regulator with 32 output channels, designed for automotive OLED and LED lighting applications. It features a UART interface compatible with CAN FD PHY for communication with a master microcontroller or ECU. Adopting a command-response protocol controlled by the host MCU, it enables register read and write operations for single or multiple cascaded IS32LT3136 devices.

The IS32LT3136 is suitable for driving common-cathode OLED panels. It supports a maximum output voltage of 22V to accommodate wide variations in OLED forward voltage. Each output channel independently supports 12-bit PWM dimming and 8-bit DC current adjustment, enabling individual driving control over each pixel of the OLED panel. The output current is adjustable from 1mA to 35mA per channel.

For added system reliability, the IS32LT3136 integrates fault detection circuitry for open/short string, single LED short, and over temperature conditions. Faults are recorded in registers which can be accessed by an external MCU. To optimize EMI performance, the IS32LT3136 features spread spectrum on the internal PWM and LED channel outputs have programmable slew rate control to mitigate EMI and power supply inrush current.

The IS32LT3136 is targeted at the automotive market such as interior accent lighting and exterior tail lighting. It is offered in QFN-48 (6mm×6mm) package.

2 APPLICATIONS

- Animation (OLED) Rear Light
- Animation Tail Light
- Animation Daytime Running Light
- Automotive Ambient Lighting

3 SAFETY RELEVANT FEATURES

- LED open, single LED short and short detect via OP and comparator
- PWM loop back test and loopback test BIST
- LBIST build in via LBIST
- Communication abnormal via communication watchdog timer
- Communication data error via CRC and checksum check
- VLED Under voltage detection via comparator.

4 FEATURES

- Input VLED voltage tolerates up to 20V, nominal operation voltage between 4.5V to 20V
- UART Communication Interface
  - UART interface compatible with CANFD physical layer, 2MHz maximum (64MHz OSC)
  - UART communication with CRC to ensure robustness of communication
  - Support up to max.64 addressable devices
  - Watch dog timer
  - Support Fail safe mode
- 32 channels capable of 35mA each
  - ±4% @ 3mA~15mA bit-to-bit output current mismatch
  - ±4% @ 3mA~15mA device-to-device output current accuracy
- Combined for higher current capability with same current accuracy
  - Minimum headroom voltage of 0.8V(Max.) at 15mA
- Individual PWM dimming to each channel
  - 4096 steps (12-bit) PWM duty cycle setting
    - 12-bit
    - 7+5-bit (with 5bits dithering)
    - 8-bit
  - Phase delay minimizes inrush current (8 groups)
- Slew rate control and spread spectrum optimize EMI performance
- 256 steps (8-bit) global current setting
- Individual 256 steps (8-bit) DC current adjustment to each channel
- Spread spectrum
- DC feedback for automatic DCDC VLED adjustment to optimize system power supply (DCFB)
- Programmable PWM frequency (8bit: 200Hz/300/400/500/700/1k/1.2k/1.4k, 8 options, 1.6kHz/3.2k/6.4k/ 12.8k/25.6k another 5 options, total 13 options)
- 10-bit ADC for pin voltage measurement
- Support on OTP for data storage with fail safe mode1
- Fault protection with reporting
  - Fail safe modes selection
  - LED string open/short detect
  - Single LED short detect
  - Programmable fault reporting delay time
  - Programmable over temperature current roll off
  - Thermal shutdown
  - CRC error detection
  - Overcurrent (ISET pin short to GND)

- ISET pin open
- Fault pin pull down fault
- LED undervoltage
- PWM loop back detect
- SCA verification

- AEC-Q100 Qualified with Temperature Grade 1: -40°C to 125°C
- QFN-48 (6mm×6mm) package
- Supports applications with safety requirements up to ASIL-B
- RoHS & Halogen-Free Compliance
- TSCA Compliance

5 TYPICAL APPLICATION CIRCUIT

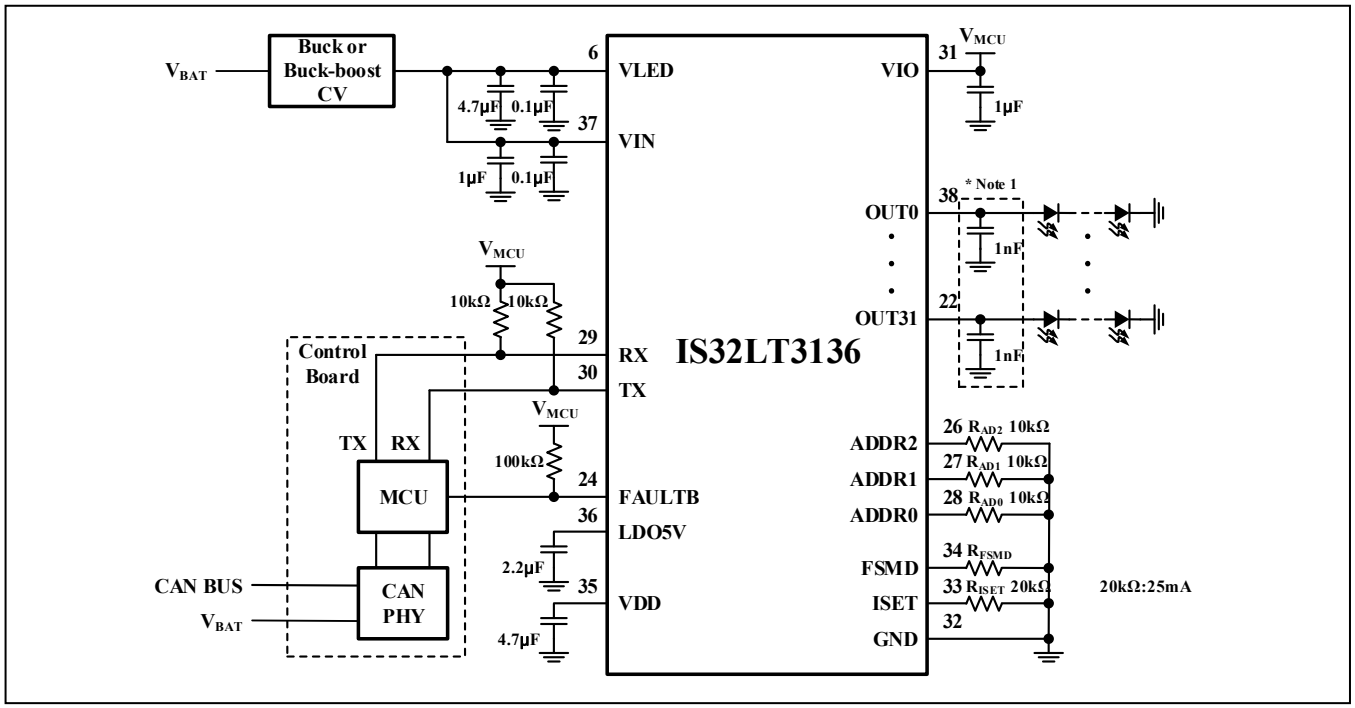


Figure 1 Typical Application Circuit of IS32LT3136 with UART Interface

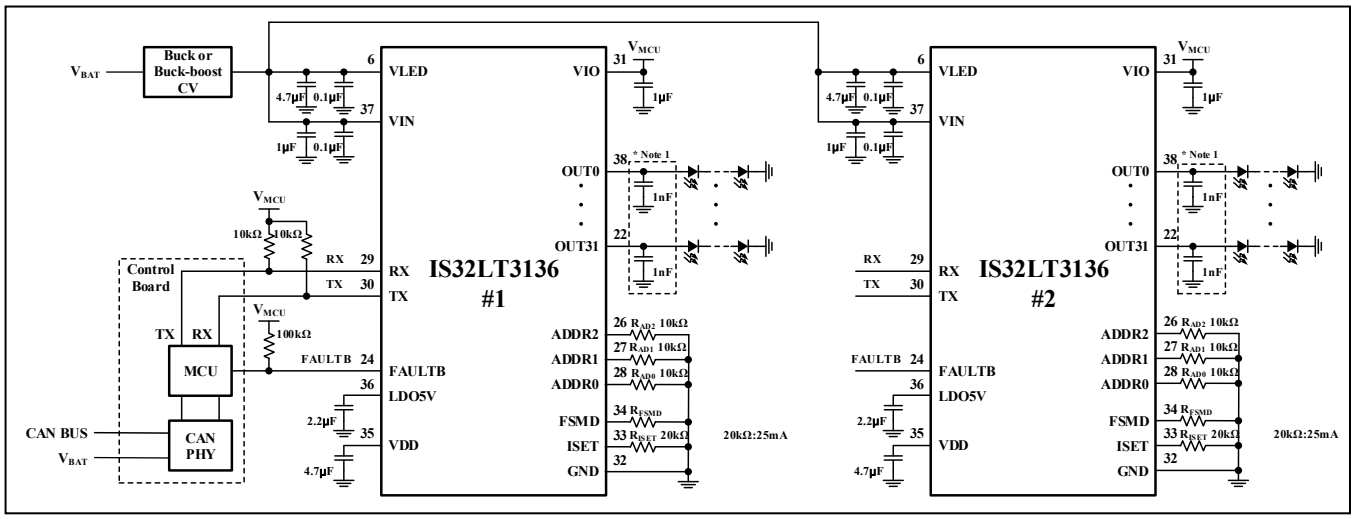


Figure 2 Typical Application Circuit of Multiple IS32LT3136 with UART Interface

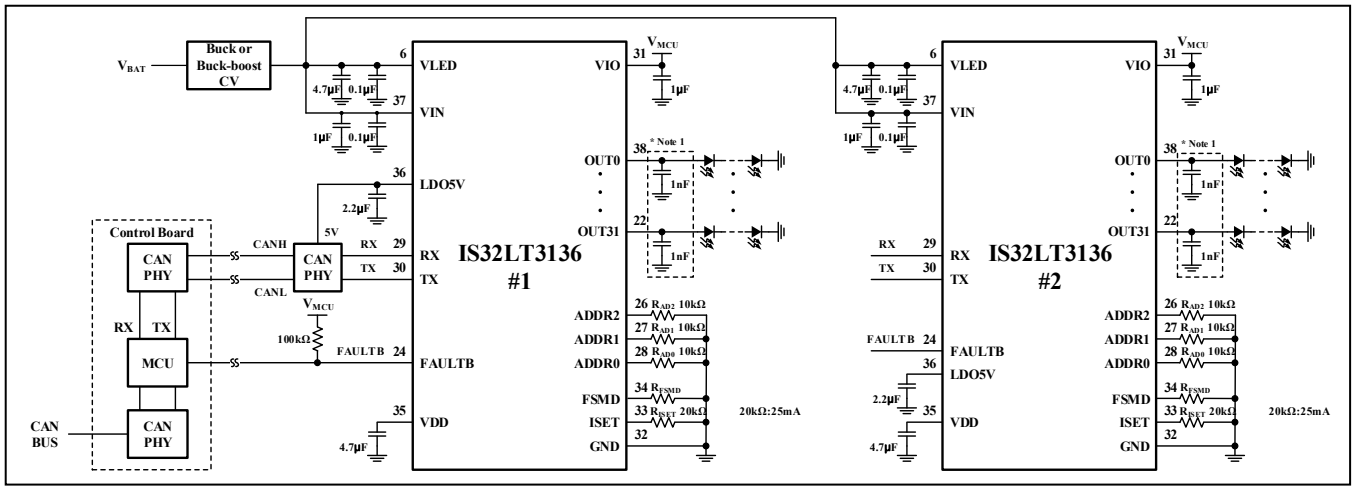
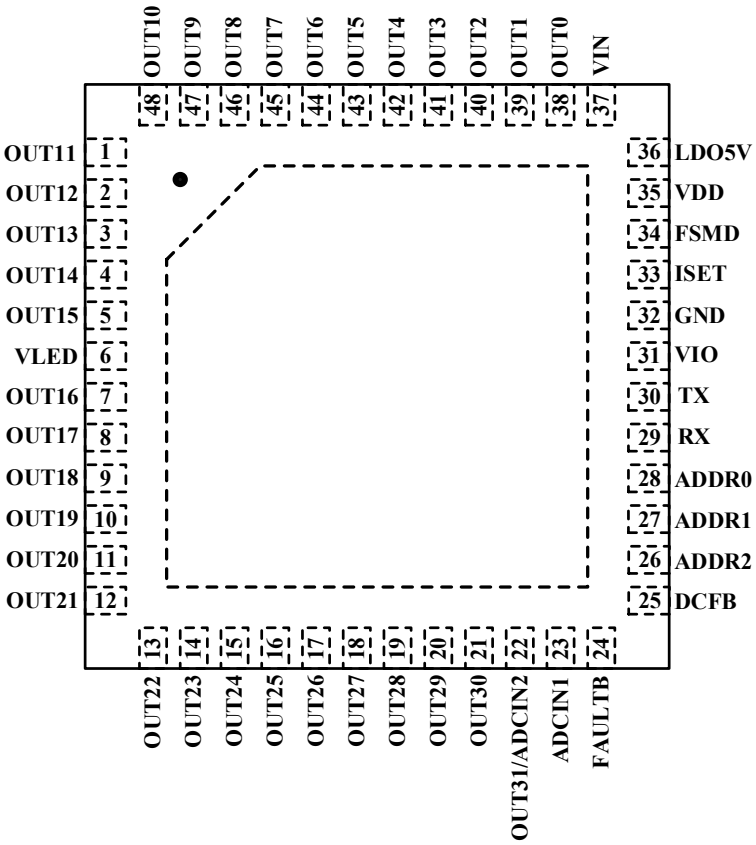


Figure 3 Typical Application Circuit of Multiple IS32LT3136 with External CAN Transceiver for Off-board Long Distance Communication

Note 1: The capacitors C_{OUT0}~C_{OUT31} are recommended for most applications. These capacitors must be placed as close to the corresponding OUTx pin as possible to optimize the EMI and ESD performance, especially the LEDs are connected to OUTx with long wires. The recommended value is 1nF.

6 PIN CONFIGURATION

Package	Pin Configuration (Top View)
QFN-48	

PIN DESCRIPTION

No.	Pin	Description
1~5,7~22,38~48	OUT0~OUT31	Current sink channels.
6	VLED	Power supply for LED.
22	ADCIN2	ADC channel input (Multiplexed pin).
23	ADCIN1	ADC channel input.
24	FAULTB	Open drain fault reporting pin. FAULTB pin is open drain output and requires an external pull-up resistor.
25	DCFB	DC feedback for automatic DCDC VLED adjustment to optimize system power supply.
26~28	ADDR2, ADDR1, ADDR0	Address setting. Connect a resistor from this pin to GND to assign the address.
29	RX	UART interface received data pin.
30	TX	UART interface transmitted data pin.
31	VIO	For TX power supply.
32	GND	Ground.
33	ISET	Input pin used to connect an external resistor to set the global output current.
34	FSMD	Connect resistor to GND to select fail safe mode.
35	VDD	4.2V LDO output. Connect a 4.7μF capacitor to GND.
36	LDO5V	For CAN PHY power supply.
37	VIN	For LDO power supply.
	Thermal Pad	Must be connected to GND. Connect thermal pad to external GND plane on board for better thermal performance.

7 ORDERING INFORMATION

Automotive Range: -40°C to +125°C

Order Part No.	Package	QTY/Reel
IS32LT3136-QFLCA3-TR	QFN-48, Lead-free	2500

8 FUNCTIONAL SAFETY

The development of this product is based on a process according to ISO 26262 which has been certified to be compliant to ISO 26262 requirements and integrity levels up to ASIL-D. Technical safety requirements for this product are rated ASIL-B. In order to achieve the IC target metrics for the appropriate ASIL, it is mandatory to consider the safety mechanisms and recommendations mentioned in the safety manual.

8.1 TECHNICAL SAFETY REQUIREMENTS

Table 1.1-1: Technical Safety Requirements

TSR	Description of Technical Safety Requirements	ASIL
TSR1	The LED channel shall perform PWM duty cycle and output peak current according to a valid control or communication data (TSR1 is derived from FSR1)	ASIL-B
TSR2	**Status and diagnostics information shall be provided (TSR2 is derived from FSR2 and FSR3):** • The IC shall provide function which allow to read back the actual state of the LED output channels • Diagnostic information shall be provided • Output channel cannot be controlled shall be detected and failure indication shall be provided • The IC will enter safe mode if it can't receive the host command	ASIL-B

8.2 SAFE STATE

The Safe State for the IC depends on the particular rear bight function. Due to the fact that there is no allocation of IC channels to particular rear bight functions, it has to be considered that any rear bight function may be allocated to any channel of the IC. For that reason, the IC implements a configurable fall-back concept for each channel, which allows to adapt the Safe State according to the requirements of the particular rear bight function.

8.3 FAULT TOLERANCE TIME INTERIAL

The diagnosis/safety mechanisms implemented in the IC have been specified in such a way that the Fault Detection and Reaction Times FFDT/FRT are compliant to the Fault Tolerant Time Interval requirements, which depend on the particular rear bight function. Due to the fact that there is no allocation of IC channels to particular rear bight functions, it has to be considered that any rear bight function may be allocated to any channel of the IC.

For that reason, the most critical Fault Tolerant Time Interval requirement among all intended rear bight functions, which amounts to 300ms, has been considered.

9 SPECIFICATIONS

9.1 ABSOLUTE MAXIMUM RATINGS

Supply voltage VIN, VLED	-0.3V ~22.0V
Voltage at TX, RX, ADDRx, ISET, FSMD, DCFB	-0.3V ~6V
Voltage at OUT0 to OUT31, FAULTB, ADCIN2, ADCIN1	+22V
Maximum junction temperature, T_{JMAX}	+150°C
Storage temperature range, T_{STG}	-65°C ~+150°C
Operating temperature range, T_A=T_J	-40°C ~ +150°C
Package thermal resistance, junction to ambient (4-layer standard test PCB based on JESD 51-2A), θ_{JA}	36.9°C/W
Package thermal resistance, junction to case (bottom) (4-layer standard test PCB based on JESD 51-14), θ_{JC_BOT}	10.1°C/W
ESD (HBM) ESD (CDM)	±4kV ±750V

Note 2: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

9.2 ELECTRICAL CHARACTERISTICS

"♦" This symbol in the table means these limits are guaranteed at room temp T_J= 25°C.
"◊" This symbol in the table means these limits are guaranteed at full temp range T_J= -40°C~125°C.
V_{IN}= 12V, T_J= -40°C ~125°C, unless otherwise noted. (Note 5)

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
V_{LED}	Power supply voltage			4.5		20	V
V_{IN}	Supply voltage			4.5		20	V
V_{IO}	TX power supply			3		5.5	V
I_{OUT}	Maximum output current	R_{ISET}= 14.4kΩ (24kΩ || 36kΩ), GCC= 0xFF, SCAx= 0xFF, PWM= 0xFFF			35.3		mA
	Output current	R_{ISET}= 33kΩ, GCC= 0xFF, SCAx= 0xFF, PWM= 0xFFF			15.4		mA
ΔI_{MAT}	I_{OUT} mismatch (bit to bit) (Note 3)	I_{OUT}= 3mA	♦	-4		4	%
			◊	-4		4	%
		I_{OUT}= 15mA	♦	-3		3	%
			◊	-3		3	%
ΔI_{OUT}	I_{OUT} accuracy (device to device) (Note 4)	I_{OUT}= 3mA	♦	-4		4	%
			◊	-4		4	%
		I_{OUT}= 15mA	♦	-3		3	%
			◊	-4		4	%
V_{HR}	Headroom voltage	I_{OUT}= 15mA			0.6	0.8	V
I_{CC}	Quiescent power supply current	R_{ISET}= 33kΩ, GCC= 0xFF, SCAx= 0xFF, PWM= 0		6	6.7	7.1	mA
V_{ISET}	ISET voltage	R_{ISET}= 33kΩ, GCC= 0xFF, SCAx= 0xFF, PWM= 0xFFF		1.94	2.0	2.06	V
I_{OZ}	Output leakage current	PWM=SL=GCC=0, V_{LED}= 20V, V_{OUT}= 0V				1	μA
f_{OUT}	PWM frequency of output	Frequency setting= 25.6kHz, 8bit PWM mode		23.81	25.6	27.39	kHz
		Frequency setting= 200Hz, 12bit PWM mode			200		Hz

9.3 ELECTRICAL CHARACTERISTICS (CONTINUE)

"♦" This symbol in the table means these limits are guaranteed at room temp T_J= 25°C.
"◊" This symbol in the table means these limits are guaranteed at full temp range T_J= -40°C~125°C.
V_{IN}= 12V, T_J= -40°C ~125°C, unless otherwise noted. (Note 5)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
T_{SD}	Thermal shutdown			168		°C
T_{SD_HYS}	Thermal shutdown hysteresis			15		°C
V_{PD_FAULTB}	FAULTB pin pull-down capability	I_{SINK}= 2mA		0.1	0.3	V
I_{LKG_FAULTB}	FAULTB pin leakage current	$V_{PULL-UP}$= 20V			2	μA
V_{IH_RX}	Logic "1" input voltage		2			V
V_{IL_RX}	Logic "0" input voltage				0.7	V
$V_{OL(TX)}$	LOW level output voltage	I_{SINK}= 5mA			0.3	V
$V_{OH(TX)}$	High level output voltage	I_{SOURCE}= 5mA	V_{IO}-0.3		V_{IO}	V
$V_{TH1\_AD/FS}$	ADDR0/ADDR1/ADDR2/FSMD threshold1		0.9	1	1.1	V
$V_{TH2\_AD/FS}$	ADDR0/ADDR1/ADDR2/FSMD threshold2		1.85	2	2.15	V
$V_{TH3\_AD/FS}$	ADDR0/ADDR1/ADDR2/FSMD threshold3		2.8	3	3.2	V
$I_{AD/FS}$	ADDR/FS source current		46	50	54	μA
V_{SC_FL}	LED string short detection falling threshold	Measured at OUTx to GND, SHORT_FLT(89h~8Ch) = "000"	0.6	0.8		V
V_{SC_RS}	LED string short detection rising threshold	Measured at OUTx to GND, SHORT_FLT(89h~8Ch) = "000"		1.0	1.2	V
V_{OC_FL}	LED string open detection falling threshold	Measured at (V_{LED}-V_{OUTx})	60	200		mV
V_{OC_RS}	LED string open detection rising threshold	Measured at (V_{LED}-V_{OUTx})		250	350	mV
V_{DD}	VDD output voltage		4.08	4.2	4.32	V
I_{DD_MAX} (Note 6)	VDD output current capability	V_{IN}> 4.5V, V_{DD}> 3.8V			50	mA
I_{DD_LIM}	VDD output current limit	V_{IN}= 12V, V_{DD}= 0V	60			mA
V_{DD_UV}	VDD undervoltage-lockout threshold	Voltage falling, IC disabled		3.6		V
V_{DD_UVHY}	VDD undervoltage-lockout hysteresis			100		mV
V_{LDO}	LDO5V output voltage		4.85	5	5.15	V

9.4 ELECTRICAL CHARACTERISTICS (CONTINUE)

"♦" This symbol in the table means these limits are guaranteed at room temp T_J= 25°C.
"◊" This symbol in the table means these limits are guaranteed at full temp range T_J= -40°C~125°C.
V_{IN}= 12V, T_J= -40°C ~125°C, unless otherwise noted. (Note 5)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{LDO_MAX}	LDO5V output current capability	V_{IN}> 5.5V， V_{LDO}> 4.65V			100	mA
I_{LDO_LIM}	LDO5V output current limit	V_{IN}= 12V, V_{LDO5V}= 0V	100			mA
V_{LDO_UV}	LDO5V undervoltage-lockout threshold	Voltage falling, IC disabled		4		V
V_{LDO_UVHY}	LDO5V undervoltage-lockout hysteresis			200		mV
V_{SLSTH}	Single LED short detect threshold	SLSTH (66h~85h) = "000101"	3.6	3.8	4	V
V_{F_UVLO}	Single LED short/String open detect UVLO	FS_FLTL (86h) = "00000100"	7.3	7.8	8.3	V
V_{IN_UV}	VIN undervoltage-lockout threshold	Voltage falling, IC disable	3.3	3.6	3.8	V
V_{IN_UVHY}	VIN undervoltage-lockout hysteresis			150		mV
V_{LED_UV}	VLED undervoltage-lockout threshold	Voltage falling, VLUF=1 (99h)	2.95	3.2	3.65	V
V_{LED_UVHY}	VLED undervoltage-lockout hysteresis			400		mV
f_{OSC}	System clock frequency		62.72	64	65.28	MHz
ADC (10-bit)						
V_{REFADC}	Reference voltage		2.43	2.5	2.57	V
DNL	Differential nonlinearity	(Note 7)	-5		+5	LSB
INL	Integral nonlinearity	(Note 7)	-8		+8	LSB
RESADC	Quantization steps			1024		LSB
ADCERR	Quantification error		-0.5		+0.5	LSB
t_{CONV}	Min. conversion Time	For max. ADC input frequency = 1MHz (Note 7)		25		μs

Note 3: I_{OUT} mismatch (bit to bit) $\triangle I_{MAT}$ is calculated:

$$\Delta I_{MAT} = MAX\left(ABS\left(\frac{I_{OUTn}(n=1\sim32)}{\frac{I_{OUT1}+I_{OUT2}+\cdots+I_{OUT32}}{32}} - 1 \right) \right) \times 100\%$$

Note 4: I_{OUT} accuracy (device to device) $\triangle I_{OUT}$ is calculated:

$$\Delta I_{OUT} = ABS\left(\frac{\frac{I_{OUT1}+I_{OUT2}+\cdots+I_{OUT32}}{32} - I_{OUT(TYP)}}{I_{OUT(TYP)}} \right) \times 100\%$$

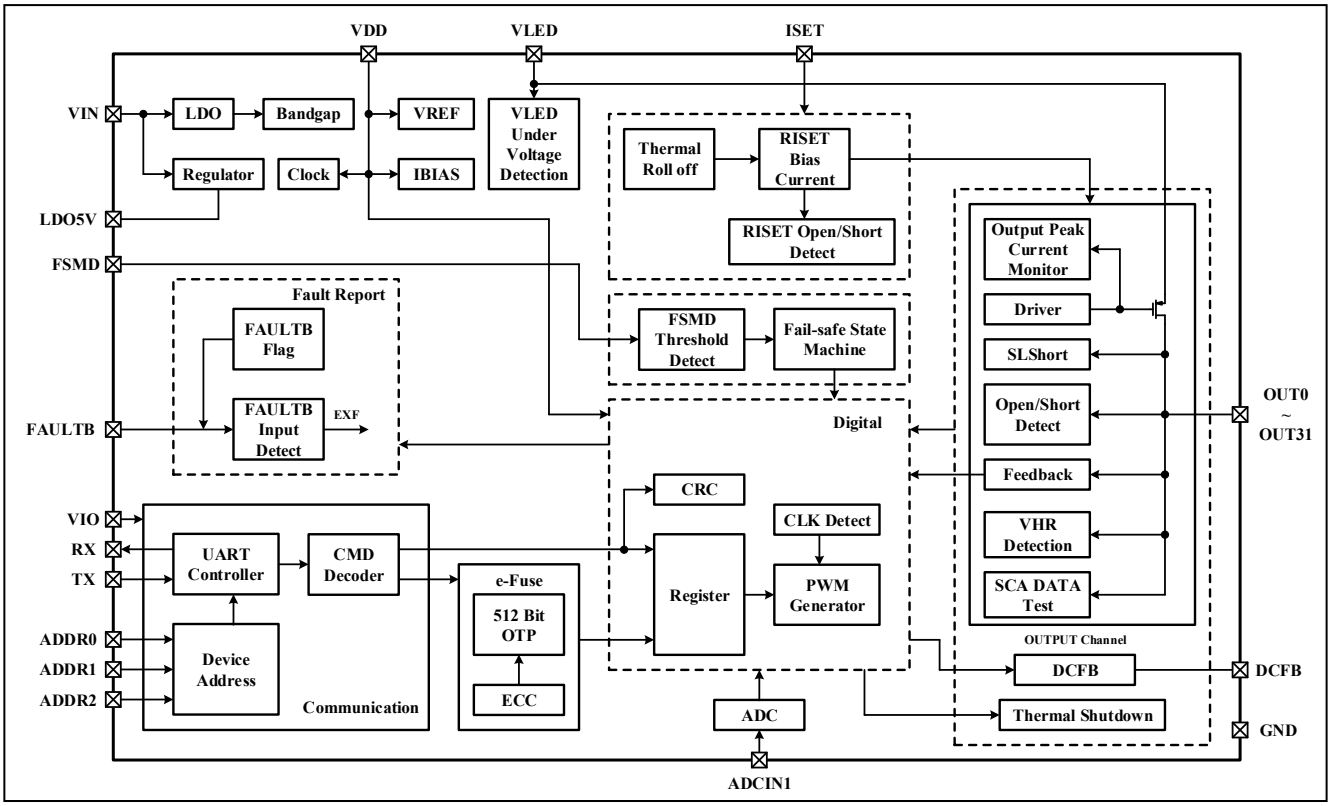
When R_{ISET}= 14.4kΩ, $I_{OUT(TYP)}$ = 35.3mA; and when R_{ISET}= 33kΩ, $I_{OUT(TYP)}$ = 15.4mA.

Note 5: Limits are 100% production tested at 25ºC. Limits over the operating temperature range verified through either bench and/or tester testing and correlation using statistical methods.

Note 6: For internal use only, external loads are prohibited.

Note 7: Guaranteed by design.

10 FUNCTIONAL BLOCK DIAGRAM



11 APPLICATION INFORMATION

11.1 OVERVIEW

The IS32LT3136 is a linear programmable current regulator consisting of 32 output channels capable of up to 35mA each. UART communication interface compatible with CANFD PHY is used for output control by a master microcontroller or ECU. Each output can individually support 65536 steps PWM dimming and 256 steps DC current adjustment. The outputs can be combined to provide higher current drive capability to max 1.12A.

For added system reliability, the IS32LT3136 features various fault protections, including LED string open/short, single LED short, overcurrent (ISET shorted), ISET pin opened, PWM duty verification fail, SCA verification fail, Thermal Rolloff, Thermal shutdown, external (One Fail All Fail modes), CRC error and watchdog 1 or watchdog 2 timeout (fail-safe modes) conditions for robust operation. Detection of these failures is reported by a dedicated reporting pin, FAULTB. There are also dedicated flag bits in registers for each failure which can be read back by the external host MCU through the interfaces. To optimize EMI performance, the IS32LT3136 features spread spectrum on the internal PWM base clock to spread the total electromagnetic emitting energy into a wider range that significantly degrades the peak energy of EMI. In addition, the output current source ON/OFF transitions during PWM dimming have a slew rate control and programmable phase delay to mitigate EMI and power supply inrush current.

The IS32LT3136 interface is UART, and it supports up to 64 slave IS32LT3136 devices. The device address can be configured by the three address pins. The UART receives data to control all output channels and sends back fault information to the host MCU. The UART interface in conjunction with an external standard CAN transceiver enables long distance communication with a host MCU placed outside of the lamp module (as shown in Figure 4). Based on the CAN physical layer, it achieves excellent EMC and EMI performance. The embedded CRC correction of the UART data stream can ensure robust communication in automotive environments. The UART interface is easily supported by most MCUs in the market.

To further increase robustness, the fail-safe mode of the device allows automatic switching to fail-safe state in case of the communication loss, for example, host MCU failure or communication cables broken. The device supports different fail-safe modes configured by the FSMD pin.

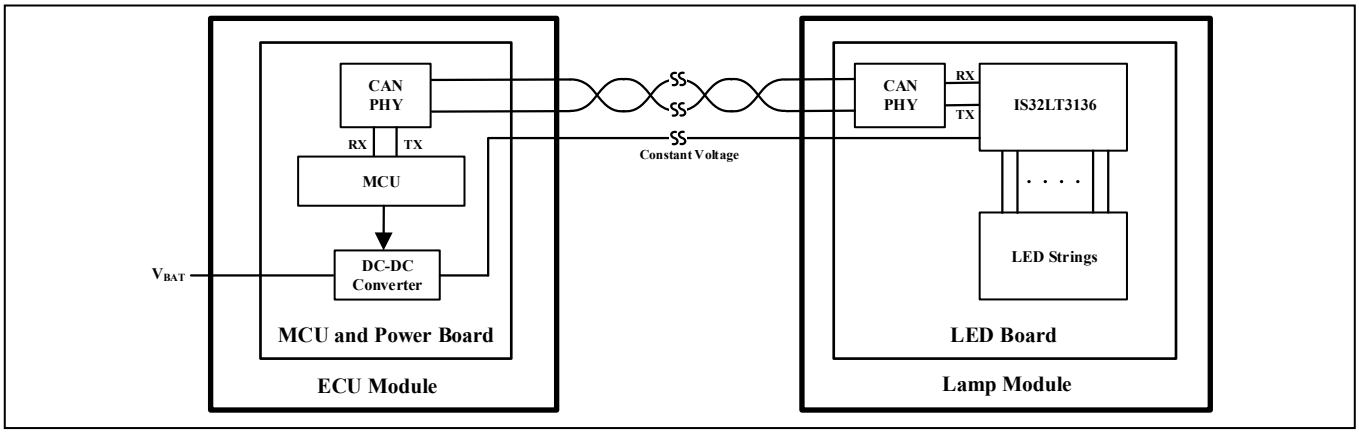


Figure 4 UART Interface with External CAN Transceiver for Outside Module Long Distance Communication

11.2 POWER SUPPLY

11.2.1 VIN UNDERVOLTAGE-LOCKOUT (UVLO)

The IS32LT3136 features an undervoltage-lockout (UVLO) function on the VIN pin to prevent unintended operation at too low supply voltages. UVLO threshold is an internally fixed value and cannot be adjusted. Entering UVLO will reset all registers to their default value. The device is disabled when the VIN voltage drops below V_{VIN_UV} and automatically resumes normal operation when the VIN voltage rises above (V_{VIN_UV}+ V_{VIN_UVHY}).

11.2.2 VLED UNDERVOLTAGE

IS32LT3136 does not have undervoltage locking function on the VLED pin. If its voltage is too low, it will cause the FAULTRAB pin to pull low and report an error.

11.2.3 INTERNAL 4.2V LINEAR REGULATOR (VDD)

The IS32LT3136 device integrates an internal linear regulator (VDD) with 4.2V (Typ.) and I_{DD_MAX} current capability

to provide power supply to the digital circuits. During operation, the internal circuitry can be subject to transient currents from this linear regulator. Therefore, a 4.7μF low ESR, X7R type ceramic capacitor is necessary from VDD pin to GND, it must be placed as close to the VDD pin as possible. This linear regulator also has the UVLO feature. The device is disabled when the V_{DD} voltage drops below V_{DD_UV} and resumes normal operation when the VDD voltage rises above (V_{DD_UV}). Entering UVLO will reset all registers to their default value. An I_{DD_LIM} current limit on VDD pin protects the IS32LT3136 from VDD output overload or short-circuit conditions.

11.2.4 INTERNAL 5V LINEAR REGULATOR (LDO5V)

The IS32LT3136 device integrates an internal linear regulator (LDO5V) with 5V (Typ.) and I_{LDO_MAX} current capability to provide power supply to the internal analog circuits. During operation, the internal circuitry can be subject to transient currents from this linear regulator. Therefore, a 2.2μF low ESR, X7R type ceramic capacitor is necessary from LDO5V pin to GND, it must be placed as close to the LDO5V pin as possible. An I_{LDO_LIM} current limit on VLDO5V pin protects the IS32LT3136 from VLDO5V output overload or short-circuit conditions.

11.2.5 VIO VOLTAGE SUPPLY

The positive voltage rail of the UART interface is supplied with the VIO pin which must be connected to a proper voltage source. Usually, the VIO pin should be connected to the same power supply as the MCU. If a 5V MCU is used for IS32LT3136 control, the VIO pin can be directly connected to the LDO5V pin.

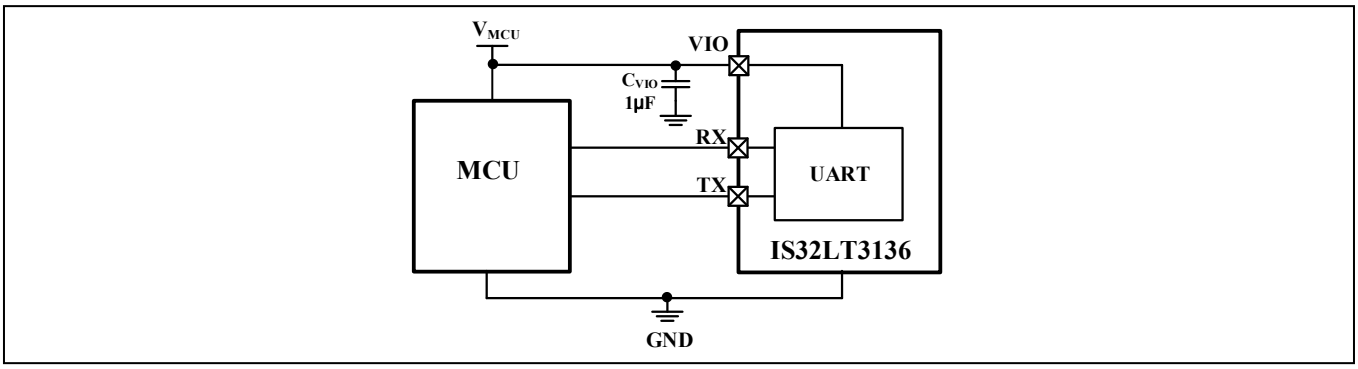


Figure 5 VIO Voltage Supply

11.3 OUTPUT CURRENT SETTING

The full DC output current (I_{OUT_FU}) for each channel is set with resistor (R_{ISET}) connected from the ISET pin to GND. This current set resistor is computed using the following equation:

Where V_{ISET} is the voltage of ISET pin, is 2V (Typ.),

$$I_{OUT\_FU} = \frac{V_{ISET}}{R_{ISET}} \times \frac{255X255}{256} \qquad (1)$$

(12kΩ ≤ R_{ISET} ≤ 100kΩ)

It is recommended that R_{ISET} be a 1% accuracy resistor with good temperature characteristic to ensure stable output current. R_{ISET} must be placed as close to ISET pin as possible on PCB layout to avoid noise interference and ground bounce. The device is protected from an output overcurrent condition caused by R_{ISET} resistor. The output current is reduced to 5mA (Typ.) if the ISET pin is shorted to ground or R_{ISET} resistor value is too low.

When R_{ISET} is fixed, the DC output current for each channel can be further adjusted in 256-steps by the GCC[7:0] bits in the GC_CTRL register (05h). Furthermore, based on the GCC[7:0] setting, each channel also supports individual 256-step programmable DC output current adjustment. This feature can be used to set binning values for output LEDs or to calibrate the LEDs to achieve high brightness homogeneity based on an external visual calibration system to further save binning cost. The 8-bit Scaling Registers SCAx (06h~25h) individually set the DC output current of each channel.

GCC[7:0] and SCAx control the OUTx current (I_{OUTx}) as shown in following equation:

$$I_{OUTx} = I_{OUT\_FU} \times \frac{GCC}{255} \times \frac{SCAx}{255} \qquad (2)$$

Where, x is from 1 to 32 for different output channels.

$$GCC = \sum_{n=0}^{7} D[n] \cdot 2^n \qquad (3)$$

$$SCAx = \sum_{n=0}^{7} D[n] \cdot 2^n \qquad (4)$$

For example: assume GCC[7:0] = 0x05 and SCA1 = 0x40. GCC = 5. Then the DC output current of OUT1 is:

$$I_{OUT1} = I_{OUT\_FU} \times \frac{5}{255} \times \frac{64}{255} \qquad (5)$$

If any channel(s) are unused, please connect the corresponding OUTx pin(s) to the GND pin to avoid false fault detection and set the corresponding PWM and scaling registers to “0x00” to turn off these output(s).

11.4 PWM DIMMING

The IS32LT3136 integrates independent 12-bit PWM generators for each output channel. The output current for each channel is turned on and off as controlled by the PWM generator. The average current of each output channel can be adjusted by its PWM duty cycle to control the LED channel brightness. The PWM Registers (26h~65h) individually set the PWM duty cycle for each channel.

The PWM dimming frequency is programmable by the CONFIG1 register (00h). The maximum PWM frequency can be up to 25.6kHz (Typ.). Due to the output current slew rate control, a high frequency PWM signal has a shorter period time that will degrade the PWM dimming linearity. Therefore, a low frequency PWM signal is good for achieving better dimming contrast ratio. Select the PWM dimming frequency based on the minimum brightness requirement for the application.

The PWM generators dim the LEDs by their duty cycle:

$$I_{OUTx\_PWM} = I_{OUTx} \times D_{PWMx} \qquad (6)$$

Where, D_{PWMx} is duty cycle of each channel independently programmed by PWM Registers (26h~65h), in 12bit or 7+5-bit PWM mode:

$$D_{PWMx} = \frac{\sum_{n=0}^{11} D[n] \cdot 2^n}{4096} \qquad (7)$$

In 8bit PWM mode:

$$D_{PWMx} = \frac{\sum_{n=4}^{11} D[n] \cdot 2^n}{256} \qquad (8)$$

11.4.1 PWM SPREAD SPECTRUM

The IS32LT3136 includes a spread spectrum feature on PWM base clock to optimize EMI performance. The spread spectrum function helps spread the total electromagnetic emitting energy into a wider range that significantly degrades the peak energy of EMI. With spread spectrum, the EMI test can be passed with smaller size and lower cost filter circuit. Spread spectrum is enabled/disabled by the CONFIG3 register (02h).

11.4.2 PWMPHASEDELAY

To mitigate transient current generation and power supply ripple, the IS32LT3136 features PWM phase delay. When PWM phase delay is disabled (PDE (00h) is set to “0”, default value is “1” phase delay enable), all channels are simultaneously turned on at the beginning of each PWM cycle. This will result in large current draw from power supply leading to high voltage ripple on the power supply rail. As shown in figure 4.

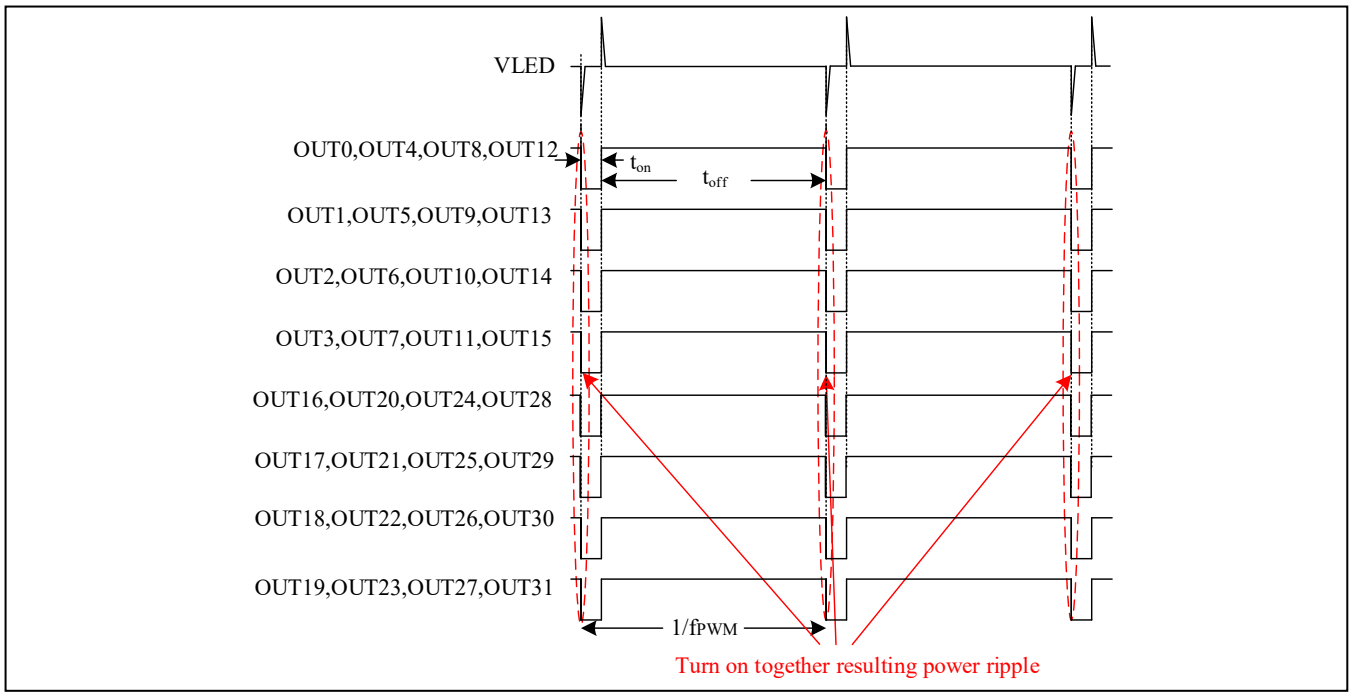


Figure 6 PWM Phase Delay Disabled

11.4.3 OUT FIXED DELAY

The IS32LT3136 divides 32 output channels into 4 groups to perform PWM delay, OUT0~OUT7 as group 1, OUT16~OUT23 as group 2, OUT8~OUT15 as group 3. OUT24~OUT31 as group 4. Delay a PWM CLK between each OUT within each group. Group 1 and Group 3 have a delay of half PWN CLK relative to Group 2 and Group 4. As shown in figure 7.

For example:

Condition1: 8 bit 25.6kHz.

1PWM CLK =1/25.6kHz/256=152ns.

0.5 PWM CLK =76.1ns.

Condition2: 12 bit400Hz.

1 PWM CLK =1/400Hz/4096=610ns.

0.5 PWM CLK =305ns.

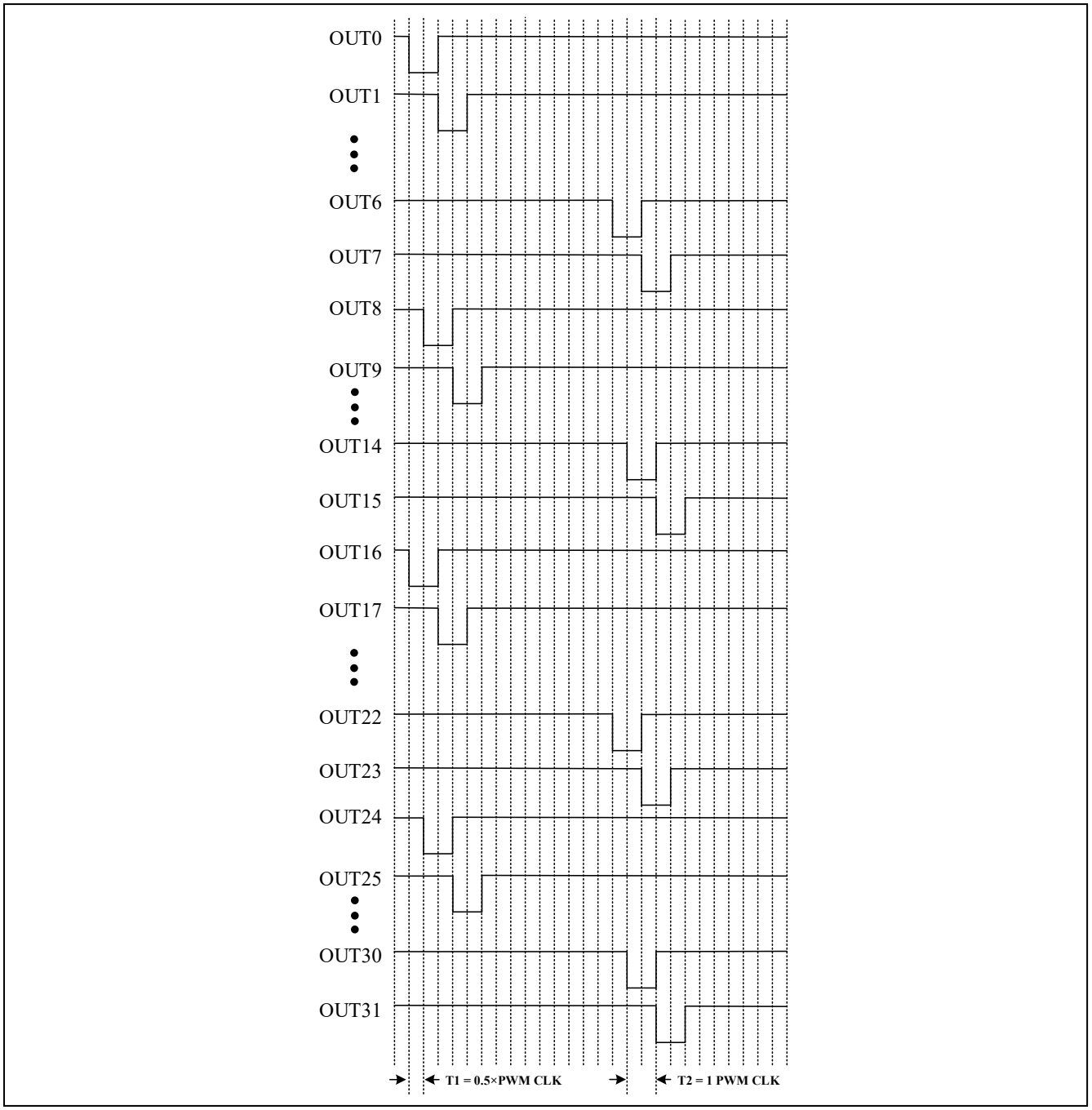


Figure 7 Channel Delay

The IS32LT3136 divides 32 output channels into 8 groups to perform PWM phase delay, OUT0&OUT4&OUT8&OUT12 as group 1, OUT1&OUT5&OUT9&OUT13 as group 2, …OUT19&OUT23&OUT27&OUT31 as group 8. When the PDE bit in the CONFIG1 register (00h) is set to "1", the phase delay is enabled, starting each group in turn from each PWM cycle. The t_{DELAY_1} is interval delay time between group n& group n+1, and t_{DELAY_1} is 1/8 PWM cycle ($1/f_{PWM}$). This minimizes the voltage ripple on the VLED power supply rail. As shown in figure 8.

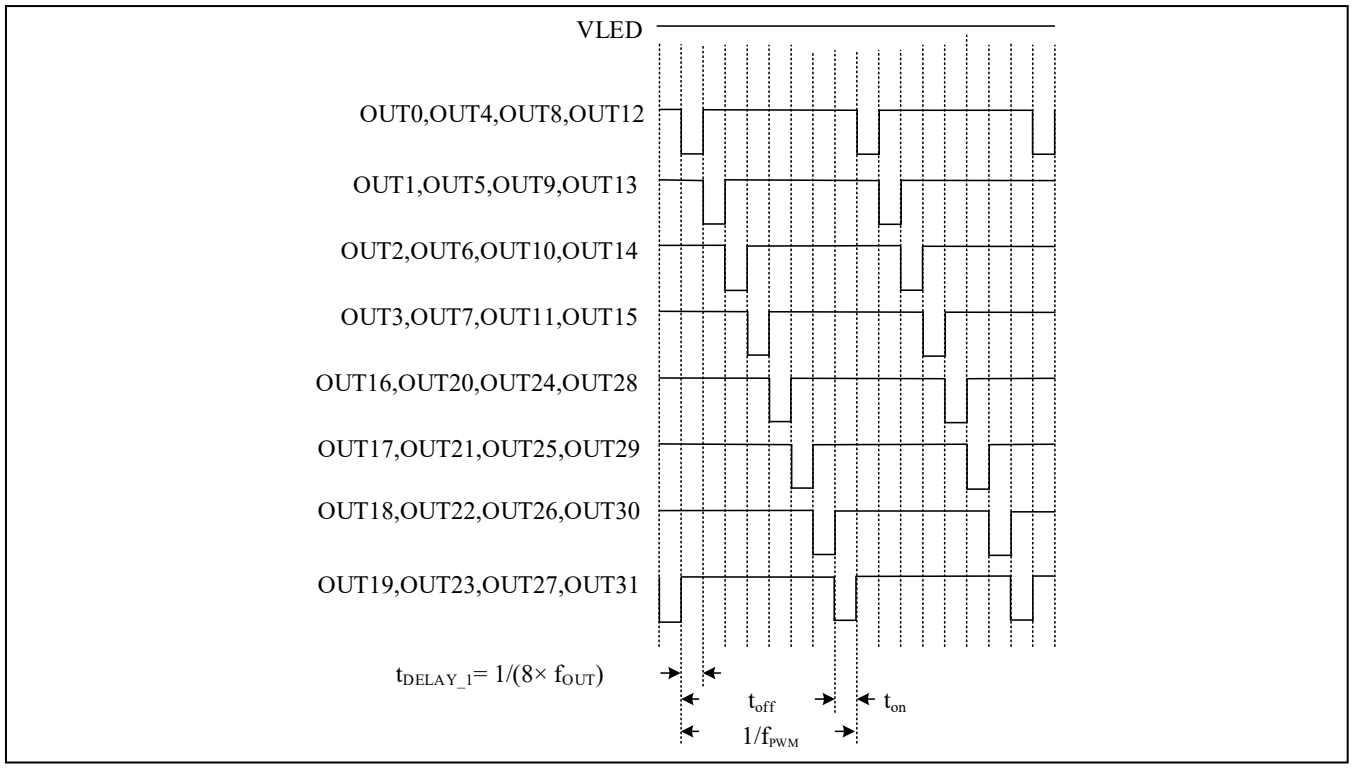


Figure 8 PWM Phase Delay Enabled

11.5 FAULT PROTECTION

11.5.1 FAULT REPORTING

For added system reliability, the IS32LT3136 integrates various fault detections for LED string open/short, single LED short, overcurrent (ISET shorted), ISET pin opened, PWM duty verification fail, SCA verification fail, Thermal Rolloff, Thermal shutdown, external (One Fail All Fail modes), CRC error and watchdog 1 or watchdog 2 timeout (fail-safe modes) conditions. The open drain pin FAULTB can be used for fault condition reporting. If any fault occurs, the corresponding bit in FLT_TYPE(97h,98h,99h) register will be set to “1” and the FAULTB pin will go low after a delay time (programmed by FT[3:0] bits in FLT_CONFIG register) to report fault condition. When it’s monitored by a host MCU, a pull-up resistor RFPU (10kΩ recommended) from the FAULTB pin to the supply of the host MCU is required.

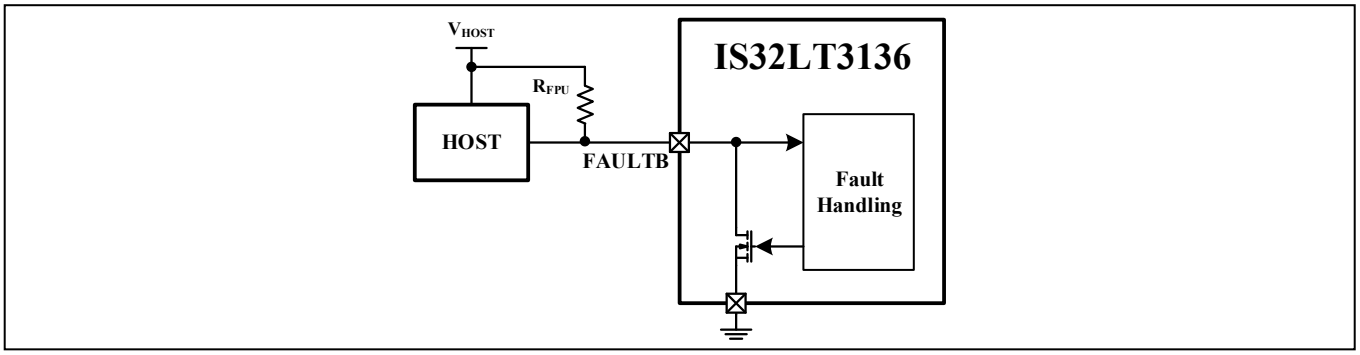


Figure 9 Host Monitors the Fault Reporting

11.5.2 LED STRING OPEN PROTECTION

The LED string open detection is enabled by setting the ODE and ODF bits in FLT_DET_EN register (87h) to “1”. If any LED string is opened, the corresponding OUTx pin voltage will be pulled up close to VLED. When the voltage (V_{LED}-V_{OUTx}) falls below the LED string open detection voltage, VOC_FL and persists for longer than a deglitch time (typical 10μs), the LED string open protection will be triggered. The corresponding fault flag bits in OPEN_FLT register (8Dh,8Eh,8Fh,90h) and the OPENF bit in FAULT_TYPE_2 register (98h) will be set to “1”. The FAULTB pin will go low after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) to report the fault condition.

The faulty channel will reserve a 4mA retry current for recovery detection.

No matter in which fault protection mode, the device will recover to normal operation and the FAULTB pin will go back to high impedance after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) expires once the open condition is removed, i.e. V_{LED}-V_{OUTx} rising above the LED string open detection voltage, VOC_RS. The corresponding fault flag bit in OPEN_FLT register will reset to “0”. However, the OPENF bit in FAULT_TYPE_2 register (98h) is latched, which means that it cannot automatically reset to “0” after open condition being removed but must be cleared by the host MCU writing it back to “0”.

When PWM dimming is implemented, the LED string open detection is only enabled during the PWM ON phase. If the PWM on-time is less than the deglitch time (typical 10μs), the device does not report any LED string open fault.

11.5.3 LED STRING SHORT PROTECTION

The LED string short detection is enabled by setting the SDE and SDF bits in FLT_DET_EN register (87h) to “1”. If any LED string is short, the corresponding OUTx pin will be pulled down close to GND. When dropout voltage from the OUTx pin, VOUTx, falls below the LED string short detection voltage, VSC_FL, and persists for longer than a deglitch time (typical 10μs), the LED string short protection will be triggered. The corresponding fault flag bits in SHORT_FLT register (89h,8Ah,8Bh,8Ch) and the SHORTF bit in FAULT_TYPE_2 register (98h) will be set to “1”. The FAULTB pin will go low after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) to report the fault condition. The faulty channel will reserve a 4mA retry current for recovery detection.

No matter in which fault protection mode, the device recovers to normal operation and the FAULTB pin will go back to high impedance after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) once the short condition is removed, VOUTx rising above the LED string short detection voltage, VSC_RS. The corresponding fault flag bit in SHORT_FLT register will reset to “0”. However, the SHORTF bit in FAULT_TYPE_2 register (98h) is latched, which means that it cannot automatically reset to “0” after short condition being removed but must be cleared by the host MCU writing it back to “0”.

When PWM dimming is implemented, the LED string short detection is only enabled during PWM ON phase. If the PWM on-time is less than the deglitch time (typical 10μs), the device does not report any LED string short fault.

When the device is operated in DC mode, the PWM function is disabled. It is recommended to not enable both LED string short and single LED short, because the IS32LT3136 may incorrectly report an LED string short as a single LED short. Individually enable either LED string short or single LED short detection. If a single LED short is reported, double check for LED string short or single LED short in software.

11.5.4 SINGLE LED SHORT PROTECTION

The single LED short detection is enabled by setting the SLSDE and SLSDF bits in FLT_DET_EN register (87h) to “1”. Then the single LED short detection is active after VLED voltage rising above the fault undervoltage-lockout voltage threshold FLT_UV. That helps to prevent false fault detection due to the insufficient power supply voltage, such as power up transience. The single LED short detect threshold V_{SLSTH} of each channel is individually programmed by the corresponding LEDx_SLS[5:0] bits in LEDx_SLSTH registers (66h~85h). If single LED of any string is shorted, the corresponding OUTx pin voltage will fall. When the OUTx pin voltage, VOUTx, fall below single LED short detect threshold, V_{SLSTH}, and persists for longer than a deglitch time (typical 10μs), the single LED short protection will be triggered.

The device recovers to normal operation and the FAULTB pin will go back to high impedance after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) once the single LED short condition is removed, VOUTx rising above the LED string short detection voltage, V_{SLSTH}. The corresponding fault flag bit in SLS_FLT(91h,92h,93h,94h) register will reset to “0”. However, the SLSHORTF bit in FAULT_TYPE_2 register (98h) is latched, which means that it cannot automatically reset to “0” after single LED short condition being removed but must be cleared by the host MCU writing it back to “0”.

When PWM dimming is implemented, the single LED string short detection is only enabled during PWM ON phase. If the PWM on-time is less than the deglitch time (typical 10μs), the device does not report any single LED short fault.

11.5.5 OUTPUT OVERCURRENT (ISET PIN SHORT)

The device is protected from an output overcurrent condition caused by the R_{ISET} resistor. All output current is limited to 45mA (Typ.) in case of the ISET pin shorted to ground or too low value R_{ISET} resistor is connected to ISET pin. If the condition persists for longer than a deglitch time (typical 1μs), the ISET pin short protection will be triggered. All output current will be reduced to 5mA (Typ.). If the RSET_SHE bit in FAULT_EN_1 register (95h) is set to 1, the RSET_SH bit in FAULT_TYPE_1 register (97h) will be set to "1" and the FAULTB pin will go low after the delay

time (programmed by FT[3:0] bits in FLT_CONFIG register) to report the fault condition.

Once the resistance from the ISET pin to GND resumes to a normal range, all channels will recover to normal operation and the FAULTB pin will recover to high impedance after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register). However, the RSET_SH bit in FAULT_TYP_1 register (97h) is latched, which means that it cannot automatically reset to “0” after ISET short condition being removed but must be cleared by the host MCU writing it back to “0”.

11.5.6 ISET PIN OPEN

In case of the ISET pin open or too High value R_{ISET} resistor is connected to ISET pin. If the condition persists for longer than a deglitch time (typical 1μs), the ISET pin open protection will be triggered. If the RSET_OPE bit in FAULT_EN_1 register (95h) is set to 1, the RSET_OP bit in FAULT_TYPE_1 register (97h) will be set to "1" and the FAULTB pin will go low after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) to report the fault condition.

Once the resistance from the ISET pin to GND resumes to a normal range, all channels will recover to normal operation and the FAULTB pin will recover to high impedance after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register). However, the RSET_OP bit in FAULT_TYP_1 register (97h) is latched, which means that it cannot automatically reset to “0” after ISET open condition being removed but must be cleared by the host MCU writing it back to “0”.

11.5.7 VDD OVERVOLTAGE

VDD overvoltage detection is enabled by opening the VOFE bit in the FAULT_EN_2 register (96h) to "1".If the external power supply is connected to the VDD pin, the external power supply voltage is too high (typical 5.6V) and persists for longer than a deglitch time(typical 10μs), the VOF bit in FAULT_TYPE_3 register (99h) will be set to "1" and the FAULTB pin will go low after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) to report the fault condition.

Once the VDD pin voltage returns to the normal range, the FAULTB pin will recover to high impedance after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register). However, the VOF bit in FAULT_TYP_3 register (99h) is latched, which means that it cannot automatically reset to “0” after VDD pin overvoltage condition being removed but must be cleared by the host MCU writing it back to “0”.

11.5.8 LDO5V UNDERVOLTAGE

LDO5V undervoltage detection is enabled by opening the LUFE bit in the FAULT_EN_2 register (96h) to "1".If the VIN power supply voltage is too low (typical 3.8V) and persists for longer than a deglitch time(typical 10μs), the LUF bit in FAULT_TYPE_3 register (99h) will be set to "1" and the FAULTB pin will go low after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) to report the fault condition.

Once the VIN voltage returns to the normal range, the FAULTB pin will recover to high impedance after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register). However, the LUF bit in FAULT_TYP_3 register (99h) is latched, which means that it cannot automatically reset to “0” after VDD pin overvoltage condition being removed but must be cleared by the host MCU writing it back to “0”.

11.5.9 VLED UNDERVOLTAGE

VLED undervoltage detection is enabled by opening the VLUFE bit in the FAULT_EN_2 register (96h) to "1".If the VLED power supply voltage is too low (typical 3.6V) and persists for longer than a deglitch time(typical 10μs), the VLUF bit in FAULT_TYPE_3 register (99h) will be set to "1" and the FAULTB pin will go low after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) to report the fault condition.

Once the VLED voltage returns to the normal range, the FAULTB pin will recover to high impedance after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register). However, the VLUF bit in FAULT_TYP_3 register (99h) is latched, which means that it cannot automatically reset to “0” after VLED pin overvoltage condition being removed but must be cleared by the host MCU writing it back to “0”.

11.5.10 EXTERNAL FAULT

External fault is to achieve the One Fail All Fail function, multiple IS32LT3136 applications by connecting the FAULTB pins of each IS32LT3136 in parallel, And set the OFA[1:0] bit of CONFIG2 register (01h) to One Fail All Fail, When FAULTB pins are pulled down externally persists for longer than a deglitch time, the EXF bit in FAULT_TYPE_2 register (98h) will be set to "1".

FAULT_TYP_2 register (98h) is latched, which means that it cannot automatically reset to “0” after External fault condition being removed but must be cleared by the host MCU writing it back to “0”.

11.5.11 SCA VERIFICATION

SCA verification fault is enabled by opening the SCAF_EN bit in the FAULT_EN_1 register (95h) to "1". Any output occurs SCA verification failure, the SCAVF bit in FAULT_TYPE_2 register (98h) will be set to "1" and the FAULTB pin will go low after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) to report the fault condition.

FAULT_TYP_2 register (98h) is latched, which means that it cannot automatically reset to “0” Even if Disabled SCA verification function but must be cleared by the host MCU writing it back to “0”.

11.5.12 PWM DUTY VERIFICATION

PWM duty verification fault is enabled by opening the DUTYF_EN bit in the FAULT_EN_1 register (95h) to "1". Any output occurs loopback verification failure, the LPBF bit in FAULT_TYPE_2 register (98h) will be set to "1" and the FAULTB pin will go low after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) to report the fault condition.

FAULT_TYP_2 register (98h) is latched, must be cleared by the host MCU writing it back to “0”, For the LPBF bit, the MODE[1:0] bit of the VFYCTL register (DFh) must be set to 00(Disabled LBT) to clear the LPBF bit of the FAULT_TYP_2 register (98h).

11.5.13 THERMAL SHUTDOWN

If the junction temperature exceeds TSD (Typ. 168˚C), all output channels will go to the OFF state and the TSD bit in FAULT_TYPE_1 register (97h) will be set to “1”. If the TSDE bit in FAULT_EN_1 register (95h) to “1”, the FAULTB pin will go low after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) to report the fault condition. At this point, the device presumably begins to cool off. Any attempt to toggle the channels back to the source condition before the device has cooled to below (T_{SD}-T_{SD_HYS}) (Typ. 155˚C) will be blocked and the device will not be allowed to restart. The FAULTB pin will recover to high impedance after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) once the device cools down. However, the TSD bit in FAULT_TYPE_1 register (97h) is latched, which means that it cannot automatically reset to “0” but must be cleared by the host MCU writing it back to “0”.

11.5.14 THERMAL ROLL-OFF PROTECTION

The device integrates the thermal shutdown protection to prevent the device from overheating. In addition, to prevent the LEDs from flickering due to rapid thermal changes, the device also includes a programmable thermal roll-off feature to reduce power dissipation at high junction temperature.

The output current will be equal to the set value I_{OUTx} if the junction temperature of the device remains below thermal roll-off temperature threshold 140˚C. If the junction temperature exceeds the temperature threshold, the output current of all channels will begin to linearly reduce following the junction temperature ramping up until thermal shutdown. The TF bit in FAULT_TYPE_1 register (97h) will be set to “1”. If the TFE bit in FAULT_EN_1 register (95h) to “1”, the FAULTB pin will go low after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) to report the fault condition. The percentage of the output current before thermal shutdown is programmable by the TROF[2:0] bits in the CONFIG2 register (01h).

The output current will linearly resume to the set value I_{OUTx} and the FAULTB pin will recover to high impedance after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) once the junction temperature cools down below the thermal roll-off temperature threshold 140˚C. However, the TF bit in FAULT_TYPE_1 register (97h) is latched, which means that it cannot automatically reset to “0” but must be cleared by the host MCU writing it back to “0”.

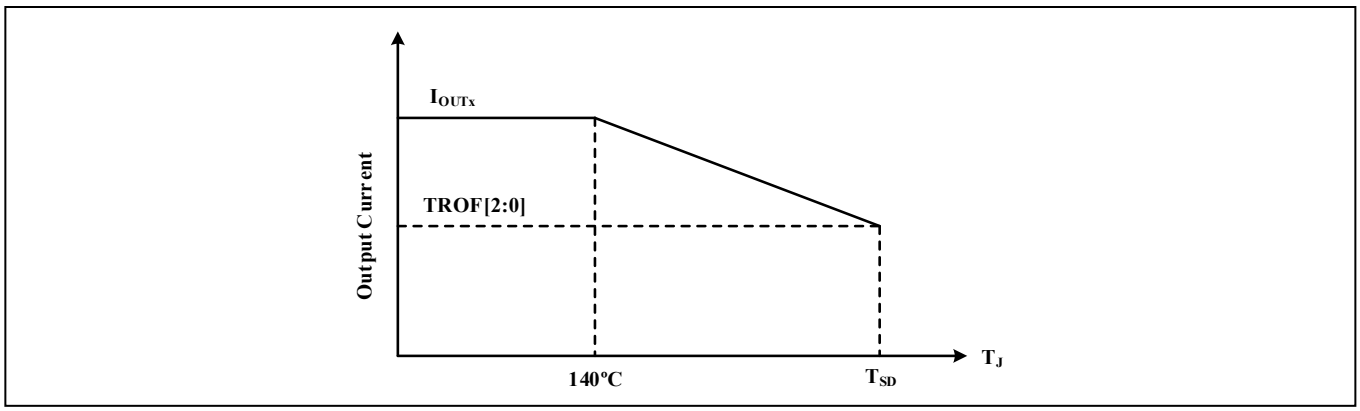


Figure 10 Thermal Roll-off Protection

By mounting the IS32LT3136 device on the same thermal substrate as the LEDs, use of this feature can also limit the dissipation of the LEDs.

11.5.15 FAULT ACTION TABLE

Fault Action Table (Both Normal State And Fail-Safe State)

Fault Type	Detection	Conditions	Actions	Fault Flags	FAULTB Pin	Recovery
Supply UVLO	$V_{IN}<V_{VIN\_UV}$ or $V_{DD}<V_{DD\_UV}$	-	Turn off all channels and reset all registers to default value	-	No action	$V_{IN}>(V_{VIN\_UV}+V_{VIN\_UVHY})$ or $V_{DD}>(V_{DD\_UV}+V_{DD\_UVHY})$
LED string open	$V_{LED}>V_{FLT\_UV}$ and $(V_{LED}-V_{OUTx})<V_{OC\_FL}$	PWM pulse width greater than 10μs (Typ.) and ODE = 1	Faulty channel outputs 4mA and other channels on (ODF = 1)	OPEN_FLT and OPENF bit	Pull low (ODF = 1)	$(V_{LED}-V_{OUTx})>V_{OC\_RS}$ Write OPENF bit to “0”
LED string short	$V_{OUTx}<V_{SC\_FL}$ (SHORT_FLT=000)	PWM pulse width greater than 10μs (Typ.) and SDE = 1	Faulty channel outputs 4mA and other channels on (SDF = 1)	SHORT_FLT and SHORTF bit	Pull low (SDF = 1)	$V_{OUTx}>V_{SC\_RS}$ (SHORT_FLT=000) Write SHORTF bit to “0”
Single LED short	$V_{LED}>V_{FLT\_UV}$ and $V_{OUTx}<V_{SLSTH}$	PWM pulse width greater than 10μs (Typ.) and SLSDE = 1	Faulty channel outputs 4mA and other channels on (SLSDF = 1)	SLST_FLT and SLSHORTF bit	Pull low (SLSDF = 1)	$V_{OUTx}>V_{SLSTH}$ Write SLSHORTF bit to “0”
ISET pin short (Overcurrent)	I_{OUTx} limited to 45mA (Typ.)	Longer than 1μs (Typ.) deglitch time and RSET_OPE = 1	All channels reduced to 5mA (Typ.)	RSET_SH bit	Pull low	ISET pin to GND resistance resumes to normal range, Write RSET_SH bit to “0”
ISET pin open	ISET pin open	Longer than 1μs (Typ.) deglitch time and RSET_SHE = 1	-	RSET_OP bit	Pull low	ISET pin to Floating resistance resumes to normal range, Write RSET_SH bit to “0”
VDD overvoltage	VDD higher than 5.6V (Typ.)	Longer than 10μs (Typ.) deglitch time and VOFE = 1	-	VOF bit	Pull low	VDD is lower than 5.2V, Write VOF bit to “0”
LDO5V undervoltage	LDO5V lower than 3.8V (Typ.)	Longer than 10μs (Typ.) deglitch time and LUFE = 1	-	LUF bit	Pull low	LDO5V is higher than 4V, Write LUF bit to “0”
VLED undervoltage	VLED lower than 3.2V (Typ.)	Longer than 10μs (Typ.) deglitch time and VLUFE = 1	-	VLUF bit	Pull low	VLED is higher than 4V, Write VLUF bit to “0”
External fault	FAULTB pins are pulled down	OFA [1:0] ≠ 11	All channels off	EXF bit	Pull low	FAULTB pins are pull up Write EXF bit to “0”
SCA verification	Any output occurs SCA verification failure	-	-	SCAVF bit	Pull low (SCAF_EN = 1)	Write SCAVF bit to “0”
PWM duty verification	Any output occurs PWM duty verification failure	-	-	LPBF bit	Pull low (DUTYF_EN = 1)	Disabled loop back, Write DUTYF_EN bit to “0”
Thermal shutdown	$T_J>T_{SD}$	-	All channels off	TSD bit	Pull low (TSDE = 1)	$T_J<(T_{SD}-T_{SD\_HYS})$ Write TSD bit to “0”
Thermal roll-off	$T_J>140^{\circ}C$	TROF[2:0] ≠ 00	All channels linearly reduce output current	TF bit	Pull low (TFE = 1)	$T_J<140^{\circ}C$ Write TF bit to “0”
CRC error	Calculated CRC does not match CRC data	-	Increments CRC Error Count register	CRCF bit	Pull low	Write CRCF bit to “0”
Communication loss	Watchdog 1 times out	R_{FSMD}=30kΩ, 51kΩ or 75kΩ and no error-free communication	Enter fail-safe modes	CMWF1 bit	Pull low	Write CMWF1 bit to “0” or Exit fail-safe modes

Fault Type	Detection	Conditions	Actions	Fault Flags	FAULTB Pin	Recovery
Communication loss	Watchdog 2 times out	R_{FSMD}=30kΩ, 51kΩ or 75kΩ and no error-free communication	Enter fail-safe modes	CMWF1 bit	Pull low	Write CMWF2 bit to "0" Feed the dog within the set WDT2 time range or Exit fail-safe modes
OTP data verification	OTP data ECC error	ECC2F _EN = 1	-	ECC_ST	Pull low	-

Note 8: OPENF, SHORTF, SLSHORTF, IOUTVF, TSD, TF, LPBF, SCAVF, VOF, LUF, VLUF, RSET_SH, RSET_OP, EXF, CMWF1, RSET_OP, CMWF2 and CRCF bits are latched. Even though the fault conditions are removed, they cannot automatically reset to "0" but must be cleared by the host MCU writing it back to "0".

11.6 UARTINTERFACES

The host MCU can communicate with the IS32LT3136 device using a Universal Asynchronous Receiver and Transmitter (UART). The UART communication process uses a command and response protocol (LumiBus protocol) mastered by the host MCU to write and read the registers to and from each IS32LT3136 device. The IS32LT3136 UART interface utilizes half-duplex communications (transmit and receive cannot overlap). A tri-state buffer in the IS32LT3136 drives the TX out pin, so it is recommended to place an external pull-up resistor on the RX input return line of the host MCU. An external pull-up on the MCU TX output will allow multiple IS32LT3136 devices to share a common pair of TX and RX signals by connecting all IS32LT3136 TX lines together and all IS32LT3136 RX lines together. The baud rate can support 100kbps~2Mbps.

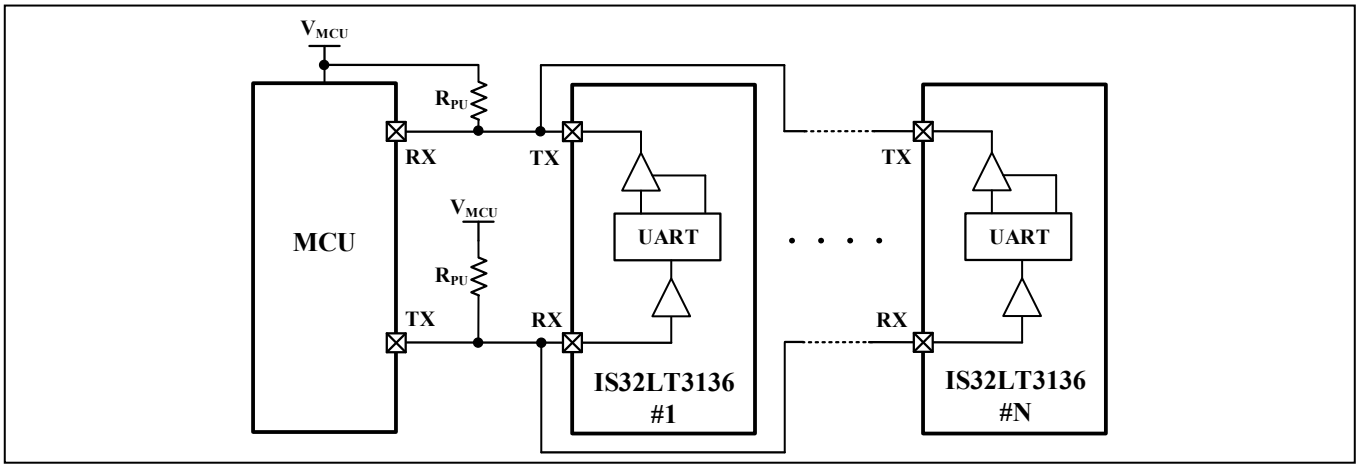


Figure 11 UART Interface Connection

Additionally, the physical TX and RX connections of IS32LT3136 can be joined together through a standard CAN transceiver (CAN PHY), as shown in Figure 13. This has the added advantage of protection from shorts to battery and/or shorts to ground on the cables and/or harnesses between the host MCU board and the IS32LT3136 board. The CAN physical layer has excellent EMI and EMS performance with long distance off-board connection.

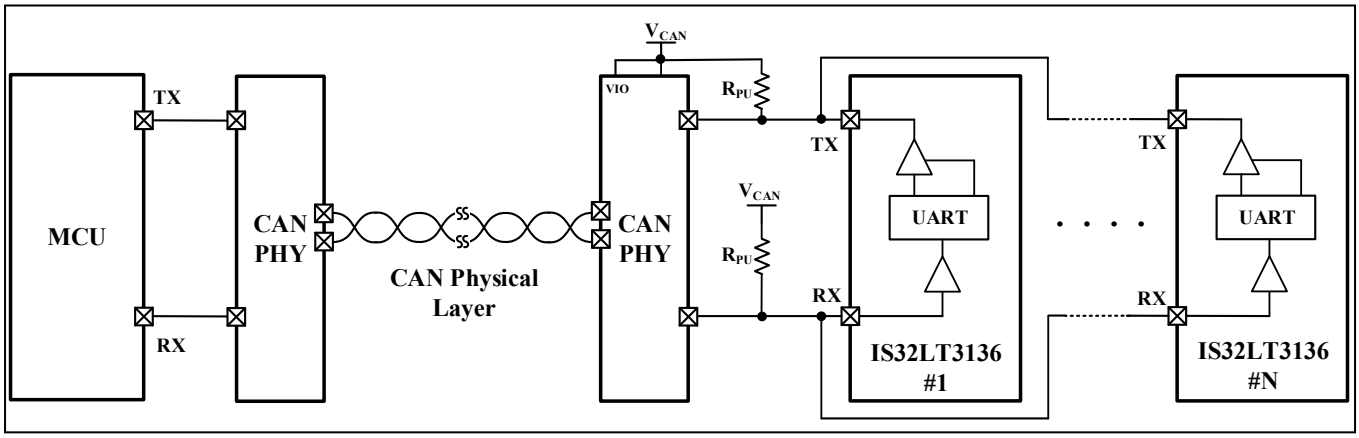


Figure 12 UART Interface with Standard CAN Transceiver Connection

11.6.1 UART DATA FORMAT

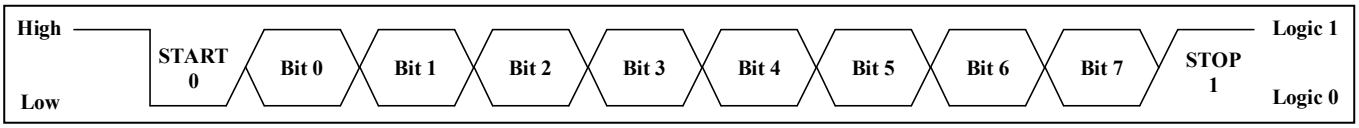


Figure 13 UART Data Byte Format

The UART operates with one start bit, eight data bits (LSbit first) and one stop bit. Above figure shows the waveform for an individual byte transfer on the UART. A logic “1” state occurs when the device drives the line to high voltage. A logic “0” state occurs when the device drives the line to ground. Below figure shows actual data bytes with UART data format.

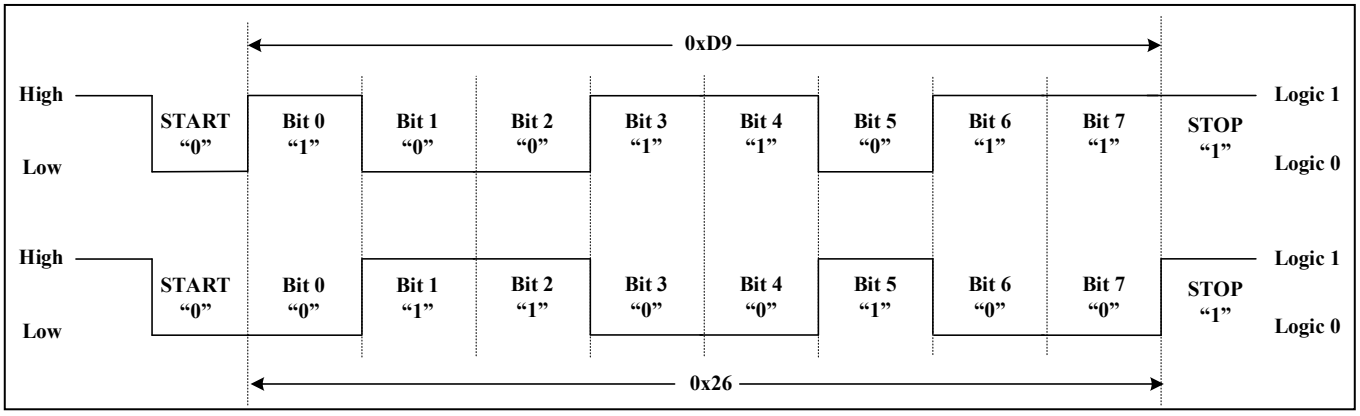


Figure 14 UART Data Transaction Example

The baud rate of UART communication can be 100kbps to 2Mbps which is synchronized by the baud rate of the SYNC byte of the BUS Reset command. The UART uses 64x over-sampling on the incoming asynchronous RX signal. Between UART data bytes, at least one bit is required as STOP bit.

11.6.2 LumiBus PROTOCOL

The communication uses the LumiBus protocol which is a UART-based protocol supported by most MCUs. The communication process of all three interfaces uses a command and response protocol mastered by the host MCU to write and read the registers to and from each IS32LT3136 device. This means that the IS32LT3136 device never initiates traffic onto the network. The LumiBus protocol maps the registers into an address space on each device. The host MCU uses the LumiBus protocol to initiate a communication transaction by sending a command frame. This command frame addresses either one IS32LT3136 device directly or broadcasts to all IS32LT3136 devices on the network. This addressing may cause a response frame to be sent back from the slave IS32LT3136 device depending on the command type of the command frame. There are four types of commands:

1) BUS Reset Command: resets the UART
2) Write Command: writes data from host MCU to specific IS32LT3136 device(s)
3) Read Command: reads data from specific IS32LT3136 device to host MCU
4) Special Command: specifies IS32LT3136 device(s) to implement specific function.

There is no response frame given following a broadcast write command frame. Therefore, only two types of response frames exist that an IS32LT3136 device sends back to the host MCU: Write Acknowledge (if enabled) and Read Response.

11.6.3 COMMAND FRAME TYPES

11.6.3.1 BUS Reset Command Frame

The host MCU can reset the device UART and LumiBus protocol state machine at any time by sending BUS Reset command. The BUS Reset command consists of reset signal and SYNC byte (0x55). The reset signal includes at 150μs~10ms break low and at 2μs~100us logic high break delimiter. Upon receiving the bus reset signal, the LumiBus protocol state machine of all IS32LT3136 devices on the bus will be reset to a known-good state. The bus reset signal must be followed by a SYNC byte (0x55) send by desired baud rate (within 100kbps to 2Mbps) to synchronize the baud rate to all IS32LT3136 devices. The subsequent communication must use the identical baud rate. With this synchronization approach, the cost of an external crystal oscillator is saved. To avoid clock drift over

time and ambient temperature, it's recommended to periodically send a BUS Reset Command to the IS32LT3136 devices.

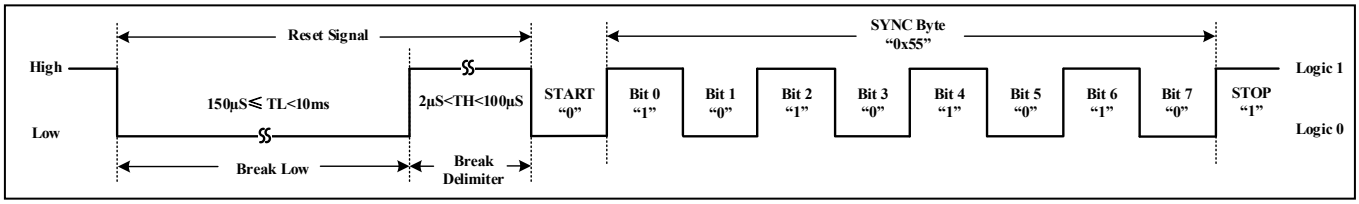


Figure 15 BUS Reset Command

Upon system power up, the host MCU must initialize the BUS by sending a BUS Reset Command before communication. This BUS reset operation can be optionally performed by the host MCU for several application scenarios: (1) upon system power up, (2) communication watchdog times out, (3) communication fault is detected, illustrated as in the following diagram:

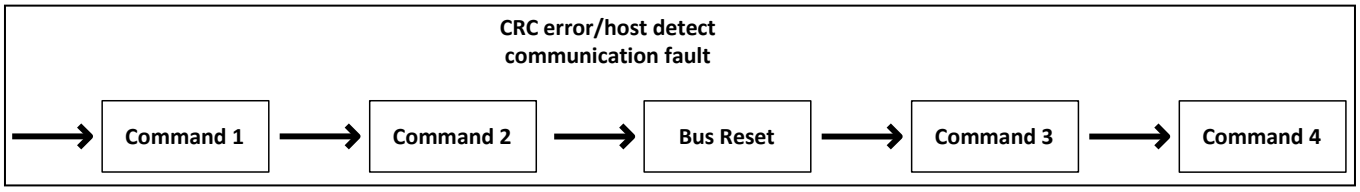


Figure 16 Communication Fault is Detected

Note that the BUS Reset command only resets the interface state machine (including stored communication baud rate). It does not reset the registers and does not halt normal LED PWM operation.

11.6.3.2 Write Command Frame

The Write Command Frame is comprised of the following sequence.

CMD Frame Header (One Byte)	Device ID (One Byte)	Start Register Address (One Byte)	Data 1 (One Byte)	…	Data N (One Byte)	CRC_L (One Byte)	CRC_H (One Byte)

11.6.3.3 Acknowledge Frame

If the ACKSEL bit is set in the CONFIG3 register, the addressed device transmits an acknowledge back to the host MCU upon a successful single device write. The Acknowledge Frame is comprised of a single byte (ACK=0x7F,02h[4:3]=01, ACK=Fault, 02h[4:3]=10 page0) or two byte (ACK=Fault + CRC,02h[4:3]=11, page0) as the following sequence.

0x7F or FAULT (One Byte)

FAULT (One Byte)	CRC (One Byte)

11.6.3.4 Read Command Frame (transferred by the host MCU)

The Read Command Frame is comprised of the following sequence.

CMD Frame Header (One Byte)	Device ID (One Byte)	Start Register Address (One Byte)	CRC_L (One Byte)	CRC_H (One Byte)

A successfully-addressed IS32LT3136 device then transfers back the appropriate Read Response Frame.

The Read Response Frame is comprised of the following sequence.

RSP Frame Header (One Byte)	Device ID (One Byte)	Data 1 (One Byte)	…	Data N (One Byte)	CRC_L (One Byte)	CRC_H (One Byte)

11.6.3.5 Special Command Frame

The special command specifies the IS32LT3136 device to implement specific function which includes:

a) Update Command

This special command is used for below scenarios:

- Update the configuration of the PWM registers data and Scaling registers data into output stages at the next PWM boundary after this command is issued.
- Update the configuration of the DC_PWM register (00h, page0).
- Update the configuration of the PDE(PHASE) register (00h, page0).

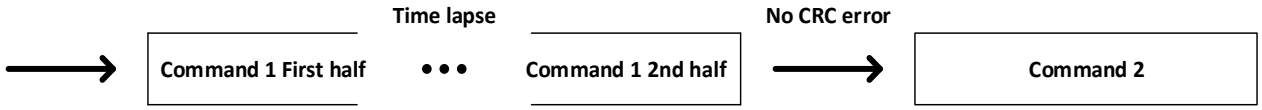
b) Registers Reset Command

Resets all registers to default value, excluding the PWR bit in CONFIG3 register (02h, page0).

The Special Command Frame is comprised of the following sequence:

CMD Frame Header (One Byte)	Device ID (One Byte)	CRC_L (One Byte)	CRC_H (One Byte)

One complete command frame can be received successfully even if the bytes in the frame is not sent continuously. CRC error could be determined by reading back the written data byte.



If host's watch dog time is disabled or time laps is within watchdog time

11.6.4 TRANSACTION FRAME DESCRIPTION

Command frames include the following byte types:

1) Frame Header Byte
2) Device ID Byte
3) Start Register Address Byte
4) N Data Byte(s) (N = 1~16, 32, 64)
5) CRC Bytes (CRC_L and CRC_H)
6) Acknowledge Byte (ACKSEL)

11.6.4.1 Frame Header Byte

The Frame Header Byte identifies the transaction as either a write/read command frame or a response frame. In addition, the Frame Header Byte indicates how many data bytes are being written/read or responded. The number of data bytes to be written/read or responded can be 1~16 or 32.

Frame Header Type	D7	D6	D5	D4:D0
CMD Frame Header	FRM_TYPE	W/R	BCON	CMD
RSP Frame Header	FRM_TYPE	RSVD	RSVD	RSP

The fields shown in the Frame Header Byte above are described in the table below.

	Value (BIN)	Description
FRM_TYPE (Bit 7)	0	Response frame sent back from the IS32LT3136 device to host MCU
	1	Command frame sent from host MCU to the IS32LT3136 device
W/R (Bit 6)	0	Write command frame
	1	Read command frame

	Value (BIN)	Description
BCON (Bit 5)	0	Single device write or read.
	1	Broadcast write. The Device ID Byte must be 0xBF to broadcast to all IS32LT3136 devices. Broadcast only accepts write command
CMD (Bit 4:0)	**Specify transmit data length for write/read command frame:**	
	00000 ~ 01111	1 byte ~ 16 bytes of data length
	10000	32 bytes of data length
	10001	64 bytes of data length
	For special commands (W/R bit must be set to "0"):	
	11000	Update Command. Valid for both single device and broadcast write
	11110	Registers Reset Command. Valid for both single device and broadcast write
RSP (Bit 4:0)	**Specify transmit data length for response frame:**	
	00000 ~ 01111	1 byte ~ 16 bytes of data length
	10000	32 bytes of data length
	10001	64 bytes of data length

11.6.4.2 Device ID Byte

	D7	D6	D5:D0
Device ID	p[1]	p[0]	DEV_ID [5:0]

There are six DEV_ID bits and two parity bits.
The parity bits for the Device ID byte are calculated with the equations below:

p[1] = ~(dev_id[1] ^ dev_id[3] ^ dev_id[4] ^ dev_id[5])

p[0] = dev_id[0] ^ dev_id[1] ^ dev_id[2] ^ dev_id[4]

The device ID of each IS32LT3136 device is determined by the resistors connected from three address pins of ADDR0, ADDR1 and ADDR2 to GND. As following mapping for the Device ID byte. For a broadcast command of UART interface, the DEV_ID[5:0] must be 0b 111111, otherwise the broadcast command will be invalid.

R_{AD2}	R_{AD1}	R_{AD0}	D7	D6	D5	D4	D3	D2	D1	D0	DEVICE ID (HEX)
(kΩ, Note 9)											
10k	10k	10k	1	0	0	0	0	0	0	0	80
10k	10k	30k	0	1	0	1	0	0	0	0	50
10k	10k	51k	0	0	1	0	0	0	0	0	20
10k	10k	75k	1	1	1	1	0	0	0	0	F0
10k	30k	10k	1	1	0	0	0	1	0	0	C4
10k	30k	30k	0	0	0	1	0	1	0	0	14
10k	30k	51k	0	1	1	0	0	1	0	0	64
10k	30k	75k	1	0	1	1	0	1	0	0	B4
10k	51k	10k	0	0	0	0	1	0	0	0	08
10k	51k	30k	1	1	0	1	1	0	0	0	D8
10k	51k	51k	1	0	1	0	1	0	0	0	A8
10k	51k	75k	0	1	1	1	1	0	0	0	78
10k	75k	10k	0	1	0	0	1	1	0	0	4C

10k	75k	30k	1	0	0	1	1	1	0	0	9C
10k	75k	51k	1	1	1	0	1	1	0	0	EC
10k	75k	75k	0	0	1	1	1	1	0	0	3C
30k	10k	10k	1	1	0	0	0	0	0	1	C1
30k	10k	30k	0	0	0	1	0	0	0	1	11
30k	10k	51k	0	1	1	0	0	0	0	1	61
30k	10k	75k	1	0	1	1	0	0	0	1	B1
30k	30k	10k	1	0	0	0	0	1	0	1	85
30k	30k	30k	0	1	0	1	0	1	0	1	55
30k	30k	51k	0	0	1	0	0	1	0	1	25
30k	30k	75k	1	1	1	1	0	1	0	1	F5
30k	51k	10k	0	1	0	0	1	0	0	1	49
30k	51k	30k	1	0	0	1	1	0	0	1	99
30k	51k	51k	1	1	1	0	1	0	0	1	E9
30k	51k	75k	0	0	1	1	1	0	0	1	39
30k	75k	10k	0	0	0	0	1	1	0	1	0D
30k	75k	30k	1	1	0	1	1	1	0	1	DD
30k	75k	51k	1	0	1	0	1	1	0	1	AD
30k	75k	75k	0	1	1	1	1	1	0	1	7D
51k	10k	10k	0	1	0	0	0	0	1	0	42
51k	10k	30k	1	0	0	1	0	0	1	0	92
51k	10k	51k	1	1	1	0	0	0	1	0	E2
51k	10k	75k	0	0	1	1	0	0	1	0	32
51k	30k	10k	0	0	0	0	0	1	1	0	06
51k	30k	30k	1	1	0	1	0	1	1	0	D6
51k	30k	51k	1	0	1	0	0	1	1	0	A6
51k	30k	75k	0	1	1	1	0	1	1	0	76
51k	51k	10k	1	1	0	0	1	0	1	0	CA
51k	51k	30k	0	0	0	1	1	0	1	0	1A
51k	51k	51k	0	1	1	0	1	0	1	0	6A
51k	51k	75k	1	0	1	1	1	0	1	0	BA
51k	75k	10k	1	0	0	0	1	1	1	0	8E
51k	75k	30k	0	1	0	1	1	1	1	0	5E
51k	75k	51k	0	0	1	0	1	1	1	0	2E
51k	75k	75k	1	1	1	1	1	1	1	0	FE
75k	10k	10k	0	0	0	0	0	0	1	1	03
75k	10k	30k	1	1	0	1	0	0	1	1	D3
75k	10k	51k	1	0	1	0	0	0	1	1	A3
75k	10k	75k	0	1	1	1	0	0	1	1	73
75k	30k	10k	0	1	0	0	0	1	1	1	47
75k	30k	30k	1	0	0	1	0	1	1	1	97
75k	30k	51k	1	1	1	0	0	1	1	1	E7
75k	30k	75k	0	0	1	1	0	1	1	1	37
75k	51k	10k	1	0	0	0	1	0	1	1	8B
75k	51k	30k	0	1	0	1	1	0	1	1	5B
75k	51k	51k	0	0	1	0	1	0	1	1	2B

75k	51k	75k	1	1	1	1	1	0	1	1	FB
75k	75k	10k	1	1	0	0	1	1	1	1	CF
75k	75k	30k	0	0	0	1	1	1	1	1	1F
75k	75k	51k	0	1	1	0	1	1	1	1	6F
75k	75k	75k	1	0	1	1	1	1	1	1	BF
-	-	-	1	0	1	1	1	1	1	1	BF (Note 10) (for broadcast command only)

Note 9: The tolerance range of resistance accuracy could be ±1% or ±5% for 10kΩ, 30kΩ, and 75kΩ, but the tolerance range of resistance accuracy should be ±1% for 51kΩ.

Note 10: The Device ID Byte must be 0xBF to broadcast to all IS32LT3136 devices. Broadcast only accepts write command.

11.6.4.3 Start Register Address Byte

The LumiBus protocol allows up to 64 successive register locations from the addressed register to be written or read by a single command frame. The Start Register Address Byte is single byte which specifies the first register being written or read. The Start Register Address byte is present in only Write and Read Command transactions, not in Read Response and Special command transactions.

11.6.4.4 N Data Byte (s)

The Frame Header Byte specifies the number of data bytes to be included in the frame.

11.6.4.5 CRC Bytes (CRC_L and CRC_H)

The host MCU sends command to IS32LT3136 using CRC-16-IBM standard for CRC checksum calculation, which will cover the whole frame bytes, e.g., Frame Header Byte, Device ID Byte, Start Register Address Byte, N Data Bytes. Lower byte first followed by higher byte. The CRC Bytes allow detection of errors within the transaction frame. The device increments the CRC Error Count Register (9Ah) each time a CRC error occurs on an incoming command frame and the CRCF bit in FAULT_TYPE_1 register (97h) will be set to “1” and the FAULTB pin will go low to report fault condition after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register).

The CRCF bit in FAULT_TYPE_1 register (97h) is latched, which means that it cannot automatically reset to “0” when no CRC error occurs but must be cleared by the host MCU writing it back to “0”. Once the CRCF bit is cleared, the FAULTB pin will go back to high impedance after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register).

The CRC bytes are also calculated by the addressed device during its Read Response. The CRC bytes are then appended to the end of the read data, lower byte first followed by higher byte. This allows the host MCU to check the read data coming from the IS32LT3136 device for any transmission errors. The following is a reference CRC checksum C code for a transmission to the IS32LT3136 devices.

```
Uint16 crc_16_ibm (Uint8 *buf, Uint8 len)
{
        Uint16 crc = 0;
        Uint16 I;
        while (len--)
        {
                crc ^= *buf++;
                for (I = 0; I < 8; I++){
                crc = (crc >> 1) ^ ((crc & 1) ? 0xa001 : 0);
                }
        }
        return crc;
}
```

Upon reading data from the IS32LT3136 device, the host MCU should calculate and compare the CRC to determine whether valid data was received. When IS32LT3136 sends back CRC bytes to the host MCU, the calculated CRC bytes must be bit-reversed before comparison to the received CRC bytes. The following is a reference code to perform received CRC bit reversal.

```
Uint8 reverse_byte(Uint8 byte)
{
        // First, swap the nibbles
```

```
        byte = (((byte & 0xF0) >> 4)| | ((byte & 0x0F) << 4));
        // Then, swap bit pairs
        byte = (((byte & 0xCC) >> 2) | ((byte & 0x33) << 2));
        // Finally, swap adjacent bits
        byte = (((byte & 0xAA) >> 1) | ((byte & 0x55) << 1));
        // We should now be reversed (bit 0 <--> bit 7, bit 1 <--> bit 6, etc.)
        return byte;
}
```

The following is a reference code for checking the read data against received CRC bytes.

```
bool is_crc_valid(Uint8 *rx_buf, Uint8 crc_start)
{
        Uint16 crc_calc; // Calculated CRC
        Uint8 crc_msb, crc_lsb; // Individual bytes of calculated CRC
        // Calculate the CRC based on bytes received
        crc_calc = crc_16_ibm(rx_buf, crc_start);
        crc_lsb = (crc_calc & 0x00FF);
        crc_msb = ((crc_calc >> 8) & 0x00FF);
        // Perform the bit reversal within each byte
        crc_msb = reverse_byte(crc_msb);
        crc_lsb = reverse_byte(crc_lsb);
        // Do they match?
        if((*(rx_buf + crc_start) == crc_lsb) && (*(rx_buf + crc_start + 1) == crc_msb))
        {
                return TRUE;
        }
        else
        {
                return FALSE;
        }
}
```

11.6.4.6 Acknowledge Byte

The Acknowledge Byte (“ACKSEL”) consists of a single byte (ACK=0x7F or ACK=FAULT) or two byte(ACK=Fault + CRC):

ACK is sent back by the addressed IS32LT3136 device only if the ACKSEL bit is set in the CONFIG3 register (02h) and only if the write is successful. A successful write yields no CRC checksum error or parity errors. Note that the acknowledge is only valid for single device write transaction of IS32LT3136.

11.6.4.7 Turnaround Time

When considering back-to-back data transfer, the turnaround time (additional time required between the end of the previous byte stop bit and the beginning of the next byte start bit) is required, that means a finite amount of dead time must be inserted between two bytes or two command frames. It’s recommended to use dual stop bits mode for the UART interface.

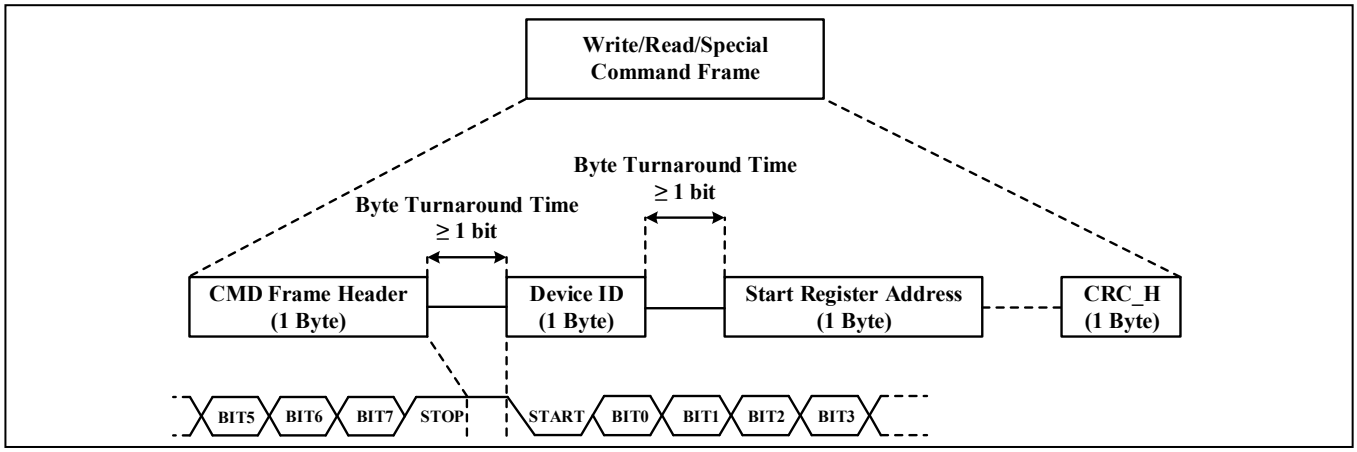


Figure 17 Turnaround Time Between Byte to Byte

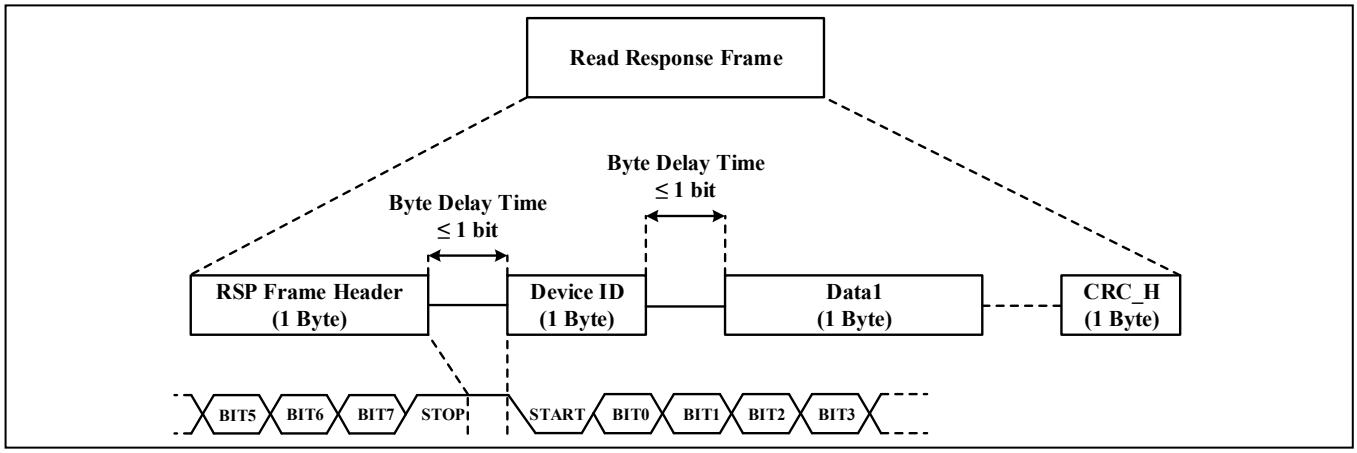


Figure 18 Delay Time Between Byte to Byte of Read Response Frame

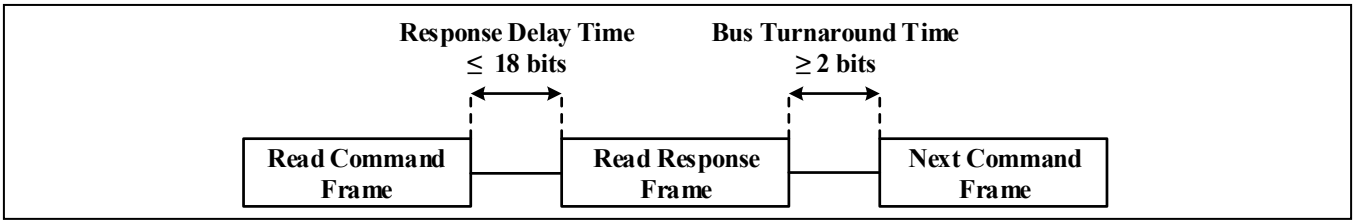


Figure 19 Turnaround Time Between Read Response Frame to Next Command Frame

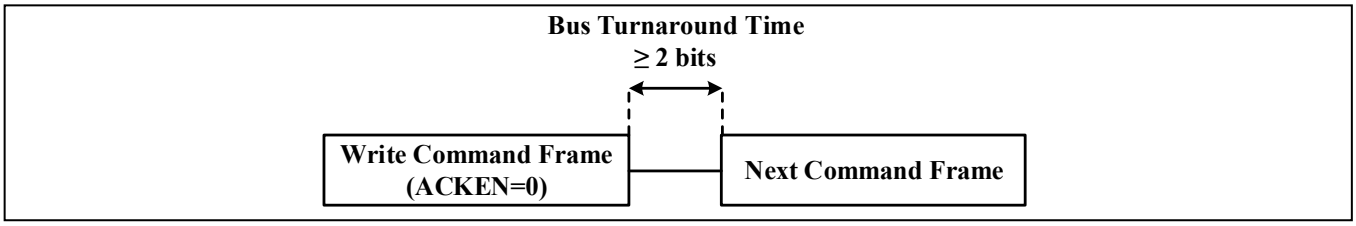


Figure 20 Turnaround Time Between Write Command Frame to Next Command Frame (ACK Disabled)

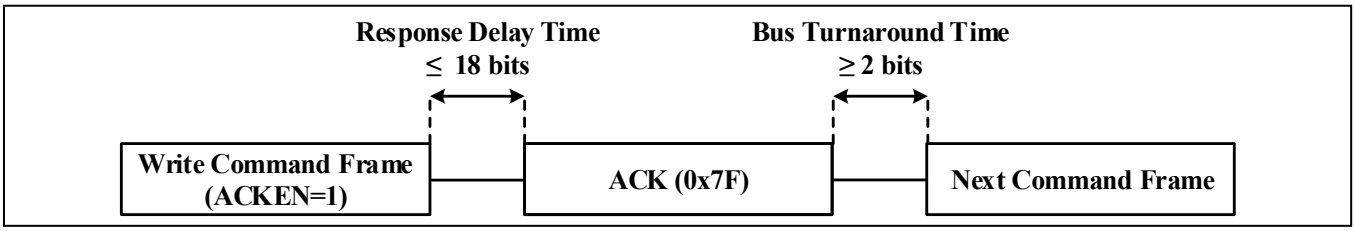


Figure 21 Turnaround Time Between ACK to Next Command Frame (ACK Enabled)

11.7 COMMUNICATIONS EXAMPLES

The total number of transmitted bytes depends on the specific task being performed. The examples below show the sequence of transmitted bytes for a given transaction.

11.7.1 Example 1: Single Device Write of 3 Bytes

Write to Device ID with parity = 0x55, R_{AD0}=30kΩ, R_{AD1}=30kΩ, R_{AD2}=30kΩ: beginning at register 26h, PWM0_H=0x1F, PWM1_H=0x2F, PWM2_H=0x3F

Byte Types	Number of Bytes
CMD Frame Header Byte	1
Device ID Byte	1
Start Register Address Byte	1
Data Bytes	3
CRC Bytes	2
Total	8

	Command Frame							
Interface	**CMD Frame Header**	**Device ID**	**Start Register Address**	**Data 1**	**Data 2**	**Data 3**	**CRC_L**	**CRC_H**
UART	0x82 (0b10000010)	0x55	0x26	0x1F	0x2F	0x3F	0x74	0x80

Acknowledge from addressed device (if enabled ACKSEL= '0X01' for IS32LT3136)

Acknowledge Frame
ACK
0x7F

11.7.2 Example 2: Single Device Read of 2 Bytes

Read from Device ID with parity = 0xA3, R_{AD0}=51kΩ, R_{AD1}=10kΩ, R_{AD2}=75kΩ: beginning at register 97H, read FAULT_TYPE_1/2

Byte Types	Number of Bytes
CMD Frame Header Byte	1
Device ID Byte	1
Start Register Address Byte	1
CRC Bytes	2
Total	5

	Command Frame				
Interface	**CMD Frame Header**	**Device ID**	**Start Register Address**	**CRC_L**	**CRC_H**
UART	0XC1 (0b11000001)	0xA3	0x97	0x68	0XA2

Read Response: FLT_TYPE1/2=0x00

Byte Types	Number of Bytes
RSP Frame Header Byte	1
Device ID Byte	1
Data Bytes	2
CRC Bytes	2
Total	6

	Command Frame					
Interface	RSP Frame Header	Device ID	Data 1	Data 2	CRC_L	CRC_H
UART	0x01 (0b00000001)	0XA3	0x00	0x00	0x8F	0x7B

11.7.3 Example 3: Broadcast Write of 3 Bytes

Broadcast write to all devices (fixed Device ID with parity = 0xBF): beginning at register 06h, SCA0=0x0F, SCA1=0x1F, SCA2=0x2F.

Byte Types	Number of Bytes
CMD Frame Header Byte	1
Device ID Byte	1
Start Register Address Byte	1
Data Bytes	3
CRC Bytes	2
Total	8

	Command Frame							
Interface	CMD Frame Header	Device ID	Start Register Address	Data 1	Data 2	Data 3	CRC_L	CRC_H
UART	0xA2 (0b10100010)	0xBF	0x06	0x0F	0x1F	0x2F	0x75	0xFE

11.7.4 Example 4: Broadcast Registers Reset Command (Special Command)

Broadcast Registers Reset Command to all devices (fixed Device ID with parity = 0xBF):

Byte Types	Number of Bytes
CMD Frame Header Byte	1
Device ID Byte	1
CRC Bytes	2
Total	4

	Command Frame			
Interface	CMD Frame Header	Device ID	CRC_L	CRC_H
UART	0xBE (0b10111110)	0xBF	0x30	0x10

11.7.5 Example 5: Broadcast Update Command (Special Command)

Broadcast Update Command to all devices (fixed Device ID with parity = 0xBF):

Byte Types	Number of Bytes
CMD Frame Header Byte	1
Device ID Byte	1
CRC Bytes	2
Total	4

	Command Frame			
Interface	CMD Frame Header	Device ID	CRC_L	CRC_H
UART	0xB8 (0b10111000)	0xBF	0x33	0xB0

11.8 DEVICE FUNCTIONAL MODES

The IS32LT3136 device operates in one of several states.

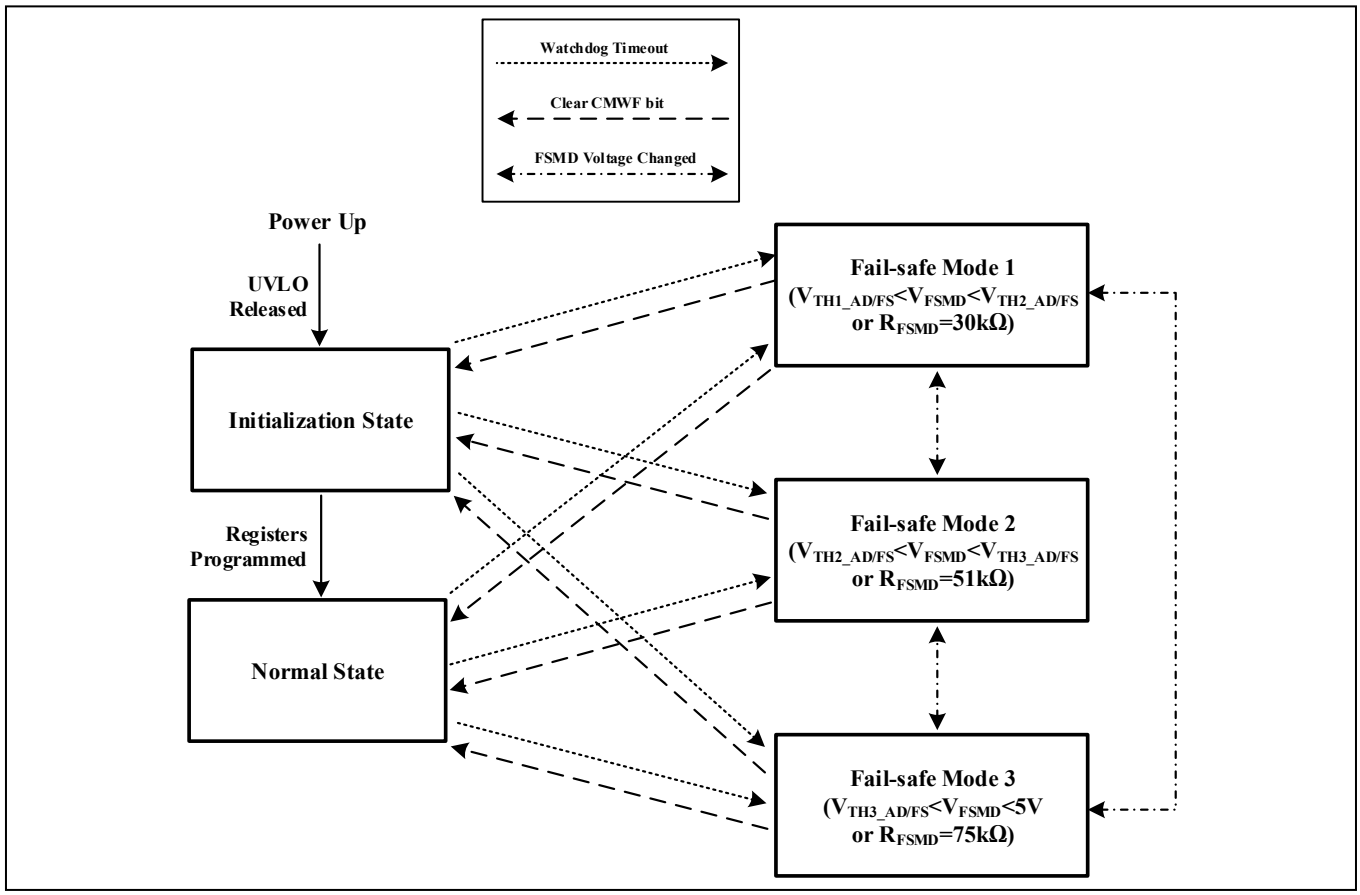


Figure 22 Operation States

11.8.1 INITIALIZATION STATE

On power up and once released from UVLO, the device enters an initialization state. In this state, all registers are reset to default values and all outputs are in off state. The device waits to receive commands from the MCU master.

11.8.2 NORMAL STATE

In normal state, the IS32LT3136 registers control its outputs by accepting interface commands and by monitoring and responding to realtime events on the inputs associated with the analog and power circuitry. This allows dimming

of the LED outputs using the registers settings.

11.8.3 FAIL-SAFE STATE

This state allows the user to preset the outputs' state if the communication is broken. The device integrates a communication watchdog timer that operates based on the system clock pulse. IS32LT3136 has two internal watchdog timers, watchdog timer 1 is a communication watchdog timer, programmed through the CMWT1 register (03h), defining the time of the communication watchdog timer. The watchdog timer 2 is the command watchdog timer, programmed through the CMWT2 register (04h), which defines the maximum/minimum feeding time range of the command watchdog timer. If the communication watchdog times out (no error-free communication is successfully received within the set number of system clock cycles) or the command watchdog overflows (no feeding command is successfully received within the set time range of feeding dog), the device will enter the fail-proof mode, including three modes: Mode 1 ~ Mode 3.

The FSMD pin is used to configure the fail-safe modes. When the resistor R_{FSMD} is connected from the FSMD pin to ground, the internal $I_{AD/FS}$ (typical 50μA) current source creates a voltage on the FSMD pin, V_{FSMD}. The device compares the V_{FSMD} with internal different reference voltage levels ($V_{TH1\_AD/FS}$, $V_{TH2\_AD/FS}$ and $V_{TH3\_AD/FS}$) to determine the fail-safe mode. It also allows to externally apply proper voltage on the FSMD pin to either choose or change the fail-safe mode. Refer to the Fail-safe Mode Setting Table.

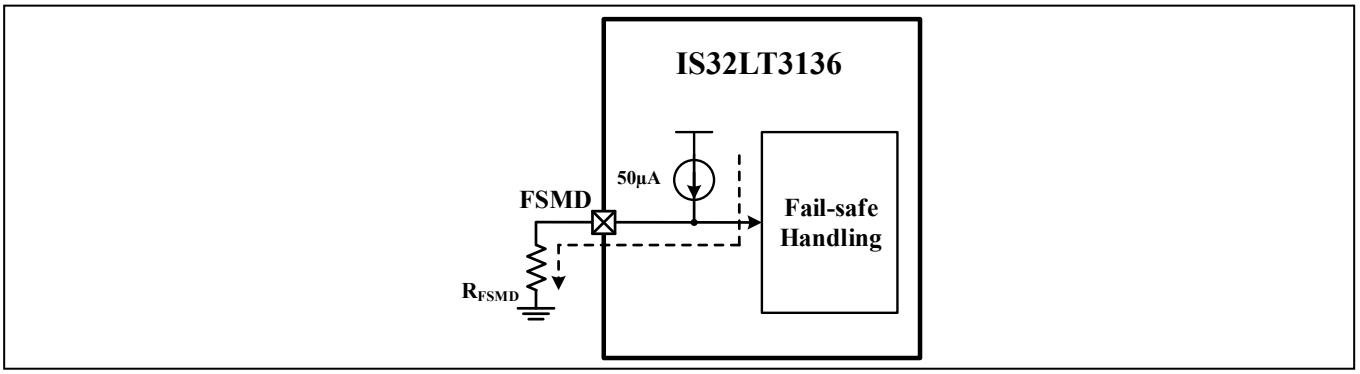


Figure 23 Fail-safe Mode Setting

When $0V<V_{FSMD}<V_{TH1\_AD/FS}$, or $R_{FSMD}=10k\Omega$, the internal communication watchdog is invalid, and the fail-safe mode is disabled. The outputs are always controlled by the scaling and PWM registers (06h~65h).

When $V_{TH1\_AD/FS}<V_{FSMD}<V_{TH2\_AD/FS}$, or $R_{FSMD}=30k\Omega$, the internal communication watchdog 1 and Command watchdog 2 is active, and the fail-safe mode is Mode 1. If the watchdog times out, the device will enter fail-safe Mode 1 and the outputs will be determined by the OTP-A DEFAULT registers (10h~29h). The CMWF 2 or CMW F1 bit in FAULT_TYPE_1 register (97h) will be set to "1" and the FAULTB pin will go low after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) to report the fault condition. To quit from the fail-safe mode to normal state, the CMWF1 and CMWF2 bit in FAULT_TYPE_1 register (97h) must be cleared by the host MCU writing it to "0", and feed the watchdog 2 for the set time. The watchdog timer will be reset and the FAULTB pin will go back to high impedance after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register).

When $V_{TH2\_AD/FS}<V_{FSMD}<V_{TH3\_AD/FS}$, or $R_{FSMD}=51k\Omega$, the internal communication watchdog 1 and Command watchdog 2 is active, and the fail-safe mode is Mode 2. If the watchdog times out, the device will enter fail-safe Mode 2 and all outputs will be forced into completely off. The CMWF2 or CMWF1 bit in FAULT_TYPE_1 register (97h) will be set to "1" and the FAULTB pin will go low after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) to report the fault condition. To quit from the fail-safe mode to normal state, the CMWF1 and CMWF2 bit in FAULT_TYPE_1 register (97h) must be cleared by the host MCU writing it to "0" and feed the watchdog 2 for the set time. The watchdog timer will be reset and the FAULTB pin will go back to high impedance after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register).

When $V_{TH3\_AD/FS}<V_{FSMD}<5V$, or $R_{FSMD}=75k\Omega$, the internal communication watchdog 1 and Command watchdog 2 is active, and the fail-safe mode is Mode 3. If the watchdog times out, the device will enter fail-safe Mode 3 and all outputs will be forced into fully on (with 98% PWM duty cycle). The CMWF 2 or CMW F1 bit in FAULT_TYPE_1 register (97h) will be set to "1" and the FAULTB pin will go low after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) to report the fault condition. To quit from the fail-safe mode to normal state, the CMWF1 and CMWF2 bit in FAULT_TYPE_1 register (97h) must be cleared by the host MCU writing it to "0" and feed the watchdog 2 for the set time. The watchdog timer will be reset and the FAULTB pin will go back to high impedance after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register).

In the fail-safe modes, the fault protections also are valid, including LED string open/short, single LED short, overcurrent (ISET shorted), and over temperature. It should be noted that even if OUT31 is set to the Special function through this register, after entering the Fail-safe mode, the Special Function pin will be set to LED OUT, and the Special Function will fail. When using DCFB function, special care should be taken not to use Fail-safe Mode 3 Mode, and the DEFLED31 bit of DEFLED4 register (16h in page 1) should be set to LED off when using Fail-safe Mode 1.

Note that the device must be re-initialized after quitting from the fail-safe mode to normal state.

11.8.4 Fail-safe Mode Setting Table

FSMD Pin	Fail-Safe Mode	LED State In Fail-Safe Mode
$0V<V_{FSMD}<V_{TH1\_AD/FS}$ or $R_{FSMD}=10k\Omega$	Disabled	-
$V_{TH1\_AD/FS}<V_{FSMD}<V_{TH2\_AD/FS}$ or $R_{FSMD}=30k\Omega$	Mode 1	Determined by OTP (10h~29h in page1)
$V_{TH2\_AD/FS}<V_{FSMD}<V_{TH3\_AD/FS}$ or $R_{FSMD}=51k\Omega$	Mode 2	All Completely Off
$V_{TH3\_AD/FS}<V_{FSMD}<5V$ or $R_{FSMD}=75k\Omega$	Mode 3	All On with 98% PWM duty cycle

12 TABLE 2 REGISTER PAGE CONTROL DEFINITION

Address	Name	Function	Table	R/W	Default
FEh	Register Page Write Lock Register	0xC5 to unlock FDh Register	-	W	0000 0000
FDh	Register Page select Register	Available Page 0 to Page 1 Registers	3	W	0101 0010

12.1 REGISTER PAGE CONTROL CONFIGURE

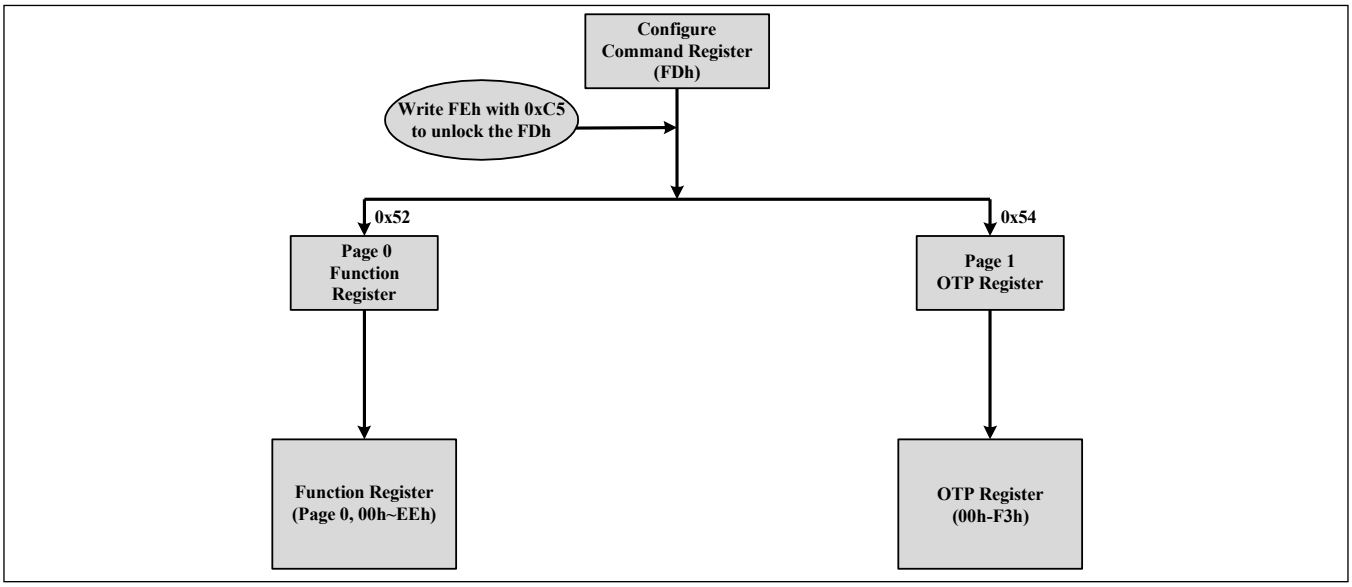


Figure 24 Register Page Control Configure

12.2 Table 3 FDh Register Page Select Register

Data	Hex	Function
0101 0010	0x52	Point to Page 0(PG0): Function Register is available (default PG0)
0101 0100	0x54	Point to Page 1(PG1): OTP Content Register is available
Others	-	Not allowed

13 REGISTER MAP

13.1 Page 0 (00h~ECh): FUNCTION REGISTER

ADDR HEX	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	R/W	DEFAULT
00	CONFIG1	-	PDE	DC_PWM	PFS [4:0]					R/W	0b 01001111
01	CONFIG2	-	-	OFA [1:0]		-	TROF [2:0]			R/W	0b 00110000
02	CONFIG3	SSCEN	SSC [1:0]		ACKSEL[1:0]		-	-	PWR	R/W	0b 00000000
03	CMWT1	-	-	-	-	-	CMWTAP [2:0]			R/W	0b 00000011
04	CMWT2	WDT2CLR	WDT2_MAX [2:0]			-	WDT2_MIN [2:0]			R/W	0b 00110000
05	GC_CTRL	GCC [7:0]								R/W	0b 11111111
06	SCA0	SCA0_DATA [7:0]								R/W	0b 00000000
07	SCA1	SCA1_DATA [7:0]								R/W	0b 00000000
08	SCA2	SCA2_DATA [7:0]								R/W	0b 00000000
09	SCA3	SCA3_DATA [7:0]								R/W	0b 00000000
0A	SCA4	SCA4_DATA [7:0]								R/W	0b 00000000
0B	SCA5	SCA5_DATA [7:0]								R/W	0b 00000000
0C	SCA6	SCA6_DATA [7:0]								R/W	0b 00000000
0D	SCA7	SCA7_DATA [7:0]								R/W	0b 00000000
0E	SCA8	SCA8_DATA [7:0]								R/W	0b 00000000
0F	SCA9	SCA9_DATA [7:0]								R/W	0b 00000000
10	SCA10	SCA10_DATA [7:0]								R/W	0b 00000000
11	SCA11	SCA11_DATA [7:0]								R/W	0b 00000000
12	SCA12	SCA12_DATA [7:0]								R/W	0b 00000000
13	SCA13	SCA13_DATA [7:0]								R/W	0b 00000000
14	SCA14	SCA14_DATA [7:0]								R/W	0b 00000000
15	SCA15	SCA15_DATA [7:0]								R/W	0b 00000000
16	SCA16	SCA16_DATA [7:0]								R/W	0b 00000000
17	SCA17	SCA17_DATA [7:0]								R/W	0b 00000000
18	SCA18	SCA18_DATA [7:0]								R/W	0b 00000000
19	SCA19	SCA19_DATA [7:0]								R/W	0b 00000000
1A	SCA20	SCA20_DATA [7:0]								R/W	0b 00000000
1B	SCA21	SCA21_DATA [7:0]								R/W	0b 00000000
1C	SCA22	SCA22_DATA [7:0]								R/W	0b 00000000
1D	SCA23	SCA23_DATA [7:0]								R/W	0b 00000000
1E	SCA24	SCA24_DATA [7:0]								R/W	0b 00000000
1F	SCA25	SCA25_DATA [7:0]								R/W	0b 00000000
20	SCA26	SCA26_DATA [7:0]								R/W	0b 00000000
21	SCA27	SCA27_DATA [7:0]								R/W	0b 00000000

ADDR HEX	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	R/W	DEFAULT
22	SCA28	SCA28_DATA [7:0]								R/W	0b 00000000
23	SCA29	SCA29_DATA [7:0]								R/W	0b 00000000
24	SCA30	SCA30_DATA [7:0]								R/W	0b 00000000
25	SCA31	SCA31_DATA [7:0]								R/W	0b 00000000
26	PWM0_H	PWM0_DATA [11:4]								R/W	0b 00000000
27	PWM1_H	PWM1_DATA [11:4]								R/W	0b 00000000
28	PWM2_H	PWM2_DATA [11:4]								R/W	0b 00000000
29	PWM3_H	PWM3_DATA [11:4]								R/W	0b 00000000
2A	PWM4_H	PWM4_DATA [11:4]								R/W	0b 00000000
2B	PWM5_H	PWM5_DATA [11:4]								R/W	0b 00000000
2C	PWM6_H	PWM6_DATA [11:4]								R/W	0b 00000000
2D	PWM7_H	PWM7_DATA [11:4]								R/W	0b 00000000
2E	PWM8_H	PWM8_DATA [11:4]								R/W	0b 00000000
2F	PWM9_H	PWM9_DATA [11:4]								R/W	0b 00000000
30	PWM10_H	PWM10_DATA [11:4]								R/W	0b 00000000
31	PWM11_H	PWM11_DATA [11:4]								R/W	0b 00000000
32	PWM12_H	PWM12_DATA [11:4]								R/W	0b 00000000
33	PWM13_H	PWM13_DATA [11:4]								R/W	0b 00000000
34	PWM14_H	PWM14_DATA [11:4]								R/W	0b 00000000
35	PWM15_H	PWM15_DATA [11:4]								R/W	0b 00000000
36	PWM16_H	PWM16_DATA [11:4]								R/W	0b 00000000
37	PWM17_H	PWM17_DATA [11:4]								R/W	0b 00000000
38	PWM18_H	PWM18_DATA [11:4]								R/W	0b 00000000
39	PWM19_H	PWM19_DATA [11:4]								R/W	0b 00000000
3A	PWM20_H	PWM20_DATA [11:4]								R/W	0b 00000000
3B	PWM21_H	PWM21_DATA [11:4]								R/W	0b 00000000
3C	PWM22_H	PWM22_DATA [11:4]								R/W	0b 00000000
3D	PWM23_H	PWM23_DATA [11:4]								R/W	0b 00000000
3E	PWM24_H	PWM24_DATA [11:4]								R/W	0b 00000000
3F	PWM25_H	PWM25_DATA [11:4]								R/W	0b 00000000
40	PWM26_H	PWM26_DATA [11:4]								R/W	0b 00000000
41	PWM27_H	PWM27_DATA [11:4]								R/W	0b 00000000
42	PWM28_H	PWM28_DATA [11:4]								R/W	0b 00000000
43	PWM29_H	PWM29_DATA [11:4]								R/W	0b 00000000
44	PWM30_H	PWM30_DATA [11:4]								R/W	0b 00000000

ADDR HEX	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	R/W	DEFAULT
45	PWM31_H	PWM31_DATA [11:4]								R/W	0b 00000000
46	PWM0_L	-	-	-	-	PWM0_DATA [3:0]				R/W	0b 00000000
47	PWM1_L	-	-	-	-	PWM1_DATA [3:0]				R/W	0b 00000000
48	PWM2_L	-	-	-	-	PWM2_DATA [3:0]				R/W	0b 00000000
49	PWM3_L	-	-	-	-	PWM3_DATA [3:0]				R/W	0b 00000000
4A	PWM4_L	-	-	-	-	PWM5_DATA [3:0]				R/W	0b 00000000
4B	PWM5_L	-	-	-	-	PWM4_DATA [3:0]				R/W	0b 00000000
4C	PWM6_L	-	-	-	-	PWM6_DATA [3:0]				R/W	0b 00000000
4D	PWM7_L	-	-	-	-	PWM7_DATA [3:0]				R/W	0b 00000000
4E	PWM8_L	-	-	-	-	PWM8_DATA [3:0]				R/W	0b 00000000
4F	PWM9_L	-	-	-	-	PWM9_DATA [3:0]				R/W	0b 00000000
50	PWM10__L	-	-	-	-	PWM10_DATA [3:0]				R/W	0b 00000000
51	PWM11_L	-	-	-	-	PWM11_DATA [3:0]				R/W	0b 00000000
52	PWM12_L	-	-	-	-	PWM12_DATA [3:0]				R/W	0b 00000000
53	PWM13_L	-	-	-	-	PWM13_DATA [3:0]				R/W	0b 00000000
54	PWM14_L	-	-	-	-	PWM14_DATA [3:0]				R/W	0b 00000000
55	PWM15_L	-	-	-	-	PWM15_DATA [3:0]				R/W	0b 00000000
56	PWM16_L	-	-	-	-	PWM16_DATA [3:0]				R/W	0b 00000000
57	PWM17_L	-	-	-	-	PWM17_DATA [3:0]				R/W	0b 00000000
58	PWM18_L	-	-	-	-	PWM18_DATA [3:0]				R/W	0b 00000000
59	PWM19_L	-	-	-	-	PWM19_DATA [3:0]				R/W	0b 00000000
5A	PWM20_L	-	-	-	-	PWM20_DATA [3:0]				R/W	0b 00000000
5B	PWM21_L	-	-	-	-	PWM21_DATA [3:0]				R/W	0b 00000000
5C	PWM22_L	-	-	-	-	PWM22_DATA [3:0]				R/W	0b 00000000
5D	PWM23_L	-	-	-	-	PWM23_DATA [3:0]				R/W	0b 00000000
5E	PWM24_L	-	-	-	-	PWM24_DATA [3:0]				R/W	0b 00000000
5F	PWM25_L	-	-	-	-	PWM25_DATA [3:0]				R/W	0b 00000000
60	PWM26_L	-	-	-	-	PWM26_DATA [3:0]				R/W	0b 00000000
61	PWM27_L	-	-	-	-	PWM27_DATA [3:0]				R/W	0b 00000000
62	PWM28_L	-	-	-	-	PWM28_DATA [3:0]				R/W	0b 00000000
63	PWM29_L	-	-	-	-	PWM29_DATA [3:0]				R/W	0b 00000000
64	PWM30_L	-	-	-	-	PWM30_DATA [3:0]				R/W	0b 00000000
65	PWM31_L	-	-	-	-	PWM31_DATA [3:0]				R/W	0b 00000000
66	LED0_SLS	-	-	LED0_SLSTH [5:0]						R/W	0b 00000000
67	LED1_SLS	-	-	LED1_SLSTH [5:0]						R/W	0b 00000000

ADDR HEX	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	R/W	DEFAULT
68	LED2_SLS	-	-	LED2_SLSTH [5:0]						R/W	0b 00000000
69	LED3_SLS	-	-	LED3_SLSTH [5:0]						R/W	0b 00000000
6A	LED4_SLS	-	-	LED4_SLSTH [5:0]						R/W	0b 00000000
6B	LED5_SLS	-	-	LED5_SLSTH [5:0]						R/W	0b 00000000
6C	LED6_SLS	-	-	LED6_SLSTH [5:0]						R/W	0b 00000000
6D	LED7_SLS	-	-	LED7_SLSTH [5:0]						R/W	0b 00000000
6E	LED8_SLS	-	-	LED8_SLSTH [5:0]						R/W	0b 00000000
6F	LED9_SLS	-	-	LED9_SLSTH [5:0]						R/W	0b 00000000
70	LED10_SLS	-	-	LED10_SLSTH [5:0]						R/W	0b 00000000
71	LED11_SLS	-	-	LED11_SLSTH [5:0]						R/W	0b 00000000
72	LED12_SLS	-	-	LED12_SLSTH [5:0]						R/W	0b 00000000
73	LED13_SLS	-	-	LED13_SLSTH [5:0]						R/W	0b 00000000
74	LED14_SLS	-	-	LED14_SLSTH [5:0]						R/W	0b 00000000
75	LED15_SLS	-	-	LED15_SLSTH [5:0]						R/W	0b 00000000
76	LED16_SLS	-	-	LED16_SLSTH [5:0]						R/W	0b 00000000
77	LED17_SLS	-	-	LED17_SLSTH [5:0]						R/W	0b 00000000
78	LED18_SLS	-	-	LED18_SLSTH [5:0]						R/W	0b 00000000
79	LED19_SLS	-	-	LED19_SLSTH [5:0]						R/W	0b 00000000
7A	LED20_SLS	-	-	LED20_SLSTH [5:0]						R/W	0b 00000000
7B	LED21_SLS	-	-	LED21_SLSTH [5:0]						R/W	0b 00000000
7C	LED22_SLS	-	-	LED22_SLSTH [5:0]						R/W	0b 00000000
7D	LED23_SLS	-	-	LED23_SLSTH [5:0]						R/W	0b 00000000
7E	LED24_SLS	-	-	LED24_SLSTH [5:0]						R/W	0b 00000000
7F	LED25_SLS	-	-	LED25_SLSTH [5:0]						R/W	0b 00000000
80	LED26_SLS	-	-	LED26_SLSTH [5:0]						R/W	0b 00000000
81	LED27_SLS	-	-	LED27_SLSTH [5:0]						R/W	0b 00000000
82	LED28_SLS	-	-	LED28_SLSTH [5:0]						R/W	0b 00000000
83	LED29_SLS	-	-	LED29_SLSTH [5:0]						R/W	0b 00000000
84	LED30_SLS	-	-	LED30_SLSTH [5:0]						R/W	0b 00000000
85	LED31_SLS	-	-	LED31_SLSTH [5:0]						R/W	0b 00000000
86	FS_FLTL	-	-	-	-	FLT_UV[3:0]				R/W	0b 00000100
87	FLT_DET_EN	-	-	SLSDF	SLSDE	SDF	SDE	ODF	ODE	R/W	0b 00001111
88	FLT_CONFIG	-	SHCR	OPENCR	SLSHCR	FT [3:0]				R/W	0b 01100011
89	SHORT_FLT1	SHORT_FLT [7:0]								R	0b 00000000
8A	SHORT_FLT2	SHORT_FLT [15:8]								R	0b 00000000

ADDR HEX	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	R/W	DEFAULT
8B	SHORT_FLT3	SHORT_FLT [23:16]								R	0b 00000000
8C	SHORT_FLT4	SHORT_FLT [31:24]								R	0b 00000000
8D	OPEN_FLT1	OPEN_FLT [7:0]								R	0b 00000000
8E	OPEN_FLT2	OPEN_FLT [15:8]								R	0b 00000000
8F	OPEN_FLT3	OPEN_FLT [23:16]								R	0b 00000000
90	OPEN_FLT4	OPEN_FLT [31:27]								R	0b 00000000
91	SLS_FLT1	SLS_FLT [7:0]								R	0b 00000000
92	SLS_FLT2	SLS_FLT [15:8]								R	0b 00000000
93	SLS_FLT3	SLS_FLT [23:16]								R	0b 00000000
94	SLS_FLT4	SLS_FLT [31:24]								R	0b 00000000
95	FAULT_EN_1	ECC2F_EN	SCAF_EN	DUTYF_EN	TFE	CRCFE	RSET_OPE	RSET_SHE	TSDE	R/W	0b 11111111
96	FAULT_EN_2	-	-	-	IOUTVFE	VOFE	-	LUFE	VLUFE	R/W	0b 00011111
97	FAULT_TYPE_1	-	CRCF	CMWF2	CMWF1	TF	TSD	RSET_OP	RSET_SH	R/W	0b 00000000
98	FAULT_TYPE_2	-	IOUTVF	SCAVF	LPBF	EXF	SLSHORTF	SHORTF	OPENF	R/W	0b 00000000
99	FAULT_TYPE_3	-	-	-	-	-	VOF	LUF	VLUF	R/W	0b 00000000
9A	CERRCNT	CERRCNT [7:0]								R/W	0b 00000000
9B	CH_FS	OUT31_FS	-	-	-	-	-	DCFB_N [1:0]		R/W	0b 00000000
9C	DCFB_OCS	DCFB_OUT [7:0]								R/W	0b 10000000
9D	CHSEL	CHSEL [7:0]								R/W	0b 00000000
9E		CHSEL [15:8]								R/W	0b 00000000
9F		CHSEL [23:16]								R/W	0b 00000000
A0		CHSEL [31:24]								R/W	0b 00000000
A1		CHSEL [39:32]								R/W	0b 00000000
A2	ADCCFG	IOUTDC_RS[1:0]		OUT_SEL[1:0]		-	ADCSH [1:0]		ADCEN	R/W	0b 00000000
A3	ADCCTL	ADCCYC_F	OUTADC_N	OTM	ADCRST	ADCCYC_T[1:0]		LOOP	SADC	R/W	0b 00000010
A4	ADC_OUT0_H	ADC_OUT0[9:2]								R	0b 00000000
A5	ADC_OUT1_H	ADC_OUT1[9:2]								R	0b 00000000
A6	ADC_OUT2_H	ADC_OUT2[9:2]								R	0b 00000000
A7	ADC_OUT3_H	ADC_OUT3[9:2]								R	0b 00000000
A8	ADC_OUT0_1_2_3_L	ADC_OUT3[1:0]		ADC_OUT2[1:0]		ADC_OUT1[1:0]		ADC_OUT0[1:0]		R	0b 00000000
A9	ADC_OUT4_H	ADC_OUT4[9:2]								R	0b 00000000
AA	ADC_OUT5_H	ADC_OUT5[9:2]								R	0b 00000000
AB	ADC_OUT6_H	ADC_OUT6[9:2]								R	0b 00000000
AC	ADC_OUT7_H	ADC_OUT7[9:2]								R	0b 00000000
AD	ADC_OUT4_5_6_7_L	ADC_OUT7[1:0]		ADC_OUT6[1:0]		ADC_OUT5[1:0]		ADC_OUT4[1:0]		R	0b 00000000

ADDR HEX	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	R/W	DEFAULT
AE	ADC_OUT8_H	ADC_OUT8[9:2]								R	0b 00000000
AF	ADC_OUT9_H	ADC_OUT9[9:2]								R	0b 00000000
B0	ADC_OUT10_H	ADC_OUT10[9:2]								R	0b 00000000
B1	ADC_OUT11_H	ADC_OUT11[9:2]								R	0b 00000000
B2	ADC_OUT8_9_10_11_L	ADC_OUT11[1:0]		ADC_OUT10[1:0]		ADC_OUT9[1:0]		ADC_OUT8[1:0]		R	0b 00000000
B3	ADC_OUT12_H	ADC_OUT12[9:2]								R	0b 00000000
B4	ADC_OUT13_H	ADC_OUT13[9:2]								R	0b 00000000
B5	ADC_OUT14_H	ADC_OUT14[9:2]								R	0b 00000000
B6	ADC_OUT15_H	ADC_OUT15[9:2]								R	0b 00000000
B7	ADC_OUT12_13_14_15_L	ADC_OUT15[1:0]		ADC_OUT14[1:0]		ADC_OUT13[1:0]		ADC_OUT12[1:0]		R	0b 00000000
B8	ADC_OUT16_H	ADC_OUT16[9:2]								R	0b 00000000
B9	ADC_OUT17_H	ADC_OUT17[9:2]								R	0b 00000000
BA	ADC_OUT18_H	ADC_OUT18[9:2]								R	0b 00000000
BB	ADC_OUT19_H	ADC_OUT19[9:2]								R	0b 00000000
BC	ADC_OUT16_17_18_19_L	ADC_OUT19[1:0]		ADC_OUT18[1:0]		ADC_OUT17[1:0]		ADC_OUT16[1:0]		R	0b 00000000
BD	ADC_OUT20_H	ADC_OUT20[9:2]								R	0b 00000000
BE	ADC_OUT21_H	ADC_OUT21[9:2]								R	0b 00000000
BF	ADC_OUT22_H	ADC_OUT22[9:2]								R	0b 00000000
C0	ADC_OUT23_H	ADC_OUT23[9:2]								R	0b 00000000
C1	ADC_OUT20_21_22_23_L	ADC_OUT23[1:0]		ADC_OUT22[1:0]		ADC_OUT21[1:0]		ADC_OUT20[1:0]		R	0b 00000000
C2	ADC_OUT24_H	ADC_OUT24[9:2]								R	0b 00000000
C3	ADC_OUT25_H	ADC_OUT25[9:2]								R	0b 00000000
C4	ADC_OUT26_H	ADC_OUT26[9:2]								R	0b 00000000
C5	ADC_OUT27_H	ADC_OUT27[9:2]								R	0b 00000000
C6	ADC_OUT24_25_26_27_L	ADC_OUT27[1:0]		ADC_OUT26[1:0]		ADC_OUT25[1:0]		ADC_OUT24[1:0]		R	0b 00000000
C7	ADC_OUT28_H	ADC_OUT28[9:2]								R	0b 00000000
C8	ADC_OUT29_H	ADC_OUT29[9:2]								R	0b 00000000
C9	ADC_OUT30_H	ADC_OUT30[9:2]								R	0b 00000000
CA	ADC_OUT31_H	ADC_OUT31[9:2]								R	0b 00000000
CB	ADC_OUT28_29_30_31_L	ADC_OUT31[1:0]		ADC_OUT30[1:0]		ADC_OUT29[1:0]		ADC_OUT28[1:0]		R	0b 00000000
CC	ADC_ VHR 0_31_MIN_H	ADC_VHR0_31_MIN [9:2]								R	0b 00000000
CD	ADC_ VHR 0_31_MIN_L	-	-	-	-	-	-	ADC_ VHR 0_31_MIN [1:0]		R	0b 00000000
CE	ADC_VREF_H	ADC_VREF [9:2]								R	0b 00000000
CF	ADC_VREF _L	-	-	-	-	-	-	ADC_VREF [1:0]		R	0b 00000000
D0	ADC_VPTAT_H	ADC_VPTAT [9:2]								R	0b 00000000

ADDR HEX	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	R/W	DEFAULT
D1	ADC_VPTAT _L	-	-	-	-	-	-	ADC_VPTAT [1:0]		R	0b 00000000
D2	ADC_VLED _H	ADC_VLED [9:2]								R	0b 00000000
D3	ADC_VLED _L	-	-	-	-	-	-	ADC_VLED [1:0]		R	0b 00000000
D4	ADC_ VIN_H	ADC_ VIN [9:2]								R	0b 00000000
D5	ADC_ VIN _L	-	-	-	-	-	-	ADC_ VIN [1:0]		R	0b 00000000
D6	ADC_VBG _H	ADC_VBG [9:2]								R	0b 00000000
D7	ADC_VBG _L	-	-	-	-	-	-	ADC_VBG [1:0]		R	0b 00000000
D8	ADC_IN1 _H	ADC_IN1 [9:2]								R	0b 00000000
D9	ADC_ IN1 _L	-	-	-	-	-	-	ADC_ IN1[1:0]		R	0b 00000000
DA	ADC_IN2 _H	ADC_IN2 [9:2]								R	0b 00000000
DB	ADC_ IN2 _L	-	-	-	-	-	-	ADC_ IN2[1:0]		R	0b 00000000
DC	ADC_VLDO5V _H	ADC_VLDO5V [9:2]								R	0b 00000000
DD	ADC_VLDO5V _L	-	-	-	-	-	-	ADC_VLDO5V [1:0]		R	0b 00000000
verification											
DE	BSTSTA	-	-	-	-	-	-	FAIL	FINISH	R	0b 00000000
DF	VFYCTL	MODE [1:0]		-	TOLERANCE [4:0]					R/W	0b 00010010
E0	VFYCFG	START/BUSY	-	ALE	PWM_LB_SEL[4:0]					R/W	0b 00000000
E1	DUTYF_1	DUTYFLT [7:0]								R	0b 00000000
E2	DUTYF_2	DUTYFLT [15:8]								R	0b 00000000
E3	DUTYF_3	DUTYFLT [23:16]								R	0b 00000000
E4	DUTYF_4	DUTYFLT [31:24]								R	0b 00000000
E5	PWMDUTY_H	PWMDUTY [15:8]								R	0b 00000000
E6	PWMDUTY_L	PWMDUTY [7:0]								R	0b 00000000
E7	SEL_PWM_DUTY_H	SEL_PWMDUTY [15:8]								R	0b 00000000
E8	SEL_PWM_DUTY_L	SEL_PWMDUTY [7:0]								R	0b 00000000
E9	SCACTL	-	-	IOUT_LE	OUTDC_FINJ	OUTDC_EN	-	-	SCA_TEN	R/W	0b 00000000
EA	IOUT_1	IOUT_FLT [7:0]								R	0b 00000000
EB	IOUT_2	IOUT_FLT [15:8]								R	0b 00000000
EC	IOUT_3	IOUT_FLT [23:16]								R	0b 00000000
ED	IOUT_4	IOUT_FLT [31:24]								R	0b 00000000
EE	RSETDATA	-	RSETDATA[6:0]							R/W	0b 00000000

13.2 Page 1 (00h~F3h): OTP REGISTER

OTP-Registers											
00	OTP_CTRL	p1	p0	Cmd[1:0]		Sel[3:0]				R/W	0b 00000000
01	OTP_ST	-	-	-	-	-	FAIL	FINISH	BUSY	R	0b 00000000
02	ECC_ST	-	IMD_2Err_eccA	-	IMD_1Err_eccA	-	-	-	-	R	0b 00000000
OTP-A											
10	DEFCONF	DEFDC_PWM	WDT_FS [1:0]		DEFPFS [4:0]					R/W	0b 00000000
11	DEFGCC	DEF_GCC [7:0]								R/W	0b 00000000
12	DEFTEMP_SSCEN	-	DEFSSCEN	DEFSSC [1:0]		-	DEFTROF [2:0]			R/W	0b 00000000
13	DEFLED1	DEFLED [7:0]								R/W	0b 00000000
14	DEFLED2	DEFLED [15:8]								R/W	0b 00000000
15	DEFLED3	DEFLED [23:16]								R/W	0b 00000000
16	DEFLED4	DEFLED [31:24]								R/W	0b 00000000
17	DEFPWM1	PWM1[3:0]				PWM0[3:0]				R/W	0b 00000000
18	DEFPWM2	PWM3[3:0]				PWM2[3:0]				R/W	0b 00000000
19	DEFPWM3	PWM5[3:0]				PWM4[3:0]				R/W	0b 00000000
1A	DEFPWM4	PWM7[3:0]				PWM6[3:0]				R/W	0b 00000000
1B	DEFPWM5	PWM9[3:0]				PWM8[3:0]				R/W	0b 00000000
1C	DEFPWM6	PWM11[3:0]				PWM10[3:0]				R/W	0b 00000000
1D	DEFPWM7	PWM13[3:0]				PWM12[3:0]				R/W	0b 00000000
1E	DEFPWM8	PWM15[3:0]				PWM14[3:0]				R/W	0b 00000000
1F	ECC_A1	ECCA1								R/W	0b 00000000
20	DEFPWM9	PWM17[3:0]				PWM16[3:0]				R/W	0b 00000000
21	DEFPWM10	PWM19[3:0]				PWM18[3:0]				R/W	0b 00000000
22	DEFPWM11	PWM21[3:0]				PWM20[3:0]				R/W	0b 00000000
23	DEFPWM12	PWM23[3:0]				PWM22[3:0]				R/W	0b 00000000

24	DEFPWM13	PWM25[3:0]	PWM24[3:0]	R/W	0b 00000000
25	DEFPWM14	PWM27[3:0]	PWM26[3:0]	R/W	0b 00000000
26	DEFPWM15	PWM29[3:0]	PWM28[3:0]	R/W	0b 00000000
27	DEFPWM16	PWM31[3:0]	PWM30[3:0]	R/W	0b 00000000
28	ECC_A2	ECCA2		W	0b 00000000
29	W_PROTECT_A	WPROTECTA		W	0b 00000000
FC	OTP_UNLOCK	OTPUNLOCK		W	0b 00000000

13.3 REGISTERS DEFINITION

13.3.1 00h CONFIG1 Register

ADDR	REG NAME	D7	D6	D5	D4:D0	DEFAULT
00h	CONFIG1	-	PDE	DC_PWM	PFS [4:0]	0b 01001111

PDE Phase delay enable
0 Disable
1 Enable (8 groups phase delay)

DC_PWM DC or PWM output select for all outputs
0 PWM dimming. PWM duty cycle is determined by PWM registers 26h~55h
1 DC output. PWM dimming is disabled, and all outputs are DC current (I_{OUTx})

PFS PWM Frequency Setting
00000 8bit Linearity, 25.6kHz, 6.5M
00001 8bit Linearity, 12.8kHz, 6.5M
00010 8bit Linearity, 6.4kHz, 6.5M
00011 8bit Linearity, 3.2kHz, 6.5M
00100 8bit Linearity, 1.6kHz, 6.5M
00101 8bit Linearity, 1.4kHz, 6.5M
00110 8bit Linearity, 1.2kHz, 6.5M
00111 8bit Linearity, 1kHz, 6.5M
01000 8bit Linearity, 700Hz, 6.5M
01001 8bit Linearity, 500Hz, 6.5M
01010 8bit Linearity, 400Hz, 6.5M
01011 8bit Linearity, 300Hz, 6.5M
01100 7+5bit Linearity, 25.6kHz
01101 7+5bit Linearity, 25.6kHz
01110 12bit Linearity, 1.6kHz, 6.5M
01111 12bit Linearity, 400Hz, 6.5M(default)
10000 12bit Linearity, 200Hz, 6.5M
10001 8bit Gamma, 1.6kHz6.5M
10010 8bit Gamma, 800Hz, 6.5M
10011 8bit Gamma, 400Hz, 6.5M
10100 8bit Gamma, 200Hz, 6.5M
10101 12bit Linearity, 5Hz, 6.5M(for blink)
10110 12bit Linearity, 2.5Hz, 6.5M(for blink)
10111 12bit Linearity, 1.25Hz, 6.5M(for blink)

Others 12bit Linearity, 400Hz, 6.5M
Note: 10101/10110/10110 the two updates of the three options must be greater than 1ms.

13.3.2 01h CONFIG2 Register

ADDR	REG NAME	D7:D6	D5:D4	D3	D2:D0	DEFAULT
01h	CONFIG2	-	OFA [1:0]	-	TROF [2:0]	0b 00110000

The current of thermal roll off will not be a fixed proportion, and the slope of roll off can be calculated by formula. I_{ROLL}= Iset × (2V-Vx) / 2, I_{ROLL} is the current after roll off, I_{SET} is the current before roll off, and Vx is the optional voltage (TROF bits) of the register.

OFAx "One Fail Others On" or "One Fail All Fail" fault action mode setting
0x "One Fail All Fail" (single LED short fault latches all outputs off, open or short auto recover)
10 "One Fail All Fail" (auto recover)
11 "One Fail Others On"(default)

TROF Percentage of output current before thermal shutdown happens
000 0V(default)
001 0.2V
010 0.4V
011 0.6V
100 0.8V
101 1.0V
110 1.2V
111 1.4V

13.3.3 02h CONFIG3 Register

ADDR	REG NAME	D7	D6:D5	D4:D3	D2:D1	D0	DEFAULT
02h	CONFIG3	SSCEN	SSC [1:0]	ACKSEL[1:0]	-	PWR	0b 00000000

ACKSEL Acknowledge Data Select
00 Disable, No acknowledge is transmitted following successfully received writes(default)
01 Return 0x7F
10 Return ACK_DATA
11 Return ACK_DATA+ACK_CRC

ACKSEL	ACK_DATA				
[1:0]	D7:D4	D3	D2	D1	D0
00	-	-	-	-	-
01	0111	1	1	1	1
10		1	0: normal 1: 99h(page0) is not 0x00	0: normal 1: 98h(page0) is not 0x00	0: normal 1: 97h(page0) is not 0x00
11		0			

PWR This bit is reset to 0 upon power-up. It may be written to a 1 by the MCU. Reading this bit allow the MCU to detect if there has been a power cycle.
0 A power cycle has occurred since last write to a '1'
1 No power cycle has occurred since the last write to a '1'

SSCEN Spread Spectrum Enable
0 Disable
1 Enable-not allowed when PWM frequency is 200Hz

SSC Spread Spectrum frequency Range
00 125Hz
01 250Hz
10 500Hz
11 1kHz

13.3.4 03h Watchdog Timer 1 Register

ADDR	REG NAME	D7:D3	D2:D0	DEFAULT
03h	CMWT1	-	CMWTAP [2:0]	0b 00000011

CMWTAP [2:0] This 3-bit value selects the tap point (i.e., bit number, starting from 0) on the 24-bit communications watchdog timer to establish the time-out condition.
000 8ms
001 16ms
010 32ms
011 64ms(default)
100 128ms
101 256ms
110 512ms
111 1024ms

13.3.5 04h Watchdog Timer 2 Register

ADDR	REG NAME	D7	D6:D4	D3	D2:D0	DEFAULT
04h	CMWT2	WDT2CLR	WDT2_MAX[2:0]	-	WDT2_MIN[2:0]	0b 00110000

WDT2CLR WDT2 Counter Clear, Writing “1” to WDT2CLR clears the WDT2 count to 0. It is self-cleared by hardware.

WDT2MAX with 8M clock
000 8ms
001 16ms
010 32ms
011 64ms(default)
100 128ms
101 256ms
110 512ms
111 1024ms
WDT2MAX hold the timeout value for watchdog timer 2. When the counter reaches WDT2 timeout value, a fault flag is generated.

WDT2MIN with 8M clock
000 8ms(default)
001 16ms
010 32ms
011 64ms
100 128ms
101 256ms
110 512ms
111 1024ms
WDT2MIN hold the timeout value for watchdog timer 2. If WDT2 is cleared before reaching WDT2MIN, a fault flag is also generated.

13.3.6 05h GC_CTRL Register

ADDR	REG NAME	D7:D0	DEFAULT
05h	GC_CTRL	GCC [7:0]	0b 11111111

GCC and SCAx control the I_{OUT} as shown in following formula:

$$I_{OUT\_F} = I_{OUT(MAX)} \times \frac{GCC}{255} \times \frac{SCAx}{255} \quad (9)$$

$$GCC = \sum_{n=0}^{7} D[n] \cdot 2^n \quad (10)$$

$$SCAx = \sum_{n=0}^{7} D[n] \cdot 2^n \quad (11)$$

11.3.7 06h~25h Scaling Registers

ADDR	REG NAME	D7:D0	DEFAULT
06h	SCA0	SCA0_DATA [7:0]	0b 00000000
07h	SCA1	SCA1_DATA [7:0]	0b 00000000
08h	SCA2	SCA2_DATA [7:0]	0b 00000000
09h	SCA3	SCA3_DATA [7:0]	0b 00000000
0Ah	SCA4	SCA4_DATA [7:0]	0b 00000000
0Bh	SCA5	SCA5_DATA [7:0]	0b 00000000
0Ch	SCA6	SCA6_DATA [7:0]	0b 00000000
0Dh	SCA7	SCA7_DATA [7:0]	0b 00000000
0Eh	SCA8	SCA8_DATA [7:0]	0b 00000000
0Fh	SCA9	SCA9_DATA [7:0]	0b 00000000
10h	SCA10	SCA10_DATA [7:0]	0b 00000000
11h	SCA11	SCA11_DATA [7:0]	0b 00000000
12h	SCA12	SCA12_DATA [7:0]	0b 00000000
13h	SCA13	SCA13_DATA [7:0]	0b 00000000
14h	SCA14	SCA14_DATA [7:0]	0b 00000000
15h	SCA15	SCA15_DATA [7:0]	0b 00000000
16h	SCA16	SCA16_DATA [7:0]	0b 00000000
17h	SCA17	SCA17_DATA [7:0]	0b 00000000
18h	SCA18	SCA18_DATA [7:0]	0b 00000000
19h	SCA19	SCA19_DATA [7:0]	0b 00000000
1Ah	SCA20	SCA20_DATA [7:0]	0b 00000000
1Bh	SCA21	SCA21_DATA [7:0]	0b 00000000
1Ch	SCA22	SCA22_DATA [7:0]	0b 00000000
1Dh	SCA23	SCA23_DATA [7:0]	0b 00000000
1Eh	SCA24	SCA24_DATA [7:0]	0b 00000000
1Fh	SCA25	SCA25_DATA [7:0]	0b 00000000
20h	SCA26	SCA26_DATA [7:0]	0b 00000000
21h	SCA27	SCA27_DATA [7:0]	0b 00000000
22h	SCA28	SCA28_DATA [7:0]	0b 00000000
23h	SCA29	SCA29_DATA [7:0]	0b 00000000
24h	SCA30	SCA30_DATA [7:0]	0b 00000000
25h	SCA31	SCA31_DATA [7:0]	0b 00000000

The 8-bit Scaling Registers SCAx (06h~25h) individually set the DC output current of each channel.

GCC [7:0] and SCAx control the OUTx current (I_{OUTx})as shown in following equation:

$$I_{OUTx} = I_{OUT\_FU} \times \frac{GCC}{255} \times \frac{SCAx}{255} \quad (12)$$

Where, x is from 0 to 31 for different output channel.

$$GCC = \sum_{n=0}^{7} D[n] \cdot 2^n \qquad (13)$$

$$SCAx = \sum_{n=0}^{7} D[n] \cdot 2^n \qquad (14)$$

13.3.8 26h~65h PWM Registers

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
26h	PWM0_H	PWM0_DATA [11:4]								0b 00000000
27h	PWM1_H	PWM1_DATA [11:4]								0b 00000000
28h	PWM2_H	PWM2_DATA [11:4]								0b 00000000
29h	PWM3_H	PWM3_DATA [11:4]								0b 00000000
2Ah	PWM4_H	PWM4_DATA [11:4]								0b 00000000
2Bh	PWM5_H	PWM5_DATA [11:4]								0b 00000000
2Ch	PWM6_H	PWM6_DATA [11:4]								0b 00000000
2Dh	PWM7_H	PWM7_DATA [11:4]								0b 00000000
2Eh	PWM8_H	PWM8_DATA [11:4]								0b 00000000
2Fh	PWM9_H	PWM9_DATA [11:4]								0b 00000000
30h	PWM10_H	PWM10_DATA [11:4]								0b 00000000
31h	PWM11_H	PWM11_DATA [11:4]								0b 00000000
32h	PWM12_H	PWM12_DATA [11:4]								0b 00000000
33h	PWM13_H	PWM13_DATA [11:4]								0b 00000000
34h	PWM14_H	PWM14_DATA [11:4]								0b 00000000
35h	PWM15_H	PWM15_DATA [11:4]								0b 00000000
36h	PWM16_H	PWM16_DATA [11:4]								0b 00000000
37h	PWM17_H	PWM17_DATA [11:4]								0b 00000000
38h	PWM18_H	PWM18_DATA [11:4]								0b 00000000
39h	PWM19_H	PWM19_DATA [11:4]								0b 00000000
3Ah	PWM20_H	PWM20_DATA [11:4]								0b 00000000
3Bh	PWM21_H	PWM21_DATA [11:4]								0b 00000000
3Ch	PWM22_H	PWM22_DATA [11:4]								0b 00000000
3Dh	PWM23_H	PWM23_DATA [11:4]								0b 00000000
3Eh	PWM24_H	PWM24_DATA [11:4]								0b 00000000
3Fh	PWM25_H	PWM25_DATA [11:4]								0b 00000000
40h	PWM26_H	PWM26_DATA [11:4]								0b 00000000
41h	PWM27_H	PWM27_DATA [11:4]								0b 00000000
42h	PWM28_H	PWM28_DATA [11:4]								0b 00000000
43h	PWM29_H	PWM29_DATA [11:4]								0b 00000000
44h	PWM30_H	PWM30_DATA [11:4]								0b 00000000
45h	PWM31_H	PWM31_DATA [11:4]								0b 00000000
46h	PWM0_L	-	-	-	-	PWM0_DATA [3:0]				0b 00000000
47h	PWM1_L	-	-	-	-	PWM1_DATA [3:0]				0b 00000000
48h	PWM2_L	-	-	-	-	PWM2_DATA [3:0]				0b 00000000
49h	PWM3_L	-	-	-	-	PWM3_DATA [3:0]				0b 00000000
4Ah	PWM4_L	-	-	-	-	PWM5_DATA [3:0]				0b 00000000
4Bh	PWM5_L	-	-	-	-	PWM4_DATA [3:0]				0b 00000000
4Ch	PWM6_L	-	-	-	-	PWM6_DATA [3:0]				0b 00000000
4Dh	PWM7_L	-	-	-	-	PWM7_DATA [3:0]				0b 00000000
4Eh	PWM8_L	-	-	-	-	PWM8_DATA [3:0]				0b 00000000
4Fh	PWM9_L	-	-	-	-	PWM9_DATA [3:0]				0b 00000000

50h	PWM10_L	-	-	-	-	PWM10_DATA [3:0]	0b 00000000
51h	PWM11_L	-	-	-	-	PWM11_DATA [3:0]	0b 00000000
52h	PWM12_L	-	-	-	-	PWM12_DATA [3:0]	0b 00000000
53h	PWM13_L	-	-	-	-	PWM13_DATA [3:0]	0b 00000000
54h	PWM14_L	-	-	-	-	PWM14_DATA [3:0]	0b 00000000
55h	PWM15_L	-	-	-	-	PWM15_DATA [3:0]	0b 00000000
56h	PWM16_L	-	-	-	-	PWM16_DATA [3:0]	0b 00000000
57h	PWM17_L	-	-	-	-	PWM17_DATA [3:0]	0b 00000000
58h	PWM18_L	-	-	-	-	PWM18_DATA [3:0]	0b 00000000
59h	PWM19_L	-	-	-	-	PWM19_DATA [3:0]	0b 00000000
5Ah	PWM20_L	-	-	-	-	PWM20_DATA [3:0]	0b 00000000
5Bh	PWM21_L	-	-	-	-	PWM21_DATA [3:0]	0b 00000000
5Ch	PWM22_L	-	-	-	-	PWM22_DATA [3:0]	0b 00000000
5Dh	PWM23_L	-	-	-	-	PWM23_DATA [3:0]	0b 00000000
5Eh	PWM24_L	-	-	-	-	PWM24_DATA [3:0]	0b 00000000
5Fh	PWM25_L	-	-	-	-	PWM25_DATA [3:0]	0b 00000000
60h	PWM26_L	-	-	-	-	PWM26_DATA [3:0]	0b 00000000
61h	PWM27_L	-	-	-	-	PWM27_DATA [3:0]	0b 00000000
62h	PWM28_L	-	-	-	-	PWM28_DATA [3:0]	0b 00000000
63h	PWM29_L	-	-	-	-	PWM29_DATA [3:0]	0b 00000000
64h	PWM30_L	-	-	-	-	PWM30_DATA [3:0]	0b 00000000
65h	PWM31_L	-	-	-	-	PWM31_DATA [3:0]	0b 00000000

Each OUTx has 12-bit (or 7+5-bit) to modulate the PWM duty cycle in 4096 steps.

The value of the PWM Registers decides the average current of each OUTx LED noted I_{LED}.

I_{LED} computed by following formula:

$$I_{OUTx\_PWM} = I_{OUTx} \times D_{PWMx} \qquad (15)$$

Where D_{PWMx} is the duty cycle of each channel independently programmed by PWM Registers (26h~65h), in 12bit or 7+5-bit PWM mode:

$$D_{PWMx} = \frac{\sum_{n=0}^{11} D[n] \cdot 2^n}{4096} \qquad (16)$$

In 8bit PWM mode:

$$D_{PWMx} = \frac{\sum_{n=0}^{7} D[n] \cdot 2^n}{256} \qquad (17)$$

13.3.9 66h~85h Single LED Short Threshold Setting Registers

ADDR	REG NAME	D7	D6	D5:D0	DEFAULT
66h	LED0_SLS	-	-	LED0_SLSTH [5:0]	0b 00000000
67h	LED1_SLS	-	-	LED1_SLSTH [5:0]	0b 00000000
68h	LED2_SLS	-	-	LED2_SLSTH [5:0]	0b 00000000
69h	LED3_SLS	-	-	LED3_SLSTH [5:0]	0b 00000000
6Ah	LED4_SLS	-	-	LED4_SLSTH [5:0]	0b 00000000
6Bh	LED5_SLS	-	-	LED5_SLSTH [5:0]	0b 00000000
6Ch	LED6_SLS	-	-	LED6_SLSTH [5:0]	0b 00000000
6Dh	LED7_SLS	-	-	LED7_SLSTH [5:0]	0b 00000000
6Eh	LED8_SLS	-	-	LED8_SLSTH [5:0]	0b 00000000
6Fh	LED9_SLS	-	-	LED9_SLSTH [5:0]	0b 00000000

ADDR	REG NAME	D7	D6	D5:D0	DEFAULT
70h	LED10_SLS	-	-	LED10_SLSTH [5:0]	0b 00000000
71h	LED11_SLS	-	-	LED11_SLSTH [5:0]	0b 00000000
72h	LED12_SLS	-	-	LED12_SLSTH [5:0]	0b 00000000
73h	LED13_SLS	-	-	LED13_SLSTH [5:0]	0b 00000000
74h	LED14_SLS	-	-	LED14_SLSTH [5:0]	0b 00000000
75h	LED15_SLS	-	-	LED15_SLSTH [5:0]	0b 00000000
76h	LED16_SLS	-	-	LED16_SLSTH [5:0]	0b 00000000
77h	LED17_SLS	-	-	LED17_SLSTH [5:0]	0b 00000000
78h	LED18_SLS	-	-	LED18_SLSTH [5:0]	0b 00000000
79h	LED19_SLS	-	-	LED19_SLSTH [5:0]	0b 00000000
7Ah	LED20_SLS	-	-	LED20_SLSTH [5:0]	0b 00000000
7Bh	LED21_SLS	-	-	LED21_SLSTH [5:0]	0b 00000000
7Ch	LED22_SLS	-	-	LED22_SLSTH [5:0]	0b 00000000
7Dh	LED23_SLS	-	-	LED23_SLSTH [5:0]	0b 00000000
7Eh	LED24_SLS	-	-	LED24_SLSTH [5:0]	0b 00000000
7Fh	LED25_SLS	-	-	LED25_SLSTH [5:0]	0b 00000000
80h	LED26_SLS	-	-	LED26_SLSTH [5:0]	0b 00000000
81h	LED27_SLS	-	-	LED27_SLSTH [5:0]	0b 00000000
82h	LED28_SLS	-	-	LED28_SLSTH [5:0]	0b 00000000
83h	LED29_SLS	-	-	LED29_SLSTH [5:0]	0b 00000000
84h	LED30_SLS	-	-	LED30_SLSTH [5:0]	0b 00000000
85h	LED31_SLS	-	-	LED31_SLSTH [5:0]	0b 00000000

LEDx_SLSTH Singe LED short threshold voltage 0.26V/step

000000 2.5V
000001 2.76V
000010 3.02V
000011 3.28V
000100 3.54V
000101 3.8V
000110 4.06V
000111 4.32V
001000 4.58V
001001 4.84V
001010 5.1V
…… ……
111011 17.84V
111100 18.1V
111101 18.36V
111110 18.62V
111111 18.88V

13.3.10 86h FS_FLTL register

ADDR	REG NAME	D7:D4	D3:D0	DEFAULT
86h	FS_FLTL	-	FLT_UV[3:0]	0b 00000100

FLT_UV set UVLO threshold VFLT_UV for the LED open fault detection and single LED short fault detection to prevent false fault triggering due to insufficient power supply voltage:

FLT_UV	UVLO threshold voltage for the LED open fault detection and single LED short fault detection
0000	4.5V
0001	5V
0010	6V
0011	7V
0100	8V(default)
0101	9V
0110	10V
0111	11V
1000	12V
1001	13V
1010	14V
1011	15V
1100	16V
1101	17V
1110	18V
1111	19V

13.3.11 87h Diagnostic Register

ADDR	REG NAME	D7:D6	D5	D4	D3	D2	D1	D0	DEFAULT
87h	FLT_DET_EN	-	SLSDF	SLSDE	SDF	SDE	ODF	ODE	0b 00001111

SLSDF	Single LED Short Report Enable at FAULTB pin
0	Report disabled
1	Report enabled

SLSDE	Single LED Short Detect Enable
0	Detect disabled
1	Detect enabled

SDF	Short Report Enable at FAULTB pin
0	Report disabled
1	Report enabled

SDE	Short Detect Enable
0	Detect disabled
1	Detect enabled

ODF	Open Report Enable at FAULTB pin
0	Report disabled
1	Report enabled

ODE	Open Detect Enable
0	Detect disabled
1	Detect enabled

13.3.12 88h~94h Diagnostic Registers

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
88h	FLT_CONFIG	-	SHCR	OPENCR	SLSHCR	FT [3:0]				0b 01100011
89h	SHORT_FLT1	SHORT_FLT [7:0]								0b 00000000
8Ah	SHORT_FLT2	SHORT_FLT [15:8]								0b 00000000
8Bh	SHORT_FLT3	SHORT_FLT [23:16]								0b 00000000
8Ch	SHORT_FLT4	SHORT_FLT [31:24]								0b 00000000
8Dh	OPEN_FLT1	OPEN_FLT [7:0]								0b 00000000
8Eh	OPEN_FLT2	OPEN_FLT [15:8]								0b 00000000
8Fh	OPEN_FLT3	OPEN_FLT [23:16]								0b 00000000
90h	OPEN_FLT4	OPEN_FLT [31:27]								0b 00000000
91h	SLS_FLT1	SLS_FLT [7:0]								0b 00000000
92h	SLS_FLT2	SLS_FLT [15:8]								0b 00000000
93h	SLS_FLT3	SLS_FLT [23:16]								0b 00000000
94h	SLS_FLT4	SLS_FLT [31:24]								0b 00000000

FT Fault report delay time setting
0000 32us
0001 64us
0010 128us
0011 256us(default)
0100 512us
0101 1.024ms
0110 2.048ms
0111 4.096ms
1000 7.8125ms
1001 15.625ms
1010 31.25ms
1011 62.5ms
1100 0.125s
1101 0.25s
1110 0.5s
1111 1s

SLSHCR Single LED short output current reduce
0 No reduce
1 Output current reduced to 4mA (Typ.)

SHCR LED short output current reduce
0 No reduce
1 Output current reduced to 4mA (Typ.)

OPENCR LED OPEN output current reduce
0 No reduce
1 Output current reduced to 4mA (Typ.)

SHORT_FLTx LED string short fault flag for each OUT0~OUT31
0 No LED string shorted
1 LED string shorted

OPEN_FLTx LED string open fault flag for each OUT0~OUT31
0 No LED string open
1 LED string open

SLS_FLTx Single LED short fault flag for each OUT0~OUT31
0 No single LED shorted
1 Single LED shorted

13.3.13 95h Fault Diagnostic1 Register

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
95h	FAULT_EN_1	ECC2F_EN	SCAF_EN	DUTYF_EN	TFE	CRCFE	RSET_OPE	RSET_SHE	TSDE	0b 11111111

ECC2F_EN ECC2 error Report Enable at FAULTB pin
0 Report disabled
1 Report enabled

SCAF_EN SCA verification fail Report Enable at FAULTB pin
0 Report disabled
1 Report enabled

DUTYF_EN loop back fail Report Enable at FAULTB pin
0 Report disabled
1 Report enabled

TFE Thermal rolloff Report Enable at FAULTB pin
0 Report disabled
1 Report enabled

CRCFE Interface communication Check Sum Failure Report Enable at FAULTB pin
0 Report disabled
1 Report enabled

RSET_OPE ISET pin open Report Enable at FAULTB pin
0 Report disabled
1 Report enabled

RSET_SHE ISET pin short Report Enable at FAULTB pin
0 Report disabled
1 Report enabled

TSDE Thermal shutdown Report Enable at FAULTB pin
0 Report disabled
1 Report enabled

13.3.14 96h Fault Diagnostic2 Register

ADDR	REG NAME	D7:D5	D4	D3	D2	D1	D0	DEFAULT
96h	FAULT_EN_2	-	IOUTVFE	VOFE	-	LUFE	VLUFE	0b 00011111

IOUTVFE IOUT verification fault Report Enable at FAULTB pin
0 Report disabled
1 Report enabled

VOFE VDD Overvoltage Report Enable at FAULTB pin
0 Report disabled
1 Report enabled

LUFE LDO5V Under Voltage Report Enable at FAULTB pin
0 Report disabled
1 Report enabled

VLUFE VLED Under Voltage Report Enable at FAULTB pin
0 Report disabled
1 Report enabled

13.3.15 97h Fault Type1 Register

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
97h	FAULT_TYPE_1	-	CRCF	CMWF2	CMWF1	TF	TSD	RSET_OP	RSET_SH	0b 00000000

Fault flags. When bit=1, fault flag is asserted.

CRCF Interface communication Check Sum Failure fault flag
0 No communication Check Sum Failure
1 Communication Check Sum Failure

CMWF2 Watch dog 2 Communication Time-Out fault flag
0 No communication time-out
1 Communication time-out

CMWF1 Watch dog 1 Communication Time-Out fault flag
0 No communication time-out
1 Communication time-out

TF Thermal rolloff fault flag
0 No thermal rolloff
1 Thermal rolloff

TSD Thermal shutdown fault flag
0 No thermal shutdown
1 Thermal shutdown

RSET_OP ISET pin open fault flag
0 No open
1 Opened

RSET_SH ISET pin short fault flag
0 No short
1 Shorted

13.3.16 98h Fault Type2 Register

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
98h	FAULT_TYPE_2	-	IOUTVF	SCAVF	LPBF	EXF	SLSHORTF	SHORTF	OPENF	0b 00000000

Fault flags. When bit=1, fault flag is asserted.

IOUTVF IOUT verification fault flag
0 No failure
1 Failure

SCAVF SCA verification fault flag. Any output occurs SCA verification failure, this bit will set to “1”.
0 No failure
1 Failure

LPBF Loopback fault flag. Any output occurs loopback verification failure, this bit will set to “1”.
0 No loopback failure
1 Loopback failure

EXF external fault flag
0 No fault pin pulled down externally
1 Fault pin pulled down externally

SLSHORTF Single LED Short fault flag. Any out occurs single LED short, this bit will set to 1.
0 No single LED short
1 Single LED short

SHORTF LED Short fault flag. Any out occurs LED short, this bit will set to 1.
0 No LED short
1 LED short

OPENF LED Open fault flag. Any out occurs LED open, this bit will set to 1.
0 No LED open
1 LED open

13.3.17 99h Fault Type3 Register

ADDR	REG NAME	D7:D4	D3	D2	D1	D0	DEFAULT
99h	FAULT_TYPE_3	-	-	VOF	LUF	VLUF	0b 00000000

Fault flags. When bit=1, fault flag is asserted.

VOF VDD over voltage fault flag
0 normal
1 overvoltage happen

LUF LDO5V under voltage fault flag
0 normal
1 under voltage happen

VLUF VLED under voltage fault flag
0 normal
1 under voltage happen

13.3.18 9Ah Diagnostic Register (Continue)

ADDR	REG NAME	D7:D0	DEFAULT
9Ah	CERRCNT	CERRCNT [7:0]	0b 00000000

This register value is incremented each time a CRC error is received. This register may be read by the MCU and then written back to 0 to clear the count. The CERRCNT value saturates at FFh; it does not wrap back to 0 when it reaches FFh. The CERRCNT register is not automatically cleared when a communications reset is received. It must be cleared manually by writing it back to 0. Note that the CERRCNT register can be written to any 8-bit value. This is intended for diagnostic purposes.

13.3.19 9Bh Channel Special Function Register

ADDR	REG NAME	D7	D6:D2	D1:D0	DEFAULT
9Bh	CH_FS	OUT31_FS	-	DCFB_N [1:0]	0b 00000000

OUT31_FS OUT31 Function select
0 LED function
1 Disable LED function, Set this pin for ADC input

DCFB_N DCFB multiple selection of output current

00 disable
01 1x (0μA~±112.14μA)
10 2x (0μA~±224.28μA)
11 3x (0μA~±336.42μA)

13.3.20 9Ch DCFB Output Current Setting Register

ADDR	REG NAME	D7:D0	DEFAULT
9Ch	DCFB_OCS	DCFB_OUT [7:0]	0b 10000000

DCFB_OUT DCFB Output Current Selection

0000 0000 0μA
0000 0001 0.89μA
0000 0010 1.78μA
0000 0011 2.67μA
0000 0100 3.56μA
0000 0101 4.45μA
…… ……
0111 1101 111.25μA
0111 1110 112.14μA
0111 1111 113.03μA
1000 0000 0μA (default)
1000 0001 -0.89μA
1000 0010 -1.78μA
…… ……
1111 1100 -110.36μA
1111 1101 -111.25μA
1111 1110 -112.14μA
1111 1111 -113.03μA

13.3.21 9Dh~A1h ADC Input Channels Select Registers

ADDR	REG NAME	D7:D0	DEFAULT
9Dh	CHSEL	CHSEL [7:0]	0b 00000000
9Eh		CHSEL [15:8]	0b 00000000
9Fh		CHSEL [23:16]	0b 00000000
A0h		CHSEL [31:24]	0b 00000000
A1h		CHSEL [39:32]	0b 00000000

CHSELX ADC sampling channels select.

The ADC has forty multiplexed input channels (CH0~CH39) which can be respectively selected by the CHSEL [0] ~CHSEL [39] bits. As below table. Multiple channels can be selected which will be periodically measured in turn.

Input Channel Select Bit	Input Signal	Setting
CHSEL [0]	V_{OUT0} or I_{OUT0} or V_{HR0}	"0" = Not Selected "1" = Selected
CHSEL [1]	V_{OUT1} or I_{OUT1} or V_{HR1}	
CHSEL [2]	V_{OUT2} or I_{OUT2} or V_{HR2}	
CHSEL [3]	V_{OUT3} or I_{OUT3} or V_{HR3}	
CHSEL [4]	V_{OUT4} or I_{OUT4} or V_{HR4}	
CHSEL [5]	V_{OUT5} or I_{OUT5} or V_{HR5}	
CHSEL [6]	V_{OUT6} or I_{OUT6} or V_{HR6}	
CHSEL [7]	V_{OUT7} or I_{OUT7} or V_{HR7}	

CHSEL [8]	V_{OUT8} or I_{OUT8} or V_{HR8}	
CHSEL [9]	V_{OUT9}or I_{OUT9} or V_{HR9}	
CHSEL [10]	V_{OUT10} or I_{OUT10} or V_{HR10}	
CHSEL [11]	V_{OUT11} or I_{OUT11} or V_{HR11}	
CHSEL [12]	V_{OUT12} or I_{OUT12} or V_{HR12}	
CHSEL [13]	V_{OUT13} or I_{OUT13} or V_{HR13}	
CHSEL [14]	V_{OUT14} or I_{OUT14} or V_{HR14}	
CHSEL [15]	V_{OUT15} or I_{OUT15} or V_{HR15}	
CHSEL [16]	V_{OUT16} or I_{OUT16} or V_{HR16}	
CHSEL [17]	V_{OUT17} or I_{OUT17} or V_{HR17}	
CHSEL [18]	V_{OUT18} or I_{OUT18} or V_{HR18}	
CHSEL [19]	V_{OUT19}or I_{OUT19} or V_{HR19}	
CHSEL [20]	V_{OUT20} or I_{OUT20} or V_{HR20}	
CHSEL [21]	V_{OUT21} or I_{OUT21} or V_{HR21}	
CHSEL [22]	V_{OUT22} or I_{OUT22} or V_{HR22}	
CHSEL [23]	V_{OUT23} or I_{OUT23} or V_{HR23}	
CHSEL [24]	V_{OUT24} or I_{OUT24} or V_{HR24}	
CHSEL [25]	V_{OUT25} or I_{OUT25} or V_{HR25}	
CHSEL [26]	V_{OUT26} or I_{OUT26} or V_{HR26}	
CHSEL [27]	V_{OUT27} or I_{OUT27} or V_{HR27}	
CHSEL [28]	V_{OUT28} or I_{OUT28} or V_{HR28}	
CHSEL [29]	V_{OUT29}or I_{OUT29} or V_{HR29}	
CHSEL [30]	V_{OUT30} or I_{OUT30} or V_{HR30}	
CHSEL [31]	V_{OUT31} or I_{OUT31} or V_{HR31}	
CHSEL [32]	V_{REF}	
CHSEL [33]	V_{PTAT}	
CHSEL [34]	VLED	
CHSEL [35]	VIN	
CHSEL [36]	VBG	
CHSEL [37]	ADC_IN1	
CHSEL [38]	ADC_IN2	
CHSEL [39]	VLDO5V	

13.3.22 A2h ADC Configuration Register

ADDR	REG NAME	D7:D6	D5:D4	D3	D2:D1	D0	DEFAULT
A2h	ADCCFG	IOUTDC_RS[1:0]	OUT_SEL[1:0]	-	ADCSH [1:0]	ADCEN	0b 00000000

IOUTDC_RS IOUTDC current range setting (It can improve IOUT detection accuracy) (Note 11)
00 12.5mA~25mA
01 6.25mA~12.5mA
10 3.125mA~6.25mA
11 1mA~3.125mA

Note 11: The 0x11 gear (1mA~3.125mA) of the IOUTDC_RS function is not allowed to be used during IOUT Loop verify enable (E9h: IOUT_LE) detection; otherwise, it will trigger false alarms of IOUT Loop verify enable.

OUT_SEL OUT ADC select
00/01 ADC detect VOUT
10 ADC detect IOUT
11 ADC detect VHR

ADCSHx ADC sample/hold time setting
00/01 ADC sample/hold time = 4 ADC CLK (Default)
10 ADC sample/hold time = 8 ADC CLK
11 ADC sample/hold time = 16 ADC CLK

ADCEN ADC Enable
0 Disabled
1 Enabled

13.3.23 A3h ADC Control Register

ADDR	REG NAME	D7	D6	D5	D4	D3:D2	D1	D0	DEFAULT
A3h	ADCCTL	ADCCYC_F	OUTADC_N	OTM	ADCRST	ADCCYC_T [1:0]	LOOP	SADC	0b 00000010

ADCCYC_F ADC sampling finished flag (Read only)
0 ADC sampling in progress, ADC result is not valid
1 ADC sampling finished, ADC result is valid reading for host MCU

OUTADC_N OUT ADC multiple select
0 9x(default)
1 4x

OTM OUT timeout flag (Read only)
0 Normal
1 All selected OUT ADC detections are timed out, registers A4h~CDh are invalid.

ADCCYC_Tx ADC cycle sampling period
00 ADC Cycle sampling for 2 PWM cycles (Default)
01 ADC Cycle sampling for 4 PWM cycles
10 ADC Cycle sampling for 8 PWM cycles
11 ADC Cycle sampling for 16 PWM cycles
To get more stable and precise result, OUTX voltage is always sampled for multiple PWM cycles to calculate the average value.

LOOP ADC sampling mode
0 ADC single conversion
1 Enable continue ADC conversion (Default)

SADC Start ADC measurement
0 ADC measurement stops (Default)
1 ADC measurement starts
Please set ADCEN bit at first, then set SADC bit, otherwise ADC cannot measure voltage.

ADCRST Reset all ADC result registers (A4h~DDh) to default value when ADC measurement starts
0 Not reset (Default)
1 Reset

13.3.24 A4h~CBh ADC CHSEL Result Registers

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
A4h	ADC_OUT0_H	ADC_OUT0[9:2]								0b 00000000
A5h	ADC_OUT1_H	ADC_OUT1[9:2]								0b 00000000
A6h	ADC_OUT2_H	ADC_OUT2[9:2]								0b 00000000
A7h	ADC_OUT3_H	ADC_OUT3[9:2]								0b 00000000
A8h	ADC_OUT0_1_2_3_L	ADC_OUT3[1:0]		ADC_OUT2[1:0]		ADC_OUT1[1:0]		ADC_OUT0[1:0]		0b 00000000
A9h	ADC_OUT4_H	ADC_OUT4[9:2]								0b 00000000
AAh	ADC_OUT5_H	ADC_OUT5[9:2]								0b 00000000
ABh	ADC_OUT6_H	ADC_OUT6[9:2]								0b 00000000
ACh	ADC_OUT7_H	ADC_OUT7[9:2]								0b 00000000
ADh	ADC_OUT4_5_6_7_L	ADC_OUT7[1:0]		ADC_OUT6[1:0]		ADC_OUT5[1:0]		ADC_OUT4[1:0]		0b 00000000
AEh	ADC_OUT8_H	ADC_OUT8[9:2]								0b 00000000
AFh	ADC_OUT9_H	ADC_OUT9[9:2]								0b 00000000
B0h	ADC_OUT10_H	ADC_OUT10[9:2]								0b 00000000
B1h	ADC_OUT11_H	ADC_OUT11[9:2]								0b 00000000
B2h	ADC_OUT8_9_10_11_L	ADC_OUT11[1:0]		ADC_OUT10[1:0]		ADC_OUT9[1:0]		ADC_OUT8[1:0]		0b 00000000
B3h	ADC_OUT12_H	ADC_OUT12[9:2]								0b 00000000
B4h	ADC_OUT13_H	ADC_OUT13[9:2]								0b 00000000
B5h	ADC_OUT14_H	ADC_OUT14[9:2]								0b 00000000
B6h	ADC_OUT15_H	ADC_OUT15[9:2]								0b 00000000
B7h	ADC_OUT12_13_14_15_L	ADC_OUT15[1:0]		ADC_OUT14[1:0]		ADC_OUT13[1:0]		ADC_OUT12[1:0]		0b 00000000
B8h	ADC_OUT16_H	ADC_OUT16[9:2]								0b 00000000
B9h	ADC_OUT17_H	ADC_OUT17[9:2]								0b 00000000
BAh	ADC_OUT18_H	ADC_OUT18[9:2]								0b 00000000
BBh	ADC_OUT19_H	ADC_OUT19[9:2]								0b 00000000
BCh	ADC_OUT16_17_18_19_L	ADC_OUT19[1:0]		ADC_OUT18[1:0]		ADC_OUT17[1:0]		ADC_OUT16[1:0]		0b 00000000
BDh	ADC_OUT20_H	ADC_OUT20[9:2]								0b 00000000
BEh	ADC_OUT21_H	ADC_OUT21[9:2]								0b 00000000
BFh	ADC_OUT22_H	ADC_OUT22[9:2]								0b 00000000
C0h	ADC_OUT23_H	ADC_OUT23[9:2]								0b 00000000
C1h	ADC_OUT20_21_22_23_L	ADC_OUT23[1:0]		ADC_OUT22[1:0]		ADC_OUT21[1:0]		ADC_OUT20[1:0]		0b 00000000
C2h	ADC_OUT24_H	ADC_OUT24[9:2]								0b 00000000
C3h	ADC_OUT25_H	ADC_OUT25[9:2]								0b 00000000
C4h	ADC_OUT26_H	ADC_OUT26[9:2]								0b 00000000
C5h	ADC_OUT27_H	ADC_OUT27[9:2]								0b 00000000
C6h	ADC_OUT24_25_26_27_L	ADC_OUT27[1:0]		ADC_OUT26[1:0]		ADC_OUT25[1:0]		ADC_OUT24[1:0]		0b 00000000
C7h	ADC_OUT28_H	ADC_OUT28[9:2]								0b 00000000
C8h	ADC_OUT29_H	ADC_OUT29[9:2]								0b 00000000
C9h	ADC_OUT30_H	ADC_OUT30[9:2]								0b 00000000
CAh	ADC_OUT31_H	ADC_OUT31[9:2]								0b 00000000
CBh	ADC_OUT28_29_30_31_L	ADC_OUT31[1:0]		ADC_OUT30[1:0]		ADC_OUT29[1:0]		ADC_OUT28[1:0]		0b 00000000

ADC_OUTx The ADC result of each OUTx pin voltage or current.

This result can be used to calculate the OUTx pin voltage by following equation:

$$V_{OUTx}(V) = \frac{\sum_{n=0}^{9} D[n]\cdot 2^n}{1024} \times V_{REFADC} \times 9 \quad \text{(A3h: OUTADC_N = 0)} \quad (18)$$

$$V_{OUTx}(V) = \frac{\sum_{n=0}^{9} D[n]\cdot 2^n}{1024} \times V_{REFADC} \times 4 \quad \text{(A3h: OUTADC_N = 1)} \quad (19)$$

This result can be used to calculate the OUTx pin current by following equation:

$$I_{OUTx}(mA) = \frac{\sum_{n=0}^{9} D[n]\cdot 2^n}{1024} \times V_{REFADC} \times \frac{25mA}{2} \quad \text{(A2h: IOUTDC_RS = 00)} \quad (20)$$

$$I_{OUTx}(mA) = \frac{\sum_{n=0}^{9} D[n]\cdot 2^n}{1024} \times V_{REFADC} \times \frac{12.5mA}{2} \quad \text{(A2h: IOUTDC_RS = 01)} \quad (21)$$

$$I_{OUTx}(mA) = \frac{\sum_{n=0}^{9} D[n]\cdot 2^n}{1024} \times V_{REFADC} \times \frac{6.25mA}{2} \quad \text{(A2h: IOUTDC_RS = 10)} \quad (22)$$

$$I_{OUTx}(mA) = \frac{\sum_{n=0}^{9} D[n]\cdot 2^n}{1024} \times V_{REFADC} \times \frac{3.125mA}{2} \quad \text{(A2h: IOUTDC_RS = 11)} \quad (23)$$

This result can be used to calculate the OUTx pin Vheadroom by following equation:

$$V_{HRx}(V) = \frac{\sum_{n=0}^{9} D[n]\cdot 2^n}{1024} \times V_{REFADC} \times \frac{6}{5} \quad (24)$$

13.3.25 CCh~CDh ADC OUT (VOUT, VHR, IOUT) Detect Minimum Result Registers

ADDR	REG NAME	D7:D2	D1:D0	DEFAULT
CCh	ADC_ OUT 0_31_MIN_H	ADC_OUT 0_31_MIN[9:2]		0b 00000000
CDh	ADC_ OUT 0_31_MIN_L	-	ADC_ OUT 0_31_MIN [1:0]	0b 00000000

If read CCh~CDh after, CCh~CDh will be clear to 0x00.

Note 12: When collecting ADC_VHR Min as the DCFB judgment condition, please first perform Faultb judgment, close the channel where Open Faultb occurred (Channel SL is written as '0'), and then collect VHR_Min value again. Otherwise, the collected ADC_VHR Min will be the OPEN Faulotb channel value, causing DCFB error.

13.3.26 CEh~CFh ADC Internal Reference Voltage Result Registers

ADDR	REG NAME	D7:D2	D1:D0	DEFAULT
CEh	ADC_VREF_H	ADC_VREF [9:2]		0b 00000000
CFh	ADC_VREF_L	-	ADC_VREF [1:0]	0b 00000000

ADC_VREFx The ADC result of the internal reference voltage.

$$V_{REF}(V) = \frac{\sum_{n=0}^{9} D[n]\cdot 2^n}{1024} \times 2.5 \times 2 \quad (25)$$

13.3.27 D0h~D1h ADC PTAT Voltage Result Register

ADDR	REG NAME	D7:D2	D1:D0	DEFAULT
D0h	ADC_VPTAT_H	ADC_VPTAT [9:2]		0b 00000000
D1h	ADC_VPTAT _L	-	ADC_VPTAT [1:0]	0b 00000000

ADC_VPTATx The ADC result of internal PTAT voltage.
This result can be used to estimate the device junction temperature by following equation:

$$T_J(°C) = \frac{\left(\frac{\sum_{n=0}^{9} D[n]\cdot 2^n}{1024} \times 2500 - 982\right)}{3.752} + 25°C \quad (26)$$

Where, V_{REFADC} is the reference voltage of the ADC, typical 2.5V.

13.3.28 D2h~D3h ADC VLED Voltage Result Register

ADDR	REG NAME	D7:D2	D1:D0	DEFAULT
D2h	ADC_VLED _H	ADC_VLED [9:2]		0b 00000000
D3h	ADC_VLED _L	-	ADC_VLED [1:0]	0b 00000000

ADC_VLEDx The ADC result of VLED voltage.

This result can be used to calculate the VLED voltage by following equation:

$$V_{VLED}(V) = \frac{\sum_{n=0}^{9} D[n] \cdot 2^n}{1024} \times V_{REFADC} \times 9 \qquad (27)$$

13.3.29 D4h~D5h ADC VIN Voltage Result Register

ADDR	REG NAME	D7:D2	D1:D0	DEFAULT
D4h	ADC_ VIN_H	ADC_ VIN[9:2]		0b 00000000
D5h	ADC_ VIN _L	-	ADC_ VIN [1:0]	0b 00000000

ADC_ VIN the ADC result of AIN voltage.

This result can be used to calculate the VIN voltage by following equation:

$$V_{VIN}(V) = \frac{\sum_{n=0}^{9} D[n] \cdot 2^n}{1024} \times V_{REFADC} \times 9 \qquad (28)$$

13.3.30 D6h~D7h ADC BG Result Register

ADDR	REG NAME	D7:D2	D1:D0	DEFAULT
D6h	ADC_VBG _H	ADC_VBG [9:2]		0b 00000000
D7h	ADC_VBG _L	-	ADC_VBG [1:0]	0b 00000000

ADC_ VBG x The ADC result of internal BG voltage.

This result can be used to calculate the BG voltage by following equation:

$$V_{VBG}(V) = \frac{\sum_{n=0}^{9} D[n] \cdot 2^n}{1024} \times V_{REFADC} \qquad (29)$$

13.3.31 D8h~DBh ADC IN1 IN2 special input Result Registers

ADDR	REG NAME	D7:D2	D1:D0	DEFAULT
D8h	ADC_IN1 _H	ADC_ IN1 [9:2]		0b 00000000
D9h	ADC_ IN1 _L	-	ADC_ IN1 [1:0]	0b 00000000
DAh	ADC_ IN2 _H	ADC_ IN2 [9:2]		0b 00000000
DBh	ADC_ IN2 _L	-	ADC_ IN2 [1:0]	0b 00000000

ADC_INx The ADC result of each OUT31(ADC_IN2) and 23(ADC_IN1) pin voltage.

This result can be used to calculate the OUT31(ADC_IN2) and 23(ADC_IN1) pin voltage by following equation:

$$V_{OUTx}(V) = \frac{\sum_{n=0}^{9} D[n] \cdot 2^n}{1024} \times V_{REFADC} \qquad (30)$$

13.3.32 DCh~DDh ADC VLDO5V Voltage Result Register

ADDR	REG NAME	D7:D2	D1:D0	DEFAULT
DCh	ADC_ VLDO5V_H	ADC_ VLDO5V [9:2]		0b 00000000
DDh	ADC_ VLDO5V _L	-	ADC_ VLDO5V [1:0]	0b 00000000

ADC_VLDO5V The ADC result of LDO5V voltage.

This result can be used to calculate the LDO5V voltage by following equation:

$$V_{VLDO5V}(V) = \frac{\sum_{n=0}^{9} D[n] \cdot 2^n}{1024} \times V_{REFADC} \times 5 \qquad (31)$$

13.3.33 DEh LBIST State Register

ADDR	REG NAME	D7:D2	D1	D0	DEFAULT
DEh	BSTSTA	-	FAIL	FINISH	0b 00000000

FINISH LBIST state flag

0 LBIST in progress

1 LBIST finished

The device will do Logic Build in Self-test (LBIST) upon UVLO being released. When it is finished, this flag will be set to “1”.

FAIL LBIST result

0 Pass

1 Failure

This result is only available for check after LBIST being finished, FINISH bit set to “1”. In case of LBIST result is failure, the device is defective and cannot be used.

13.3.34 DFh Loopback Control Register

ADDR	REG NAME	D7:D6	D5	D4	D3:D0	DEFAULT
DFh	VFYCTL	MODE[1:0]	-	TOLERANCE_H	TOLERANCE_L [3:0]	0b 00010010

MODE Mode select

00 Disabled LBT

01 Test pwm_lb = ‘0’

10 Test pwm_lb = all ‘1’

11 Normal loop back test

TOLERANCEx Loopback comparison tolerance setting

Preset PWM duty cycle deviation tolerance between the measurement result and the PWM duty cycle setting value in the PWM buffer.

When TOLERANCE_H = ‘0’

$$Tolerance = \sum_{n=0}^{3} D[n] \cdot 2^n \qquad (32)$$

When TOLERANCE_H = ‘1’

$$Tolerance = \sum_{n=0}^{3} D[n] \cdot 2^n \times 8 \qquad (33)$$

13.3.35 E0h Loopback Configuration Register

ADDR	REG NAME	D7	D6	D5	D4:D0	DEFAULT
E0h	VFYCFG	START/BUSY	-	ALE	PWM_LB_SEL[4:0]	0b 00000000

START/BUSY Loopback verification state flag (write 1 only and auto hardware clear when single OUT(ALE=0) or loop OUT0~OUT31(ALE=1) complete loop back)

0 Finished

1 start LB test

ALE Auto Loop Enable

0 Disable

1 Enable (OUT0~OUT31 loopback auto loop detect)

PWM_LB_SEL Loopback channel select

00000 PWM signal from output stage of OUT0

00001 PWM signal from output stage of OUT1

00010 PWM signal from output stage of OUT2

…… ……

01111 PWM signal from output stage of OUT15

10000 PWM signal from output stage of OUT16

10001 PWM signal from output stage of OUT17

…… ……

11110 PWM signal from output stage of OUT30

11111 PWM signal from output stage of OUT31

The PWM duty cycle loopback verification circuit has Thirty-two multiplexed inputs to monitor the PWM duty cycle of output channels. The thirty-two input channels (LPBCH0~LPBCH31) are respectively connected to each current source output stage. As below table. Only one channel can be verified at a time.

13.3.36 E1h~E4h Loopback Fault Flag Registers

ADDR	REG NAME	D7:D0	DEFAULT
E1h	DUTYF_1	DUTYFLT [7:0]	0b 00000000
E2h	DUTYF_2	DUTYFLT [15:8]	0b 00000000
E3h	DUTYF_3	DUTYFLT [23:16]	0b 00000000
E4h	DUTYF_4	DUTYFLT [31:24]	0b 00000000

DUTYFLTx Loopback fault flag for each OUT0~OUT31

0 No loopback failure

1 Loopback failure

13.3.37 E5h~E6h Loopback PWM Duty Cycle Registers

ADDR	REG NAME	D7:D4	D3:D0	DEFAULT
E5h	PWMDUTY_H	PWMDUTY [11:4]		0b 00000000
E6h	PWMDUTY_L	-	PWMDUTY [3:0]	0b 00000000

PWMDUTYx The PWM duty cycle measure result of the selected channel.

13.3.38 E7h~E8h Select PWM Duty Cycle Registers

ADDR	REG NAME	D7:D4	D3:D0	DEFAULT
E7h	SEL_PWMDUTY_H	SEL_PWMDUTY [11:4]		0b 00000000
E8h	SEL_PWMDUTY_L		SEL_PWMDUTY [3:0]	0b 00000000

SEL_PWMDUTYx The PWM duty cycle of the selected channel.

13.3.39 E9h SCA verification Control Register

ADDR	REG NAME	D7:D6	D5	D4	D3	D2:D1	D0	DEFAULT
E9h	SCACTL	-	IOUT_LE	OUTDC_FINJ	OUTDC_EN	-	SCA_TEN	0b 00000000

IOUT_LE IOUT Loop verify enable (auto comparison, tolerance 40%) (Note 13)
0 Disabled, EAh~EDh will clear to '0'
1 Enabled

Note 13: The IOUT Loop verify enable (E9h: IOUT_LE) function applies only when R_{ISET} is 20kΩ~47kΩ (10.8mA~25mA). For the corresponding Iout ADC current acquisition accuracy (A2h: IOUTDC_RS), only gears 0x00, 0x01, 0x10 (3.125mA~25mA) are allowed. Non-compliance triggers false activation of IOUT Loop verify enable.

OUTDC_ FINJ IOUT 15mA detect verification
0 Disabled
1 Enabled

OUTDC_EN IOUT detect enable
0 Disabled
1 Enabled

SCA_TEN SCA verification function enable
0 Disabled
1 Enabled

13.3.40 EAh~EDh IOUT Fault Flag Registers

ADDR	REG NAME	D7:D0	DEFAULT
EAh	IOUT_1	IOUT_FLT [7:0]	0b 00000000
EBh	IOUT_2	IOUT_FLT [15:8]	0b 00000000
ECh	IOUT_3	IOUT_FLT [23:16]	0b 00000000
EDh	IOUT_4	IOUT_FLT [31:24]	0b 00000000

IOUT_x IOUT fault flag for each OUT0~OUT31
0 No IOUT failure
1 IOUT failure

13.3.41 EEh R_{ISET} Information Register

ADDR	REG NAME	D7	D6:D0	DEFAULT
EE	RISETDATA	-	RISETDATA[6:0]	0b 00000000

R_{ISET} Setting for IOUT verification, set the same resistance value as R_{ISET} pin according to the formula

$$\text{RISETDATA} = (50 - \frac{1000}{R_{ISET}(K\Omega)})/0.315 \qquad (34)$$

For example:
If R_{ISET} = 20kΩ,
RISETDATA = (50-1000/20)/0.315 = 0; RISETDATA[6:0] = 000 0000.

If R_{ISET} = 47kΩ,
RISETDATA = (50-1000/47)/0.315 = 95.23≈91; RISETDATA[6:0] = 101 1011.
Note 14: R_{ISET} Information Register (EEh) must be used with IOUT Loop verify enable (E9h: IOUT_LE); its configuration is restricted to R_{ISET} 20KΩ~47KΩ (RISETDATA[6:0]: 000 0000~101 1011).

13.3.42 00h OTP Control Register

ADDR	REG NAME	D7	D6	D5:D4	D3:D0	DEFAULT
00h	OTP_CTRL	p1	p0	Cmd[1:0]	Sel[3:0]	0b 10000000

This register must be written after a special command
There are four select OTP ZoneX bits, two OTP operation bits and two parity bits.
The parity bits for the OTP control byte are calculated with the equations below:
p[1] = ~(Sel[1] ^ Sel[3] ^ Cmd[0] ^ Cmd[1])
p[0] = Sel[0] ^ Sel[1] ^ Sel[2] ^ Cmd[0]

Cmd	Comand Select
01	OTP write operation
11	OTP read operation
Other	Not allow

Sel	Zone Select
0001	Select OTP Zone A
Other	No allow

13.3.43 01h OTP Status Register

ADDR	REG NAME	D7:D3	D2	D1	D0	DEFAULT
01h	OTP_ST	-	FAIL	FINISH	BUSY	0b 00000000

FAIL	OTP write fail
FINISH	OTP write finish
BUSY	OTP operation in progress

13.3.44 02h ECC Status Register

ADDR	REG NAME	D7	D6	D5	D4	D3:D0	DEFAULT
02h	ECC_ST	-	IMD_2Err_ecc A	-	IMD_1Err_ecc A	-	0b 00000000

IMD_2Err_ecc A	ECC detects 2bit or more errors
IMD_1Err_ecc A	ECC detected 1bit error

13.3.45 10h DEFCONFIG Register (fail safe mode 1)

ADDR	REG NAME	D7	D6:D5	D4:D0	DEFAULT
10h	DEFCONF	DEFDC_PWM	WDT_FS[1:0]	DEFPFS [4:0]	0b 00000000

DEFPFS	PWM Frequency Setting
00000	8bit Linearity, 25.6kHz, 6.5M(default)
00001	8bit Linearity, 12.8kHz, 6.5M
00010	8bit Linearity, 6.4kHz, 6.5M
00011	8bit Linearity, 3.2kHz, 6.5M
00100	8bit Linearity, 1.6kHz, 6.5M
00101	8bit Linearity, 1.4kHz, 6.5M
00110	8bit Linearity, 1.2kHz, 6.5M
00111	8bit Linearity, 1kHz, 6.5M
01000	8bit Linearity, 700Hz, 6.5M
01001	8bit Linearity, 500Hz, 6.5M
01010	8bit Linearity, 400Hz, 6.5M
01011	8bit Linearity, 300Hz, 6.5M
01100	7+5bit Linearity, 25.6kHz
01101	7+5bit Linearity, 25.6kHz
01110	12bit Linearity, 1.6kHz, 6.5M
01111	12bit Linearity, 400Hz, 6.5M

10000	12bit Linearity, 200Hz, 6.5M
10001	8bit Gamma, 1.6kHz6.5M
10010	8bit Gamma, 800Hz, 6.5M
10011	8bit Gamma, 400Hz, 6.5M
10100	8bit Gamma, 200Hz, 6.5M
10101	12bit Linearity, 5Hz, 6.5M(for blink)
10110	12bit Linearity, 2.5Hz, 6.5M(for blink)
10111	12bit Linearity, 1.25Hz, 6.5M(for blink)
Others	12bit Linearity, 400Hz, 6.5M

WDT_FS	Command Watchdog Timer Trigged Fail Safe Mode
00/11	Watchdog Timer 1&2 enable, when watchdog timer 1 or 2 time out, enter to fail safe mode
01	Watchdog Timer 1 enable, Watchdog Timer 2 disable, when watchdog timer 1 time out, enter to fail safe mode(default)
10	Watchdog Timer 2 enable, Watchdog Timer 1 disable, when watchdog timer 2 time out, enter to fail safe mode

DEFDC_PWM	DC or PWM output select for all outputs
0	PWM dimming. PWM duty cycle is determined by PWM registers 17h~27h
1	DC output. PWM dimming is disabled, and all outputs are DC current (I_{OUTx})

13.3.46 11h DEFGCC Register (fail safe mode 1)

ADDR	REG NAME	D7:D0	DEFAULT
11h	DEFGCC	DEFGCC [7:0]	0b 00000000

DEFGCC control the I_{OUT} as shown in following formula:

$$I_{OUT\_F} = I_{OUT(MAX)} \times \frac{GCC}{255} \quad (35)$$

$$GCC = \sum_{n=0}^{7} D[n] \cdot 2^n \quad (36)$$

13.3.47 12h DEFCONFIG Register (fail safe mode 1)

ADDR	REG NAME	D7	D6	D5:D4	D3	D2:D0	DEFAULT
12h	DEFTEMP_ SSCEN	-	DEFSSCEN	DEFSSC [1:0]	-	DEFTROF [2:0]	0b 00000000

The current of thermal roll off will not be a fixed proportion, and the slope of roll off can be calculated by formula. I_{ROLL}= Iset × (2V-Vx) / 2, I_{ROLL} is the current after roll off, I_{SET} is the current before roll off, and Vx is the optional voltage (TROF bits) of the register.

EDFTROF	Percentage of output current before thermal shutdown happens
000	0V
001	0.2V
010	0.4V
011	0.6V
100	0.8V
101	1.0V
110	1.2V
111	1.4V

DEFSSCEN	Spread Spectrum Enable
0	Disable
1	Enable-not allowed when PWM frequency is 200Hz

DEFSSC	Spread Spectrum frequency Range
00	125Hz
01	250Hz

10 500Hz
11 1kHz

13.3.48 13h~16h DEFLED Register (fail safe mode 1)

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
13	DEFLED1	DEFLED7	DEFLED6	DEFLED5	DEFLED4	DEFLED3	DEFLED2	DEFLED1	DEFLED0	0b 00000000
14	DEFLED2	DEFLED15	DEFLED14	DEFLED13	DEFLED12	DEFLED11	DEFLED10	DEFLED9	DEFLED8	0b 00000000
15	DEFLED3	DEFLED23	DEFLED22	DEFLED21	DEFLED20	DEFLED19	DEFLED18	DEFLED17	DEFLED16	0b 00000000
16	DEFLED4	DEFLED31	DEFLED30	DEFLED29	DEFLED28	DEFLED27	DEFLED26	DEFLED25	DEFLED24	0b 00000000

DEFLEDx LED State Bit
0 LED off
1 LED on

13.3.49 17h~27h DEFPWM Register (fail safe mode 1)

ADDR	REG NAME	D7:D4	D3:D0	DEFAULT
17	DEFPWM1	PWM1[3:0]	PWM0[3:0]	0b 00000000
18	DEFPWM2	PWM3[3:0]	PWM2[3:0]	0b 00000000
19	DEFPWM3	PWM5[3:0]	PWM4[3:0]	0b 00000000
1A	DEFPWM4	PWM7[3:0]	PWM6[3:0]	0b 00000000
1B	DEFPWM5	PWM9[3:0]	PWM8[3:0]	0b 00000000
1C	DEFPWM6	PWM11[3:0]	PWM10[3:0]	0b 00000000
1D	DEFPWM7	PWM13[3:0]	PWM12[3:0]	0b 00000000
1E	DEFPWM8	PWM15[3:0]	PWM14[3:0]	0b 00000000
20	DEFPWM9	PWM17[3:0]	PWM16[3:0]	0b 00000000
21	DEFPWM10	PWM19[3:0]	PWM18[3:0]	0b 00000000
22	DEFPWM11	PWM21[3:0]	PWM20[3:0]	0b 00000000
23	DEFPWM12	PWM23[3:0]	PWM22[3:0]	0b 00000000
24	DEFPWM13	PWM25[3:0]	PWM24[3:0]	0b 00000000
25	DEFPWM14	PWM27[3:0]	PWM26[3:0]	0b 00000000
26	DEFPWM15	PWM29[3:0]	PWM28[3:0]	0b 00000000
27	DEFPWM16	PWM31[3:0]	PWM30[3:0]	0b 00000000

Each OUTx has 4-bit to modulate the PWM duty cycle in 16 steps.
The value of the PWM Registers decides the average current of each OUTx LED noted I_{LED}.
I_{LED} computed by following formula:

$$I_{OUTx\_PWM} = I_{OUTx} \times D_{PWMx} \qquad (37)$$

Where, D_{PWMx} is duty cycle of each channel independently programmed by PWM Registers (17h~27h),

In 4bit PWM mode:

$$D_{PWMx} = \frac{\sum_{n=0}^{3} D[n] \cdot 2^n}{16} \qquad (38)$$

13.3.50 1Fh 28h ECC_A Register

ADDR	REG NAME	D7:D0	DEFAULT
1F	ECC_A1	ECCA1	0b 00000000
28	ECC_A2	ECCA2	0b 00000000

Data check byte 0x10~0x1E, 0x20~0x2A.

13.3.51 29h Write Protect area A Register

ADDR	REG NAME	D7:D0	DEFAULT
29h	W_PROTECT_A	WPROTECTA	0b 00000000

OTP-A data protect byte, it must be written 0xFF.

13.3.52 FCh OTP Write Unlock Register

ADDR	REG NAME	D7:D0	DEFAULT
FCh	OTP_UNLOCK	OTPUNLOCK	0b 00000000

OTP register unlock byte, unlock OTP registers(10h~29h)

Write 0xA5->0x69 unlock OTPA

Other lock OTPA,and test mode.

14 CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

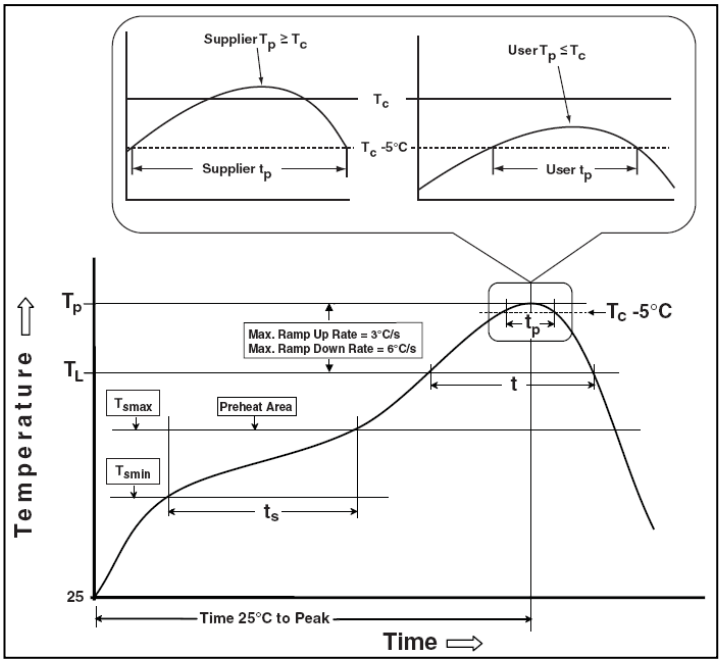
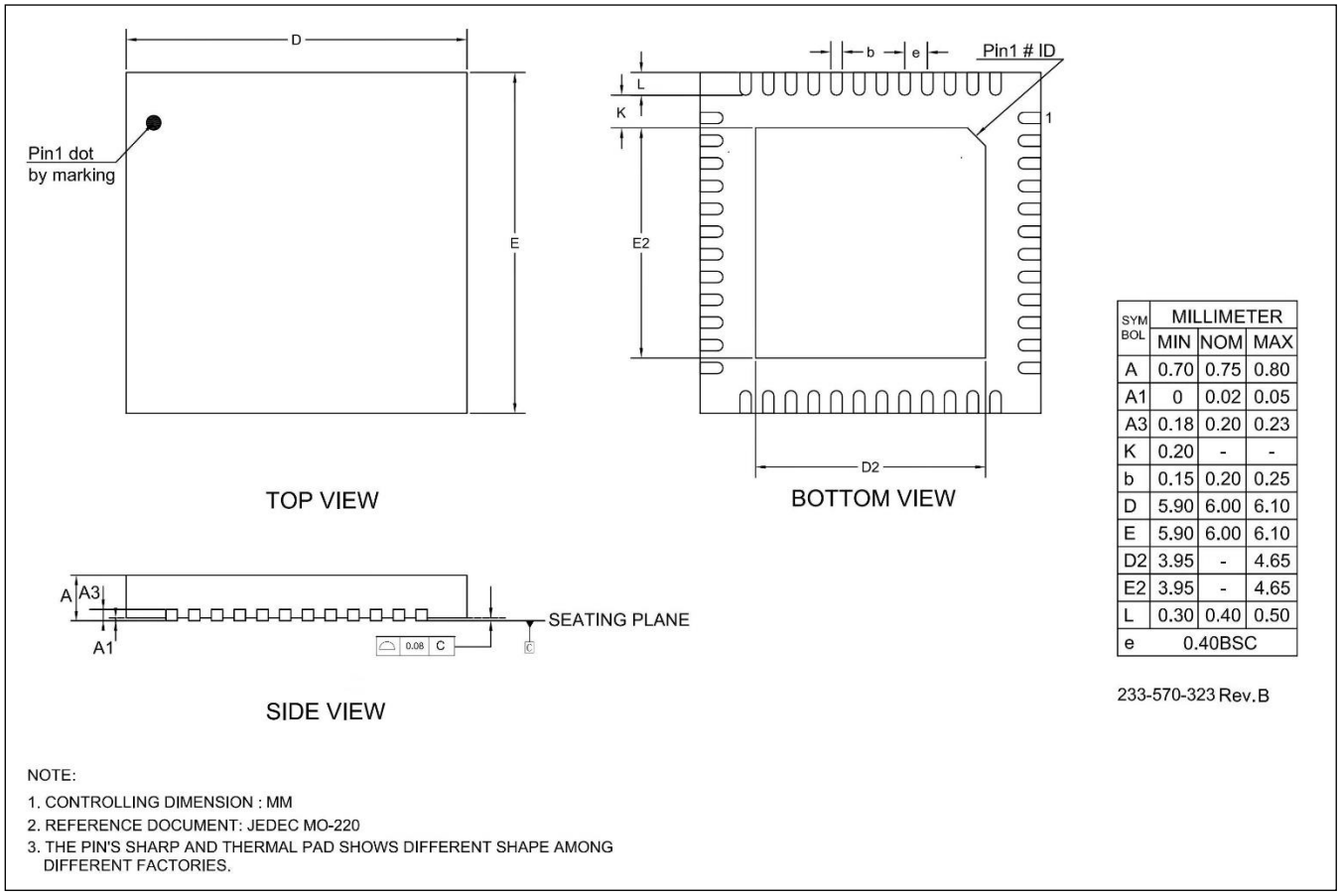


Figure 25 Classification Profile

15 PACKAGEINFORMATION

QFN-48



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3	0.18	0.20	0.23
K	0.20	-	-
b	0.15	0.20	0.25
D	5.90	6.00	6.10
E	5.90	6.00	6.10
D2	3.95	-	4.65
E2	3.95	-	4.65
L	0.30	0.40	0.50
e	0.40BSC		

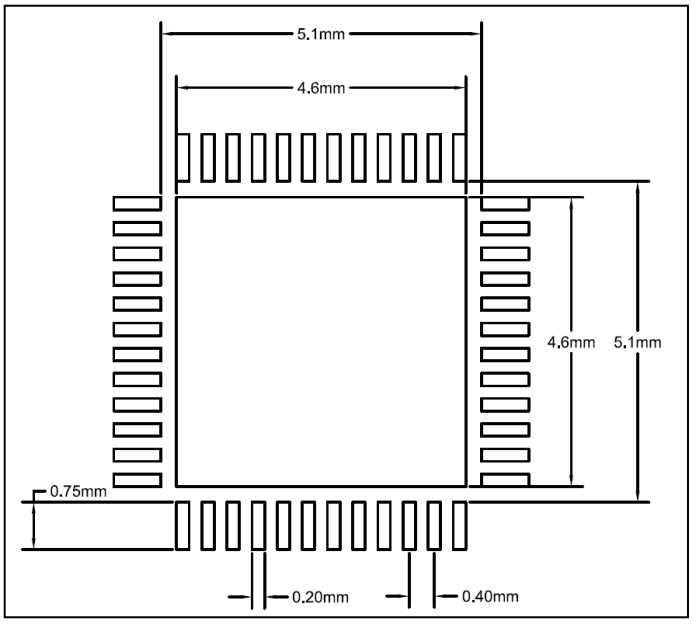
233-570-323 Rev.B

NOTE:

1. CONTROLLING DIMENSION : MM
2. REFERENCE DOCUMENT: JEDEC MO-220
3. THE PIN'S SHARP AND THERMAL PAD SHOWS DIFFERENT SHAPE AMONG DIFFERENT FACTORIES.

16 RECOMMENDEDLAND PATTERN

QFN-48



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. User's board manufacturing specs), user must determine suitability for use.

17 REVISIONHISTORY

Revision	Detail Information	Date
0A	Initial release	2024.11.21
0B	1. Update EC table. 2. Update 11.3.25 CCh-CDh register description. 3. Add Note12 for CCh-CDh registers. 4. Update function description for the LDO5V OV FAULT section.	2025.05.12
0C	1. Update EC table. 2. Update the FBK diagram. 3. Register format alignment. 4. Update the 11.5.15 Fault Action Table LED Open detection from "VIN >VFLT_UV" to "VLED >VFLT_UV". 5. Update OFAx register from "one fail all on" to "one fail others on" 6. Update the page1 00h register p0 calculation formula. 7. Update the turnaround time item about ACK response delay time and read response delay time (From ≤9 bits update to ≤18 bits).	2025.10.11
0D	1. Updated Register A2h in section 13.3.22, adding usage restrictions for IOUTDC_RS gears (specifically for IOUT Loop verifyenable detection). 2. Updated Register E9h in section 13.3.39, adding usage restrictions for the IOUT_LE function (during IOUT Loop verifyenable detection, only three IOUT ADC current accuracy gears—0x00, 0x01, and 0x10—can be selected). 3. Updated Register EEh in section 13.3.41, adding usage restrictions for the RISETDATA[6:0] register range. 4. θ_{JP} changes to θ_{JC_BOT}	2025.12.12
A	1. Update EC table, modify the 3mA mismatch and IOUT accuracy spec to ±4%. 2. Update EC table, modify the V_{LED_UV} threshold from 3.3V(Min.)/3.6V(Type.)/3.8V(Max.) to 2.95V(Min.)/3.2V(Type.)/3.65V(Max.) 3. Update EC table, modify the V_{LED_UVHY} hysteresis voltage from 300mV (Type.) to 400mV (Type.) 4. Update EC table, modify the Icc Limit. 5. Update ABSOLUTE table, update the ESD Parameters.	2026.05.09