CAN Bus Transceiver

GENERAL DESCRIPTION

The IS32IO1044 is a CAN transceiver designed according to the ISO 11898-2 and SAE J2284. It allows CAN FD bus speed up to 5Mbps

It uses 5V VDD supply for CAN front-end and a separate VIO supply host interface. It can be put in standby (STB) mode by STB=1 with very low power dissipation. In the STB mode, a low power low speed receiver is still enabled to detect bus wakeup condition and the bus wakeup is reflected on the RXD output.

IS32IO1044 tolerate up to +/- 12V on bus common-mode for bus signal and can withstand +/- 40V on the bus pins CANH and CANL. It also incorporates slope-control at the CAN bus driver to minimize EMC impact. The front-end disengages itself during loss of power or ground presenting zero load on the bus. Other fail-safe functions include bus dominant time out and under-voltage detection as well as thermal shutdown.

IS32IO1044 has two options in pin 5. IS32IO1044A pin 5 is NC and VIO is internally connected to VDD for 5V interface. IS32IO1044B pin 5 is VIO allowing 3.3V compatible.

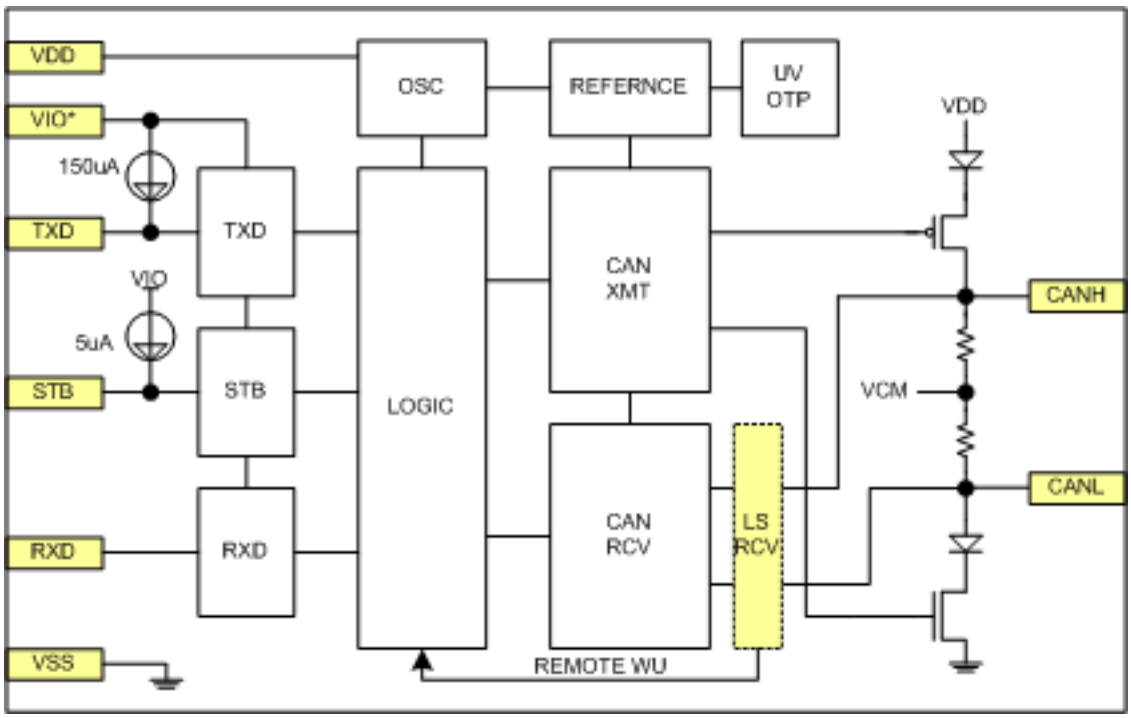
APPLICATIONS

- Automotive networking
- Industrial networking

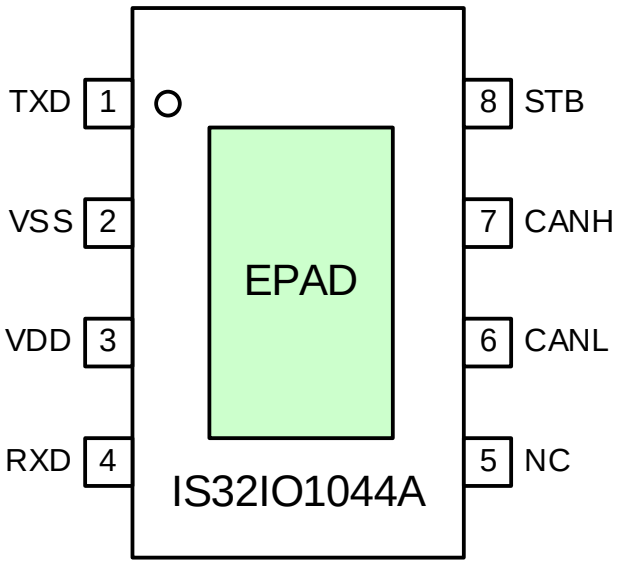
FEATURES

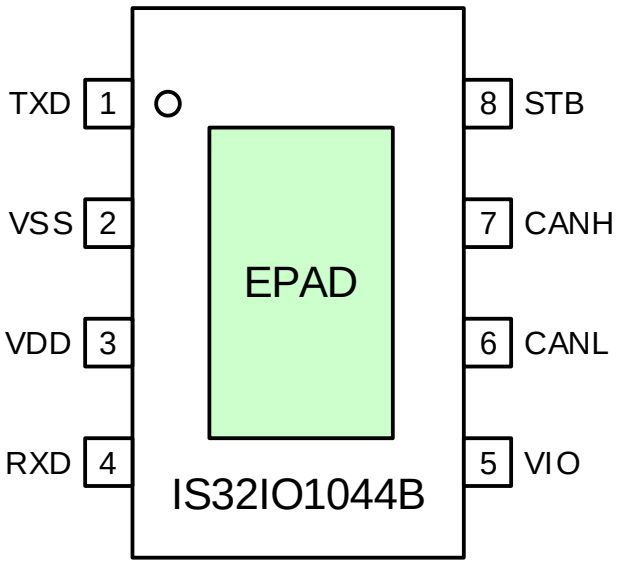
- ISO 11898-2 and SAE J2284 compliant
- CANH/CANL
  - No load at power/ground loss
  - +/- 12V common-mode
  - +/-8KV ESD
- Supply voltage
  - V_{DD} = 4.75V to 5.25V, $I_{VDD,STB}$ < 35uA
  - V_{IO} = 2.9V to V_{DD} with $I_{VIO,STB}$ < 10uA
- TXD
  - Internal pull-up
  - Dominant time out
- RXD
  - Wakeup status
- STB
  - Internal pull-up
- Fail-Safe
  - Under-voltage protection, VDD = 4.1V
  - Under-voltage protection, V_{IO} = 2.4V
  - Thermal shutdown 170℃
- SOP-8 with exposed pad (eSOP-8)
  - RoHS and Halogen-Free compliant
- AEC-Q100 qualification
- TSCA Compliance

BLOCK DIAGRAM



PIN OUT


TXD
1
VSS
2
VDD
3
RXD
4
EPAD
IS32IO1044A
8
STB
7
CANH
6
CANL
5
NC


TXD
1
VSS
2
VDD
3
RXD
4
EPAD
IS32IO1044B
8
STB
7
CANH
6
CANL
5
VIO

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1. PIN DESCRIPTION

PIN #	NAME	I/O	DESCRIPTION
1	TXD	I	Transmit data input. TXD has internal pullup to VIO.
2	VSS	G	Ground power supply.
3	VDD	P	Positive power supply for internal circuits and CAN bus front-end.
4	RXD	O	Receive data output. Also indicates remote wakeup status.
5	VIO	P	I/O interface supply voltage. VIO should be equal to or lower than VDD but > 2.9V.
	NC	-	No connection
6	CANL	I/O	CAN bus pin low.
7	CANH	I/O	CAN bus pin high.
8	STB	I	Standby control. STB has internal pullup to VIO.
ePAD	VSS	G	Exposed pad is internally shorted to VSS

Table 1-1 PIN Description

2. Pin Functional Descriptions

IS32IO1044 integrated the physical layer function for conventional CAN and FD CAN bus applications. It is compliant with ISO-11898-2:2016 and SAE-J2284.

2.1 Supply Pin (VDD)

VDD is the primary supply for the internal circuits and CAN bus front-end. It must be supplied with a voltage of 4.75V to 5.25V. If VDD is lost, the bus pins present no load on the bus. There is undervoltage detection on VDD. The undervoltage level is at 4.1V and it results the transceiver in STB mode.

2.2 Ground Pin (VSS)

This is the negative supply.

2.3 Supply Pin (VIO)

VIO supplies the host interface circuits. It can range from 2.9V up to VDD. It should not be higher than VDD. All the IO buffers are referenced to VIO voltage level. If interface is in 5V, then VIO should be shorted to VDD externally.

2.4 Mode Control Pin (STB)

STB controls the operation mode. If STB=0, normal transceiver operation is turned on. STB=1, the transceiver is in standby low power mode. In standby mode, only low-power transceiver front-end is in operation to detect any remote wakeup condition. STB has internal pull up.

The transition time from standby to normal mode is around 100usec. External MCU should allow at least 150usec to start transmission.

2.5 Transmit Data Pin (TXD)

TXD is transmit data input. TXD=1 is for recessive bus state and TXD=0 for dominant bus state. TXD=0 has time out mechanism to prevent rogue behavior. When transition from standby to normal mode, TXD=1 must be met first for further normal transmission of dominant output.

2.6 Receive Data Pin (RXD)

RXD is receive data output. RXD=1 for recessive bus state and RXD=0 for dominant bus state. RXD is kept high during standby mode and responds to bus remote wakeup pattern. After wakeup, RXD follows bus state with time filter of 1usec. When transition from standby to normal mode, RXD may see output glitches due to output handover from low power receiver circuit to high speed receiver circuit.

2.7 Bus Pin (CANH and CANL)

CANH and CANL are CAN bus pins. Typically, the CAN bus is terminated at both ends with 120Ohm termination resistors. And the effective 120Ohm is implemented using two 60Ohm in series with center tap connects to a split voltage at $½V_{DD}$. Within IO1044, the CANH and CANL pins are also internally biased to VCM ($½V_{DD}$) through two 15K resistors separately. This bias is enabled during normal mode, and in standby mode, VCM is 0V to minimize power dissipation.

For recessive output, the transceiver driver is not driving, CANH and CANL remains at $½ V_{DD}$. When transmitting dominant output, the transceiver drives equivalent 60Ohm load and develop a symmetric pseudo-differential voltage centered at $½V_{DD}$.

A high-speed receiver detects a single-end 0.7V threshold of CANH>CAHL to determines if the bus is in dominant state. The receiver output is then sent to RXD buffer. This high-speed receiver is disabled in the standby mode to save power. An additional low-power receiver is active in the standby mode with similar characteristics for the purpose of detecting wakeup event on the bus.

3. Operation Modes

There are two main operation modes, NRM (Normal) mode and STB (Standby) mode. This is controlled by STB pin. STB=0 puts the transceiver in NRM mode and STB=1 puts the transceiver in STB mode. Note the mode transition is not immediate but typically takes 10usec to 60usec. During mode transitions, the RXD output may have glitches especially if the bus is in dominant state.

In addition to NRM and STB modes, there is an OFF mode. OFF mode is entered during power on/off transient when supply voltage under-voltage is detected and when over-temperature protection is detected. In OFF mode, only the internal reference circuits are in operation and all other circuits are turned off. OFF mode always transits to STB mode first and then depending on STB pin state to enter NRM mode.

3.1 STB Mode

In this mode, the transmitter and high speed receive path are shut down. STB mode is enabled when STB pin is pulled high.

Only low power low speed receive path is enabled to detect wakeup pattern as defined in ISO-11898-2:2016 Figure 11 state diagram without automatic biasing. Or in short, the bus signal has gone through two consecutive dominant states with a recessive state in between. The duration of these dominant and recessive states must be longer than $T_{WU.}$ This pattern must be met within T_{WUTO}, otherwise the pattern detection is nullified and needs restart of the detection. When the wakeup pattern is detected, RXD output follows bus signal state and filters out any pulse shorter than T_{WU}. This is illustrated in the following waveform. Wakeup detection is only in STB mode. The wakeup flag is cleared once exiting STB mode.

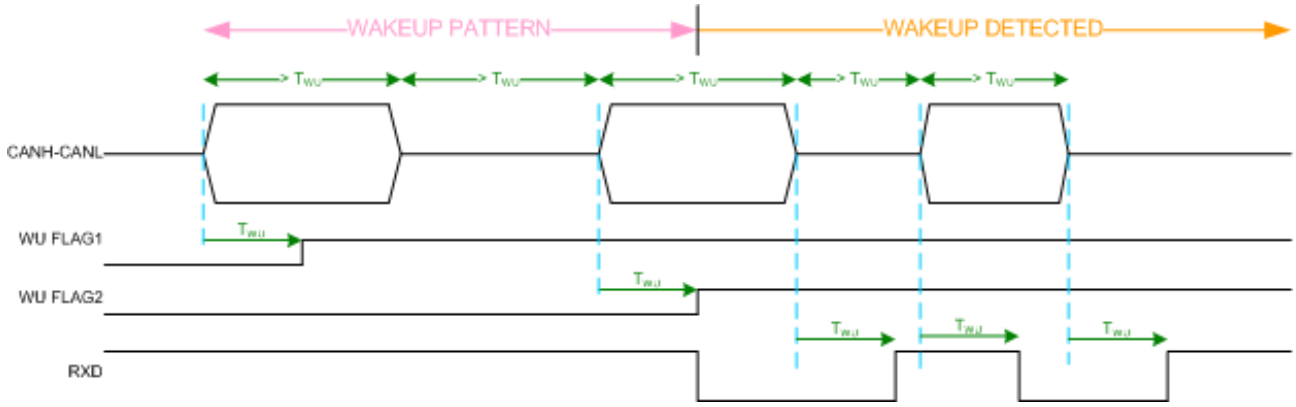


Figure 3-1 IS32IO1044 Wake-up timing

3.2 Normal Mode

When STB pin is pulled low, the transceiver enters normal mode. In NRM mode, the transceiver is in full operation. To start transmission after entering NRM mode, TXD input must be recessive state first. In other words, if TXD is low when entering NRM mode, the dominant state will not be output.

In addition, a TXD=0 timeout timer is used to monitor the duration of dominant output state. If the duration exceeds T_{DOMTO}, the transmitter is blocked off. This is to prevent a rogue transmission preventing other CAN nodes from accessing the bus. The timeout behavior is cleared when TXD=1 is observed. NRM mode transits to STB mode when STB=1.

The transition time from standby to normal mode is around 100usec for bias to stabilize. External MCU should allow at least 150usec to start transmission.

3.3 Under-voltage/Over-Temperature Protection

VDD and VIO are monitored for under-voltage. VDD's threshold is around 4.1V with hysteresis of 0.5V. VIO's threshold is 2.6V with hysteresis of 0.2V. Over temperature protection is set at 170C.

When under-voltage and over temperature are detected, the transceiver is put in OFF mode. The receive and transmit paths are disabled. Only internal regulator and reference circuits are in operation.

OFF mode always exits to STB mode first.

3.4 Loss of Supply and Ground

In the events when supply or ground loss, the transceiver presents no load to the bus. This is accomplished by the isolation diodes at the transmitter driver output. The bus still sees a differential resistance of around 40K Ohm due to receiver biasing network, however there is minimum DC leakage path to supply or ground.

3.5 Test Circuits

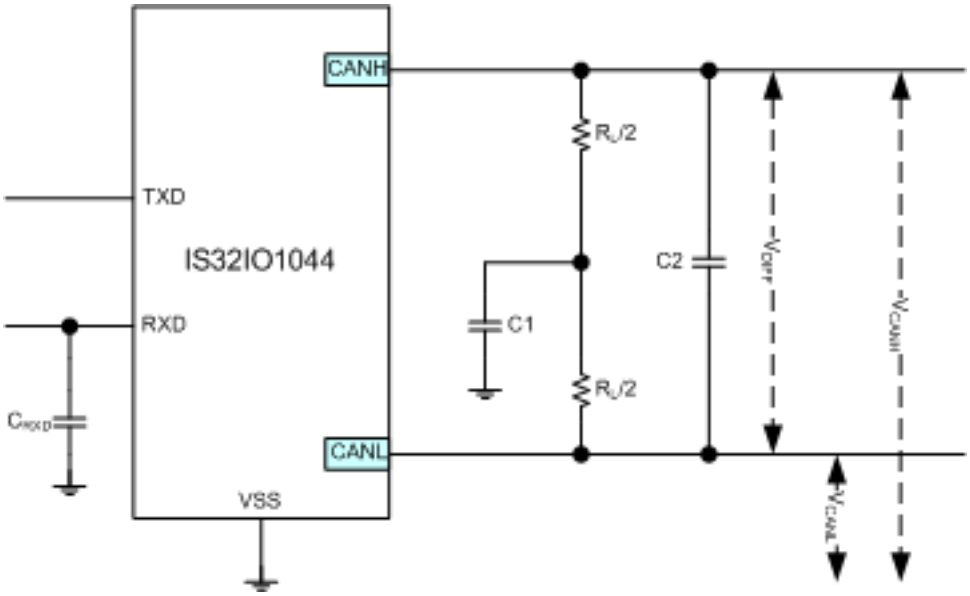


Figure 3-2 IS32IO1044 HS-PMA test circuit

V_{DIFF} Differential voltage between CANH and CANL.

V_{CANH} Single-end voltage on CANH.

V_{CANL} Single-end voltage on CANL.

R_L Bus load resistance. 60 Ohm unless otherwise specified.

C1 4.7nF unless otherwise specified.

C2 100pF unless otherwise specified.

C_{RXD} 15pF unless otherwise specified.

3.6 Timing Diagram

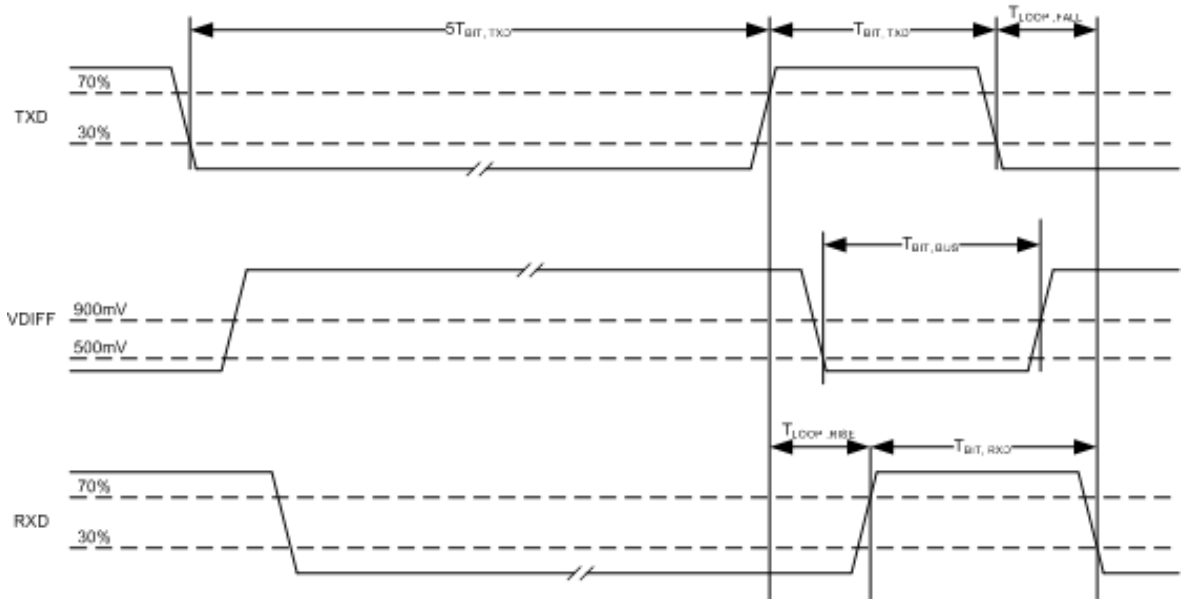


Figure 3-3 HS-PMA implementation timing diagram

$T_{BIT, TXD}$ = 1000ns for 1Mbit/s

$T_{BIT, TXD}$ = 500ns for 2Mbit/s

$T_{BIT, TXD}$ = 200ns for 5Mbit/s

4. Electrical Specifications

4.1 Maximum Limits

Parameter	Conditions	MIN	MAX	Unit
Voltage on Pin	Pin VDD	-0.3	6.0	V
	Pin VIO	-0.3	V_{DD}	V
	PIN RXD, TXD, STB	-0.3	V_{IO}	V
	Pin CANH CANL	-40	+40	V
	Voltage between CANH and CANL	-27	+27	V
ESD Rating	HBM			
	Pin CANH CANL (note 1)	-8	+8	kV
	at any other pin	-2	+2	kV
	MM			
	Any Pin	-250	+250	V
	CDM			
	Corner Pins	-750	+750	V
	Any Pin	-500	+500	V
Junction Temperature		-40	+150	℃
Storage Temperature		-55	+150	℃

Note 1: VDD and VSS tie to ground.

4.2 Thermal Characteristics

Symbol	Parameter	Conditions	TYP	Unit
RTHJA	thermal resistance from junction to ambient	eSO8 package free air	60	℃/W
		HVSON8 package free air	67	℃/W

4.3 DC Characteristics

V_{DD} = V_{IO} = 4.75V to 5.25V. T_J = -40℃ to +150℃. V(CANH) and V(CANL) within +/- 12V. Typical values are given at V_{DD} = 5.0V unless otherwise specified. All voltages are defined with respect to VSS or ground.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
Pin VDD and VIO						
V_{DD}	Supply voltage		4.75	5	5.25	V
$V_{DD, ON}$	V_{DD} under-voltage ramp up		3.8	4.1	4.4	V
$V_{DD, OFF}$	V_{DD} under-voltage ramp down		3.4	3.8	4.2	V
V_{IO}	IO supply voltage		2.9	-	V_{DD}	V
$V_{IO, UV}$	V_{IO} under-voltage	V_{DD} = 5.0V	2.2	2.5	2.8	V
I_{VDD}	VDD Supply current	STB mode	-	35	50	μA
		NRM mode recessive	-	4	10	mA
		NRM mode dominant (60Ohm)	-	45	60	mA
I_{VIO}	VIO Supply current	V_{DD} = 5.0V, STB=TXD=HIGH	-	20	50	μA
Pin STB, TXD, RXD						
V_{IH}	Logic input high voltage	STB, TXD pins	0.7 V_{IO}	-	-	V
V_{IL}	Logic input low voltage	STB, TXD pins	-	-	0.3 V_{IO}	V

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
$I_{IL, STB}$	Logic input low current, STB	V(STB)=0V	-	5	15	μA
$I_{IL, TXD}$	Logic input low current, TXD	V(TXD)=0V	-	150	250	μA
V_{OH}	Logic output high voltage	RXD pin @ I_{OH} = 4mA	V_{IO}–0.5	-	-	V
V_{OL}	Logic output low voltage	RXD pin @ I_{OL} = 8mA	-	-	0.5	V
Bus CANH/CANL						
R_{DIFF}	Differential Input Resistance		20	40	80	KΩ
R_{CAN}	Single-End Resistance		10	20	40	KΩ
M_{CANR}	Matching of Resistance		-2.5	0	+2.5	%
C_{CAND}	Differential Capacitance	Not tested.	-	10	-	pF
C_{CANS}	Single-End Capacitance	Not tested.	-	8	-	pF
I_{CANLK}	Leakage Current, loss of power	V(CANH)=V(CANL)=5V V1=VIO=GND=0V or short to 0V through 47KΩ	-10	-	+10	μA
Bus Receive						
$V_{TH, NRM}$	Normal mode threshold	12V <= V(CANH) <= +12V -12V <= V(CANL) <= +12V	0.5	-	0.9	V
$V_{HYS, NRM}$	Normal mode hysteresis	12V <= V(CANH) <= +12V -12V <= V(CANL) <= +12V	50	85	125	mV
$V_{REC, NRM}$	Normal mode recessive differential input voltage	V(CANH) – V(CANL) -12V <= V(CANH) <= +12V -12V <= V(CANL) <= +12V	-3.0	-	0.5	V
$V_{DOM, NRM}$	Normal mode dominant differential input voltage	V(CANH) – V(CANL) -12V <= V(CANH) <= +12V -12V <= V(CANL) <= +12V	0.9	-	8.0	V
$V_{TH, STB}$	Standby mode threshold	12V <= V(CANH) <= +12V -12V <= V(CANL) <= +12V	0.4	-	1.15	V
$V_{REC, STB}$	Standby mode recessive differential input voltage	V(CANH) – V(CANL) -12V <= V(CANH) <= +12V -12V <= V(CANL) <= +12V	-3.0	-	0.4	V
$V_{DOM, STB}$	Standby mode dominant differential input voltage	V(CANH) – V(CANL) -12V <= V(CANH) <= +12V -12V <= V(CANL) <= +12V	1.15	-	8.0	V
V_{CANCM}	Common mode voltage range		-12	2.5	12	V
Bus Transmit						
$V_{OUT, RECN}$	NRM Recessive CANH/CANL output voltage	R_L not present	0.45	0.5	0.55	V_{DD}
$V_{OUTD, RECN}$	NRM Recessive Differential Output Voltage	R_L not present	-50	0	50	mV
$I_{OUT, RECN}$	NRM Recessive Current	CANH=CANL= +32V to -15V, R_L = 50Ω - 65Ω	-5	0	5	mA
$V_{OUTH, DOM}$	CANH dominant single-end output	R_L = 50Ω - 65Ω	2.75	3.6	4.50	V
$V_{OUTL, DOM}$	CANL dominant single-end output	R_L = 50Ω - 65Ω	0.50	1.4	2.25	V
$V_{OUTD, DOM}$	Dominant output differential swing	$V_{OUTH, DOM}$ - $V_{OUTL, DOM}$ R_L = 50Ω - 65Ω	1.50	2.2	3.00	V

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
$V_{OUTD, DOM, ARB}$	Dominant output differential swing, arbitration	$V_{OUTH, DOM}$ - $V_{OUTL, DOM}$ R_L = 2240Ω	1.50	3.8	5.00	V
$S_{OUT, DOM}$	Dominant output symmetry	V1 - ($V_{OUT, CANH}$ + $V_{OUT, CANL}$) R_L = 50Ω - 65Ω	-0.50	0	0.50	V
V_{SYM}	Driver symmetry	R_L = 60Ω, C_1=4.7nF 1MHz square wave	0.9	1	1.1	-
$I_{OSCH, DOM}$	CANH dominant output short-circuit current	V(CANH) = 0V	-	50	80	mA
$I_{CANH, MAX}$	CANH output maximum current	V(CANH) = -3V to 18V	-	-	115	mA
$I_{OSCL, DOM}$	CANL dominant output short-circuit current	V(CANL) = 5V	-	50	80	mA
$I_{CANL, MAX}$	CANL output maximum current	V(CANL) = -3V to 18V	-	-	115	mA
$V_{OUT, RECS}$	STB mode Recessive CANH/CANL output voltage	R_L not present	-100	0	100	mV
$V_{OUTD, RECS}$	STB mode Recessive Differential output Voltage	R_L not present	-150	0	150	mV
Thermal Protection						
T_{JOTS}	Shutdown temperature	Not tested. *1	-	175	-	℃
T_{JOTR}	Recovery temperature	Not tested. *1	-	120	-	℃

Table 4-1 IS32IO1044 DC Characteristics

Note 1: Not tested. Guaranteed by design and characterization.

4.4 AC Characteristics

V_{DD} = V_{IO} = 4.75V to 5.25V. T_J = -40℃ to +150℃. V(CANH) and V(CANL) within +/- 12V.

Refer to Sections 2.6/2.7 for the test circuit with typical values of R_L=60Ω, C_1=4.7nF, C_{RXD}=15pF used and timing waveform.

Typical values are given at V_{DD} = 5.0V unless otherwise specified.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
$T_{VDD,RAMP}$	Supply ramp up/down time	*1	-	-	50	ms
$T_{STARTUP}$	Start up time	*1	-	-	10	ms
$T_{PD,RX}$	Receive Propagation Delay	V_{CANCM}=2.5V, V_{CANDF}=1.5V C_{RXD} = 15 pF	-	90	-	ns
$T_{SYM,RX}$	Receive propagation delay mismatch	Recessive bit time distortion. *1	-20	-	+5	ns
$T_{PD,TX}$	Transmit Propagation Delay		-	60	-	ns
$T_{PDMS,TX}$	Transmit propagation delay mismatch	Recessive bit time distortion. *1	-25	-	+5	ns
T_{LOOP}	Loop delay	R_L = 60 Ω, C_1=4.7nF, C_2 = 100 pF, C_{RXD} = 15 pF	65	85	105	ns
$T_{BIT BUS, 2M}$	Transmitted recessive bit width 2Mbps	R_L = 60 Ω, C_2 = 100 pF. *1	435	-	530	ns
$T_{BIT RXD, 2M}$	Received recessive bit width 2Mbps	R_L = 60 Ω, C_2 = 100 pF, C_{RXD} = 15 pF. *1	400	-	550	ns
$\Delta T_{BIT RXD, 2M}$	Received timing symmetry 2Mbps $T_{RXD,DOM} - T_{RXD,REC}$	R_L = 60 Ω, C_2 = 100 pF, C_{RXD} = 15 pF. *1	-65	-	40	ns

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
$T_{BIT\ BUS,\ 5M}$	Transmitted recessive bit width 5Mbps	R_L = 60 Ω, C_2 = 100 pF. *1	155	-	210	ns
$T_{BIT\ RXD,\ 5M}$	Received recessive bit width 5Mbps	R_L = 60 Ω, C_2 = 100 pF, C_{RXD} = 15 pF. *1	120	-	220	ns
$\Delta T_{BIT\ RXD,\ 5M}$	Received timing symmetry 5Mbps $T_{RXD,DOM} - T_{RXD,REC}$	R_L = 60 Ω, C_2 = 100 pF, C_{RXD} = 15 pF. *1	-45	-	15	ns
$T_{DOM,TO}$	TXD dominant time-out time		1	5	10	ms
T_{WU}	Wakeup Filter Time	$V_{CAN,CM}$=2.5V, $V_{CAN,DIFF}$=1.2V	0.5	1.0	1.8	µs
T_{WUTO}	Wakeup detection window		1	5	10	ms
T_{STDLY}	Transition time from STB to NRM state	*1	-	100	150	µs

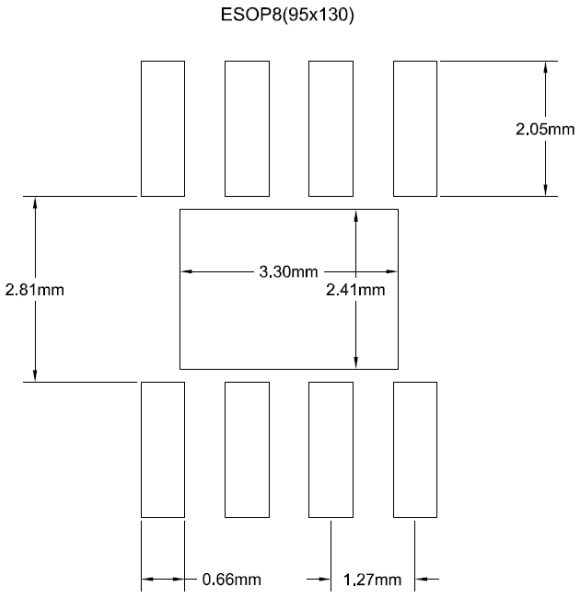
Table 4-2 IS32IO1044 AC Characteristics

Note *1: Not tested. Guaranteed by design and characterization.

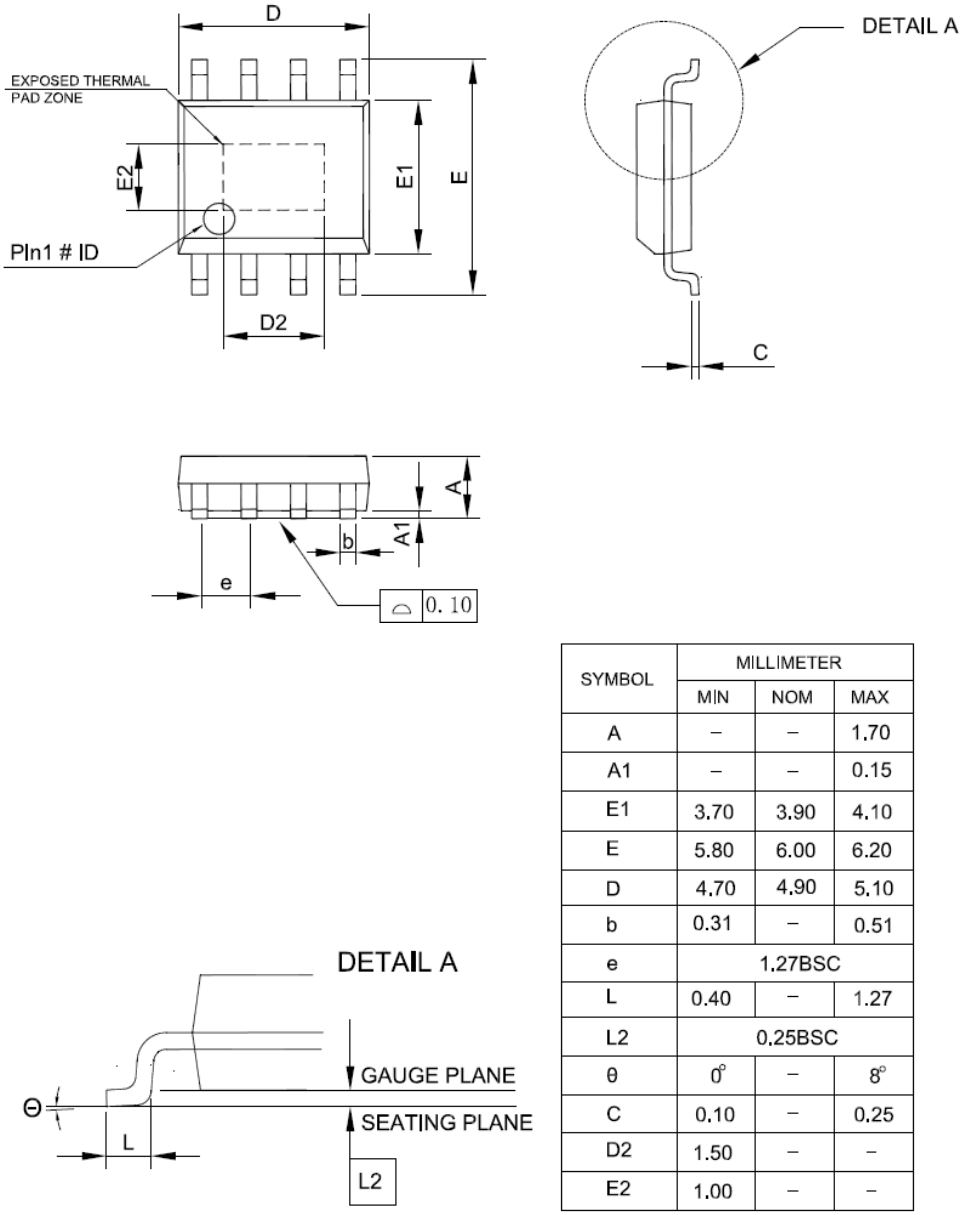
5. Packaging Outline

5.1 eSOP-8

5.1.1 RECOMMENDED LAND PATTERN



5.1.2 POD



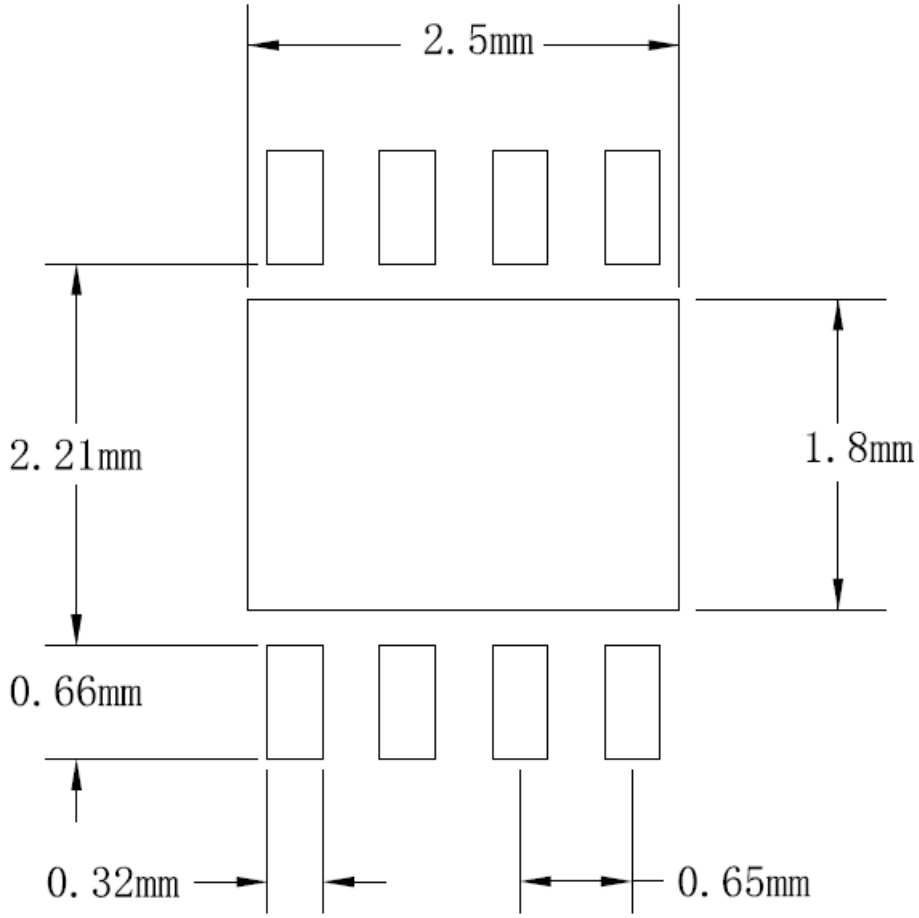
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	–	–	1.70
A1	–	–	0.15
E1	3.70	3.90	4.10
E	5.80	6.00	6.20
D	4.70	4.90	5.10
b	0.31	–	0.51
e	1.27BSC		
L	0.40	–	1.27
L2	0.25BSC		
θ	0°	–	8°
C	0.10	–	0.25
D2	1.50	–	–
E2	1.00	–	–

NOTE:

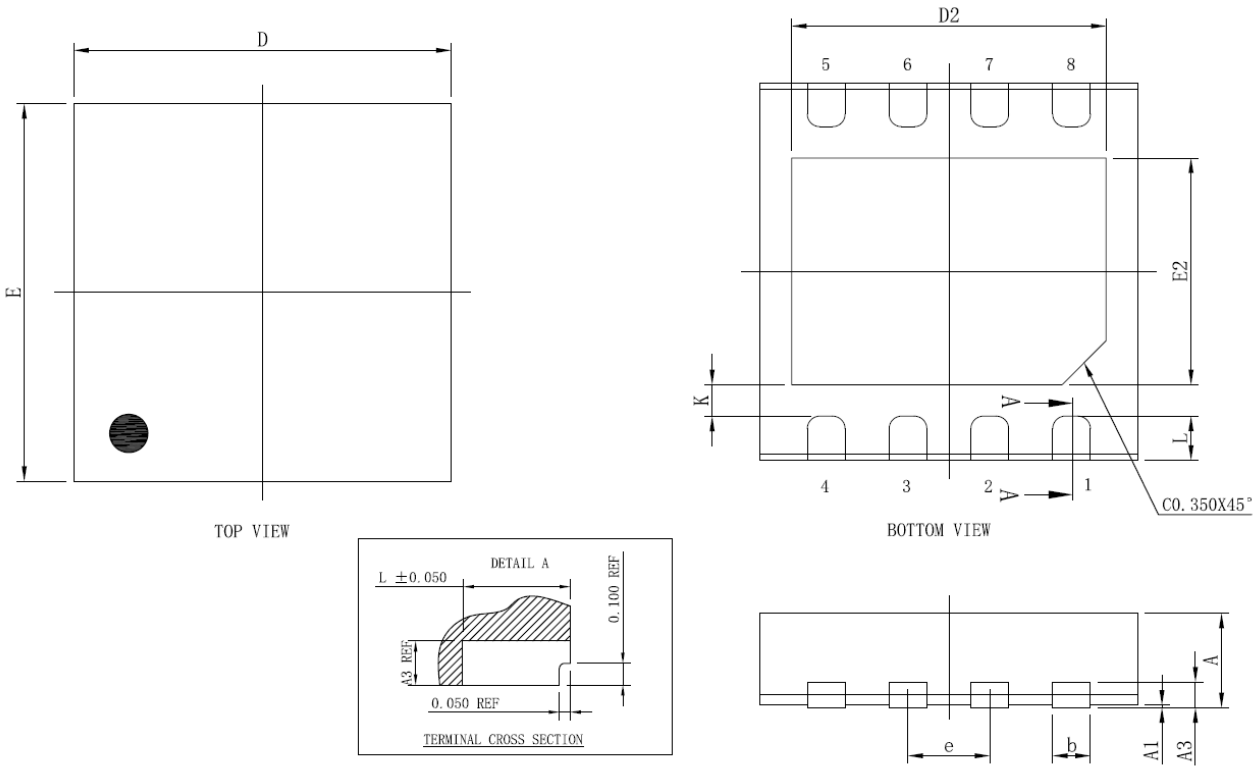
1. CONTROLLING DIMENSION:MM
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3. DIMESION b DOES NOT INCLUDE DAMBAR PROTRUSION.
4. REFERENCE DOCUMENT: JEDEC MS-012
5. THE SHAPE OF BODY AND THERMAL PAD SHOW DIFFERENT SHAPE AMONG DIFFERENT FACTORIES.

5.2 WDFN-8 Package Outline

5.2.1 RECOMMENDED LAND PATTERN



5.2.2 POD



SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF.	
b	0.25	0.30	0.35
D	2.90	3.00	3.10
E	2.90	3.00	3.10
e		0.65 BSC	
L	0.30	0.35	0.40
D2	2.45	2.50	2.55
E2	1.75	1.80	1.85
K	0.20	—	—

NOTE:

1. CONTROLLING DIMENSION: MM
2. REFERENCE DOCUMENT: JEDEC MO-229F

6. Ordering Information

Temperature Range: -40℃ to 125℃

Part No.	Package	QTY/Reel	Remark
IS32IO1044A-GRLA3-TR	SOP-8 with exposed pad, Lead-free	2500/Reel	VIO internally connects to VDD
IS32IO1044B-GRLA3-TR	SOP-8 with exposed pad, Lead-free	2500/Reel	Independent VIO pin

7. ERRATA

8. Revisions

Revision	Detailed Information	Date
0A	The initial engineering phase released version	2023.03.14
A	Formal release version	2026.03.16