IS32FL3105

2×18 MATRIX LED DRIVER

May 2026

1 GENERAL DESCRIPTIONS

The IS32FL3105 is a general-purpose 2×18 LED Matrix programmed via a Lumissil proprietary bus (LumiBus™). Each LED can be dimmed individually with 16-bit/14+2-bit/13+3-bit/8+8-bit PWM data and 6-bit DC scaling data which allows 65536 steps of linear PWM dimming and 64 steps of DC current adjustable level.

The maximum output current of each LED channel (for R, G, B) is 60mA. All registers in the IS32FL3105 can be accessed by CAN communication interface (IS32FL3105A/B) or UART communication interface (IS32FL3105C/D) are used for control and management by a host MCU.

IS32FL3105A/C supports direct address can assign up to 25 devices by ADDR0 and ADRR1 pin. IS32FL3105B/D supports LAA (Location Address Assignment) for random LED driver access without address pins, up to 254 devices can be addressed.

Additionally, each LED open/short state can be detected, IS32FL3105 stores the open information in Open/Short Detect Registers. The Open/Short Detect Registers allow MCU to read out via LumiBus, inform MCU whether there are LEDs open or LEDs short.

The IS32FL3105 operates from 3.0V to 12V for VLED 5V to 28V for VS and features a low shutdown and operational current.

IS32FL3105 is available in WFQFN-32 (5mm×5mm) package. It operates from 3.0V to 12V over the temperature range of -40°C to +125°C.

2 APPLICATIONS

- Ambient LED Light
- Automotive rear light
- Automotive clusters
- Automotive interiors

3 FEATURES

- VLED operates with a power supply range of 3.0V to 12V for each LED channel
- VS power supply voltage ranges from 5V to 28V, providing normal operation for the IS32FL3105
- Built- in LDO to generate V50 to power on chip logic circuit operation and powering internal CAN PHY
- CAN interface (IS32FL3105A/B) and UART interface (IS32FL3105C/D) with Lumissil's proprietary LumiBus protocol support communication from 100kHz to 2MHz
- Direct address for IS32FL3105A/C, can support up to 25 devices
- LAA (Location Address Assignment) for random IS32FL3105B/D register access without address pins, up to 254 devices can be addressed
- Support 12 LED RGB color dots (2×18 channel)
  - ✓ Each LED channel has 16-bit/14+2-bit/13+3-bit/8+8-bit PWM engines and independent 4-bit Save PWM State on OTP
  - ✓ Independent 6-bit configurable DC configurations ranging from 0 mA to 60 mA
  - ✓ 6-bit global output current adjustment for each RGB group
  - ✓ Inter and intra channel accuracy:
    - Channel to Channel 60mA: ±4%(Max.25°C)
    - Channel to Channel 60mA: ±6%(Max.-40°C~125°C)
- Support on die OTP for fail safe mode
- Provide constant luminance over wide temperature range by temperature compensation algorithm in PWM space for each individual channel
- Support spread spectrum on PWM clock to reduce EMI from driver
- Built-in standard CAN PHY (physical layer)
- Cross fading accelerator
- DC feedback for automatic DCDC VLED adjustment to optimize system power supply (DCFB)
- Fault detection and protection
  - ✓ LED open/short detection: cycle by cycle detection and configure LED short threshold
  - ✓ SW short to VLED detection
  - ✓ SW over-current protection
  - ✓ VLED under-voltage detection
  - ✓ ECC on OTP for error detection
  - ✓ Support thermal shutdown protection and thermal roll-off mechanism
  - ✓ CS loop back and SW loop back detection

- ✓ IOUT monitor and LED VF monitor detection
- ✓ Internal PWM clock monitor detection
- ✓ CRC error detection for communication
- ✓ Communication watch dog and watch dog timer2 detection

- Developed according to ISO26262 with process complying with ASIL-B Potential applications
- AEC-Q100 Qualified with Temperature Grade 1: -40°C to 125°C
- WFQFN-32 (5mm× 5mm) package
- RoHS & Halogen-Free Compliance
- TSCA Compliance

4 TYPICAL APPLICATION CIRCUIT

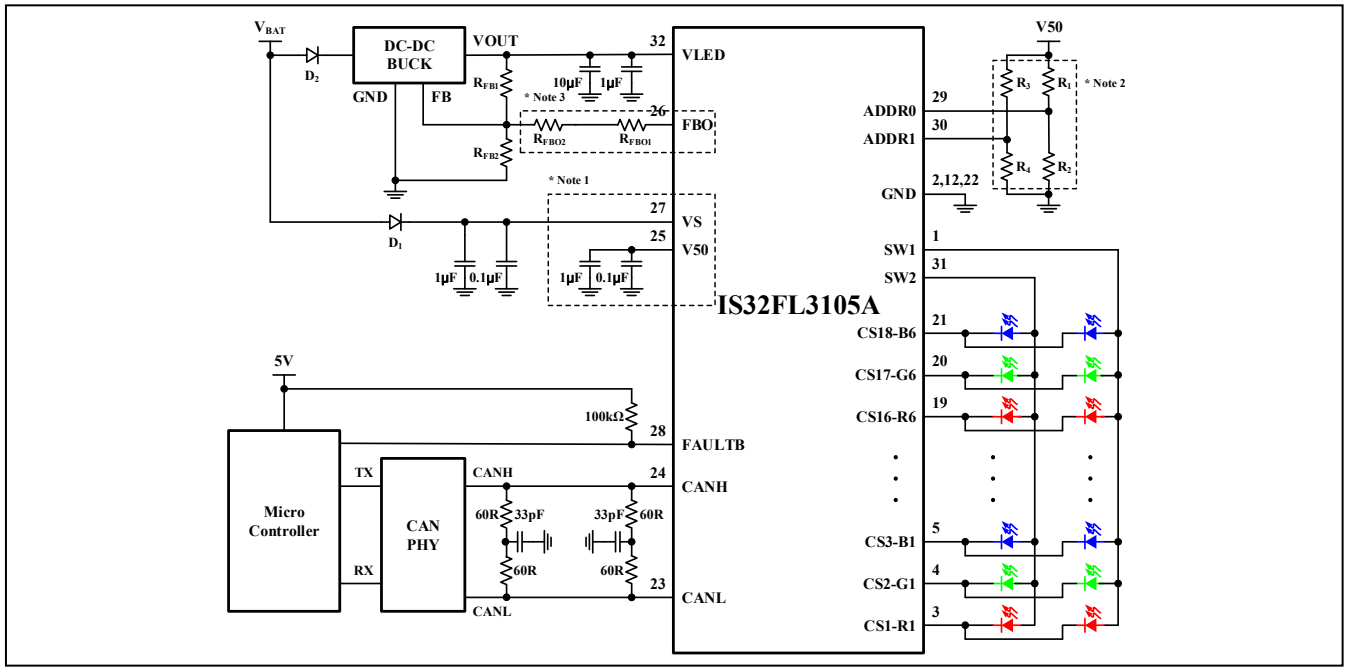


Figure 1 Typical Application Circuit of IS32FL3105A with CAN Interface for On-Board Communication

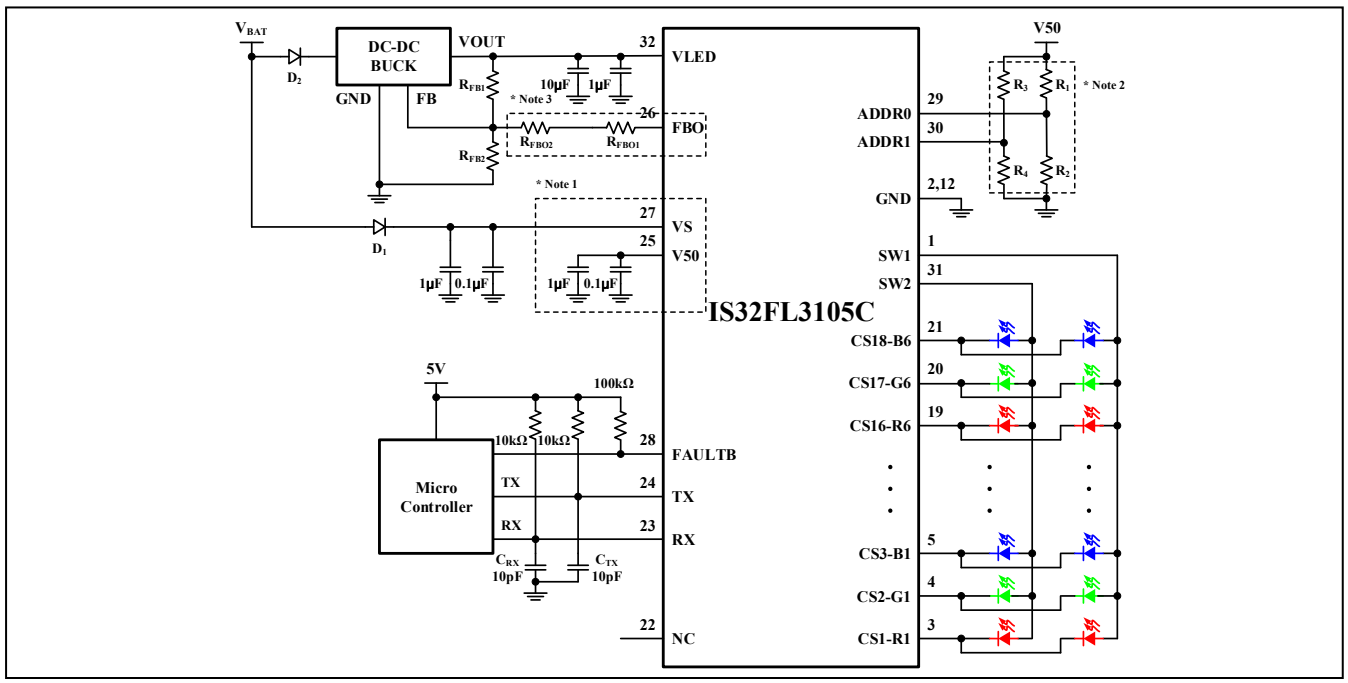


Figure 2 Typical Application Circuit of IS32FL3105C with UART Interface for On-Board Communication

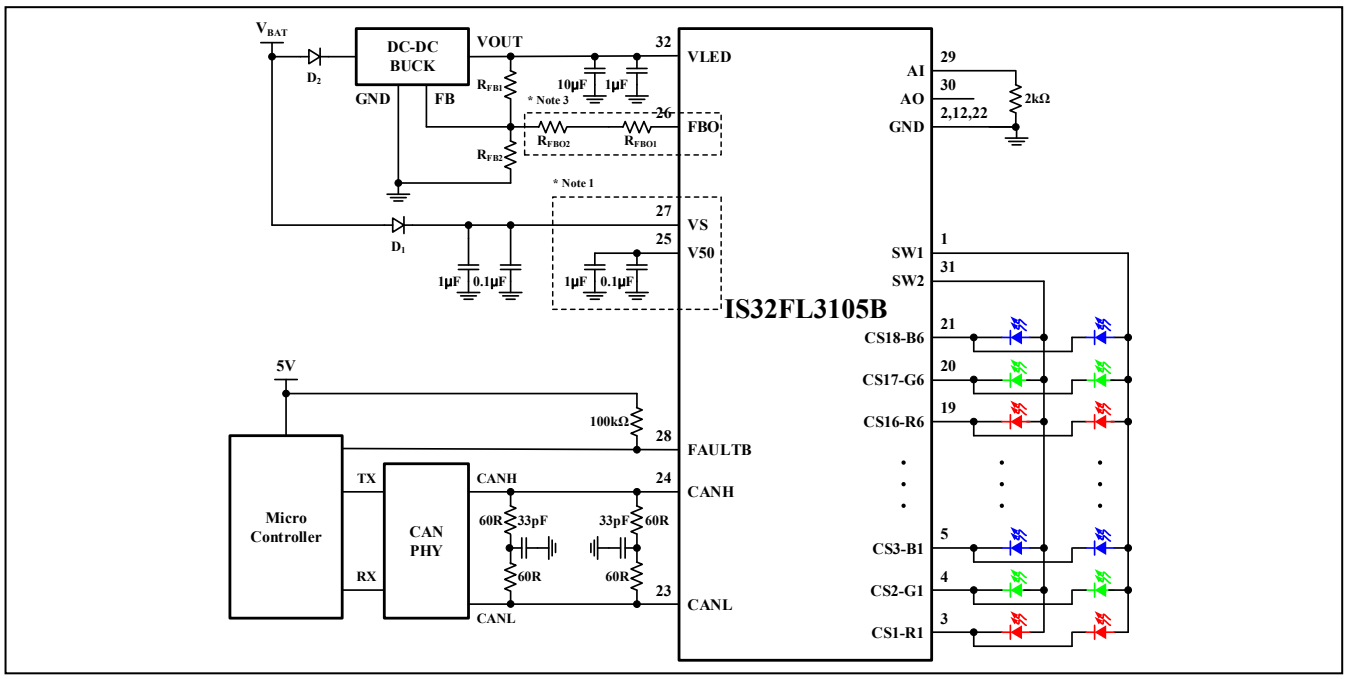


Figure 3 Typical Application Circuit of IS32FL3105B with CAN Interface for On-Board Communication

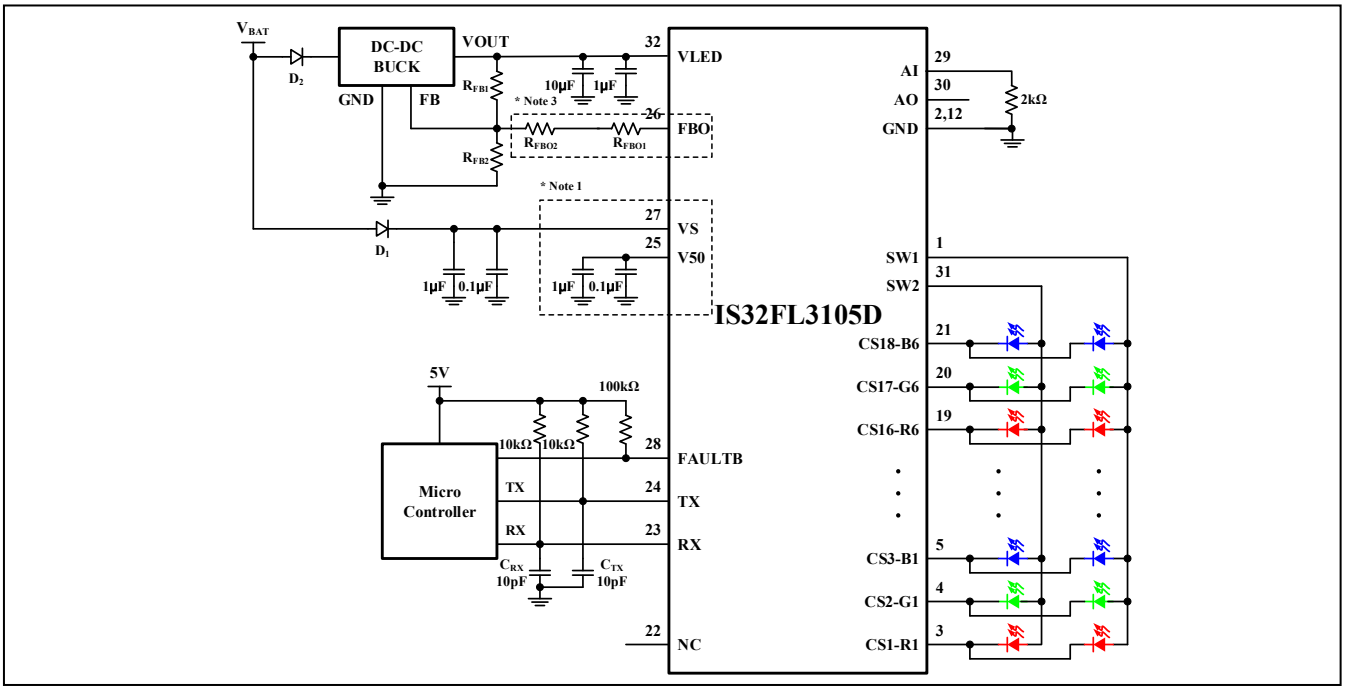


Figure 4 Typical Application Circuit of IS32FL3105D with UART Interface for On-Board Communication

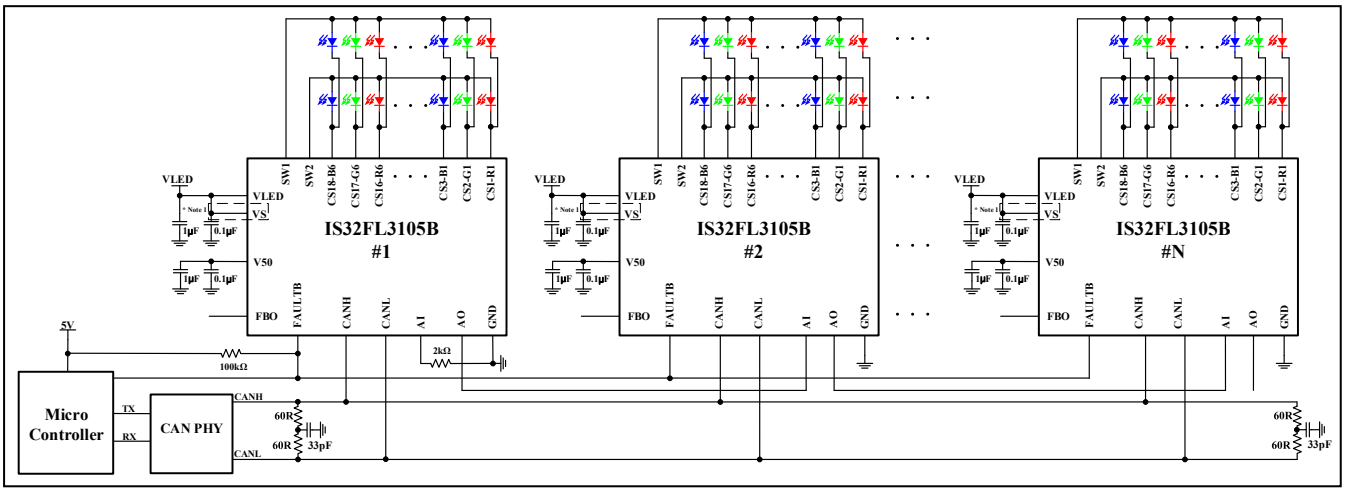


Figure 5 Typical Application Circuit of IS32FL3105B with CAN Interface (Cascade at SNPD Address Mode)

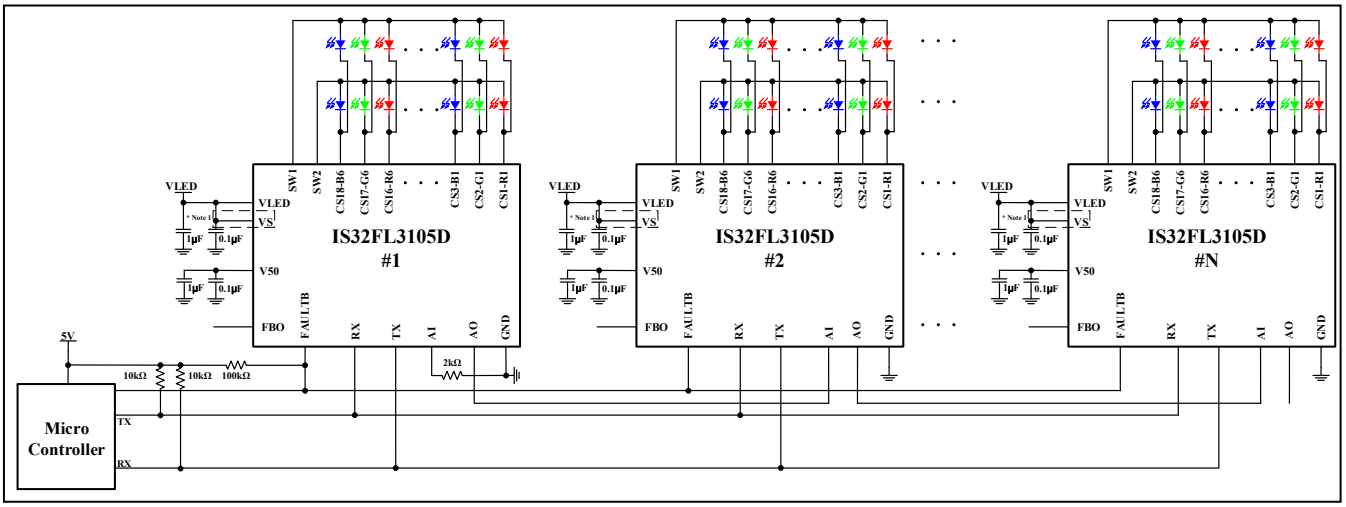


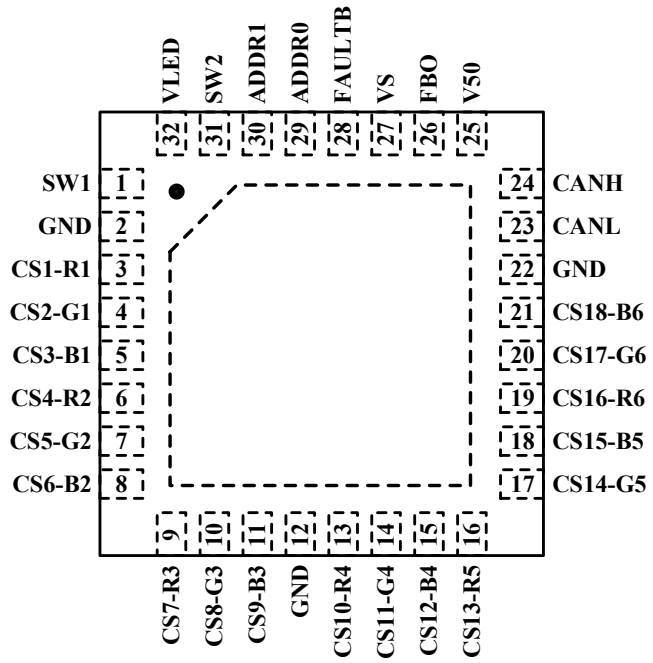
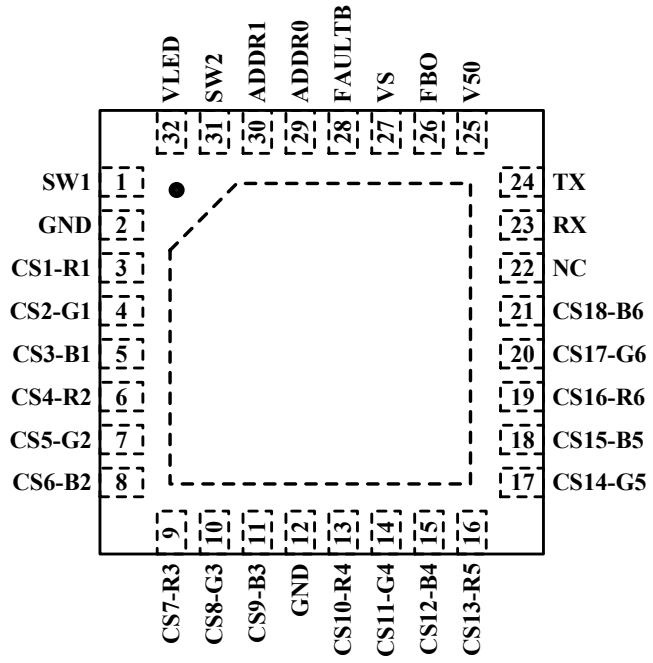
Figure 6 Typical Application Circuit of IS32FL3105D with UART Interface (Cascade at SNPD Address Mode)

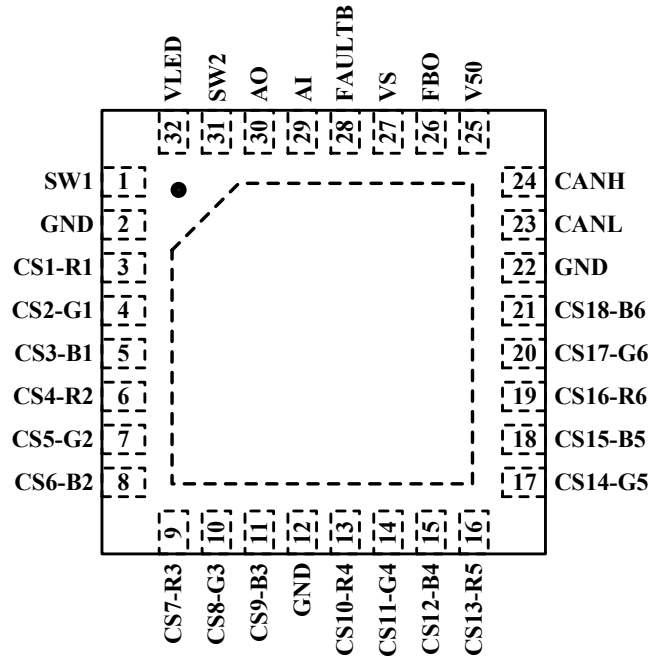
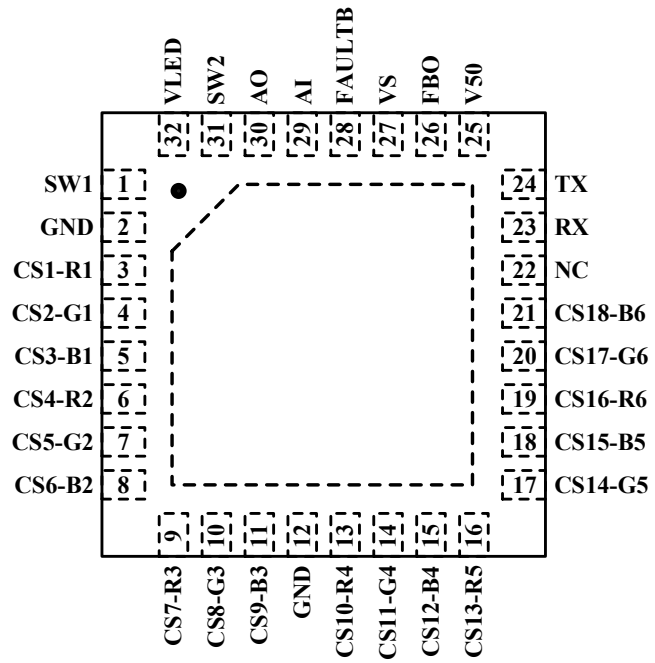
Note 1: The VS pin is analog and digital circuits' power, support 5V~28V, which can directly supply power from VLED when V_{LED} ≥5.5V, and it is recommend connecting V50 and VS together when VS power supply is less than 5.5V.

Note 2: The R_1 ~ R_4 are for select devices address, selection of address please check Direct Address Setting description for more information.

Note 3: Resistors R_{FBO1} and R_{FBO2} can improve the immunity against interference for the FBO input/output current of the IS32FL3105. One R_{FBOx} resistor should be placed close to the FB pin of the BUCK chip, and the other should be placed close to the FBO pin of the IS32FL3105.

5 PIN CONFIGURATION

Package	Part No.	Pin Configuration (Top View)
WFQFN-32	IS32FL3105A	
	IS32FL3105C	

Package	Part No.	Pin Configuration (Top View)
WFQFN-32	IS32FL3105B	
	IS32FL3105D	

PIN DESCRIPTION

No.	Pin	Description
1, 31	SW1, SW2	High side power switches, for 2×LED channels scanning.
2,12	GND	Ground.
22 (A, B)	GND	Ground.
22 (C, D)	NC	Not Connect.
3~11,13~21	CS [1:18]	18 LED current sink channels.
23 (A, B)	CANL	LumiBus differential input Low level.
24 (A, B)	CANH	LumiBus differential input High level.
23 (C, D)	RX	UART interface received data pin.
24 (C, D)	TX	UART interface transmitted data pin.
25	V50	Internal 5V LDO power, the V50 pin needs decoupling capacitor.
26	FBO	Feedback output. If used connect FB to the feedback divider of the external LED DC/DC converter.
27	VS	Analog and digital circuits power.
28	FAULTB	Fault report pin. Fault Register 01h~02h at Page 1 can read the function of the FAULTB pin and active low when the fault event happens. Can be NC (float) if fault report function is not used.
29,30 (A, C)	ADDR0~ADDR1	Address setting.
29 (B, D)	AI	Address setting, AI is LAA mode input.
30 (B, D)	AO	Address setting, AO is LAA mode output.
32	VLED	Power for current source SWx.
	Thermal pad	Need to connect to GND.

6 ORDERING INFORMATION

Automotive Range: -40°C To +125°C

Order Part No.	Package	QTY/Reel
IS32FL3105A-QWLCA3-TR IS32FL3105B-QWLCA3-TR IS32FL3105C-QWLCA3-TR IS32FL3105D-QWLCA3-TR	WFQFN-32, Lead-free	2500

7 SPECIFICATIONS

7.1 ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{LED}	-0.3V ~ +16V
Supply voltage, V_S	-0.3V ~ +40V
Voltage at CSy pin	-0.3V ~ +16V
Voltage at CANH, CAHL pin	-40V ~ +40V
Voltage at TX, RX, ADDRx, AI, AO, V50, FAULTB	-0.3V ~6V
Maximum junction temperature, T_{JMAX}	+150°C
Storage temperature range, T_{STG}	-65°C ~+150°C
Operating temperature range, T_A=T_J	-40°C ~ +150°C
Package thermal resistance, junction to ambient (4-layer standard test PCB based on JESD 51-2A), θ_{JA}	38.5°C/W
Package thermal resistance, junction to case (bottom) (4-layer standard test PCB based on JESD 51-14), θ_{JC_BOT}	10.1°C/W
ESD (HBM) ESD (HBM)-CANH&CANL ESD (CDM)	±6kV ±8kV ±750V

Note 4: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7.2 ELECTRICAL CHARACTERISTICS

"♦" This symbol in the table means these limits are guaranteed at room temp T_J= 25°C.
"◊" This symbol in the table means these limits are guaranteed at full temp range T_J= -40°C~125°C.
The following specifications apply for T_J= -40°C ~ +125°C, V_S= 12V, V_{LED}= 5V, the detail refers to each condition description. Typical values are at T_J= 25°, V_S= 12V, V_{LED}= 5V, unless otherwise noted (Note 5).

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_{LED}	Power supply voltage			3		12	V
V_S	Supply voltage			5		28	V
I_{CC}(VLED)	Quiescent power supply current	V_{LED}=5V, V_S=12V, OSC=16MHz, all LEDs off, PWM Update Enable.		1.2	1.4	1.6	mA
I_{CC}(VS)		V_{LED}=5V, V_S=12V, OSC=16MHz, all LEDs off, PWM Update Enable.		9	10	11.5	mA
I_{SD}	Shutdown current	V_{LED}=5V, V_S=12V, OSC=16MHz, PSM=1, all LEDs off	♦		50	100	μA
		V_{LED}=5V, V_S=12V, OSC=16MHz, PSM=1, all LEDs off	◊		50	600	μA
$I_{OUT(MAX)}$	Maximum constant current of CSy	GCCx=0x3F, SL=0x3F, PWM=0xFFFF, V_{OUT}= 0.6V	♦	57.5	60	62.5	mA
		GCCx=0x3F, SL=0x3F, PWM=0xFFFF, V_{OUT}= 0.6V	◊	56	60	64.5	mA
ΔI_{MAT}	I_{OUT} mismatch (channel to channel) (Note 6)	PWM=0xFFFF, V_{OUT}= 0.6V, I_{OUT}=60mA.	♦	-4		4	%
		PWM=0xFFFF, V_{OUT}= 0.6V, I_{OUT}=60mA.	◊	-6		6	%
		PWM=0xFFFF, V_{OUT}= 0.6V, I_{OUT}=20mA.	♦	-4		4	%
		PWM=0xFFFF, V_{OUT}= 0.6V, I_{OUT}=20mA.	◊	-5		5	%

7.3 ELECTRICAL CHARACTERISTICS (CONTINUED)

"♦" This symbol in the table means these limits are guaranteed at room temp T_J= 25°C.
"◊" This symbol in the table means these limits are guaranteed at full temp range T_J= -40°C~125°C.
The following specifications apply for T_J= -40°C ~ +125°C, V_S= 12V, V_{LED}= 5V, the detail refers to each condition description. Typical values are at T_J= 25°C, V_S= 12V, V_{LED}= 5V, unless otherwise noted (Note 5).

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
ΔI_{ACC}	I_{OUT} accuracy (device to device) (Note 7)	PWM=0xFFFF, V_{OUT}= 0.6V, I_{OUT}=60mA	♦	-3		3	%
			◊	-4		4	%
		PWM=0xFFFF, V_{OUT}= 0.6V I_{OUT}=20mA		-3		3	%
VHR	Current switch headroom voltage SWx	I_{SWITCH}=400mA, PWM=0xFFFF			200	500	mV
		I_{SWITCH}=1080mA, PWM=0xFFFF (Note 8)			500		mV
	Current sink headroom voltage CSy	I_{SINK}=60mA, GCCx=0x3F, SL=0x3F, PWM=0xFFFF			300	550	mV
t_{SCAN}	Period of SWx scanning	OSC=16MHz, 16-bit PWM Mode		3.7	4.096	4.5	ms
		OSC=16MHz, 14+2-bit PWM Mode		0.92	1.024	1.13	ms
		OSC=16MHz, 13+3-bit PWM Mode		460	512	565	µs
		OSC=16MHz, 8+8-bit PWM Mode		14.2	16.5	17.8	µs
t_{CSON}	CS-ON time during scan, the CSy are all on during this time	OSC=16MHz, 16-bit PWM Mode		3.7	4.095	4.5	ms
		OSC=16MHz, 14+2-bit PWM Mode		0.92	1.023	1.13	ms
		OSC=16MHz, 13+3-bit PWM Mode		460	511	565	µs
		OSC=16MHz, 8+8-bit PWM Mode		13.6	15.9	17.2	µs
t_{NOL1}	Non-overlap blanking time during scan, the SWx and CSy are all off during this time	OSC=16MHz			0.3		µs
t_{NOL2}	Delay total time for CS1 to CS 18, during this time, the SW is on, but CS is not all turned on	OSC=16MHz (Note 8)			0.2		µs
V_{OD}	LED open detect threshold	V_{LED}=5V, I_{OUT}≥1mA, PWM> 25% (OSC=16MHz), measured at CSy		0.06	0.1		V
V_{SD}	LED short detect threshold	V_{LED}=5V, I_{OUT}≥1mA, PWM> 25%(OSC=16MHz), measured at (V_{LED}-V_{CSy}), SDRNT = "00"			V_{LED}-1.0	V_{LED}-0.7	V
T_{SD}	Thermal shutdown	(Note 8)			165		°C
T_{SD_HYS}	Thermal shutdown hysteresis	(Note 8)			25		°C

7.4 LUMIBUS INTERFACE CHARACTERISTICS

The following specifications apply for T_J= -40°C ~ +125°C, V_S= 12V, V_{LED}= 5V, the detail refers to each condition description. Typical values are at T_J= 25°C, V_S= 12V, V_{LED}= 5V, unless otherwise noted (Note 5).

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
CAN Interface						
V_{O_DOM}	Dominant output voltage	V_{CANH}, R_{LOAD}= 50Ω to 65Ω	2.75	3.5	4.5	V
		V_{CANL}, R_{LOAD}= 50Ω to 65Ω	0.5	1.5	2.25	V
V_{O_RES}	Recessive output voltage	V_{CANH} and V_{CANL}, R_{LOAD}= 50Ω to 65Ω	0.45× V50	0.5× V50	0.55× V50	V
V_{O_DIF}	Differential output voltage (V_{CANH}-V_{CANL})	Dominant, R_{LOAD}= 50Ω to 65Ω	1.5	2	3	V
		Dominant, R_{LOAD}= 45Ω to 70Ω	1.4	2	3.3	
		Dominant, R_{LOAD}= 2240Ω	1.5		5	
		Recessive, R_{LOAD}= 60Ω	-120	0	120	mV
V_{SYM}	Driver symmetry (V_{CANH}+V_{CANL})/V50	R_{LOAD}= 60Ω, Operation Frequency 2MHz	0.9	1.0	1.1	V/V
V_{SYM_DC}	DC output voltage symmetry (V50-V_{CANH}-V_{CANL})	Dominant or recessive, R_{LOAD}= 60Ω	-400		+400	mV
V_{CM}	Common mode voltage range		-12		12	V
V_{REC_IN}	Recessive state differential input voltage	(V_{CANH}-V_{CANL}), -8V≤V_{CM}≤12V	-3		0.5	V
V_{TH_DIF}	Differential receiver threshold voltage	(V_{CANH}-V_{CANL}), -8V≤V_{CM}≤12V	0.5	0.7	0.9	V
V_{HYS_DIF}	Differential receiver threshold voltage hysteresis	(V_{CANH}-V_{CANL}), -8V≤V_{CM}≤12V		200		mV
V_{DOM_IN}	Dominate state differential input voltage	(V_{CANH}-V_{CANL}), -8V≤V_{CM}≤12V	0.9		8	V
I_{O_DOM}	Dominant output current	CANH pin, -3V≤V_{CANH}≤18V	-115	-60		mA
		CANL pin, -3V≤V_{CANL}≤18V		60	115	mA
I_{O_REC}	Recessive output current	-8V≤V_{CANH}≤12V, -8V≤V_{CANL}≤12V	-5		5	mA
R_{IN_H}	Single ended input resistance (CANH pin)	-2V≤V_{CANH}≤7V		45		kΩ
R_{IN_L}	Single ended input resistance (CANL pin)	-2V≤V_{CANL}≤7V		45		kΩ
R_{I_DIF}	Differential input resistance	-2V≤V_{CANH}≤7V, -2V≤V_{CANL}≤7V		75		kΩ
M_{RIN}	Input resistance matching 2×(R_{IN_H}-R_{IN_L})/(R_{IN_H}+R_{IN_L})	V_{CANH}= V_{CANL}= 5V	-3		3	%

7.5 LUMIBUS INTERFACE CHARACTERISTICS (CONTINUED)

The following specifications apply for T_J= -40°C ~ +125°C, V_S= 12V, V_{LED}= 5V, the detail refers to each condition description. Typical values are at T_J= 25°C, V_S= 12V, V_{LED}= 5V, unless otherwise noted (Note 5).

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
UART Interface						
V_{IH_RX}	RX logic “1” input voltage	V_S=5V~28V	2.4			V
V_{IL_RX}	RX logic “0” input voltage	V_S=5V~28V			0.7	V
V_{OL_TX}	TX low level output voltage	I_{SINK}=5mA	0		0.3	V
V_{OH_TX}	TX high level output voltage	I_{SOURCE}=-5mA	V_{50}-0.3V		V_{50}	V
I_{LKG_UART}	TX, RX leakage current	V_S=12V, TX high-z state	-1		1	μA
C_{IN_RX}	TX, RX input capacitance	TX high-z state (Note 8)		5	10	pF
$t_{R\text{-}DO1}$	Rise time of digital output	C_{LOAD}= 20pF, TX pin (Note 8)		10		ns
$t_{F\text{-}DO1}$	Fall time of digital output	C_{LOAD}= 20pF, TX pin (Note 8)		10		ns
$I_{OS\text{-}SRC}$	Output short source current	PIN= 0V, TX pin		40		mA
$I_{OS\text{-}SNK}$	Output short sink current	PIN= 5V, TX pin		35		mA

Note 5: Limits are 100% production tested at 25ºC. Limits over the operating temperature range verified through either bench and/or tester testing and correlation using statistical methods.

Note 6 I_{OUT} mismatch (channel to channel) $\triangle I_{MAT}$ is calculated:

$$\Delta I_{MAT}=\pm\left(\frac{I_{OUTn(n=1\sim18)}}{\left(\frac{I_{OUT1}+I_{OUT2}\cdots+I_{OUT18}}{18}\right)}-1\right)\times100\%$$

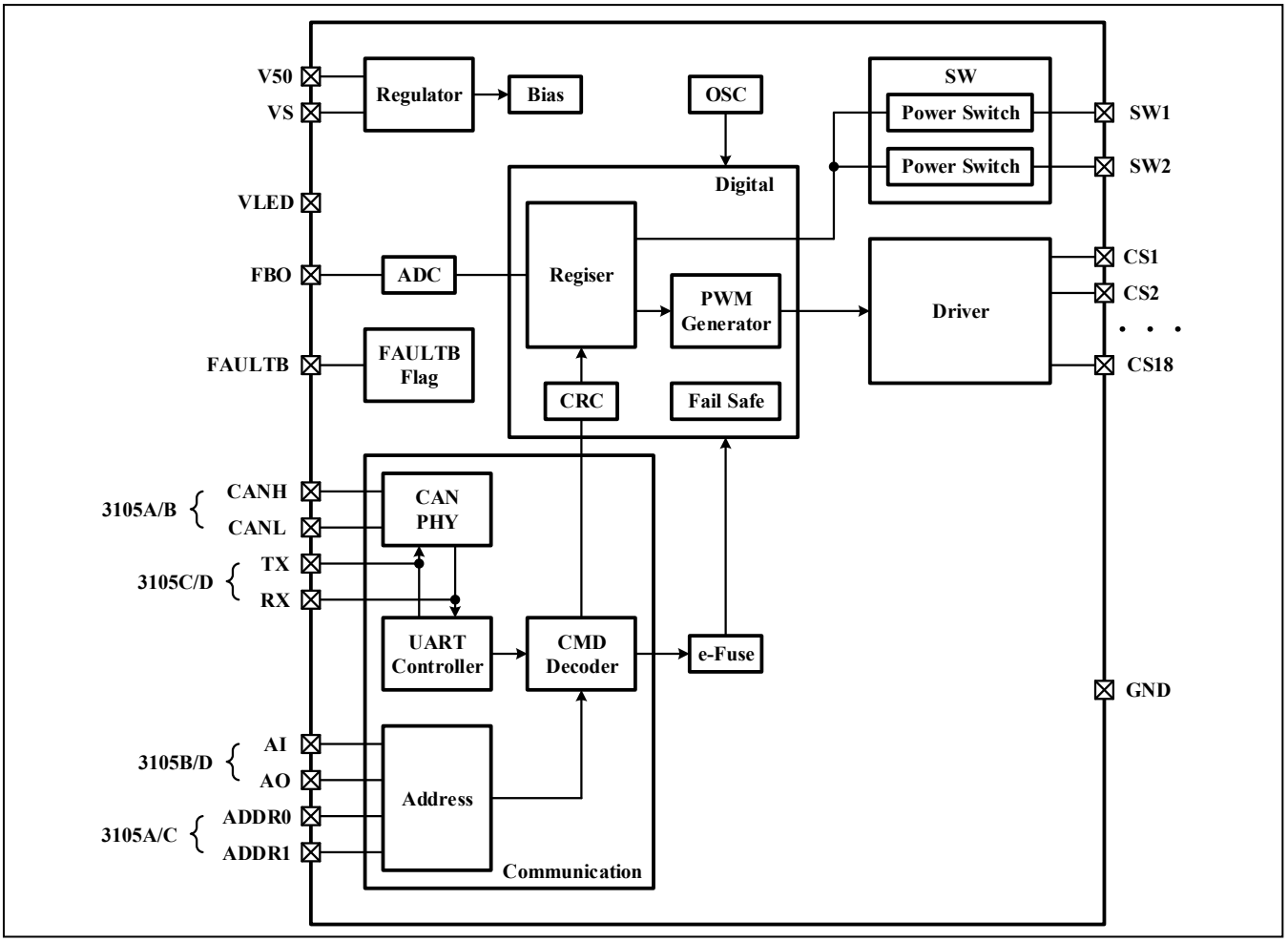
Note 7: I_{OUT} accuracy (device to device) $\triangle I_{ACC}$ is calculated:

$$\Delta I_{ACC}=\left(\frac{\left(\frac{I_{OUT1}+I_{OUT2}\cdots+I_{OUT18}}{18}-I_{OUT(IDEAL)}\right)}{I_{OUT(IDEAL)}}\right)\times100\%$$

Where $I_{OUT(IDEAL)}$= 60mA.

Note 8: Guaranteed by design.

8 FUNCTIONAL BLOCK DIAGRAM



9 APPLICATION INFORMATION

9.1 OVERVIEW

IS32FL3105 is a 2 × 18-channel RGB automotive LED driver. It communicates via Lumissil's unique LumiBus protocol and can individually control each LED. Each channel acts as a constant current absorb, capable of up to 60mA, supporting DC regulation and PWM dimming. Each channel's output current and PWM duty cycle can be individually configured via the LumiBus protocol.

To enhance system reliability, IS32FL3105 is equipped with various fault protection functions. These include LED open circuit, LED short circuit, thermal shutdown protection, thermal roll off, SW overcurrent protection, CRC error, and watchdog timeout (fail safe mode) conditions, enabling robust operation. Additionally, IS32FL3105 complies with ASIL-B functionality and integrates PWM loopback, SW loopback, IOUT monitor, and VF monitor to ensure normal chip operation. Faults are detected and reported via the dedicated reporting pin FAULT. Each fault in the register has a dedicated flag, which can be read back by an external host MCU through an interface.

To optimize EMI performance, IS32FL3105 features a spread spectrum function on the internal PWM base clock. This function spreads the total electromagnetic emission energy over a wider range, significantly reducing the peak EMI energy. Moreover, during PWM dimming, the output current source ON/OFF conversion has conversion rate control and a 180-degree phase delay to mitigate EMI and power inrush current.

Based on communication interfaces, IS32FL3105 is categorized into two groups. IS32FL3105A and IS32FL3105B support CAN physical interfaces, while IS32FL3105C and IS32FL3105D support UART interfaces. IS32FL3105A and IS32FL3105C support up to 25 slave devices, and device addresses can be configured through two address pins. IS32FL3105B and IS32FL3105D support up to 254 slave devices, and device addresses can be configured through two address pins in combination with SNPD functionality. Through LumiBus, all output channels can be controlled, and fault information can be sent back to the host MCU.

IS32FL3105A and IS32FL3105B have a standard CAN physical interface, which can be directly connected to the CAN bus for remote communication with the host MCU located outside the lamp module, enabling a more streamlined circuit design. The UART interface of IS32FL3105C and IS32FL3105D can be combined with external standard CAN transceivers to achieve remote communication with the host MCU outside the lamp module. Based on the CAN physical layer, it delivers excellent EMC and EMI performance. The embedded CRC correction of UART data streams ensures reliable communication in automotive environments. Most MCUs on the market readily support UART interfaces.

9.2 POWER SUPPLY

9.2.1 INTERNAL 5.0V LINEAR REGULATOR (V50)

The IS32FL3105 device integrates an internal linear regulator (LDO) with 5.0V (Typ.) and IDD_MAX current capability to provide power supply to the internal analog and digital circuits. During operation, the internal circuitry can be subject to transient currents from this linear regulator. Therefore, 1μF + 0.1μF low ESR, X7R type ceramic capacitor is necessary from V50 pin to GND, it must be placed as close to the V50 pin as possible. This linear regulator also has the UVLO feature. The device is disabled when the V50 voltage drops below V50_UV and resumes normal operation when the V50 voltage rises above (V50_UV). Entering UVLO will reset all registers to their default value.

9.3 SCANING TIMING

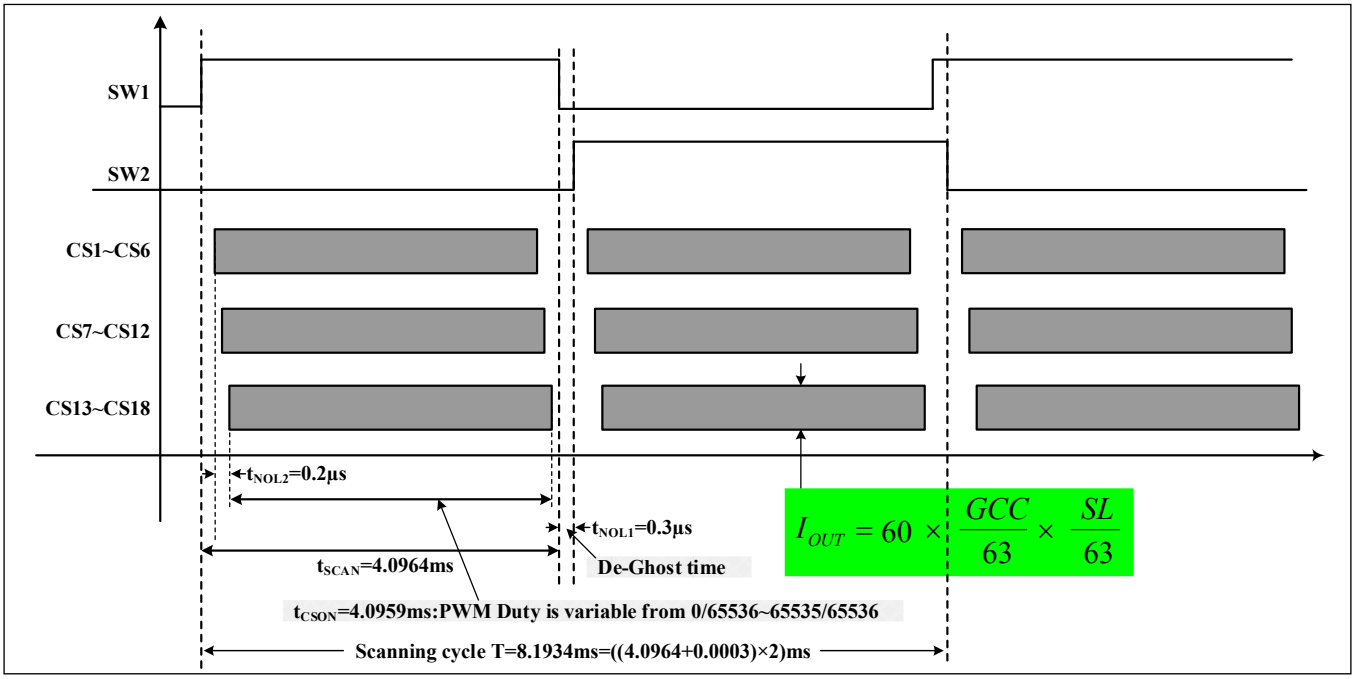


Figure 7 Scanning Timing (16-bit PWM Mode OSC=16MHz)

As shown in Figure 7, the SW1 and SW2 is turned on by serial, LED is driven 2 by 2 within the SWx (x= 1~2) on time (SWx, x= 1~2 is source and it is high when LED on) and in 16-bit PWM mode (OSC=16MHz), including the non-overlap blanking time during scan, the duty cycle of SWx (active high, x= 1~2) is:

$$Duty = \frac{4.095ms}{(4.096ms+0.3\mu s)} \times \frac{1}{2} = \frac{1}{2.147} \qquad (2)$$

Where 4.096ms is t_{SCAN}, the period of SWx scanning, 4.096ms is t_{CSON}, the CS-ON time during scan, 0.3μs is t_{NOL1}, the non-overlap time, the calculation is applicable to 16-bit PWM mode and OSC=16MHz.

9.4 PWM DIMMING

After setting GCC and SL, the brightness of each LEDs (LED average current (I_{LED})) can be modulated with 65536 steps by PWM Register.

The value of the PWM Registers decides the average current of each LED noted I_{LED}, I_{LED} is computed as Formula:

$$I_{LED} = \frac{PWM}{N} \times I_{OUT(PEAK)} \times Duty \qquad (1)$$

N=65536:$PWM = \sum_{n=0}^{15} D[n] \cdot 2^n$

For 16-bit PWM mode and OSC=16MHz, Duty is computed by the Formula:

$$Duty = \frac{4.0959ms}{(4.0964ms+0.3\mu s)} \times \frac{1}{2} = \frac{1}{2.0004} \qquad (2)$$

$I_{OUT(PEAK)}$ is the current output of CSy (y=1~18), is computed by the Formula:

$$I_{OUT(PEAK)} = 60 \times \frac{GCC}{63} \times \frac{SL}{63} \qquad (3)$$

$$GCC = \sum_{n=0}^{5} D[n] \cdot 2^n$$

$$SL = \sum_{n=0}^{5} D[n] \cdot 2^n$$

Where D[n] stands for the individual bit value, 1 or 0, in location n.

For example, if in 16-bit PWM mode, PWM= 32768, and GCC= 63, SL= 63, then

$$I_{OUT(PEAK)} = 60 \times \frac{63}{63} \times \frac{63}{63} = 60mA$$

$$I_{LED} = I_{OUT(PEAK)} \times \frac{1}{2.0004} \times \frac{PWM}{65536} = 14.997mA$$

9.4.1 PWM SPREAD SPECTRUM

The IS32FL3105 incorporates a spread spectrum feature on its PWM base clock, a key mechanism for optimizing EMI (Electromagnetic Interference) performance. This spread spectrum function effectively disperses the total electromagnetic emission energy across a broader frequency range. As a result, it effectively reduces the peak energy of EMI, which is crucial for maintaining electromagnetic compatibility.

With the activation of the spread spectrum feature, the device can pass EMI tests using smaller - sized and lower - cost filter circuits. This not only simplifies the circuit design but also helps in reducing overall system costs.

The spread spectrum functionality can be enabled or disabled by configuring the OSC Frequency Setting register (address 72h in PAGE0). This register provides a convenient and precise way to control the spread spectrum operation, allowing designers to balance EMI performance and other system requirements according to their specific application scenarios.

9.4.2 PWM 180-DEGREE PHASE DELAY

IS32FL3105 supports 180 - degree PWM phase delay. Odd channels (CS1, 3, 5... CS17) and even channels (CS2, 4, 6... CS18) can be enabled or disabled by configuring the CHO and CHE bits in the Power Noise Reduction register (71h in PAGE0). This controls the 180-degree phase delay; even channels are enabled by default.

This function effectively reduces overall power system ripple. The current fluctuations of the two channel groups cancel each other out, significantly decreasing the power network's instantaneous current demand and stress on the input capacitor.

9.5 FAULT PROTECTION

9.5.1 FAULT REPORTING

To enhance system reliability, the IS32FL3105 detects multiple faults, including LED open/short circuits, SW short - circuit overcurrent, overtemperature, CRC errors, and watchdog timeout (fail - safe mode).

Faults are reported via the open - drain FAULTB pin. When a fault occurs, the relevant bits in Fault Flag registers 1 and 2 (01h, 02h) in PAGE1 are set to "1", and the FAULTB pin goes low. To enable proper monitoring by the host, connect a 10kΩ pull - up resistor (R_{FPU}) between the FAULTB pin and the host MCU's power supply.

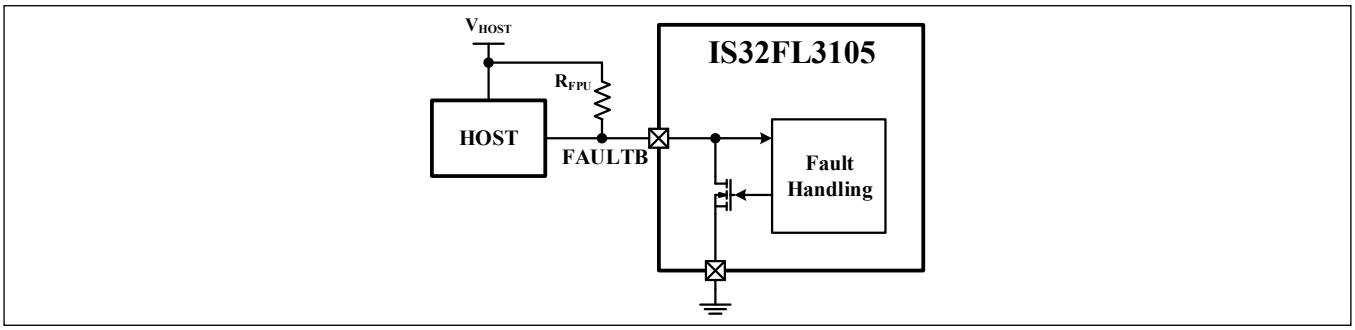


Figure 8 FAULTB Pin Application

9.5.2 LED OPEN PROTECTION

To enable LED open - circuit detection, set the OSD_DIS bit in the operation configuration register (70h of PAGE0) to "1". If an LED is open, the voltage of the corresponding CSy pin will drop nearly to zero. When the CSy pin voltage V_{CSy} remains below the LED open - circuit detection voltage V_{OD} for a certain period, the LED open - circuit protection will be triggered. The corresponding fault flag bit in the open result register (03h - 07h of PAGE1) and the OPENF bit in fault flag register 1 (01h of PAGE1) will be set to "1", and the FAULT pin will go low to indicate the fault.

Before enabling open-circuit detection, configure the following three settings:

1 0x0F≤GCC≤0x20

2 SWx Pull Down Voltage = floating,

CSy Pull Up Voltage = floating,

3 PWM >25% (OSC=16MHz)

Regardless of the fault - protection mode, once the open - circuit condition is resolved (i.e., VCSy rises above the LED string open - circuit detection voltage V_{OD}), the device will resume normal operation. The corresponding fault flag in the open result register will reset to "0". However, the OPENF bit in fault flag register 1 (01h of PAGE1) is latched. After the open state is removed, it won't reset to "0" automatically. The host MCU must write "0" to it, and the FAULTB pin will return to high impedance.

During PWM dimming, LED string open - circuit detection is only active during the PWM ON phase. If the PWM on - time is shorter than the detection time, the device won't report any LED open - circuit faults.

9.5.3 LED SHORT PROTECTION

To enable LED short - circuit detection, set the OSD_DIS bit in the operation configuration register (70h of PAGE0) to "1". If an LED is short - circuit, the voltage of the corresponding CSy pin will rise close to VLED. When the CSy pin voltage V_{CSy} rises above the LED short - circuit detection V_{SD} for a certain period, the LED short - circuit protection will be triggered. The corresponding fault flag bit in the short result register (08h - 0Ch of PAGE1) and the SHORTF bit in fault flag register 1 (01h of PAGE1) will be set to "1", and the FAULTB pin will go low to indicate the fault.

Before enabling short - circuit detection, you need to make the following three configurations:

1 0x0F≤GCC≤0x20

2 SWx Pull Down Voltage = floating,

CSy Pull Up Voltage = floating,

3 PWM >25% (OSC=16MHz)

Regardless of the fault - protection mode, once the short - circuit condition is resolved, i.e., VCSy falls below the LED string short - circuit detection voltage V_{SD}, the device will resume normal operation. The corresponding fault flag in the short result register will reset to "0". However, the SHORTF bit in fault flag register 1 (01h of PAGE1) is latched. After the short - circuit state is removed, it cannot be reset to "0" automatically; the host MCU must write "0" back to it, and the FAULTB pin will return to high impedance.

During PWM dimming, LED string short - circuit detection is only active during the PWM ON phase. If the PWM on - time is shorter than the detection time, the device will not report any LED short - circuit faults.

9.5.4 SWx (x = 1,2) SHORT to VLED DETECT

IS32FL3105 continuously monitors the voltage at the SWx pins. When the SWx voltage approaches the VLED level (indicating a potential short circuit between SWx and VLED), the IC sets the SWSHF flag to "1" in the fault status register to alert the system of the fault condition.

However, the SWSHF bit in fault flag register 1 (01h of PAGE1) is latched. This means that after the SWx short-to-VLED state is resolved, the bit cannot reset to "0" automatically. Instead, the host MCU must write "0" back to this bit, and the FAULTB pin will then return to high impedance.

9.5.5 SWx (x = 1,2) OVER-CURRENT PROTECTION

If excessive current is drawn from the SWx pins (exceeding the threshold configured in PAGE0 Register 77h), the IC triggers overcurrent protection to prevent damage (e.g., short to GND). The affected SWx output is immediately disabled, and Fault Register 1 sets the SWOCF fault flag to "1" to alert the system. When the SWOC_RE bit in PAGE0 Register 82h (fault flag report control) is set to "1", the FAULTB pin goes low to indicate the fault.

To restore normal operation:

1 Ensure stable hardware conditions on the SWx pin.

2 Clear the fault by setting the RECOVER bit in PAGE0 Register 77h to "1", allowing SWx to resume operation.

However, the SWOCF bit in PAGE1 Register 01h (Fault Flag Register 1) is latched. This means it cannot auto-reset to "0" when SWx resumes normal operation; the host MCU must manually write "0" to clear it, and the FAULTB pin will return to high impedance.

9.5.6 VLED UNDER-VOLTAGE DETECT

IS32FL3105 continuously monitors VLED voltage. If VLED drops below the undervoltage protection threshold, the IC sets the UVLEDF flag to "1" in the fault status register to alert the host of a VLED undervoltage condition. When

the UVLED_RE bit in the fault flag report control register (PAGE0, 82h) is set to "1", the FAULTB pin goes low to signal the fault.

However, the UVLEDF bit in Fault Flag Register 1 (PAGE1, 01h) is latched. This means it cannot auto-reset to "0" when VLED recovers from undervoltage; the host MCU must manually write "0" to clear the bit, and the FAULTB pin will return to high impedance.

9.5.7 THERMAL SHUTDOWN PROTECTION

If the junction temperature exceeds the Thermal Shutdown (T_{SD}) threshold (Typ. 165˚C), all output channels will turn off, and the TSDF bit in Fault Flag Register 1 (01h of PAGE1) will be set to “1”. If the TSDF_RE bit in the Fault Flag Report Control Register (82h of PAGE0) is set to “1”, the FAULTB pin will go low to indicate the fault.

At this point, the device will start to cool down. Any attempt to switch the channels back to their original state before the device has cooled to below (T_{SD} - T_{SD_HYS}) (Typ. 140˚C) will be blocked, and the device cannot be restarted.

However, the TSDF bit in Fault Flag Register 1 (01h of PAGE1) is latched. This means that when the device cools down, it won't automatically reset to “0”. Instead, the host MCU must clear it by writing “0” back to the register, and then the FAULTB pin will return to a high - impedance state.

9.5.8 OUTPUT CURRENT MONITOR

The IS32FL3105 integrates an internal output current monitoring function. This allows the chip to detect and provide feedback on the output current status of each channel.

This function can precisely monitor the current of each channel. The host can select and detect the corresponding channel by configuring Register 7Fh of PAGE0. The output current monitoring results of the corresponding channel are reported in the Output Current Monitor Result Registers (17h - 1Bh).

If any channel malfunctions, the IMONF bit in Fault Flag Register 1 (02h of PAGE1) will be set to “1”. If the IMONF_RE bit in the Fault Flag Report Control Register (83h of PAGE0) is set to “1”, the FAULTB pin will go low to signal the fault.

However, the IMONF bit in Fault Flag Register 1 (02h of PAGE1) is latched. This means that even when the output current monitoring results of all channels return to normal, it won't reset to “0” automatically. The host MCU must write “0” back to the register to clear it, and then the FAULTB pin will return to high impedance.

9.5.9 LED VF MONITOR

The IS32FL3105 is internally integrated with an LED VF voltage monitoring function. This function enables the chip to detect and provide feedback on the voltage status across the LED load. It helps the host monitor the LED's working status and identify abnormal LED VF, such as voltage drop fluctuations due to LED aging or temperature changes.

The host can configure the LED VF monitoring threshold range for the corresponding R, G, and B channels by switching Registers 7Bh, 7Ch, and 7Dh of PAGE0. The VF monitoring results of the corresponding LED are reported in the VF Voltage Monitor Result Registers (12h - 16h).

If any channel malfunctions, the VFWDF bit in Fault Flag Register 1 (02h of PAGE1) will be set to “1”. If the VFWDF_RE bit in the Fault Flag Report Control Register (83h of PAGE0) is set to “1”, the FAULTB pin will go low to indicate the fault.

However, the VFWDF bit in Fault Flag Register 1 (02h of PAGE1) is latched. This means that when all LED VFs are within the normal voltage threshold range, it won't automatically reset to “0”. The host MCU must write “0” back to the register to clear it, and then the FAULTB pin will return to high impedance.

9.5.10 PWM DUTY VERIFICATION (CS LOOP BACK)

The IS32FL3105 integrates a PWM Duty detection function called CS Loop Back. This function allows the chip to detect the duty cycle of the output PWM signal, provide feedback on the actual PWM duty at the end - output, and compare it with the PWM of the input command. The tolerance for this comparison can be configured via Register 80h of PAGE0.

This function helps the host monitor whether the input PWM command is accurately synchronized with the output PWM signal. It can identify signal abnormalities such as sudden duty - cycle changes and frequency offsets, thereby preventing brightness fluctuations or LED damage caused by PWM signal distortion. The host can select the corresponding detection channel by configuring and switching Register 81h of PAGE0.

If an exception occurs, the PWM Duty detection result of the corresponding channel will be reported in the CS Loop Back Test Result Registers (0Dh - 11h). When any channel fails, the CSLTF bit in Fault Flag Register 1 (02h of PAGE1) will be set to “1”. If the CSLTF_RE bit in the Fault Flag Report Control Register (83h of PAGE0) is set to “1”, the FAULTB pin will go low to indicate the fault.

However, the CSLTF bit in Fault Flag Register 1 (02h of PAGE1) is latched. This means that when the output PWM of all channels returns to normal, it won't automatically reset to “0”. The host MCU must write “0” back to the register to clear it, and then the FAULTB pin will return to high impedance.

9.5.11 SCAN DUTY VERIFICATION (SW LOOP BACK)

The IS32FL3105 integrates an SW Loop Back function for SCAN Duty detection. This feature monitors the matching degree between each scan's actual duty cycle and the expected value during dynamic multi-channel LED load scanning. The allowable deviation for this matching degree can be configured via Register 76h of PAGE0.

This function helps the host accurately identify duty cycle distortion caused by scanning timing deviations, signal delays, or abnormal loads. When the duty cycle error exceeds the threshold, the chip reports the corresponding SCAN Duty detection result in the SW Loop Back Test Result Register (11h). If any scan fails, the SWLTF bit in Fault Flag Register 1 (02h of PAGE1) is set to “1”. When the SWLTF_RE bit in the Fault Flag Report Control Register (83h of PAGE0) is set to “1”, the FAULTB pin goes low to signal the fault.

However, the SWLTF bit in Fault Flag Register 1 (02h of PAGE1) is latched. This means it cannot auto-reset to “0” when all scanned output duty cycles return to normal; the host MCU must manually write “0” to clear the bit, and the FAULTB pin will revert to high impedance.

9.5.12 INTERNAL PWM CLOCK MONITOR

The IS32FL3105 is integrated with an internal PWM clock monitoring function. This function enables real - time monitoring of the operating clock frequency and stability of its built - in PWM generator and compares it with a preset benchmark.

When clock abnormalities, such as frequency deviation or excessive jitter, are detected, the chip sets the INCKF bit in Fault Flag Register 1 (02h of PAGE1) to "1". If the INCKF_RE bit in the Fault Flag Report Control Register (83h of PAGE0) is set to "1", the FAULTB pin will go low to indicate the fault condition.

However, the INCKF bit in Fault Flag Register 1 (02h of PAGE1) is latched. This implies that even when the internal clock monitoring result returns to normal, it cannot automatically reset to "0". Instead, the host MCU must write "0" back to the register to clear it, and then the fault pin will return to a high - impedance state.

9.5.13 CRC (FRAME CHECKSUM) ERROR

The IS32FL3105 integrates internal cyclic redundancy check (CRC) and frame header format error-reporting functions for communication data frames, ensuring reliability through a dual-check mechanism during external data reception. The CRC function verifies packet integrity by using a built-in algorithm to perform cyclic redundancy calculations on each received data frame and compare results with the frame’s two-byte checksum, mitigating errors caused by transmission interference, signal distortion, or data tampering. The chip also checks the frame header format against LumiBus protocol standards and triggers an error when a mismatch is detected. Upon identifying a CRC error or invalid header, the chip sets the CRCF bit in Fault Flag Register 1 (02h, PAGE1) to "1" and pulls the FAULTB pin low if the CRCF_RE bit in Register 83h (PAGE0) is enabled. For CRC errors, the chip increments the CRC Error Count register (1Dh, PAGE1) by 1 per occurrence, up to a limit of 255; the counter does not clear automatically on overflow and requires manual reset by writing "0" to the register.

However, the CRCF bit (PAGE1 02h) in fault flag register 1 is latched, which means that when the CRC check result is normal and the frame header format is normal, it cannot be automatically reset to "0” but must be written back to "0" by the host MCU for clearing, and the fault pin will be restored to high impedance.

9.5.14 COMMUNICATION WATCH DOG

The IS32FL3105 integrates a communication watchdog timeout detection function (communication watchdog), which uses a built-in timer (configured via PAGE0 Register 8Ah) to monitor real-time communication intervals and ensure stable system operation. The watchdog counter is automatically cleared when the chip successfully receives a valid data frame. If no new communication commands are detected within the preset time threshold, the watchdog counter overflows, triggering a timeout protection mechanism. If the host has pre-configured PWM fail-safe mode, the chip immediately switches to a fail-safe state, driving the LED with customer-preset PWM parameters for visual alarm while maintaining safe current output. Concurrently, the IS32FL3105 sets the WDTF1 bit in Fault Flag Register 1 (02h, PAGE1) to "1" and pulls the FAULTB pin low to report the fault if the WDTF1_RE bit in PAGE0 Register 83h is enabled. This function employs a dual protection mechanism (timing monitoring and security mode switching) to

mitigate system crashes, communication interruptions, and other anomalies, ensuring predictable security policies are enforced in extreme scenarios.

However, the WDTF1 bit (PAGE1 02h) in fault flag register 1 is latched, which means that when communication is normal, it cannot automatically reset to "0" but must be written back to "0" by the host MCU for clearing, and the fault pin will be restored to high impedance.

9.5.15 WATCH DOG TIMER2

The IS32FL3105 features an internally integrated window watchdog timeout detection function (Watch Dog Timer 2). This advanced monitoring mechanism mandates that the host write "1" to a specific bit in a designated register (the 8Bh register of PAGE0) within a predefined time window (ranging from the minimum threshold T_{min} to the maximum threshold T_{max}) for the dog - feeding operation. Otherwise, it will trigger a timeout reset or an alarm. If the dog-feeding action isn't carried out within the preset time threshold, Watch Dog Timer 2 will overflow, activating the protection mechanism.

When the host has pre - configured the PWM fail - safe mode, the chip will promptly switch to a fail - safe state. It will drive the LED based on the customer's preset PWM parameters for a visual alarm and maintain a safe current output. Simultaneously, the IS32FL3105 will set the WDTF2 bit in fault flag register 1 (02h of PAGE1) to "1". If the WDTF2_RE bit in the fault flag report control register (83h of PAGE0) is set to "1", the FAULTB pin will go low to signal the fault condition.

This function offers two key advantages: Firstly, the strict time-window constraints preclude premature or delayed dog-feeding operations, ensuring the system operates at a set pace and preventing software from hanging or running out of control. Secondly, the dual-threshold design is more precise than traditional watchdogs. It can detect system stagnation (failing to feed the dog beyond T_{max}) and identify abnormal acceleration (feeding the dog before reaching T_{min}), thereby substantially enhancing system reliability.

However, the WDTF2 bit (02h of PAGE1) in fault flag register 1 is latched, which means that when communication is normal, it cannot be automatically reset to "0" but must be written back to "0" by the host MCU for clearing, and the fault pin will be restored to high impedance.

9.5.16 THERMAL ROLL-OFF PROTECTION

The device incorporates thermal shutdown protection to prevent overheating and includes a programmable thermal roll-off function to mitigate LED flickering caused by rapid thermal changes, reducing power consumption at high junction temperatures. If the device's junction temperature remains below the default hot roll-off temperature threshold of 140°C (configurable via the TS[1:0] bits in PAGE0 Register 71h, with options including 140°C, 120°C, 100°C, and 90°C), the output current remains at the set value IOUTx. When the junction temperature exceeds the threshold, all channels' output current begins to decrease linearly with temperature until thermal shutdown, with the pre-shutdown current percentage programmable via the TROF[1:0] bits in the Thermal Roll-off register (PAGE0 Register 71h) at four levels: 100%, 75%, 55%, and 30%. Once the junction temperature drops below the configured threshold (140°C default), the output current linearly reverts to IOUTx.

9.6 CHARACTERISTIC FUNCTION

9.6.1 DE-GHOST FUNCTION

The term "ghost" refers to an LED that remains dimly lit when it should be off while another LED is illuminated, a phenomenon typically occurring in LED multiplexing scenarios. In matrix architectures, parasitic capacitance in constant-current outputs or PCB traces can supply enough current to faintly light the LED, creating this ghosting effect. To address this, the IS32FL3105 integrates pull-down voltage settings for each SWx (x=1,2) and pull-up voltage settings for each CSy (y=1~18). By selecting appropriate values in the SW De-ghost register (PAGE0 Register 73h) for SWx pull-down voltages and the CS De-ghost register (PAGE0 Register 74h) for CSy pull-ups, LED ghosting in specific matrix layouts can be eliminated. The optimal voltage settings generally depend on the number of series-connected LEDs at each matrix point, with proper selection typically sufficient to resolve the issue.

9.6.2 TEMPERATURE COMPENSATION

The IS32FL3105 features an LED temperature compensation function with three configurable compensation curves for R, G, and B LEDs. Once users configure the temperature threshold, room temperature data, and compensation parameters for each segment and enable the function, the chip can achieve fully automatic compensation through a dual-mode temperature detection mechanism. In the indirect detection mode, it monitors the changes in the forward voltage drop (VF) of the LED via an internal high - precision ADC to dynamically calculate and compensate for the LED's junction temperature. In the direct detection mode, it uses on-chip integrated temperature sensors to measure the real-time environmental temperature for compensation. These two independent modes intelligently

match the preset three-stage compensation curve, accurately offsetting the brightness and color temperature deviation caused by temperature.

9.6.3 COLOR CROSSFADE

The IS32FL3105 is equipped with an RGB color gradient function (Color Crossfading) that enables flexible control of color transitions. Users can first set the starting color, activate the gradient function, and then specify the target color. Subsequently, the device will automatically perform a smooth color gradient from the starting color to the target one. This function offers two operating modes. In the host external command gradient mode, the host sends gradient parameters in real-time via a communication interface for precise control. In the internal automatic gradient mode, the chips' built-in gradient algorithm independently accomplishes color transitions without host intervention. The gradient order is configured using the STP_EN bit of the Color Crossfade Steps and PWM Count Register (89h of PAGE0). Both modes support adjustable gradient speeds, which notably lessens the computational burden on the host. They are highly suitable for scenarios demanding dynamic color switching, such as smart lighting and RGB decoration, delivering a smooth and natural visual experience.

9.6.4 DCFB FUNTION

IS32FL3105 supports DC feedback output function (FBO), which is used to dynamically adjust the DC-DC BUCK output voltage VOUT to optimize the system power supply. It controls the current (output or absorption current) of the external DCDC BUCK circuit FB pin through the FBO pin, dynamically changes the voltage of the feedback network, and precisely adjusts the DCDC BUCK output voltage to achieve the optimal operating point (DCFB, DC Feedback). This function works in conjunction with the host to obtain the minimum voltage in all CSy channels at regular intervals. And control the output voltage of DCDC BUCK by adjusting the output of FBO pin or absorbing current through the host, so that it is slightly higher than the minimum voltage difference required by the load (usually maintained within the range of 0.5V-0.8V above the normal operating voltage of the channel). This dynamic voltage regulation (DVS) technology achieves voltage regulation through current mode control of FBO pins, which can reduce the power consumption of driving chips compared to fixed voltage schemes. It is particularly suitable for application scenarios with large input voltage fluctuations or LED string voltage changes, such as automotive lighting and boost/buck LED drivers, because it can optimize system energy efficiency and effectively suppress the rise in chip temperature.

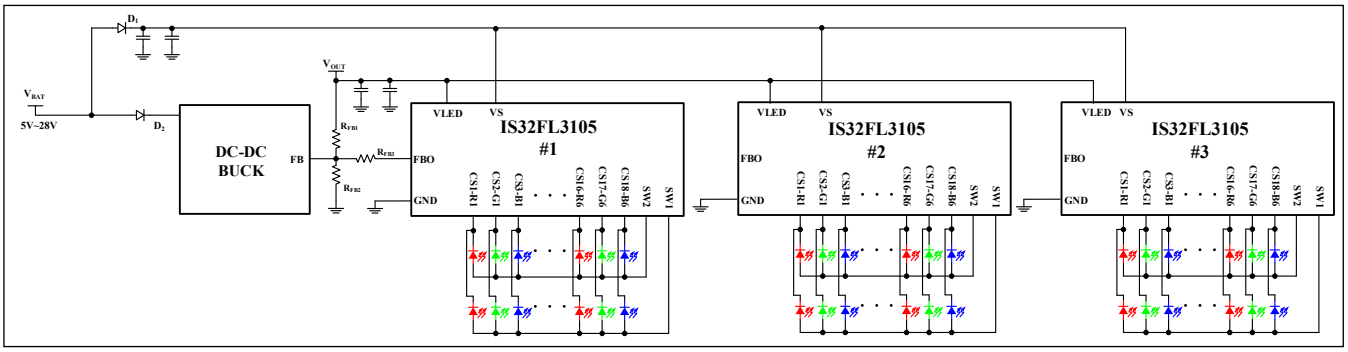


Figure 9 DCFB Application

9.6.5 ADC FUNCTION (ANALOG-TO-DIGITAL CONVERTER)

The IS32FL3105, a constant - current driver chip, supports an integrated ADC module and an on-die temperature sensor. It can collect key voltages such as VSW, VLED, and LED VF to enable precise real - time monitoring and closed - loop control, thereby enhancing the system's reliability and energy-efficiency performance.

9.7 POWER SAVING MODE

Power-saving mode can be used as a method to reduce power consumption. All register data will be retained when the device enters power-saving mode.

The IS32FL3105 can be put into power-saving mode by configuring the PSM Bit of the register at address 70h to "1" via broadcast command. When the chip is in power-saving mode, all current sinks will be turned off, and the LED matrix will be blanked accordingly.

9.8 LAYOUT

The IS32FL3105 has relatively high-power consumption, so a well - designed PCB layout is crucial for enhancing the chips' reliability. When laying out the PCB, the following factors should be considered.

During the PCB layout pattern design, the first consideration should be the supply lines and GND connections, especially for high - current traces. Additionally, the supply lines and GND for digital and analog blocks should be separated to prevent digital noise from interfering with the analog block.

For the VLED pin, at least one combination of a 10μF and a 0.1μF capacitor is required; for the VS pin and the V50 pin, a 1μF and a 0.1μF capacitor combination is needed. These capacitors should be placed close to the corresponding chip pins, and their ground nets should be well - connected to the GND plane.

The VLED, VS, and V50 capacitors must be positioned close to the chip pins, and their ground sides should be connected to the chip's GND. The thermal pad of the chip should be connected to the ground pins, and the PCB should also have a thermal pad. Typically, this pad should have 16 or 25 vias connecting to the ground area on the other side of the PCB to facilitate heat dissipation. For the size of the thermal pad, refer to the land pattern of each package.

The maximum current of the CSy pins is 60mA, while that of the SWx pins is larger. Therefore, the traces for SWx should be wider than those for CSy.

9.9 LUMIBUS INTERFACE

9.9.1 UART DATA FORMAT

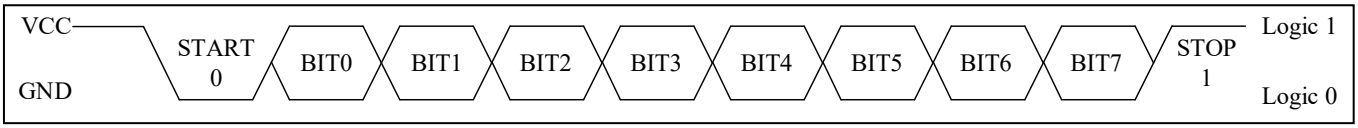


Figure 10 UART Data Byte Format

9.9.2 COMMAND FRAME TYPES

9.9.2.1 BUS Reset and SYNC Command Frame

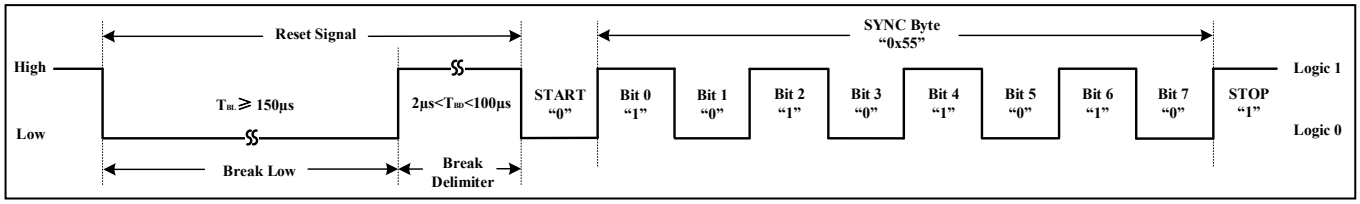


Figure 11 BUS Reset and SYNC Command

Break Low time (T_{BL}): min time 150μs, max timeout 10ms (depend on external CAN PHY)

Break Delimiter time (T_{BD}): Greater than 2μs, max timeout 100μs

SYNC 0x55: The first SYNC bit length is decided by lowest baud-rate (≥100Kbps)

Before communication, the host needs to first send a bus reset comment to reset all slaves' internal state machine.

9.9.2.2 Protocol: UART Protocol (Not Including Special Command)

CMD Frame Header	Device ID	Register Address	N Bytes of Data	CRC checksum
1 Byte	1 Byte	1 Byte	N Bytes	2 Bytes

Device ID is established via the voltage of ADDRx (3105A/3105C) or LAA (3105B/3105D).

9.9.2.3 Bus Reset and SYNC

When the system is powered up, normally the system host is initialized before initializing peripherals. Before initializing LumiBus devices, a bus reset operation is required.

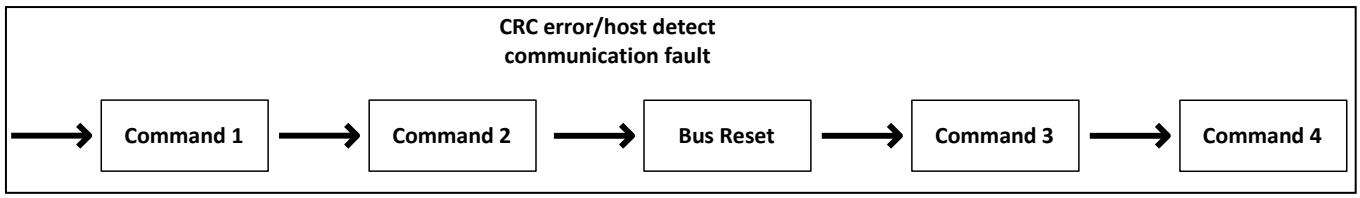
Upon receiving the bus reset command, all devices on the LumiBus will be in reset status. This operation can be optionally performed by the host for several application scenarios:

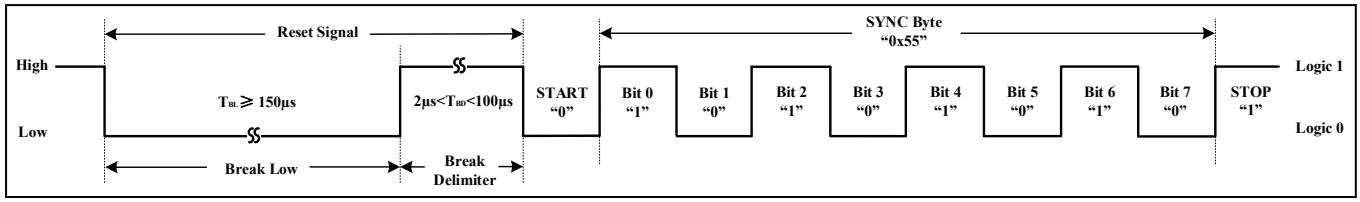
(1) During system power up, as stated above.

(2) Host watchdog time has expired.

(3) LumiBus communication fault is detected.

illustrated as in the following diagram:



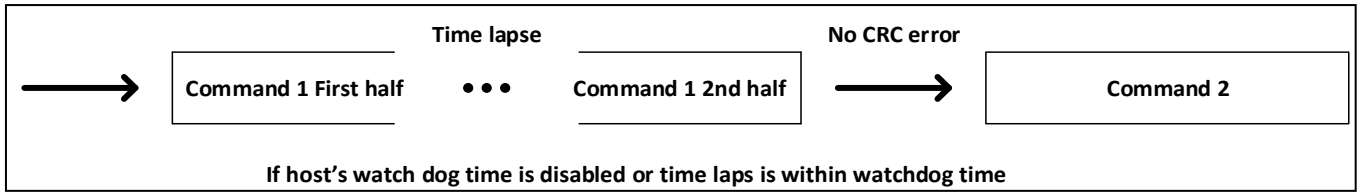


Break Low time (T_{BL}): min time 150μs, max timeout 10ms (depend on external CAN PHY)

Break Delimiter time (T_{BD}): Greater than 2μs, max timeout 100μs

SYNC 0x55: The first SYNC bit length is decided by lowest baud-rate (≥100kbps)

One complete UART frame can be received successfully even if the frame is not sent continuously. CRC error could be determined by reading back the written data byte.



9.9.2.4 Write Command Frame Structure (Write: N= 1~16, 32, 36, 72)

CMD Frame Header	Device ID	Register Address	N Bytes of Data	CRC checksum
1 Byte	1 Byte	1 Byte	N Bytes	2 Bytes

9.9.2.5 Read Command Frame Structure

CMD Frame Header	Device ID	Register Address	CRC checksum
1 Byte	1 Byte	1 Byte	2 Bytes

9.9.2.6 Response Frame Structure (Response: N= 1~16, 32, 36, 72)

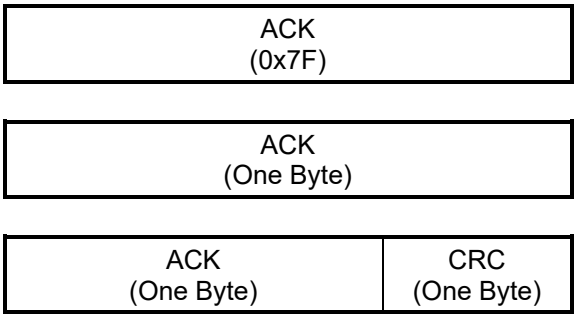
RSP Frame Header	Device ID	N Bytes of Data	CRC checksum
1 Byte	1 Byte	N Bytes	2 Bytes

9.9.2.7 Special Command Frame Structure

CMD Frame Header	Device ID	CRC checksum
1 Byte	1 Byte	2 Bytes

9.9.2.8 Acknowledge Frame

If the ACKEN bit is set in the SYSCFG register, the addressed device transmits an acknowledge back to the host MCU upon a successful single device write. The Acknowledge Frame is comprised of a single byte (ACK=0x7F) as the following sequence.



The CRC bytes are calculated during its ACK response, the CRC bytes are then appended to the end of the read data. This allows the host MCU to check the ACK data coming from the IS32FL3105 device for any transmission errors. Upon reading data from the IS32FL3105 device, the host MCU should calculate and compare the CRC to determine whether valid data was received.

ACK CRC formula: x8 + x5 + x4 + 1

The following is a reference CRC checksum C code for a transmission to the IS32FL3105 devices.

```
Uint8 reverse_byte(Uint8 byte)
{
// First, swap the nibbles
byte = (((byte & 0xF0) >> 4)| | ((byte & 0x0F) << 4));
// Then, swap bit pairs
byte = (((byte & 0xCC) >> 2) | ((byte & 0x33) << 2));
// Finally, swap adjacent bits
byte = (((byte & 0xAA) >> 1) | ((byte & 0x55) << 1));
// We should now be reversed (bit 0 <--> bit 7, bit 1 <--> bit 6, etc.)
return byte;
}

uint8_t calculate_crc8(uint8_t *buf, int8_t length)
{
        uint8_t crc = 0x00;
        uint8_t I;
        while (length--)
        {
                crc ^= reverse_byte(*buf++);

                for (I = 0; I < 8; I++)
                {
                        crc = (crc << 1) ^ ((crc & 0x80) ? 0x31 : 0);
                }
        }
        return reverse_byte(crc);
}

bool is_crc_valid_ACK(uint8_t *rx_buf, uint8_t crc_start)
{
        uint8_t crc_calc; // Calculated CRC
        // Calculate the CRC based on bytes received
```

```
        crc_calc = calculate_crc8(rx_buf, crc_start);
        // Do they match?
        if(*(rx_buf + crc_start) == crc_calc)
        {
        return TRUE;
        }
        else
        {
        return FALSE;
        }
}
```

9.9.3 TRANSACTION FRAME DESCRIPTION

Command frames include the following byte types:

1) Frame Header Byte.
2) Device ID Byte.
3) Start Register Address Byte.
4) N Data Byte(s) (N = 1~16, 32,36, 72).
5) CRC Bytes (CRC_L and CRC_H).
6) Acknowledge Byte (ACK, optional).

9.9.3.1 Frame Header Byte

Bit	D7	D6	D5	D4:D0
CMD Frame Header	FRM_TYPE =1	W/R	BCON	DATA [4:0]
Response Frame Header	FRM_TYPE=0	-	-	RESP [4:0]

CMD Frame Header

D7(FRM_TYPE): 0 = Response Frame.
1 = Command Frame.

D6(W/R): 0 = Write.
1 = Read.

D5(BCON): 0 = Normal single device writes and read command.
1 = Broadcast write command; When BCON = 1 and Device ID = FFh, broadcast to all devices, broadcast only accepts write command.

D4~D0(DATA [4:0]) When DATA [4] =0: the DATA [3:0] determines transmit data length,
DATA [4:0] = [00000] = 1 byte, …, DATA [4:0] = [01111] = 16 Bytes,
DATA [4:0] = [10000] = 32 Bytes,
DATA [4:0] = [10001] = 36 Bytes,
DATA [4:0] = [10010] = 72 Bytes.
When DATA [4] =1: the DATA [3:0] represents special written command, as below:
DATA [4:0] = [11110] Registers reset command: to reset all function registers to default values (Page 0 register and Page 1 register, but excluding the PWR bit in Page 0 F4h) when receiving this command (support both normal command and broadcast command).

Note 9: The reset command only resets the registers of page 0 and page 1, but the PWR bit of F4h in page 0 can't be reset.

DATA [4:0] = [11000] PWM data update latch command; PWM data is loaded upon when receiving this command (support both normal command and broadcast command).

Response Frame Header

D7(FRM_TYPE): 0 = Response Frame.
1 = Command Frame.

D6:D5 Reserved

D4~D0(RESP [4:0]): Response data length,
RESP [4:0] = [00000] = 1 byte, …, RESP [4:0] = [01111] = 16 bytes,
RESP [4:0] = [10000] = 32 bytes,
RESP [4:0] = [10001] = 36 Bytes,
RESP [4:0] = [10010] = 72 Bytes.

9.9.3.2 Device ID Byte

	D7:D0
Device ID	DEV_ID [7:0]

Note 10: Device address is set by the voltage of $ADDR_X$ or LAA.

9.9.3.2.1 IS32FL3105A/C Direct Address Setting

The device ID of each IS32FL3105A/C device is determined by the voltage of ADDR0 pin and ADDR1 pin. The voltage of $ADDR_X$ can be divided from V50 through two resistors (as illustrated below in Figure 12). As following mapping for the Device ID byte. For a broadcast command of LumiBus, Device ID Byte must be 0xFF, otherwise the broadcast command will be invalid.

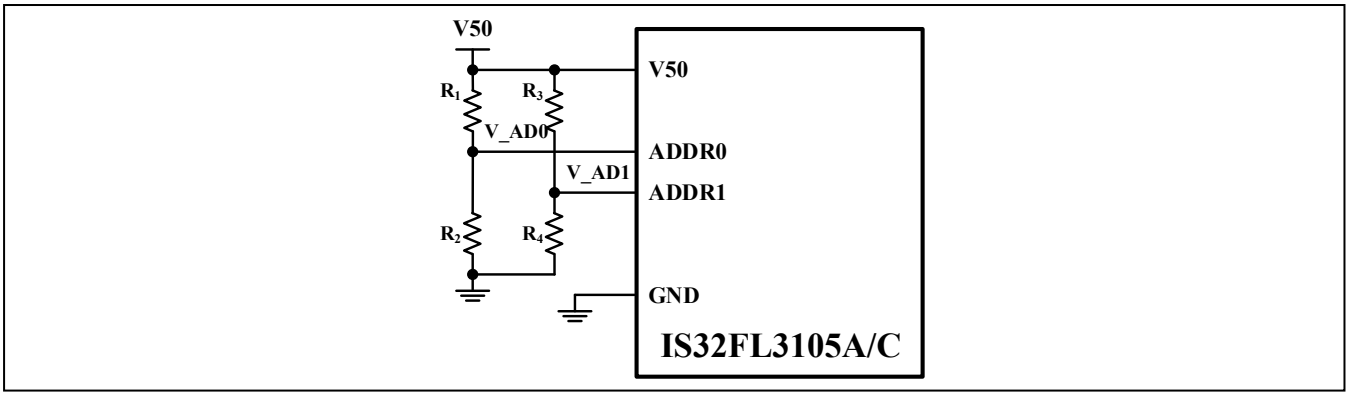


Figure 12 Direct Address Setting

The recommendation for five direct address selection options with voltage divider resistors (The tolerance range of resistance accuracy could be ±1%):

ADDRx (V_ADx) (V)	R1 / R3 (shown in Figure 12)	R2 / R4 (shown in Figure 12)
(1/10) ×V50	91kΩ	10kΩ
(3/10) ×V50	75kΩ	33kΩ
(5/10) ×V50	51kΩ	51kΩ
(7/10) ×V50	33kΩ	75kΩ
(9/10) ×V50	10kΩ	91kΩ

Direct Address Mapping

ADDRx= 1/10×V50, 3/10×V50, 5/10×V50, 7/10×V50, 9/10×V50

ADDR1 (V_AD1) (V)	ADDR0 (V_AD0) (V)	D7	D6	D5	D4	D3	D2	D1	D0	DEVICE ID (HEX)
(1/10) ×V50	(1/10) ×V50	0	0	0	0	0	0	0	0	00
(1/10) ×V50	(3/10) ×V50	0	0	0	0	0	0	0	1	01
(1/10) ×V50	(5/10) ×V50	0	0	0	0	0	0	1	1	03
(1/10) ×V50	(7/10) ×V50	0	0	0	0	0	1	0	1	05
(1/10) ×V50	(9/10) ×V50	0	0	0	0	0	1	1	1	07
(3/10) ×V50	(1/10) ×V50	0	0	0	0	1	0	0	0	08
(3/10) ×V50	(3/10) ×V50	0	0	0	0	1	0	0	1	09
(3/10) ×V50	(5/10) ×V50	0	0	0	0	1	0	1	1	0B
(3/10) ×V50	(7/10) ×V50	0	0	0	0	1	1	0	1	0D
(3/10) ×V50	(9/10) ×V50	0	0	0	0	1	1	1	1	0F
(5/10) ×V50	(1/10) ×V50	0	0	0	1	1	0	0	0	18
(5/10) ×V50	(3/10) ×V50	0	0	0	1	1	0	0	1	19
(5/10) ×V50	(5/10) ×V50	0	0	0	1	1	0	1	1	1B
(5/10) ×V50	(7/10) ×V50	0	0	0	1	1	1	0	1	1D
(5/10) ×V50	(9/10) ×V50	0	0	0	1	1	1	1	1	1F
(7/10) ×V50	(1/10) ×V50	0	0	1	0	1	0	0	0	28
(7/10) ×V50	(3/10) ×V50	0	0	1	0	1	0	0	1	29
(7/10) ×V50	(5/10) ×V50	0	0	1	0	1	0	1	1	2B
(7/10) ×V50	(7/10) ×V50	0	0	1	0	1	1	0	1	2D
(7/10) ×V50	(9/10) ×V50	0	0	1	0	1	1	1	1	2F
(9/10) ×V50	(1/10) ×V50	0	0	1	1	1	0	0	0	38
(9/10) ×V50	(3/10) ×V50	0	0	1	1	1	0	0	1	39
(9/10) ×V50	(5/10) ×V50	0	0	1	1	1	0	1	1	3B
(9/10) ×V50	(7/10) ×V50	0	0	1	1	1	1	0	1	3D
(9/10) ×V50	(9/10) ×V50	0	0	1	1	1	1	1	1	3F
-	-	1	1	1	1	1	1	1	1	FF (Note 11) (for broadcast command only)

Note 11: The Device ID Byte must be 0xFF to broadcast to all IS32FL3105A/B/C/D devices and broadcast only accepts writing command.

9.9.3.2.2 IS32FL3105B/D Location Address

LAA Location Address Assignment

Location Address Assignment method (LAA) refers to the method that is used to automatically assign a unit address to the equally built slave devices, e.g., IS32FL3105B/D, that are located within a LumiBus system. LAA method is used in conjunction with ISSI's proprietary bus, LumiBus as described earlier, that is a modification of LUMINUS bus to take advantage of its well-established physical layer definition, as well as UART protocol, for its robust, long distance, chip-to-chip and board-to-board communication.

LAA Basic Function

Each IS32FL3105B/D device has to provide two extra pins, One input pin AI and one output pin AO. The input of the first SNPD node is either set to a low level (e.g. by connecting it to ground) or connected via a configuration wire to the output of the master. Another configuration wire is routed from the output AO of the first LAA node to the input AI of the second and so on, resulting in a daisy chain.

In the beginning, the outputs of all LAA nodes feature a high level. In case the NAD of a LAA node is not configured and its input AI is on low level, the LAA node is selected and the node address configuration messages via the LumiBus are addressed to this LAA node. After finishing the configuration, the LAA node switches its output AO to

a low level, which selects the second LAA node, and so on. This way a LAA node can signal to the next LAA node in line that the next configuration messages apply to it.

The following system block diagram shows the LAA configuration flow (write), as well as SNPD read back flow. Normal data follows the same data flow.

The LAA configuration process starts with an LAA initialization command.

LAA Initialization Command

The host needs to first send this LAA Initialization command before any LAA NAD Assignment action. After IS32FL3105B/D receives this LAA Initialization command, register 0x1E at Page 2 then can use LAA NAD Assignment command for NAD assignment.

CMD Frame Header	Device ID	Register Address	CNAD	LDAT	CRC checksum	
0xA1	0xFF	0xF5	0X7F	0x01	0x7C	0x0F

LAA NAD Assignment Command

LAA NAD assignment command is to change register 0x1E for new NAD address. Before sending the LAA NAD assignment command, it is necessary to point the register page to Page 2 first.

CMD Frame Header	Device ID	Register Address	CNAD	CRC checksum
0x80	iNAD	0x1E (Page 2)	NAD	CRC16-bit

iNAD: Current NAD stored in 0x1E at Page 2 (Initial value = 0x00)

LAA NAD Succeeded Command

After completing LAA NAD assignment command to change IS32FL3105B/D NAD address, the host needs to send this LAA NAD succeeded command to complete slave NAD assignment action. After sending LAA NAD succeeded command LAA NAD Assignment will become inactive, and the AO pin pull low.

CMD Frame Header	Device ID	Register Address	CNAD	LDAT	CRC checksum
0x81	NAD	0xF5	0x7F	0x02	CRC16-bit

LAA NAD Finished Command

After completing LAA NAD Assignment Command to change all IS32FL3105B/D NAD address, host needs to send this LAA NAD Finished Command to complete NAD assignment action. After receiving LAA NAD Finished Command，all devices LAA NAD Assignment will become inactive.

CMD Frame Header	Device ID	Register Address	CNAD	LDAT	CRC checksum	
0xA1	0xFF	0xF5	0X7F	0x03	0xFD	0xCE

LAA Read NAD register

Read register 0x1E at Page 2

CMD Frame Header	Device ID	Register Address	CRC checksum
0xC0	NAD	0x1E (Page 2)	CRC16-bit

iNAD: Current NAD stored in 0x1E at Page 2 (Initial value = 0x00)

Response

RSP Frame Header	Device ID	Register Address	Register Data	CRC checksum
0x00	NAD (new NAD)	0X1E (Page 2)	New NAD	CRC16-bit

LAA Configuration Flow

The LAA uses five LAA node configuration services. They are distinguished via SNPD sub functions. The LAA node configuration services are listed below table.

SNPD sub function	Service Description
LAA Initialization Command	Starts LAA configuration process
LAA NAD Assignment Command	Assigns LAA slave with new NAD
LAA read NAD register	Read out NAD From NAD register
LAA NAD Succeeded Command	Notify a single node that the address assignment is complete
LAA Finished Command	Information about LAA configuration process closure

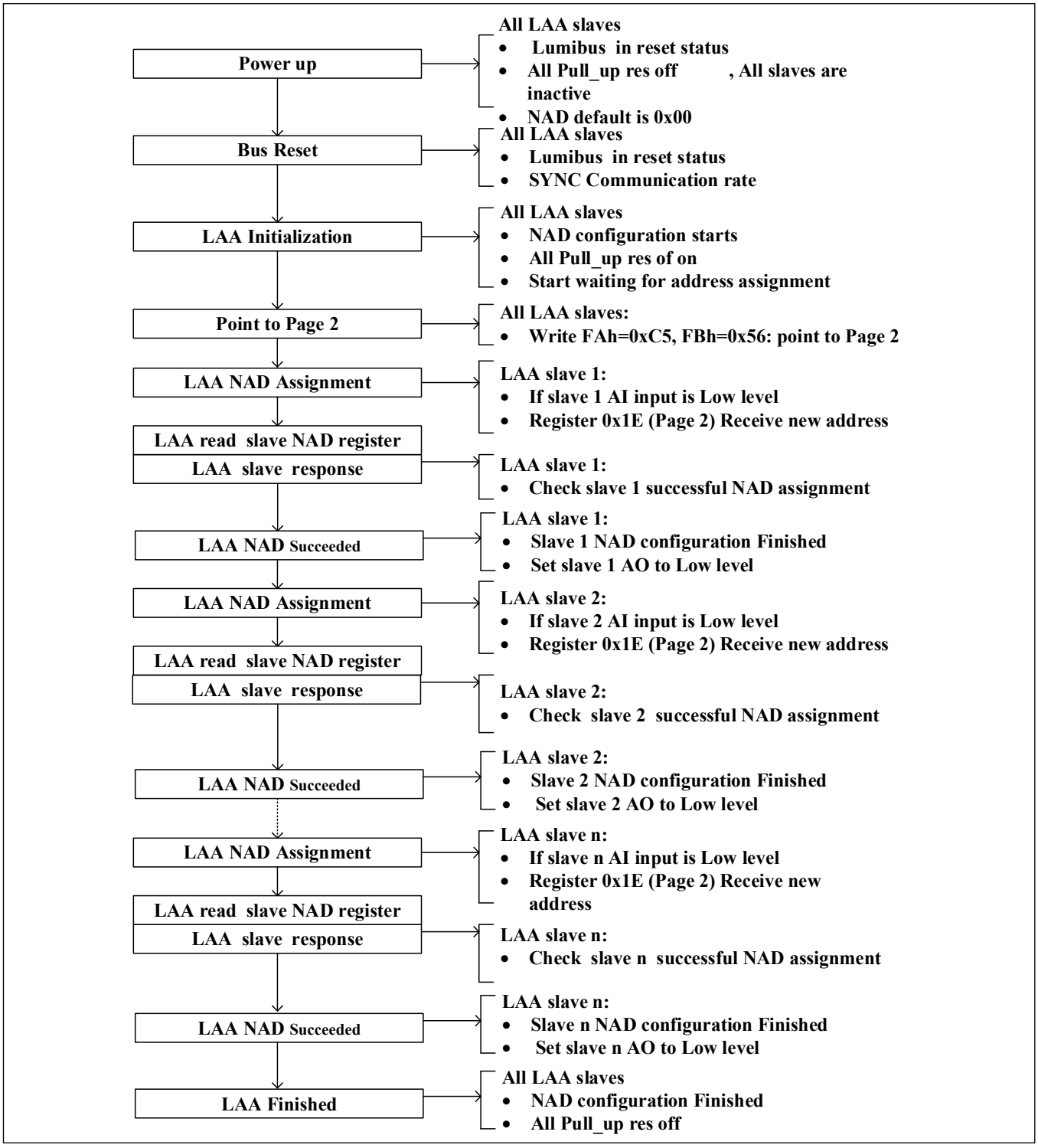


Figure 13 LAA SNPD Configuration Flow

9.9.4 START REGISTER ADDRESS BYTE

The LumiBus protocol allows up to 72(1~16, 32, 36, 72) successive register locations from the addressed register to be written or read by a single command frame. The Start Register Address Byte is a single byte which specifies the first register being written or read. The Start Register Address byte is present only in Write and Read Command transactions, not in Read Response and Special command transactions.

9.9.5 N DATA BYTE (S)

The Frame Header Byte specifies the number of data bytes to be included in the frame.

9.9.6 CRC BYTES (CRC_L AND CRC_H)

CRC [15:0] Frame CRC checksum, 2 bytes.

The host sends command to IS32FL3105 using CRC-16-IBM standard for CRC checksum calculation, which will cover the whole frame data, e.g., CMD Frame Header, Device I, Register Address, N Bytes of Data. Lower byte first followed by higher byte.

CMD Frame Header	Device ID	Register Address	Register Data	CRC_L	CRC_H
1 Byte	1 Byte	1 Byte	N Byte	1 Byte	1 Byte

The following is a reference CRC checksum C code.

```
Uint16 crc_16_ibm (Uint8 *buf, Uint8 len)
{
  Uint16 crc = 0;
  Uint16 I;
  while (len--)
  {
    crc ^= *buf++;
    for (I = 0; I < 8; I++)
    {
      crc = (crc >> 1) ^ ((crc & 1)? 0xa001: 0);
    }
  }
  return crc;
}
```

When IS32FL3105 sends back CRC to the host, the data needs to be bit reversed then compare with the CRC data. The following is a reference CRC reverse bit checksum code.

```
Uint8 reverse_byte(Uint8 byte)
{
  // First, swap the nibbles
  byte = (((byte & 0xF0) >> 4) | ((byte & 0x0F) << 4));
  // Then, swap bit pairs
  byte = (((byte & 0xCC) >> 2) | ((byte & 0x33) << 2));
  // Finally, swap adjacent  bit
  byte = (((byte & 0xAA) >> 1) | ((byte & 0x55) << 1));
  // We should now be reversed (bit 0 <--> bit 7, bit 1 <--> bit 6, etc.)
  return byte;
}
```

The following is a reference code for checking the returned data against CRC data.

```
bool is_crc_valid(Uint8 *rx_buf, Uint8 crc_start)
{
  Uint16 crc_calc; // Calculated CRC
  Uint8 crc_msb, crc_lsb; // Individual bytes of calculated CRC
  // Calculate the CRC based on bytes received
  crc_calc = crc_16_ibm(rx_buf, crc_start);
  crc_lsb = (crc_calc & 0x00FF);
  crc_msb = ((crc_calc >> 8) & 0x00FF);
  // Perform the bit reversal within each byte
  crc_msb = reverse_byte(crc_msb);
  crc_lsb = reverse_byte(crc_lsb);
  // Do they match?
  if((*(rx_buf + crc_start) == crc_lsb) && (*(rx_buf + crc_start + 1) == crc_msb))
  {
    return TRUE;
```

```
    }

    else
    {
        return FALSE;
    }
}
```

9.9.7 ACKNOWLEDGE BYTE

The acknowledgement byte (ACK) consists of 1-2 bytes (When ACKSEL = “01”, ACK 0x7F):

Only when the ACKSEL bit is configured in the F4h register of PAGE0 and the write is successful, will the addressed IS32FL3105 device send back an ACK. Successful writing will not generate CRC checksum errors. Please note that the confirmation is only valid for writing transactions to a single device of IS32FL3105.

9.9.8 TURNAROUND TIME

When considering back-to-back data transfer, the turnaround time (additional time required between the end of the previous byte stop bit and the beginning of the next byte start bit) is required, that means a finite amount of dead time must be inserted between two bytes or two command frames. It’s recommended to use dual stop bits mode for the UART interface.

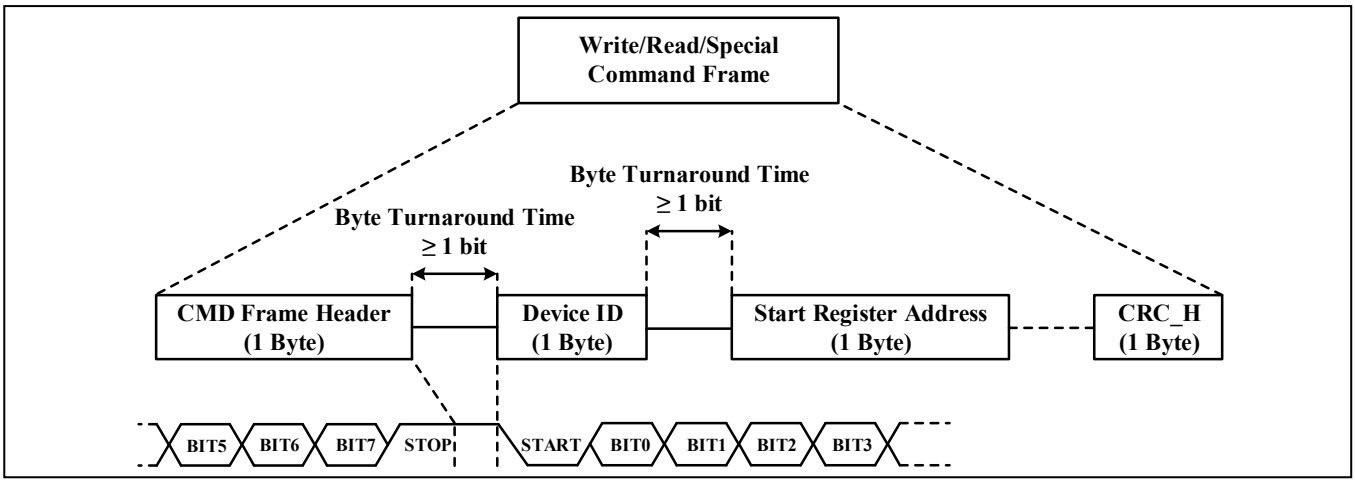


Figure 14 Turnaround Time Between Byte to Byte

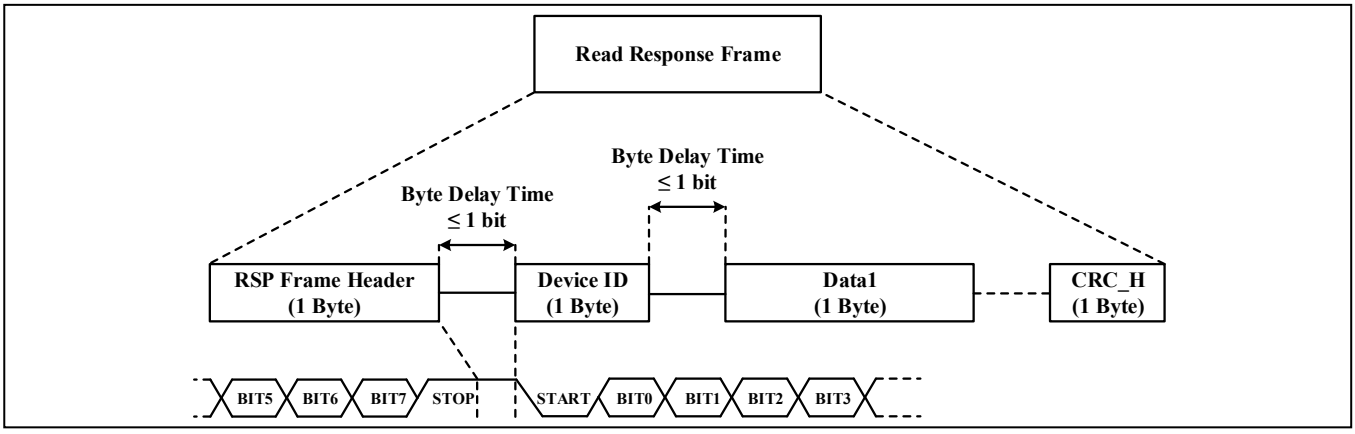


Figure 15 Delay Time Between Byte to Byte of Read Response Frame

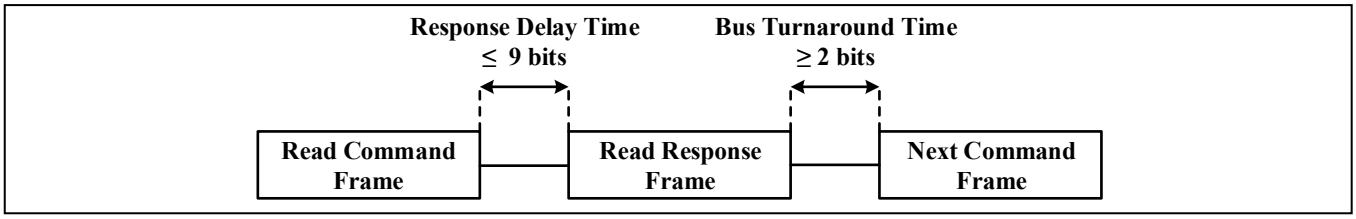


Figure 16 Turnaround Time Between Read Response Frame to Next Command Frame

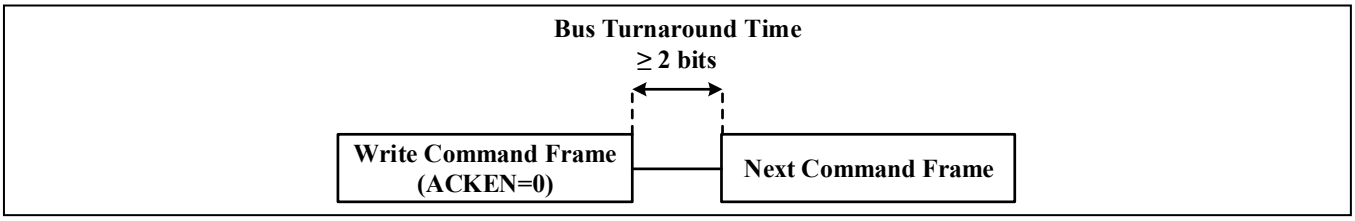


Figure 17 Turnaround Time Between Write Command Frame to Next Command Frame (ACK Disabled)

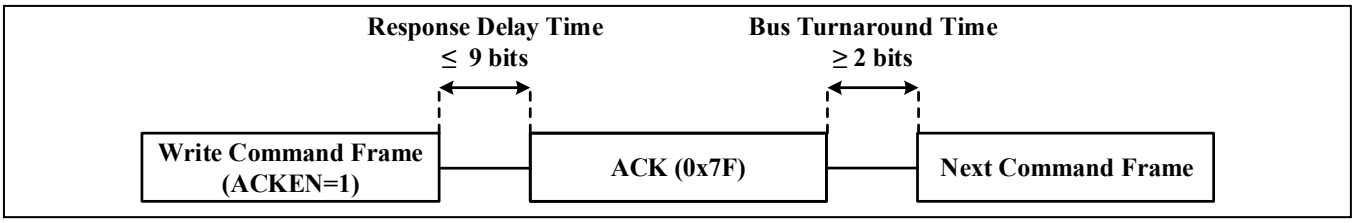


Figure 18 Turnaround Time Between ACK to Next Command Frame (ACK Enabled)

9.10 OTP COMMAND FRAME

9.10.1 OTP Content Register Write Frame (Write to OTP Content Register at Page 2, N=1~16-byte data)

CMD Frame Header	Device ID	Register Address	N Bytes of Data	CRC checksum
0b100{N}	1Byte	0x08-0x1F (Page 2)	N Bytes Data	CRC16-bit

9.10.2 OTP Content Register Read Frame (Read from OTP Content Register at Page 2)

CMD Frame Header	Device ID	Register Address	CRC checksum
0b110{N}	1Byte	0x08-0x1F (Page 2)	CRC16-bit

9.10.3 OTP Content Register Response Frame

CMD Frame Header	Device ID	N Bytes of Data	CRC checksum
0b000{N}	1Byte	N Bytes Data	CRC16-bit

9.10.4 OTP Program Sequence Timing

The OTP Zone B, Zone C and Zone D are set to 0 when freshly out of factory. Bit may be set during the programming cycle, which is no longer erasable. Regardless of the status of the -bit. Once the Fuse-Protection bit is programmed to 1, The OTP content is no longer programmable.

Programming any bit of the OTP memory is executed by issuing the program command. During the whole programming procedure, the actual programming sequence is fully self-controlled by the device.

The programming procedure takes some time. Depending on the number of bits to be programmed to logic 1, it is required to wait an appropriate time before issuing the next command. The programming procedure cannot be interrupted. If another command is issued too early, it gets ignored.

The device's internal oscillator does not provide enough accuracy for the timing of the OTP programming sequence. Thus, the device uses the bit length of the last received message as the time base. The programming procedure takes some time. Depending on the number of bits to be programmed to logic 1 and programming each digit requires at least 0.5ms Typ.

Please note it is crucial to use accurate bit timing for every programming command.

10 REGISTER MAPPING

10.1 REGISTER PAGE CONTROL DEFINITION

Register Address	Name	Function	Table	R/W	Default
FAh	Register Page Write Lock Register	To unlock Command Register	-	W	0000 0000
FBh	Register Page Select Register	Available Page 0 to Page 2 Registers	-	W	0101 0010

10.1.1 REGISTER PAGE CONTROL CONFIGURE

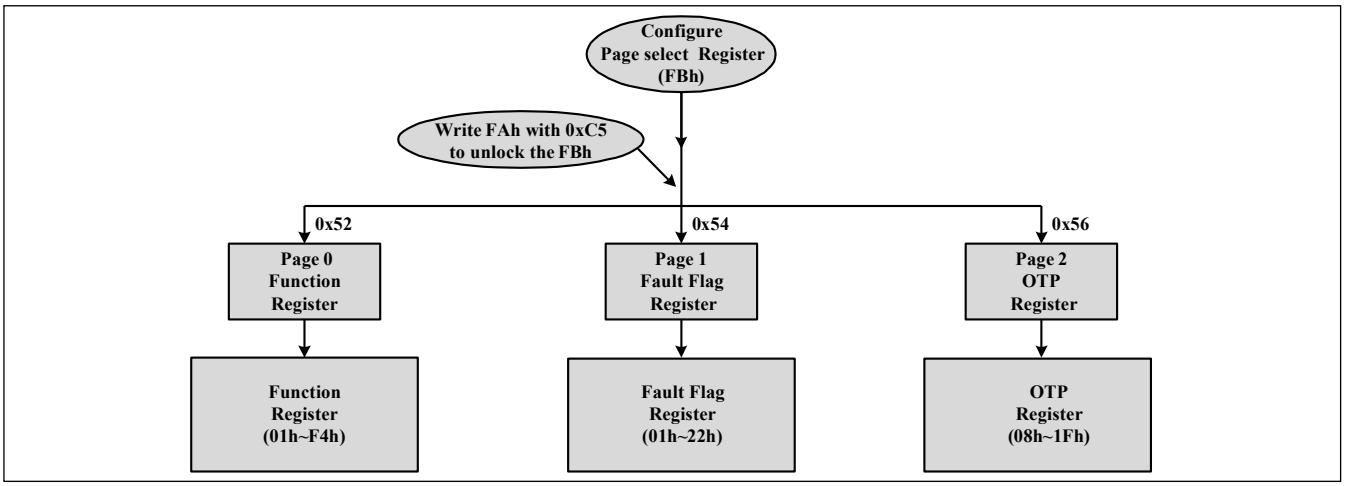


Figure 19 Register Page Control Configure

10.1.2 FBh Register Page Select Register

Data	Hex	Function
0101 0010 (default)	0x52 (default)	Point to Page 0(PG0): Function Register is available (default)
0101 0100	0x54	Point to Page 1(PG1): Fault Flag Register is available
0101 0110	0x56	Point to Page 2(PG2): OTP Register is available
Others	-	Not allowed

10.1.3 PAGE 0 (01H~F4H): FUNCTION REGISTER DEFINITION

Register Address	Name	Function	Table	R/W	Default
01h	CS1 PWML Register for SW1 (PWML _SW1_CS1)	Set SW1 CS1 PWML value	1	R/W	0000 0000
02h	CS1 PWMH Register for SW1 (PWMH_ SW1_CS1)	Set SW1 CS1 PWMH value	1	R/W	0000 0000
03h	CS2 PWML Register for SW1 (PWML_ SW1_CS2)	Set SW1 CS2 PWML value	1	R/W	0000 0000
04h	CS2 PWMH Register for SW1 (PWMH_ SW1_CS2)	Set SW1 CS2 PWMH value	1	R/W	0000 0000
05h	CS3 PWML Register for SW1 (PWML_ SW1_CS3)	Set SW1 CS3 PWML value	1	R/W	0000 0000
06h	CS3 PWMH Register for SW1 (PWMH_SW1_CS3)	Set SW1 CS3 PWMH value	1	R/W	0000 0000
…	…	…	…	…	…
1Fh	CS16 PWML Register for SW1 (PWML _SW1_ CS16)	Set SW1 CS16 PWML value	1	R/W	0000 0000
20h	CS16 PWMH Register for SW1 (PWMH_SW1_ CS16)	Set SW1 CS16 PWMH value	1	R/W	0000 0000
21h	CS17 PWML Register for SW1 (PWML _SW1_ CS17)	Set SW1 CS17 PWML value	1	R/W	0000 0000
22h	CS17 PWMH Register for SW1 (PWMH _SW1_ CS17)	Set SW1 CS17 PWMH value	1	R/W	0000 0000
23h	CS18 PWML Register for SW1 (PWML _SW1_ CS18)	Set SW1 CS18 PWML value	1	R/W	0000 0000
24h	CS18 PWMH Register for SW1 (PWMH _SW1_ CS18)	Set SW1 CS18 PWMH value	1	R/W	0000 0000
25h	CS1 PWML Register for SW2 (PWML _SW2_CS1)	Set SW2 CS1 PWML value	1	R/W	0000 0000
26h	CS1 PWMH Register for SW2 (PWMH_ SW2_CS1)	Set SW2 CS1 PWMH value	1	R/W	0000 0000
27h	CS2 PWML Register for SW2 (PWML_ SW2_CS2)	Set SW2 CS2 PWML value	1	R/W	0000 0000
28h	CS2 PWMH Register for SW2 (PWMH_ SW2_CS2)	Set SW2 CS2 PWMH value	1	R/W	0000 0000
29h	CS3 PWML Register for SW2 (PWML_ SW2_CS3)	Set SW2 CS3 PWML value	1	R/W	0000 0000
2Ah	CS3 PWMH Register for SW2 (PWMH_SW2_CS3)	Set SW2 CS3 PWMH value	1	R/W	0000 0000
…	…	…	…	…	…
43h	CS16 PWML Register for SW2 (PWML _SW2_ CS16)	Set SW2 CS16 PWML value	1	R/W	0000 0000
44h	CS16 PWMH Register for SW2 (PWMH_SW2_ CS16)	Set SW2 CS16 PWMH value	1	R/W	0000 0000
45h	CS17 PWML Register for SW2 (PWML _SW2_ CS17)	Set SW2 CS17 PWML value	1	R/W	0000 0000
46h	CS17 PWMH Register for SW2 (PWMH _SW2_ CS17)	Set SW2 CS17 PWMH value	1	R/W	0000 0000
47h	CS18 PWML Register for SW2 (PWML _SW2_ CS18)	Set SW2 CS18 PWML value	1	R/W	0000 0000
48h	CS18 PWMH Register for SW2 (PWMH _SW2_ CS18)	Set SW2 CS18 PWMH value	1	R/W	0000 0000
49h~5Ah	SL Register for SW1	Set DC data for SW1	2	R/W	0011 1111
5Bh~6Ch	SL Register for SW2	Set DC data for SW2	2	R/W	0011 1111
6Dh~6Fh	R group GCC Register	R group global current adjustment	3	R/W	0011 1111
6Eh	G group GCC Register	G group global current adjustment	4	R/W	0011 1111
6Fh	B group GCC Register	B group global current adjustment	5	R/W	0011 1111
70h	Operating Configure Register	General control	6	R/W	1100 0000
71h	Power Noise Reduction & Thermal Register	Set power noise reduction function and thermal shutdown/thermal roll off	7	R/W	0100 0001
72h	OSC Frequency Setting and SSP Register	Set OSC frequency and spread spectrum function	8	R/W	0000 0000
73h	SW de-ghost Register	Set SW pull down voltage	10	R/W	0000 0000
74h	CS de-ghost Register	Set CS pull up voltage	11	R/W	0000 0000
75h	DCFB Threshold Enable and Short Detect Threshold Register	Set short detect Threshold and DCFB threshold enable control	12	R/W	1000 0000
76h	SW Loop Back Test Control Register	Set SW loop back Test	13	R/W	0000 0000
77h	SW Over Current Protect Register	SW over current protect control	14	R/W	0000 0100

Register Address	Name	Function	Table	R/W	Default
78h	DCFB Output Control and DCFB Threshold Select Register	Set DCFB mode, DCFB threshold and DCFB output current multiple	15	R/W	0100 0000
79h	DCFB Output Current Setting Register	Select DCFB output current	16	R/W	1000 0000
7Ah	External NTC/PTC Temperature Measurement Register	Select external NTC/PTC temperature measurement channel	17	R/W	0000 0000
7Bh~7Dh	R Channels LED VF Monitoring Register	Configure R channels LED VF monitoring	18	R/W	0000 0000
7Ch	G Channels LED VF Monitoring Register	Configure G channels LED VF monitoring	19	R/W	0000 0000
7Dh	B Channels LED VF Monitoring Register	Configure B channels LED VF monitoring	20	R/W	0000 0000
7Eh	VF Monitoring and Output Current Monitoring Control Register	Set output current monitoring mode and tolerance	21	R/W	0000 0000
7Fh	Output Current Monitoring Selection Register	Select output current monitoring channel and start output current monitoring	22	R/W	0000 0000
80h	CS Loop Back Test Control Register	Set CS loop back test and tolerance	23	R/W	0000 0000
81h	CS Loop Back Test Channel Selection Register	Select CS channel of loop back test	24	R/W	0000 0000
82h	Fault Flag Report Control Register 1	Fault flag report control 1	25	R/W	1111 1111
83h	Fault Flag Report Control Register 2	Fault flag report control 2	26	R/W	1111 1111
84h~88h	Color Crossfade Control Register	Color crossfade setting and enable	27	R/W	0000 0000
89h	Color Crossfade Steps and Crossfade Duration Time Register	Set color crossfade steps and crossfade duration time	28	R/W	0000 0000
8Ah	Communication Watchdog Timer Register	Set communications watchdog	30	R/W	1011 0000
8Bh	Watchdog Timer 2 Register	Set watchdog timer	31	R/W	0001 1000
8Ch	Temperature Compensation Control and Steps Register	Set temperature compensation control and steps	32	R/W	0000 0000
8Dh	Temperature Compensation R Channels Calibrate Register	Set PWM output calibrate after temperature compensation	33	R/W	1111 1111
8Eh	Temperature Compensation G Channels Calibrate Register	Set PWM output calibrate after temperature compensation	34	R/W	1111 1111
8Fh	Temperature Compensation B Channels Calibrate Register	Set PWM output calibrate after temperature compensation	35	R/W	1111 1111
90h~92h	Temperature Compensation Red LED channels Percentage Register	Set temperature compensation red LED channels percentage	36	R/W	0000 0000
93h~95h	Temperature Compensation Green LED channels Percentage Register	Set temperature compensation green LED channels percentage	37	R/W	0000 0000
96h~98h	Temperature Compensation Blue LED channels Percentage Register	Set temperature compensation blue LED channels percentage	38	R/W	0000 0000
99h~AAh	ADC VF Reference for SW1_CSy Register	Set SW1_CSy channels ADC VF reference	39	R/W	0000 0000
ABh~BCh	ADC VF Reference for SW2_CSy Register	Set SW2_CSy channels ADC VF reference	40	R/W	0000 0000
BDh	ADC Control Register 1	ADC control register 1	41	R/W	0000 0000
BEh	ADC Control Register 2	ADC control register 2	42	R/W	0000 0010
BFh	ADC Control Register 3	ADC control register 3	43	R/W	0000 0010
C0h~D1h	VF ADC Value at Room Temperature for SW1_CSy Register	Store VF ADC Value at room temperature for SW1_Csy channels	44	R/W	0000 0000
D2h~E3h	VF ADC Value at Room Temperature for SW2_CSy Register	Store VF ADC Value at room temperature for SW2_CSy channels	45	R/W	0000 0000

Register Address	Name	Function	Table	R/W	Default
E4h	On-die Temperature Sensor Room Temperature Value Register	Store on-die sensor ADC Value at room temperature	46	R/W	0000 0000
E5h	On-die Temperature Sensor ADC Reference Register	Set on-die senor ADC reference	47	R/W	0000 0000
E6h~E7h	ADC Data Register for Single Sampling	Read back ADC content data for single sampling	48/49	R	0000 0000
E8h~E9h	ADC Data Register for Cycle Sampling	Read back ADC content data for cycle sampling	50/51	R	0000 0000
EAh	On-die Temperature Sensor ADC Data for Cycle Sampling (High 8bit)	Read back on-die senor ADC content data for cycle sampling	52	R	1000 0000
EBh	DCFB Result Register	Result of the dynamic control	53	R	0111 1111
ECh	After Compensation PWM duty Read Out Channel Select Register	Select PWM duty read out Channel after compensation or crossfade	54	R/W	0000 0000
EDh	Read PWM_L Duty after Temperature Compensation or Crossfade	Read back PWM_L duty after compensation or crossfade	55	R	0000 0000
EEh	Read PWM_H duty after Temperature Compensation or Crossfade	Read back PWM_H duty after compensation or crossfade	55	R	0000 0000
EFh	PWM Data Update Register	Update PWM data	56	W	0000 0000
F0h	Reset Register	Reset Page 0 and Page 1 register to default value	57	W	1111 1111
F1h	OTP Control Register	Control OTP operation	58	R/W	1000 0000
F2h	PWM_L Active Output Duty After Update Register	Read back PWM_L active output duty data after update	59	R	0000 0000
F3h	PWM_H Active Output Duty after Update Register	Read back PWM_H active output duty data after update	60	R	0000 0000
F4h	Power Status and Communication Configuration Register	Communication configuration and set power status	61	R/W	0000 0000

10.1.4 PAGE 1 (01H~22H): FAULT FLAG REGISTER DEFINITION

Register Address	Name	Function	Table	R/W	Default
01h	Fault Flag Register1	To report fault flag	62	R/W	0000 0000
02h	Fault Flag Register2	To report fault flag	63	R/W	0000 0000
03h~07h	Open Detect Register	Store open detect result	64	R	0000 0000
08h~0Ch	Short Detect Register	Store short detect result	65	R	0000 0000
0Dh~11h	SW and CS Loop Back Test Result Register	Store SWx and CSy loop back test result	66	R	0000 0000
12h~16h	VF Voltage Monitor Result Register	Store VF voltage monitor result	67	R	0000 0000
17h~1Bh	Output Current Monitor Result Register	Store output current monitor result	68	R	0000 0000
1Ch	Self-check Status and Result Register	Store self-check status and result	69	R/W	0000 0000
1Dh	CRC Error Count	CRC Error Status Count	70	R/W	0000 0000
1Eh	OTP Status Register	OTP Status	71	R	---- ----
21h	ECC Status	Store ECC status for 1Err_Ecc	72	R	---- ----
22h	ECC Status	Store ECC status for 2Err_Ecc	73	R	---- ----

10.1.5 PAGE 2 (00H~1FH): OTP REGISTER DEFINITION

Register Address	Name	Function	Table	R/W	Default
Zone B: 08h ~ 12h					
08h~10h	Save PWM State for SW1 register	Save PWM State for SW1	74	R/W	0000 0000
11h	ECC_B Register	ECC for Zone B	75	R/W	0000 0000
12h	PT_B Register	Protection bit for Zone B	76	R/W	0000 0000
Zone C: 13h ~ 1Dh					
13h~1Bh	Save PWM State for SW2 Register	Save PWM State for SW2	77	R/W	0000 0000
1Ch	ECC_C Register	ECC for Zone C	78	R/W	0000 0000
1Dh	PT_C and Watchdog Fail Safe Mode Trigged Register	Set watchdog fail safe mode trigged and protection bit for Zone C	79	R/W	0000 0000
Zone D: 1Eh ~ 1Fh					
1Eh	SNPD Address Register	Store device address	80	R/W	0000 0000
1Fh	PT_D and ECC_D register	ECC and protection bit for Zone D	81	R/W	0000 0000

10.2 REGISTER DEFINITION

10.2.1 PAGE 0 (01H~F4H): FUNCTION REGISTER MAPPING

Table 1 01h ~ 48h PWM Control Register of SW1~SW2

Register	02h,04h,06h,08h,0Ah,0Ch…44h,46h,48h	01h,03h,05h,07h,09h,0Bh…43h,45h,47h
Bit	D7:D0	D7:D0
Name	PWM_H	PWM_L
Default	0000 0000	0000 0000

There are 36 PWM Data Registers for SW1. Registers 01h (03h, 05h…23h) and 02h (04h, 06h…24h) are used together to define channel 1(2, 3…) 's PWM data. Register 02h defines channel CS1's higher -bit PWM data while register 01h defines CS1's lower -bit PWM data. Similarly, registers 04h and 03h are used together to define CS2's PWM data, while Registers 06h and 05h are used together to define CS3's PWM data.

There are 36 PWM Data Registers for SW2. Registers 25h (27h, 29h…47h) and 28h (2Ah, 2Ch…48h) are used together to define channel 1(2, 3…) 's PWM data. Register 26h defines channel CS1's higher -bit PWM data while register 25h defines CS1's lower -bit PWM data. Similarly, registers 28h and 27h are used together to define CS2's PWM data, while Registers 2Ah and 29h are used together to define CS3's PWM data.

In the Operating Configure Register, D2:D1 is defined as PWM Mode, which has 4 settings. When PWMM setting is 00 (default), Data Registers serve as 16-bit PWM mode for channel CS1~CS18.

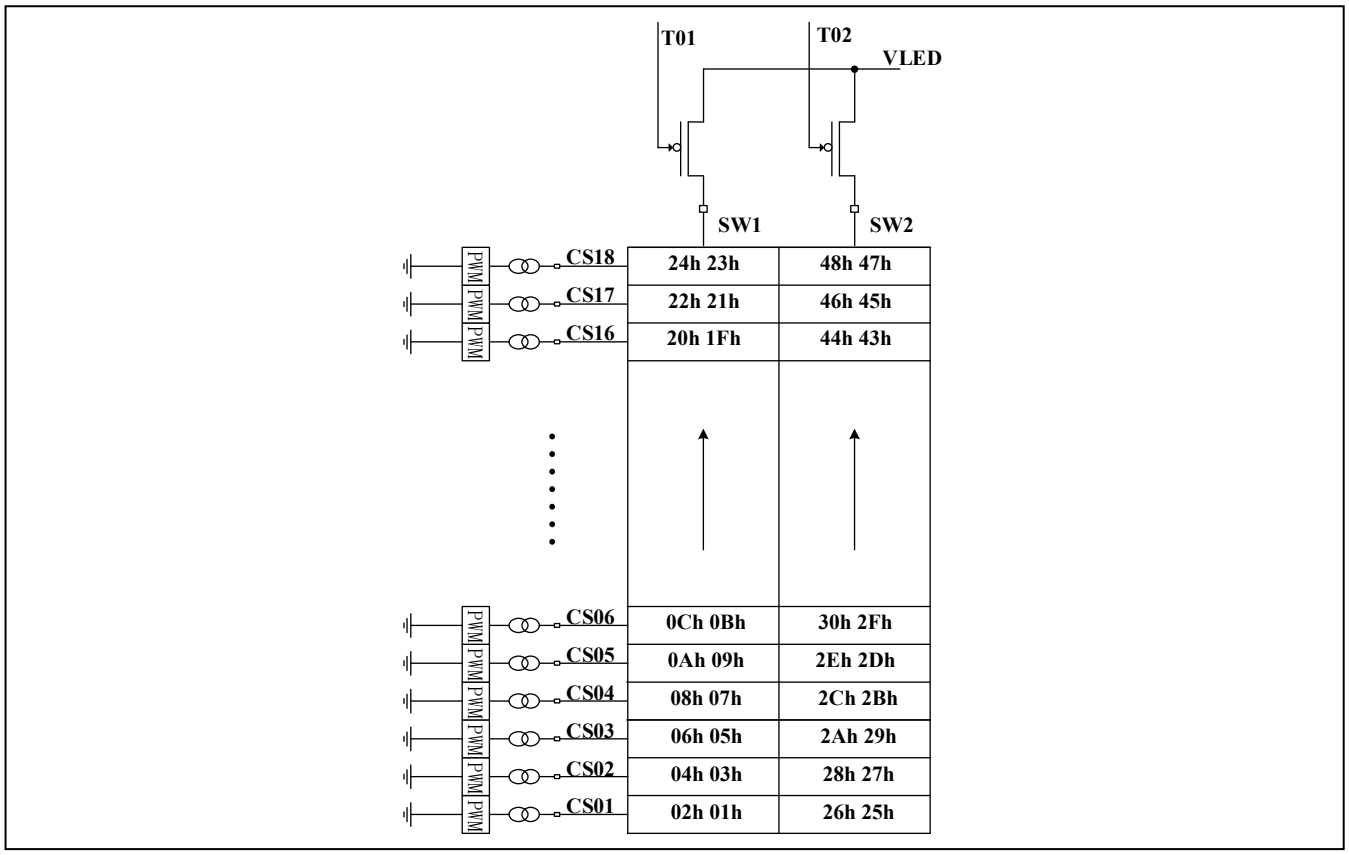


Figure 20 PWM Register

Each LED PWM is modulated by 2 bytes of data, stored in PWM registers. There are 4 options: 16-bit, 14-bit+2-bit, 13-bit+3-bit, or 8-bit+8-bit PWM mode.

The value of the PWM Registers decides the average current of each LED noted I_{LED}.

I_{LED} computed by Formula (1):

$$I_{LED} = \frac{PWM}{N} \times I_{OUT(PEAK)} \times Duty \quad (1)$$

N=65536:$PWM = \sum_{n=0}^{15} D[n] \cdot 2^n$

Where Duty is the duty cycle of SWx, see SCANING TIMING section for more information.

When SW_X= “1” and in 16-bit PWM mode (OSC=16MHz), Duty is computed as below:

$$Duty = \frac{4.0959ms}{(4.0964ms+0.0003ms)} \times \frac{1}{2} = \frac{1}{2.0004} \quad \text{(2, 16-bit mode)}$$

$I_{OUT(PEAK)}$ is the output current of CSy (y=1~18),

$$I_{OUT(PEAK)} = 60 \times \frac{GCC}{63} \times \frac{SL}{63} \qquad (3)$$

GCC is the Global Current Control register value and SL is the Scaling register value.

For example: if in 16-bit PWM mode, PWM register D15:D0=1000 000 1011 0101 (0x80B5, 32949), GCC=11 1111, SL=11 1111:

$$I_{LED} = 60 \times \frac{63}{63} \times \frac{63}{63} \times \frac{1}{2.001} \times \frac{32949}{65536}$$

Table 2 49h ~ 6Ch SL(DC) Register for SW1~SW2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	invalid		SL(DC)					
Default	-	-	1	1	1	1	1	1

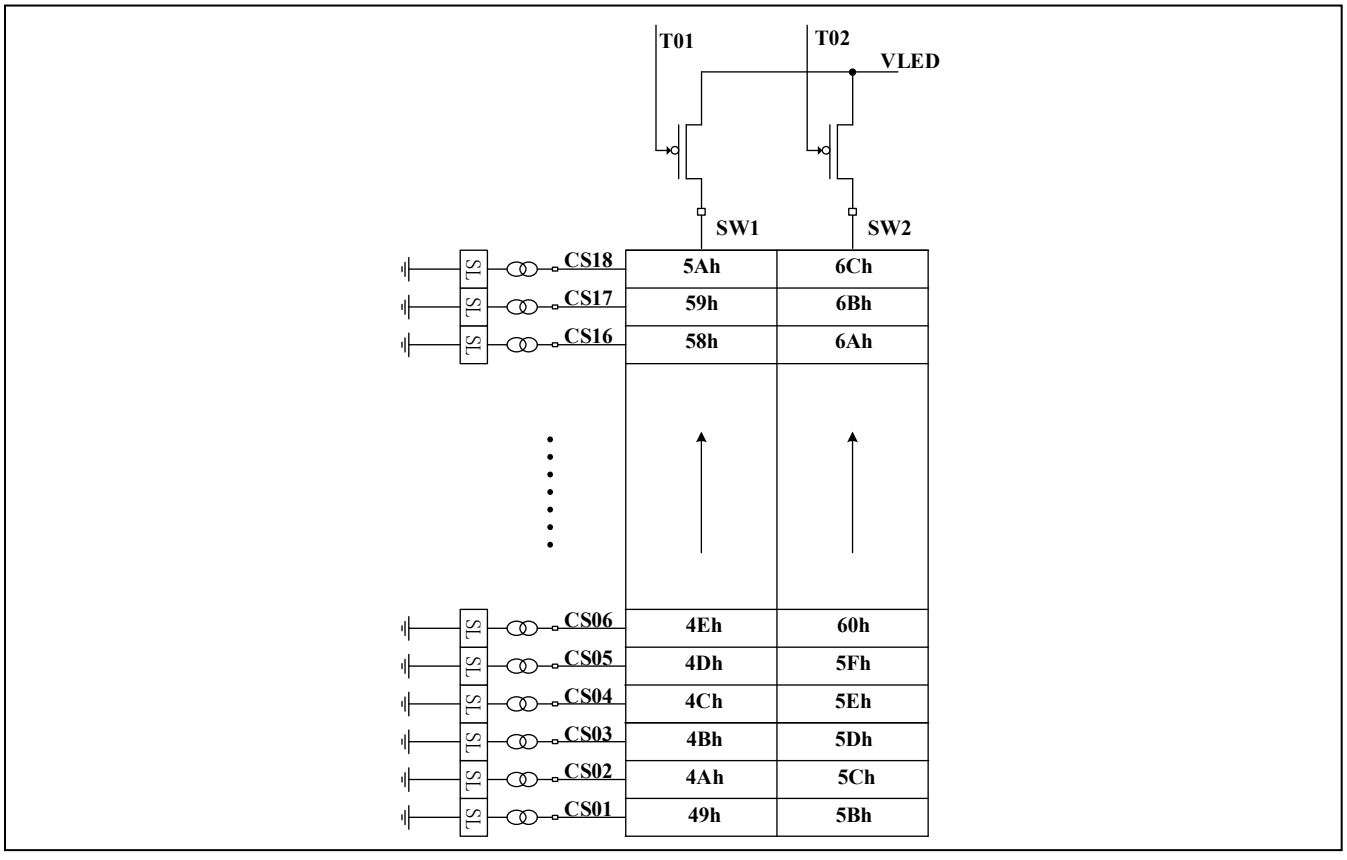


Figure 21 SL Register

The scaling register controls the DC output current of each dot. Each dot has a byte (only Low 6 -bit needs to be set) to modulate DC current in 64 steps.
The value of the Scaling Register decides the peak current of each LED noted $I_{OUT(PEAK)}$.
$I_{OUT(PEAK)}$ computed by Formula (3):

$$I_{OUT(PEAK)} = 60 \times \frac{GCC}{63} \times \frac{SL}{63} \qquad (3)$$

$$SL = \sum_{n=0}^{7} D[n] \cdot 2^n$$

Table 3 6Dh Global Current Control Register for R group channels

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	invalid		GCCR					
Default	-	-	1	1	1	1	1	1

Set global current for R group channels (CS1-R1, CS4-R2…CS16-R6)

Table 4 6Eh Global Current Control Register for G group channels

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	invalid		GCCG					
Default	-	-	1	1	1	1	1	1

Set global current for G group channels (CS2-G1, CS5-G2…CS17-G6)

Table 5 6Fh Global Current Control Register for B group channels

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	invalid		GCCB					
Default	-	-	1	1	1	1	1	1

Set global current for B group channels (CS3-B1, CS6-B2…CS18-B6)

The Global Current Control Register modulates all CSy (y=1~18) global current which is noted as $I_{OUT(PEAK)}$ in 64 steps.

$I_{OUT(PEAK)}$ is computed by the Formula (3):

$$I_{OUT(PEAK)} = 60 \times \frac{GCC}{63} \times \frac{SL}{63} \qquad (3)$$

$$GCC = \sum_{n=0}^{7} D[n] \cdot 2^n$$

Where D[n] stands for the individual bit value, 1 or 0, in location n.

Table 6 70h Operating Configure Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SW1_EN	SW2_EN	-	OSD_DIS	PWMM		CALI_EN	PSM
Default	1	1	0	0	0	0	0	0

SW1_EN **Odd SW Control**
0 SW1 disable
1 SW1 enable (Default)

SW2_EN **Even SW Control**
0 SW2 disable
1 SW2 enable (Default)
When both SW1 and SW2 are enabled, SW1 and SW2 turn on alternately.

OSD_DIS **Open and Short Detect**
0 Open and short detection enable (Default)
1 Open and short detection disable

PWMM	PWM Mode Select
00	16-bit (Default)
01	14+2-bit
10	13+3-bit
11	8+8-bit

CALI_EN	PWM Output multiply Calibrate function
0	PWM Output multiply calibrate function disable (Default) PWM output= PWM Control register value×100%
1	PWM Output multiply calibrate function enable PWM output= PWM Control register value×100%×CALI ratio (at 8Dh~8Fh)

PSM	Power Saving Mode
0	Wake up mode (Default)
1	Enter sleep, power saving mode; in this mode, PWM clock is disabled, and output is turned off (Send this command and use the broadcast command to make all 3105 devices on the bus enter Sleep Mode).

Wakeup Operation

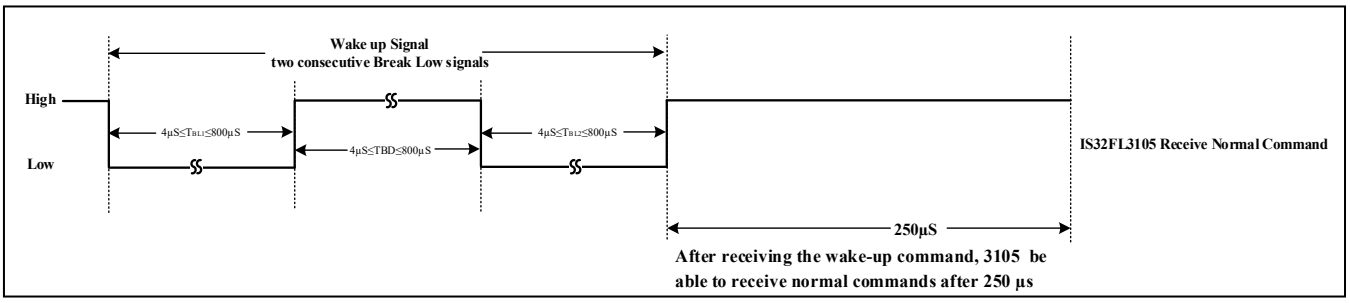


Figure 22 Wake up Signal

After IS32FL3105 enters power saving mode, it can be awakened by receiving two consecutive Break Low signals.

And after receiving the wake-up command, 3105 needs to wait at least 250μs to receive the normal command.

Break Low 1 time (TBL1): Greater than 4μs, max timeout 800μs.

Break Delimiter time (TBD): Greater than 4μs, max timeout 800μs.

Break Low 2 time (TBL2): Greater than 4μs, max timeout 800μs.

Table 7 71h Power Noise Reduction & Temperature Status/Thermal Roll off Register

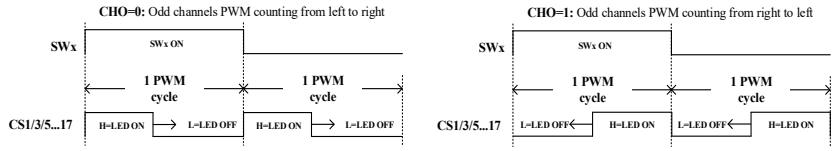
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	TSD_EN	TS		TROF		CHO	CHE
Default	0	1	0	0	0	0	0	1

TSD_EN	Thermal Shutdown Enable
0	Disable
1	Enable (Default)

TS	Thermal roll off Temperature Starting Temperature
00	140°C (Default)
01	120°C
10	100°C
11	90°C

TROF	Percentage of Output Current
00	100% (Default)
01	75%
10	55%
11	30%

CHO	Odd Channels Phase Delay Mode
0	PWM counting from left to right in one PWM cycle (Default)
1	PWM counting from right to left in one PWM cycle



CHE	Even Channels Phase Delay Mode
0	PWM counting from left to right in one PWM cycle
1	PWM counting from right to left in one PWM cycle (Default)

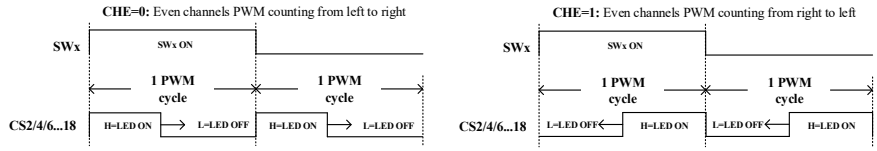


Table 8 72h OSC Frequency Setting Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SCLT		RNG		SSP	OFS		
Default	0	0	0	0	0	0	0	0

SCLT	Spread Spectrum Cycle Time
00	1980μs (Default)
01	1200μs
10	650μs
11	320μs

RNG	Spread Spectrum Range
00	±7.5%(Default)
01	±19%
10	±24%
11	±35%

SSP	Spread Spectrum Enable
0	Disable (Default)
1	Enable

OFS	OSC Frequency Setting for PWM
000	16MHz (Default)
001	32MHz
010	8MHz
011	4MHz
Other	Not allowed

Table 9 PWM Frequency

PWM Mode	32MHz	16MHz	8MHz	4MHz
16-bit	488Hz	244Hz	122Hz	61Hz
14-bit + 2-bit	488Hz~1.95kHz	244Hz~0.97kHz	122Hz~485Hz	61Hz~242Hz
13-bit + 3-bit	488Hz~3.9kHz	244Hz~1.95kHz	122Hz~0.97kHz	61Hz~485Hz
8-bit + 8-bit	488Hz~125kHz	244Hz~62.5kHz	122Hz~31.25kHz	61Hz~15.625kHz

Table 10 73h SW De-ghost Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	DTS		SWTS	SWPD			
Default	0	0	0	0	0	0	0	0

DTS	**De-ghost Time (including SW and CS)**
00	4 PWM clocks cycle (Default)
01	8 PWM clocks cycle
10	16 PWM clocks cycle
11	20 PWM clocks cycle

SWTS	**SW Pull Down Time Select**
0	SW de ghost pulls down during off time (Default)
1	SW pull-down during de ghost time

SWPD	**SW De-ghost Pull down Voltage**
0000	No pull down (Default)
0001	GND
0010	0.7V
0011	1.05V
0100	1.4V
0101	1.75V
0110	2.1V
0111	2.45V
1000	2.8V
1001	3.15V
1010	3.5V
1011	3.85V
1100	4.2V
1101	4.55V
1110	4.9V
1111	5.6V

Table 11 74h CS De-ghost Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CSPUR_GB				CSPUR_R			
Default	0	0	0	0	0	0	0	0

CSPUGB	**G&B Group Pull up Voltage**
0000	No pull up (Default)
0001/1111	VLED
0010	VLED -4.3V
0011	VLED -4.1V
0100	VLED -3.8V

0101	VLED -3.5V
0110	VLED -3.2V
0111	VLED -2.9V
1000	VLED -2.6V
1001	VLED -2.3V
1010	VLED -2.0V
1011	VLED -1.8V
1100	VLED -1.6V
1101	VLED -1.4V
1110	VLED -1.2V

CSPURR	**Group Pull up Voltage**
0000	No pull up (Default)
0001/1111	VLED
0010	VLED -4.3V
0011	VLED -4.1V
0100	VLED -3.8V
0101	VLED -3.5V
0110	VLED -3.2V
0111	VLED -2.9V
1000	VLED -2.6V
1001	VLED -2.3V
1010	VLED -2.0V
1011	VLED -1.8V
1100	VLED -1.6V
1101	VLED -1.4V
1110	VLED -1.2V

Table 12 75h DCFB Threshold Enable and Short Detect Threshold Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DCFB_VTH_EN	-			SDRNT		-	
Default	1	0	0	0	0	0	0	0

DCFB_VTH_EN	**DCFB Voltage Threshold High Limit Enable**
0	Disable DCFB_VTH
1	Enable DCFB_VTH (Default)

The DCFB_VTH_EN bit enables the comparison function to set the minimum threshold for DCFB detection results. This minimum threshold is configured via the DCFB_VTH bit in register 78h. Once the DCFB_VTH_EN function is enabled, the DCFB result register (address EBh) will output the minimum channel voltage that exceeds the DCFB_VTH threshold. This feature is designed to prevent inaccurate DCFB detection results and abnormal system behavior when the chip is in an open-circuit condition.

SDRNT	**Short Select Threshold Select**
00	(VLED-1.0) V (default)
01	(VLED-0.8) V
10	(VLED-0.6) V
11	(VLED-1.25) V

PWM Duty Threshold of LED Open / Short Detection:

PWM Mode	32MHz	16MHz	8MHz	4MHz
16-bit	PWM > 128	PWM > 64	PWM >32	PWM >16
14-bit + 2-bit	PWM > 512	PWM > 256	PWM >128	PWM >64
13-bit + 3-bit	PWM > 1024	PWM > 512	PWM >256	PWM >128
8-bit + 8-bit	PWM > 32768	PWM > 16384	PWM >8192	PWM >4096

Table 13 76h SW Loop Back Test Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	SWLT_SC	SWLT_EN	LBS		LBT	
Default	0	0	0	0	0	0	0	0

SWLT_SC **SW Loop Back Self-check Control**

0 Disable (Default)
1 Enable

SWLT_EN **SW Loop Back Test Control**

0 Disable (Default)
1 Enable

LBS **Loop Back Test Start Time**

00 4 PWM clocks (Default)
01 6 PWM clocks
10 8 PWM clocks
11 10 PWM clocks

LBT **Loop Back Test Tolerance**

00 3 PWM clocks (Default)
01 5 PWM clocks
10 7 PWM clocks
11 9 PWM clocks

Table 14 77h SW Over Current Protect Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-				RECOVER	OC_EN	OC_SEL	
Default	0	0	0	0	0	1	0	0

RECOVER **SW Recover to Normal Operation**

0 Disable (Default)
1 Enable, When SWx is turned off by OC protection, set RECOVER to 1 each time, SWx will be turned on again.

OC_EN **SW Over Current Protect Control**

0 Disable over current protection
1 Enable over current protection (Default)

OC_SEL	SW Over Current Protect Threshold
00	1.7A (Default)
01	1.5A
10	2.1A
11	1.9A

Table 15 78h DCFB Output Control and DCFB Threshold Select Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DCFB_VTH					DCFB_N		DCFB_EN
Default	0	1	0	0	0	0	0	0

DCFB_VTH DCFB Voltage Threshold High Limit

When the DCFB_VTH_EN bit (address 75h in PAGE0) is enabled, the system compares the VOUT ADC value detected by the DCFB circuit with the threshold value specified by DCFB_VTH [4:0] (with DCFB_VTH [6:5] = “00”).

DCFB_EN	DCFB function enable
0	DCFB function disable (Default)
1	DCFB function enable, output current from FBO pin

DCFB_N	DCFB multiple selection of output current
00/11	1x (Default)
01	2x
10	3x

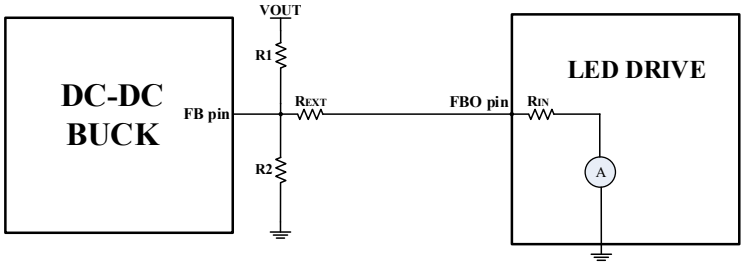
Table 16 79h DCFB Output Current Setting Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DCFB_OUT							
Default	1	0	0	0	0	0	0	0

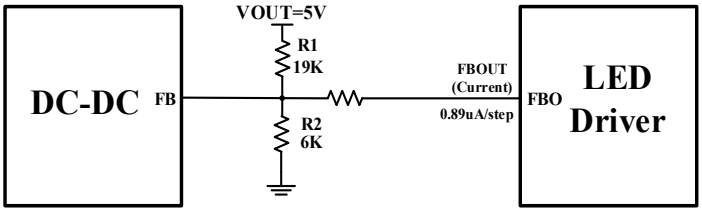
DCFB_OUT	DCFB Output Current Selection
00000000	0μA
00000001	0.89μA
00000010	1.78μA
……	……
01111101	111.25μA
01111110	112.14μA
01111111	113.03μA
1000000	0μA (Default)
1000001	-0.89μA
1000010	-1.78μA
1000011	-2.67μA
……	……
11111101	-111.25μA
11111110	-112.14μA
11111111	-113.03μA

Note 12:

To dynamically adjust output voltage, a small amount of current is injected in the voltage regulator feedback network as shown below figure. This changes the effective gain (VFB/VOUT) of the feedback network. A similar result would be observed if a resistor was connected in parallel with either the top or bottom feedback resistor. In some systems, resistors are switched in and out for output margining. Hence, another way of thinking of the current injected to the feedback node is to view it as adapting to a virtual resistance. If positive current is injected at the feedback node (VFB), it appears that the resistance of the top resistor (R1) has decreased, and the output voltage decreases as a result. When current is pulled out (negative current), the output voltage increases because the bottom resistor (R2) appears to have lower resistance. The following methods based on this concept allow for more control, flexibility, and precision than typical resistor-based techniques.



When the two partial voltage resistors of the DCDC are 19kΩ and 6kΩ (as shown below), the output current of each stage is ±0.89μA Typ. Single LED application, can achieve positive and negative 128 steps, each step adjustment ±17mV Typ., adjustable voltage range is ±2.071V Typ.



DCFB output current calculation formula:

$$I_{FBO}=\left(\frac{VOUT-V_{FB}}{R1}\right)-\left(\frac{V_{FB}}{R2}\right)$$

Table 17 7Ah External NTC/PTC Temperature Measurement Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Invalid			EXTM_SEL				
Default	0	0	0	0	0	0	0	0

EXTM_SEL	External NTC/PTC Temperature Measurement Selection
00000	All channels are used for current sink (Default)
00001	CS1 external temperature measurement enable
00010	CS2 external temperature measurement enable
00011	CS3 external temperature measurement enable
00100	CS4 external temperature measurement enable
00101	CS5 external temperature measurement enable
00110	CS6 external temperature measurement enable
00111	CS7 external temperature measurement enable
01000	CS8 external temperature measurement enable
01001	CS9 external temperature measurement enable
01010	CS10 external temperature measurement enable
01011	CS11 external temperature measurement enable
01100	CS12 external temperature measurement enable
01101	CS13 external temperature measurement enable
01110	CS14 external temperature measurement enable
01111	CS15 external temperature measurement enable
10000	CS16 external temperature measurement enable
10001	CS17 external temperature measurement enable
10010	CS18 external temperature measurement enable
Other	invalid

In the default state, all CSy channels are used for current sink.

When CSy channel external temperature measurement is enabled, the corresponding CSy is not used for current sink and can be connected to the external NTC or PTC to measure the external temperature. When using the temperature measurement function, ADC needs to be selected as the NTC/PTC measurement channel. This function only supports single sampling, and the sampling ADC results are stored in the E6h/E7h register.

Table 18 7Bh R Group Channels LED VF Monitoring Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	VFWD_R_MAX			VFWD_R_MIN		
Default	0	0	0	0	0	0	0	0

VFWD_R_MAX	**R Group Channels LED VF Monitoring Threshold Maximum Value Setting**
000	2.4V (Default)
001	1.6V
010	1.8V
011	2.0V
100	2.2V
101	2.6V

VFWD_R_MIN	**R Group Channels LED VF Monitoring Threshold Minimum Value Setting**
000	1.6V (Default)
001	1.0V
010	1.2V
011	1.4V
100	1.8V
101	2.0V

Table 19 7Ch G Group Channels LED VF Monitoring Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	VFWD_G_MAX			VFWD_G_MIN		
Default	0	0	0	0	0	0	0	0

VFWD_G_MAX	**G Group Channel LED VF Monitoring Threshold Maximum Value Setting**
000	3.0V (Default)
001	2.4V
010	2.6V
011	2.8V
100	3.2V
101	3.4V
110	3.6V
110	3.8 V

VFWD_G_MIN	**G Group channel LED VF Monitoring Threshold Minimum Value Setting**
000	2.6V (Default)
001	1.8V
010	2.0V
011	2.2V
100	2.4V
101	2.8V
110	3.0V
110	3.2V

Table 20 7Dh B Group Channels LED VF Monitoring Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	VFWD_B_MAX			VFWD_B_MIN		
Default	0	0	0	0	0	0	0	0

VFWD_B_MAX	**B Group Channel LED VF Monitoring Threshold Maximum Value Setting**
000	3.0V (Default)
001	2.4V
010	2.6V
011	2.8V
100	3.2V
101	3.4V
110	3.6V
110	3.8 V

VFWD_B_MIN	**B Group channel LED VF Monitoring Threshold Minimum Value Setting**
000	2.6V (Default)
001	1.8V
010	2.0V
011	2.2V
100	2.4V
101	2.8V
110	3.0V
110	3.2V

Table 21 7Eh VF Monitoring and Output Current Monitoring Control Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	VFMON_START	VFMON_F	VFSC_MODE[1:0]		IMONSC_MODE		-	IMON_TOR
Default	0	0	0	0	0	0	0	0

VFMON_START	**VF Monitoring start**
0	VF Monitoring stops (Default)
1	VF Monitoring starts

VFMON_ F	**VF Monitoring completed flag**
0	VF Monitoring is not Completed (Default)
1	VF Monitoring is Completed

VFSC_MODE	**VF monitoring mode selection**
00	VF monitoring enable (Default)
01	VF monitoring self-check stage 1, limit low
10	VF monitoring self-check stage 2, normal
11	VF monitoring self-check stage 3, limit high

IMONSC_MODE	**Output Current monitoring mode selection**
00	Output Current monitoring enable (Default)
01	Output Current monitoring self-check stage 1, limit low
10	Output Current monitoring self-check stage 2, normal
11	Output Current monitoring self-check stage 3, limit high

IMON_TOR	Output Current monitoring tolerance setting
0	30% (Default)
1	50%

Table 22 7Fh Output Current Monitoring Selection Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	IMON_START	-	IMON_SEL[5:0]					
Default	0	0	0	0	0	0	0	0

IMON_START	CS channels Output Current Monitoring start
0	CS channels Output Current Monitoring stops (Default)
1	CS channels Output Current Monitoring starts

IMON_SEL	CS channels Output Current Monitoring selection
000000	All channels output current monitoring disables (Default)
000001	SW1_CS1 channel output current monitoring enable
000010	SW1_CS2 channel output current monitoring enable
000011	SW1_CS3 channel output current monitoring enable
000100	SW1_CS4 channel output current monitoring enable
000101	SW1_CS5 channel output current monitoring enable
000110	SW1_CS6 channel output current monitoring enable
000111	SW1_CS7 channel output current monitoring enable
001000	SW1_CS8 channel output current monitoring enable
001001	SW1_CS9 channel output current monitoring enable
001010	SW1_CS10 channel output current monitoring enable
001011	SW1_CS11 channel output current monitoring enable
001100	SW1_CS12 channel output current monitoring enable
001101	SW1_CS13 channel output current monitoring enable
001110	SW1_CS14 channel output current monitoring enable
001111	SW1_CS15 channel output current monitoring enable
010000	SW1_CS16 channel output current monitoring enable
010001	SW1_CS17 channel output current monitoring enable
010010	SW1_CS18 channel output current monitoring enable
100001	SW2_CS1 channel output current monitoring enable
100010	SW2_CS2 channel output current monitoring enable
100011	SW2_CS3 channel output current monitoring enable
100100	SW2_CS4 channel output current monitoring enable
100101	SW2_CS5 channel output current monitoring enable
100110	SW2_CS6 channel output current monitoring enable
100111	SW2_CS7 channel output current monitoring enable
101000	SW2_CS8 channel output current monitoring enable
101001	SW2_CS9 channel output current monitoring enable
101010	SW2_CS10 channel output current monitoring enable
101011	SW2_CS11 channel output current monitoring enable
101100	SW2_CS12 channel output current monitoring enable
101101	SW2_CS13 channel output current monitoring enable
101110	SW2_CS14 channel output current monitoring enable
101111	SW2_CS15 channel output current monitoring enable
110000	SW2_CS16 channel output current monitoring enable

110001	SW2_CS17 channel output current monitoring enable
110010	SW2_CS18 channel output current monitoring enable
Other	invalid

Table 23 80h CS Loop Back test Control Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CSLT_MODE		-	CSLT_TOR[5:0]				
Default	0	0	0	0	0	0	0	0

CSLT_MODE	**CS Loop Back test mode selection**
00	CS loop back test disable (Default)
01	CS loop back self-check, DC low
10	CS loop back self-check, DC high
11	CS loop back test enable

CSLT_TOR	**CS Loop Back test tolerance setting**
00000	12 PWM Clock (Default)
00001	12 PWM Clock
00010	12 PWM Clock
00011	16 PWM Clock
00100	20 PWM Clock
00101	24 PWM Clock
00110	28 PWM Clock
00111	32 PWM Clock
……..	……
11000	100 PWM Clock
11001	104 PWM Clock
11010	108 PWM Clock
11011	112 PWM Clock
11100	116 PWM Clock
11101	120 PWM Clock
11110	124 PWM Clock
11111	128 PWM Clock

Table 24 81h CS Loop Back Test Channel Selection Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CSLT_START	-	CSLT_PWMAT_SEL[5:0]					
Default	0	0	0	0	0	0	0	0

CSLT_START	**CS channels Loop Back test start**
0	CS channels loop back test stops (Default)
1	CS channels loop back test starts

CSLT_PWMAT_SEL	**CS channels Loop Back test selection and PWM active duty readout channel selection**
000000	All channels channel loop back test disables (Default)
000001	SW1_CS1 channel loop back test enable Read SW1_CS1 channel PWM active output duty
000010	SW1_CS2 channel loop back test enable

	Read SW1_CS2 channel PWM active output duty
000011	SW1_CS3 channel loop back test enable
	Read SW1_CS3 channel PWM active output duty
000100	SW1_CS4 channel loop back test enable
	Read SW1_CS4 channel PWM active output duty
000101	SW1_CS5 channel loop back test enable
	Read SW1_CS5 channel PWM active output duty
000110	SW1_CS6 channel loop back test enable
	Read SW1_CS6 channel PWM active output duty
000111	SW1_CS7 channel loop back test enable
	Read SW1_CS7 channel PWM active output duty
001000	SW1_CS8 channel loop back test enable
	Read SW1_CS8 channel PWM active output duty
001001	SW1_CS9 channel loop back test enable
	Read SW1_CS9 channel PWM active output duty
001010	SW1_CS10 channel loop back test enable
	Read SW1_CS10 channel PWM active output duty
001011	SW1_CS11 channel loop back test enable
	Read SW1_CS11 channel PWM active output duty
001100	SW1_CS12 channel loop back test enable
	Read SW1_CS12 channel PWM active output duty
001101	SW1_CS13 channel loop back test enable
	Read SW1_CS13 channel PWM active output duty
001110	SW1_CS14 channel loop back test enable
	Read SW1_CS14 channel PWM active output duty
001111	SW1_CS15 channel loop back test enable
	Read SW1_CS15 channel PWM active output duty
010000	SW1_CS16 channel loop back test enable
	Read SW1_CS16 channel PWM active output duty
010001	SW1_CS17 channel loop back test enable
	Read SW1_CS17 channel PWM active output duty
010010	SW1_CS18 channel loop back test enable
	Read SW1_CS18 channel PWM active output duty
100001	SW2_CS1 channel loop back test enable
	Read SW2_CS1 channel PWM active output duty
100010	SW2_CS2 channel loop back test enable
	Read SW2_CS2 channel PWM active output duty
100011	SW2_CS3 channel loop back test enable
	Read SW2_CS3 channel PWM active output duty
100100	SW2_CS4 channel loop back test enable
	Read SW2_CS4 channel PWM active output duty
100101	SW2_CS5 channel loop back test enable
	Read SW2_CS5 channel PWM active output duty
100110	SW2_CS6 channel loop back test enable
	Read SW2_CS6 channel PWM active output duty
100111	SW2_CS7 channel loop back test enable
	Read SW2_CS7 channel PWM active output duty
101000	SW2_CS8 channel loop back test enable
	Read SW2_CS8 channel PWM active output duty
101001	SW2_CS9 channel loop back test enable

	Read SW2_CS9 channel PWM active output duty
101010	SW2_CS10 channel loop back test enable
	Read SW2_CS10 channel PWM active output duty
101011	SW2_CS11 channel loop back test enable
	Read SW2_CS11 channel PWM active output duty
101100	SW2_CS12 channel loop back test enable
	Read SW2_CS12 channel PWM active output duty
101101	SW2_CS13 channel loop back test enable
	Read SW2_CS13 channel PWM active output duty
101111	SW2_CS14 channel loop back test enable
	Read SW2_CS14 channel PWM active output duty
110000	SW2_CS15 channel loop back test enable
	Read SW2_CS15 channel PWM active output duty
110001	SW2_CS16 channel loop back test enable
	Read SW2_CS16 channel PWM active output duty
110010	SW2_CS17 channel loop back test enable
	Read SW2_CS17 channel PWM active output duty
110011	SW2_CS18 channel loop back test enable
	Read SW2_CS18 channel PWM active output duty
Other	invalid

Table 25 82h Fault Flag Report Control Register 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	TSDF_RE	UVLED_RE	-	SWOC_RE	SWSH_RE	SHORTF_RE	OPENF_RE
Default	-	1	1	-	1	1	1	1

TSDF_RE	**Thermal Shutdown Report**
0	Disable
1	Enable (Default)

UVLED_RE	**VLED under-voltage Detected Report**
0	Disable
1	Enable (Default)

SWOC_RE	**SW Over Current Fault Report**
0	Disable
1	Enable (Default)

SWSH_RE	**SW short to VLED Fault Report**
0	Disable
1	Enable (Default)

SHORTF_RE	**LED Short Report**
0	Disable
1	Enable (Default)

OPENF_RE	**LED Open Report**
0	Disable
1	Enable (Default)

Table 26 83h Fault Flag Report Control Register 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	WDTF2_RE	WDTF1_RE	CRCF_RE	INCKF_RE	SWLTF_RE	CSLTF_RE	VFWDF_RE	IMONF_RE
Default	1	1	1	1	1	1	1	1

WDTF2_RE **Watch Dog Timer 2 Time out Report**
0 Disable
1 Enable (Default)

WDTF1_RE **Communication Watch Dog Timer Time out Report**
0 Disable
1 Enable (Default)

CRCF_RE **CRC Error Report**
0 Disable
1 Enable (Default)

INCKF_RE **Internal Clock Monitoring Fail Report**
0 Disable
1 Enable (Default)

SWLTF_RE **SW Loop Back Test Fail Report**
0 Disable
1 Enable (Default)

CSLTF_RE **CS Channel Loop Back Test Fail Report**
0 Disable
1 Enable (Default)

VFWDF_RE **LED VF Monitoring Fail Report**
0 Disable
1 Enable (Default)

IMON_RE **Output Current Monitoring Fail Report**
0 Disable
1 Enable (Default)

If reporting is enabled, the FAULTB pin actively low when the corresponding flag event happens.

Table 27 84h~88h Color Crossfade Control Register

84h:

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SW1_CS4_CFEN	SW1_CS3_CFEN	SW1_CS2_CFEN	SW1_CS1_CFEN	-	-	MAUL_STP	STP_CON
Default	0	0	0	0	-	-	0	0

SW1_CSy_CFEN **Color crossfade control**
0 SW1_CSy channel Color crossfade function disable (Default)
1 SW1_CSy channel Color crossfade function enable

MAUL_STP **Manual step control**

0 Color crossfade steps hold (Default)

1 Color crossfade steps increase one step

STP_CON **Step mode control**

0 Color crossfade steps increase automatically (Default)

1 Color crossfade steps increase manually by command

85h:

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SW1_CS12_CFEN	SW1_CS11_CFEN	SW1_CS10_CFEN	SW1_CS9_CFEN	SW1_CS8_CFEN	SW1_CS7_CFEN	SW1_CS6_CFEN	SW1_CS5_CFEN
Default	0	0	0	0	0	0	0	0

86h:

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SW2_CS2_CFEN	SW2_CS1_CFEN	SW1_CS18_CFEN	SW1_CS17_CFEN	SW1_CS16_CFEN	SW1_CS15_CFEN	SW1_CS14_CFEN	SW1_CS13_CFEN
Default	0	0	0	0	0	0	0	0

87h:

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SW2_CS10_CFEN	SW2_CS9_CFEN	SW2_CS8_CFEN	SW2_CS7_CFEN	SW2_CS6_CFEN	SW2_CS5_CFEN	SW2_CS4_CFEN	SW2_CS3_CFEN
Default	0	0	0	0	0	0	0	0

88h:

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SW2_CS18_CFEN	SW2_CS17_CFEN	SW2_CS16_CFEN	SW2_CS15_CFEN	SW2_CS14_CFEN	SW2_CS13_CFEN	SW2_CS12_CFEN	SW2_CS11_CFEN
Default	0	0	0	0	0	0	0	0

SW1_CSy_CFEN **Color crossfade control**

0 SW1_CSy channel Color crossfade function disable (Default)

1 SW1_CSy channel Color crossfade function enable one time

SW2_CSy_CFEN **Color crossfade control**

0 SW2_CSy channel Color crossfade function disable (Default)

1 SW2_CSy channel Color crossfade function enable one time

Table 28 89h Color Crossfade Steps and PWM Count Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		STP_N				STP_DT		
Default	0	0	0	0	0	0	0	0

STP_N	Crossfade steps number between starting and ending time
000	128 (Default)
001	8
010	16
011	32
100	64
101	256
110	512
111	1024

STP_DT	Crossfade Duration Time of Each Step
000	1 PWM Frame (Default)
001	2 PWM Frame
010	3 PWM Frame
011	4 PWM Frame
100	5 PWM Frame
101	6 PWM Frame
110	7 PWM Frame
111	8 PWM Frame

Table 29 One PWM Frame Time (SW1 and SW2 are all enable, two scans)

PWM Mode	32MHz	16MHz	8MHz	4MHz
16-bit	4.096ms	8.192ms	16.38ms	32.77ms
14-bit + 2-bit	4.096ms	8.192ms	16.38ms	32.77ms
13-bit + 3-bit	4.096ms	8.192ms	16.38ms	32.77ms
8-bit + 8-bit	4.096ms	8.192ms	16.38ms	32.77ms

Table 30 8Ah Communication Watchdog Timer Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CMTWT_EN	CMTWT_SET			-		-	
Default	1	0	1	1	0	0	0	0

LumiBus bus must complete correct operation (read/write/response) within WDT specified time frame. If this WDT timer expired without completion of the operation, a WDTF1 flag will be set to indicate that there is some communication error. Such scenario could occur, for instance, LumiBus host needs to periodically poll status of 3105 devices and if LumiBus is idled for too long without accessing any 3105 devices, exceeding this specified time frame, this error flag will also be raised. After this flag is raised, the interface state machine is reset to the normal state, ready for the next host communication.

Read Watchdog Timer is used when the host attempts to read 3105 registers. If the read access behaves normally, this Read Watchdog Timer is reset to its initial state, waiting for the next read access command. If, however, after the pre-specified time frame there is still no response, this error flag will be raised and the interface read state machine is reset to the normal state, ready for the next host communication. This could occur, for instance, when the host attempts to read a non-existing device address due to, e.g., a corrupted signal on the LumiBus.

CMTWT_EN	Communication Watchdog Timer Control
0	Disable
1	Enable the Communication Watchdog Timer (Default)

CMTWT_SET	Communication Watchdog Time out Select(64M)
000	8ms
001	16ms
010	32ms
011	64ms (Default)

100	128ms
101	256ms
110	512ms
111	1024ms

Table 31 8Bh Watchdog Timer 2 Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	WDT2_EN	WDT2CLR	WDT2_MAX			WDT2_MIN		
Default	0	0	0	1	1	0	0	0

WDT2_EN **Watchdog 2 Counter Enable**

0	Disable Watchdog 2 (Default)
1	Enable Watchdog 2

WDT2CLR **Watchdog2 Counter Clear**

Writing “1” to WDT2CLR clears the watchdog 2 count to 0. It is self-cleared with hardware.

WDT2MAX **Maximum Timeout Value for Watchdog Timer 2**

000	8ms
001	16ms
010	32ms
011	64ms (Default)
100	128ms
101	256ms
110	512ms
111	1024ms

WDTMAX holds the maximum timeout value for watchdog timer 2. When the counter reaches WDT2 timeout value, a fault flag is generated.

WDT2MIN **Minimum Timeout Value for Watchdog Timer 2**

000	8ms (Default)
001	16ms
010	32ms
011	64ms
100	128ms
101	256ms
110	512ms
111	1024ms

WDTMIN holds the minimum timeout value for watchdog timer 2. If WDT2 is cleared before reaching WDT2MIN, a fault flag is also generated.

Table 32 8Ch Temperature Compensation Control and Steps Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	TCLOCKF			-	-	TC_STP		TC_EN
Default	0	0	0	0	0	0	0	0

TC_STP **Temperature Compensation Steps**

00	8°C for each step (Default)
01	2°C for each step
10	4°C for each step
11	16°C for each step

TC_EN **Temperature Compensation Enable**

0	Temperature compensation disable (Default)
1	Temperature compensation enable

Table 33 8Dh Temperature Compensation Red LED channels Calibrate Ratio Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	R_CALI [7:0]							
Default	1	1	1	1	1	1	1	1

Table 34 8Eh Temperature Compensation Green LED channels Calibrate Ratio Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	G_CALI [7:0]							
Default	1	1	1	1	1	1	1	1

Table 35 8Fh Temperature Compensation Blue LED channels Calibrate Ratio Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	B_CALI [7:0]							
Default	1	1	1	1	1	1	1	1

R/G/B_CALI	Temperature Compensation Red LED channels Calibrate
00001100	4.7%
00011001	9.8%
00100110	14.8%
00110011	19.9%
00111111	24.6%
01001100	29.7%
01011001	34.8%
01100110	39.8%
01110011	44.9%
10000000	50.0%
10001100	54.7%
10011001	59.8%
10100110	64.8%
10110011	69.9%
11000000	75.0%
11000000	79.7%
11011001	84.8%
11100110	89.8%
11110011	94.9%
11111111	99.6% (Default)

When CALI_EN (at 70h: PWM Output multiply Calibrate function enabled), PWM output= PWM Control register value*100%*CALI ratio and if PWM register is set to the maximum value of 0xFFFF and the function is enabled, the maximum PWM output value is 0xFEFF when CALI_EN =1 or TC_EN = 1.

Table 36 90h~92h Temperature Compensation Red LED channels Percentage Register
90h:

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	TC_POL_R1	N_R1[5:0]					
Default	0	0	0	0	0	0	0	0

91h:

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	TC_POL_R2	N_R2[5:0]					
Default	0	0	0	0	0	0	0	0

92h:

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	TC_POL_R3	N_R3[5:0]					
Default	0	0	0	0	0	0	0	0

N_R1[5:0]: Red LED channels temperature compensation percentage at -40°C ~15°C

N_R2[5:0]: Red LED channels temperature compensation percentage at 16°C ~70°C

N_R3[5:0]: Red LED channels temperature compensation percentage at 71°C ~125℃

TC_POL_Rx	**Red LED channels Temperature Compensation Polarity selection**
0	Positive (Default, positive compensation with temperature increases at -40°C ~125°C)
1	Negative (negative compensation with temperature increases at -40°C ~125°C)

Table 37 93h~95h Temperature Compensation Green LED channels Percentage Register

93h:

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	TC_POL_G1	N_G1[5:0]					
Default	0	0	0	0	0	0	0	0

94h:

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	TC_POL_G2	N_G2[5:0]					
Default	0	0	0	0	0	0	0	0

95h:

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	TC_POL_G3	N_G3[5:0]					
Default	0	0	0	0	0	0	0	0

N_G1[5:0]: Green LED channels temperature compensation percentage at -40°C ~15°C

N_G2[5:0]: Green LED channels temperature compensation percentage at 16°C ~70°C

N_G3[5:0]: Green LED channels temperature compensation percentage at 71°C ~125°C

TC_POL_Gx	**Green LED channels Temperature Compensation Polarity selection**
0	Positive (Default, positive compensation with temperature increases at -40°C ~125°C)
1	Negative (negative compensation with temperature increases at -40°C ~125°C)

Table 38 96h~98h Temperature Compensation Blue LED channels Percentage Register

96h:

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	TC_POL_B1	N_B1[5:0]					
Default	0	0	0	0	0	0	0	0

97h:

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	TC_POL_B2	N_B2[5:0]					
Default	0	0	0	0	0	0	0	0

98h:

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	TC_POL_B3	N_B3[5:0]					
Default	0	0	0	0	0	0	0	0

N_B1[5:0]: Blue LED channels temperature compensation percentage at -40°C ~15°C

N_B2[5:0]: Blue LED channels temperature compensation percentage at 16°C ~70°C

N_B3[5:0]: Blue LED channels temperature compensation percentage at 71°C ~125°C

TC_POL_Bx	Blue LED channels Temperature Compensation Polarity selection
0	Positive (Default, positive compensation with temperature increases at -40°C ~125°C)
1	Negative (negative compensation with temperature increases at -40°C ~125°C)

Table 39 99h~AAh ADC VF reference for SW1_CSy Register

99h: SW1_CS1 channel ADC VF reference Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-		VF_REF_SW1_CS1[5:0]					
Default	0	0	0	0	0	0	0	0

9Ah: SW1_CS2 channel ADC VF reference Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-		VF_REF_SW1_CS2[5:0]					
Default	0	0	0	0	0	0	0	0

9Bh: SW1_CS3 channel ADC VF reference Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-		VF_REF_SW1_CS3[5:0]					
Default	0	0	0	0	0	0	0	0

9Ch: SW1_CS4 channel ADC VF reference Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-		VF_REF_SW1_CS4[5:0]					
Default	0	0	0	0	0	0	0	0

9Dh: SW1_CS5 channel ADC VF reference Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-		VF_REF_SW1_CS5[5:0]					
Default	0	0	0	0	0	0	0	0

9Eh: SW1_CS6 channel ADC VF reference Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-		VF_REF_SW1_CS6[5:0]					
Default	0	0	0	0	0	0	0	0

9Fh: SW1_CS7 channel ADC VF reference Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-		VF_REF_SW1_CS7[5:0]					
Default	0	0	0	0	0	0	0	0

A0h: SW1_CS8 channel ADC VF reference Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-		VF_REF_SW1_CS8[5:0]					
Default	0	0	0	0	0	0	0	0

A1h: SW1_CS9 channel ADC VF reference Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-		VF_REF_SW1_CS9[5:0]					
Default	0	0	0	0	0	0	0	0

A2h: SW1_CS10 channel ADC VF reference Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-		VF_REF_SW1_CS10[5:0]					
Default	0	0	0	0	0	0	0	0

A3h: SW1_CS11 channel ADC VF reference Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-		VF_REF_SW1_CS11[5:0]					
Default	0	0	0	0	0	0	0	0

A4h: SW1_CS12 channel ADC VF reference Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-		VF_REF_SW1_CS12[5:0]					
Default	0	0	0	0	0	0	0	0

A5h: SW1_CS13 channel ADC VF reference Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-		VF_REF_SW1_CS13[5:0]					
Default	0	0	0	0	0	0	0	0

A6h: SW1_CS14 channel ADC VF reference Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-		VF_REF_SW1_CS14[5:0]					
Default	0	0	0	0	0	0	0	0

A7h: SW1_CS15 channel ADC VF reference Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-		VF_REF_SW1_CS15[5:0]					
Default	0	0	0	0	0	0	0	0

A8h: SW1_CS16 channel ADC VF reference Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-		VF_REF_SW1_CS16[5:0]					
Default	0	0	0	0	0	0	0	0

A9h: SW1_CS17 channel ADC VF reference Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-		VF_REF_SW1_CS17[5:0]					
Default	0	0	0	0	0	0	0	0

AAh: SW1_CS18 channel ADC VF reference Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-		VF_REF_SW1_CS18[5:0]					
Default	0	0	0	0	0	0	0	0

VF_REF_SW1_CSy set SW1_CSy channels ADC VF reference, use for trim VF ADC value.

Table 40 ABh~BCh ADC VF reference for SW2_CSy Register

ABh: SW2_CS1 channel ADC VF reference Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-		VF_REF_SW2_CS1[5:0]					
Default	0	0	0	0	0	0	0	0

ACh: SW2_CS2 channel ADC VF reference Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-		VF_REF_SW2_CS2[5:0]					
Default	0	0	0	0	0	0	0	0

ADh: SW2_CS3 channel ADC VF reference Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-		VF_REF_SW2_CS3[5:0]					
Default	0	0	0	0	0	0	0	0

AEh: SW2_CS4 channel ADC VF reference Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-		VF_REF_SW2_CS4[5:0]					
Default	0	0	0	0	0	0	0	0

AFh: SW2_CS5 channel ADC VF reference Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-		VF_REF_SW2_CS5[5:0]					
Default	0	0	0	0	0	0	0	0

B0h: SW2_CS6 channel ADC VF reference Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-		VF_REF_SW2_CS6[5:0]					
Default	0	0	0	0	0	0	0	0

B1h: SW2_CS7 channel ADC VF reference Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-		VF_REF_SW2_CS7[5:0]					
Default	0	0	0	0	0	0	0	0

B2h: SW2_CS8 channel ADC VF reference Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-		VF_REF_SW2_CS8[5:0]					
Default	0	0	0	0	0	0	0	0

B3h: SW2_CS9 channel ADC VF reference Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-		VF_REF_SW2_CS9[5:0]					
Default	0	0	0	0	0	0	0	0

B4h: SW2_CS10 channel ADC VF reference Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-		VF_REF_SW2_CS10[5:0]					
Default	0	0	0	0	0	0	0	0

B5h: SW2_CS11 channel ADC VF reference Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-		VF_REF_SW2_CS11[5:0]					
Default	0	0	0	0	0	0	0	0

B6h: SW2_CS12 channel ADC VF reference Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-		VF_REF_SW2_CS12[5:0]					
Default	0	0	0	0	0	0	0	0

B7h: SW2_CS13 channel ADC VF reference Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-		VF_REF_SW2_CS13[5:0]					
Default	0	0	0	0	0	0	0	0

B8h: SW2_CS14 channel ADC VF reference Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-		VF_REF_SW2_CS14[5:0]					
Default	0	0	0	0	0	0	0	0

B9h: SW2_CS15 channel ADC VF reference Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-		VF_REF_SW2_CS15[5:0]					
Default	0	0	0	0	0	0	0	0

BAh: SW2_CS16 channel ADC VF reference Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-		VF_REF_SW2_CS16[5:0]					
Default	0	0	0	0	0	0	0	0

BBh: SW2_CS17 channel ADC VF reference Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-		VF_REF_SW2_CS17[5:0]					
Default	0	0	0	0	0	0	0	0

BCh: SW2_CS18 channel ADC VF reference Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-		VF_REF_SW2_CS18[5:0]					
Default	0	0	0	0	0	0	0	0

VF_REF_SW2_CSy: set SW2_CSy channels ADC VF reference, use for trim VF ADC value.

Table 41 BDh ADC Control Register1 (ADC)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	TSW1_EN	ADTC					
Default	0	0	0	0	0	0	0	0

When the on-die ADC is to read on-die temperature sensor, bandgap, VSW1 and VSW2 pin, the ADC samples 2/4/8 times (selected by ADCSH[1:0] bits) to get the average data.

When the on-die ADC is to read VOUT and VF values, it samples once per PWM period for 1/2/4/8 times (selected by ADCCYC_T) to get the average data. When the ADC is to sample VOUT and VF, the minimum PWM width is limited by the minimum ADC sampling time (selected by ADC_CLK[1:0] bits and ADCSH[1:0] bits). When PWM width is less than this minimum sampling time, the result is not counted for that PWM period. If the PWM width is shorter than this minimum sampling time for a long period of time, the average reading cannot be finalized. In that case, assuming that this measurement is for temperature compensation, there is no need to perform temperature compensation since the LED temperature is assumed to be low, therefore, there is no need to do any temperature compensation, e.g., lower PWM duty, hence less heat will be generated.

TSW1_EN	**SW1 ADC Measurement enable**
0	ADC measure SW2's LED VOUT or LED VF (Default)
1	ADC measure SW1's LED VOUT or LED VF

ADTC	**ADC Measurement Target**
000000	No ADC measurement (Default)
000001	On-die temperature sensor
000010	Bandgap

000011	VSW1
000100	VSW2
000101	VLED
000110	V50
000111	NTC or PTC measurement (only single sampling)
001000	No ADC measurement
001001	CS1-R1 LED VOUT
001010	CS4-R2 LED VOUT
001011	CS7-R3 LED VOUT
001100	CS10-R4 LED VOUT
001101	CS13-R5 LED VOUT
001110	CS16-R6 LED VOUT
001111	No ADC measurement
010000	No ADC measurement
010001	CS2-G1 LED VOUT
010010	CH5-G2 LED VOUT
010011	CH8-G3 LED VOUT
010100	CH11-G4 LED VOUT
010101	CH14-G5 LED VOUT
010110	CS17-G6 LED VOUT
010111	No ADC measurement
011000	No ADC measurement
011001	CS3-B1 LED VOUT
011010	CS6-B2 LED VOUT
011011	CS9-B3 LED VOUT
011100	CS12-B4 LED VOUT
011101	CS15-B5 LED VOUT
011110	CS18-B6 LED VOUT
011111	No ADC measurement
100000	No ADC measurement
100001	CS1-R1 LED VF (Difference value with power supply and VOUT)
100010	CS4-R2 LED VF
100011	CS7-R3 LED VF
100100	CS10-R4 LED VF
100101	CS13-R5 LED VF
100110	CS16-R6 LED VF
100111	No ADC measurement
101000	No ADC measurement
101001	CS2-G1 LED VF
101010	CS5-G2 LED VF
101011	CS8-G3 LED VF
101100	CS11-G4 LED VF
101101	CS14-G5 LED VF
101110	CS17-G6 LED VF
101111	No ADC measurement
110000	No ADC measurement
110001	CS3-B1 LED VF
110010	CS6-B2 LED VF
110011	CS9-B3 LED VF
110100	CS12-B4 LED VF

110101 CS15-B5 LED VF
110110 CS18-B6 LED VF
111111 DCFB_DET, ADC measures all the 36 channels output voltage, stores the minimum output voltage to EBh register.

Table 42 BEh ADC Control Register2 (ADC)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	ADCCYC_F	SADC	ADCCYC	AD_CEN	ADC_CLK		ADCSH	
Default	0	0	0	0	0	0	1	0

ADCCYC_F Effective Reading
0 ADC sampling in progress, ADCR is not valid (Default)
1 ADC sampling finished, ADCR is valid reading for host

SADC Start ADC Measurement
0 ADC measurement stops (Default)
1 ADC measurement starts

ADCCYC ADC Sampling Mode
0 ADC Cycle sampling (Default)
1 ADC single sampling

ADC_EN ADC Enable
0 Disable (Default)
1 Enable

ADC_CLK ADC Frequency
00 4MHz (Default)
01 2MHz
10 1MHz
11 0.5MHz

ADCSH ADC Sample Hold Time Select
00/01 ADC sample hold time = 2 ADC CLK
10 ADC sample hold time = 4 ADC CLK (Default)
11 ADC sample hold time = 8 ADC CLK

To achieve more accurate data acquisition, it is recommended that the ADC clock (ADC_CLK) be set to 1 MHz, and the ADC sample hold time (ADCSH) be configured as 4 ADC CLK.

Table 43 BFh ADC Control Register3 (ADC)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	VF_N		ADCCYC_T		ADJEN
Default	0	0	0	0	0	0	1	0

VF_N LED number selection of VF ADC Measurement
00/11 1 LED connect (Default)
01 2 LEDs in series
10 3 LEDs in series

ADCCYC_T	ADC Cycle Sampling Period
00	ADC Cycle sampling for 1 PWM cycles
01	ADC Cycle sampling for 2 PWM cycles (Default)
10	ADC Cycle sampling for 4 PWM cycles
11	ADC Cycle sampling for 8 PWM cycles

ADJEN	Auto ADC Gain and Offset Adjustment
0	Disable (Default)
1	Enable

Table 44 C0h~D1h VF ADC Value at Room Temperature for SW1_CSy Register

C0h: Store SW1_CS1 channel VF ADC at Room Temperature Register

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VF_RT_SW1_CS1[7:0]							
Default	0	0	0	0	0	0	0	0

C1h: Store SW1_CS2 channel VF ADC at Room Temperature Register

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VF_RT_SW1_CS2[7:0]							
Default	0	0	0	0	0	0	0	0

C2h: Store SW1_CS3 channel VF ADC at Room Temperature Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	VF_RT_SW1_CS3[7:0]							
Default	0	0	0	0	0	0	0	0

C3h: Store SW1_CS4 channel VF ADC at Room Temperature Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	VF_RT_SW1_CS4[7:0]							
Default	0	0	0	0	0	0	0	0

C4h: Store SW1_CS5 channel VF ADC at Room Temperature Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	VF_RT_SW1_CS5[7:0]							
Default	0	0	0	0	0	0	0	0

C5h: Store SW1_CS6 channel VF ADC at Room Temperature Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	VF_RT_SW1_CS6[7:0]							
Default	0	0	0	0	0	0	0	0

C6h: Store SW1_CS7 channel VF ADC at Room Temperature Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	VF_RT_SW1_CS7[7:0]							
Default	0	0	0	0	0	0	0	0

C7h: Store SW1_CS8 channel VF ADC at Room Temperature Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	VF_RT_SW1_CS8[7:0]							
Default	0	0	0	0	0	0	0	0

C8h: Store SW1_CS9 channel VF ADC at Room Temperature Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	VF_RT_SW1_CS9[7:0]							
Default	0	0	0	0	0	0	0	0

C9h: Store SW1_CS10 channel VF ADC at Room Temperature Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	VF_RT_SW1_CS10[7:0]							
Default	0	0	0	0	0	0	0	0

CAh: Store SW1_CS11 channel VF ADC at Room Temperature Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	VF_RT_SW1_CS11[7:0]							
Default	0	0	0	0	0	0	0	0

CBh: Store SW1_CS12 channel VF ADC at Room Temperature Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	VF_RT_SW1_CS12[7:0]							
Default	0	0	0	0	0	0	0	0

CCh: Store SW1_CS13 channel VF ADC at Room Temperature Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	VF_RT_SW1_CS13[7:0]							
Default	0	0	0	0	0	0	0	0

CDh: Store SW1_CS14 channel VF ADC at Room Temperature Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	VF_RT_SW1_CS14[7:0]							
Default	0	0	0	0	0	0	0	0

CEh: Store SW1_CS15 channel VF ADC at Room Temperature Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	VF_RT_SW1_CS15[7:0]							
Default	0	0	0	0	0	0	0	0

CFh: Store SW1_CS16 channel VF ADC at Room Temperature Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	VF_RT_SW1_CS16[7:0]							
Default	0	0	0	0	0	0	0	0

D0h: Store SW1_CS17 channel VF ADC at Room Temperature Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	VF_RT_SW1_CS17[7:0]							
Default	0	0	0	0	0	0	0	0

D1h: Store SW1_CS18 channel VF ADC at Room Temperature Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	VF_RT_SW1_CS18[7:0]							
Default	0	0	0	0	0	0	0	0

VF_RT_SW1_CSy: used to store the ADC value of VF at room temperature in SW1_CSy channel, as a benchmark for temperature compensation.

Table 45 D2h~E3h VF ADC Value at Room Temperature for SW2_CSy Register

D2h: Store SW2_CS1 channel VF ADC at Room Temperature Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	VF_RT_SW2_CS1[7:0]							
Default	0	0	0	0	0	0	0	0

D3h: Store SW2_CS2 channel VF ADC at Room Temperature Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	VF_RT_SW2_CS2[7:0]							
Default	0	0	0	0	0	0	0	0

D4h: Store SW2_CS3 channel VF ADC at Room Temperature Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	VF_RT_SW2_CS3[7:0]							
Default	0	0	0	0	0	0	0	0

D5h: Store SW2_CS4 channel VF ADC at Room Temperature Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	VF_RT_SW2_CS4[7:0]							
Default	0	0	0	0	0	0	0	0

D6h: Store SW2_CS5 channel VF ADC at Room Temperature Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	VF_RT_SW2_CS5[7:0]							
Default	0	0	0	0	0	0	0	0

D7h: Store SW2_CS6 channel VF ADC at Room Temperature Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	VF_RT_SW2_CS6[7:0]							
Default	0	0	0	0	0	0	0	0

D8h: Store SW2_CS7 channel VF ADC at Room Temperature Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	VF_RT_SW2_CS7[7:0]							
Default	0	0	0	0	0	0	0	0

D9h: Store SW2_CS8 channel VF ADC at Room Temperature Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	VF_RT_SW2_CS8[7:0]							
Default	0	0	0	0	0	0	0	0

DAh: Store SW2_CS9 channel VF ADC at Room Temperature Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	VF_RT_SW2_CS9[7:0]							
Default	0	0	0	0	0	0	0	0

DBh: Store SW2_CS10 channel VF ADC at Room Temperature Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	VF_RT_SW2_CS10[7:0]							
Default	0	0	0	0	0	0	0	0

DCh: Store SW2_CS11 channel VF ADC at Room Temperature Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	VF_RT_SW2_CS11[7:0]							
Default	0	0	0	0	0	0	0	0

DDh: Store SW2_CS12 channel VF ADC at Room Temperature Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	VF_RT_SW2_CS12[7:0]							
Default	0	0	0	0	0	0	0	0

DEh: Store SW2_CS13 channel VF ADC at Room Temperature Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	VF_RT_SW2_CS13[7:0]							
Default	0	0	0	0	0	0	0	0

DFh: Store SW2_CS14 channel VF ADC at Room Temperature Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	VF_RT_SW2_CS14[7:0]							
Default	0	0	0	0	0	0	0	0

E0h: Store SW2_CS15 channel VF ADC at Room Temperature Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	VF_RT_SW2_CS15[7:0]							
Default	0	0	0	0	0	0	0	0

E1h: Store SW2_CS16 channel VF ADC at Room Temperature Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	VF_RT_SW2_CS16[7:0]							
Default	0	0	0	0	0	0	0	0

E2h: Store SW2_CS17 channel VF ADC at Room Temperature Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	VF_RT_SW2_CS17[7:0]							
Default	0	0	0	0	0	0	0	0

E3h: Store SW2_CS18 channel VF ADC at Room Temperature Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	VF_RT_SW2_CS18[7:0]							
Default	0	0	0	0	0	0	0	0

VF_RT_SW2_CSy: used to store the ADC value of VF at room temperature in SW2_CSy channel, as a benchmark for temperature compensation.

Table 46 E4h On Die Temperature Sensor Room Temperature Value Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	TS_RT							
Default	0	0	0	0	0	0	0	0

TS_RT: used to store ADC values of on temperature die sensor at room temperature as a benchmark for temperature compensation.

Table 47 E5h On Die Temperature Sensor Reference Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					VTS_REF[3:0]			
Default	0	0	0	0	0	0	0	0

Table 48 E6h ADC Measurement Result Register ADC Single Sampling (ADCR1H, Read only)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	D11	D10	D9	D8	D7	D6	D5	D4
Default	-	-	-	-	-	-	-	-

Table 49 E7h ADC Measurement Result Register ADC single sampling (ADCR1L, Read only)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	D3	D2	D1	D0
Default	-	-	-	-	-	-	-	-

Store the ADC result of On-die temperature sensor, bandgap, SW1/SW2, VLED, V50 voltage, channels output voltage. These are single samplings.

Table 50 E8h ADC Measurement Result Register ADC cycle sampling (ADCR2H, Read only)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	D11	D10	D9	D8	D7	D6	D5	D4
Default	-	-	-	-	-	-	-	-

Table 51 E9h ADC Measurement Result Register ADC cycle sampling (ADCR2L, Read only)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	D3	D2	D1	D0
Default	-	-	-	-	-	-	-	-

LED's VF voltage is measured by ADC cycle sampling, 8+4-bit ADC measurement result. There are a total of 36 channels, when command to measure LED's VF, the ADC will measure one of 36 channels' VF voltage and store the results in E8h/E9h registers.

Table 52 EAh On-die Temperature Sensor Real Time High 8bit Value by ADC cycle sampling (Read only)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	D11	D10	D9	D8	D7	D6	D5	D4
Default	-	-	-	-	-	-	-	-

Table 53 EBh DCFB Result Register (Read only)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DCFB_F	VCH_MIN[6:0]						
Default	0	1	1	1	1	1	1	1

DCFB_ F **DCFB Calculation Completed**

0 DCFB calculation is not Completed (Default)

1 DCFB calculation is Completed

VCH_MIN **Minimum VOUT ADC Value**

The minimum value of the 36 channels' output voltage (voltage of SWx_CSy, where x = 1,2, y = 1~18).

Table 54 ECh Read PWM duty after Temperature Compensation or Crossfade channel Select Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	PWM_RD_SEL[5:0]					
Default	0	0	0	0	0	0	0	0

PWM_RD_SEL **Read PWM duty Value Channel Selection**

000001 Read SW1_CS1 channel PWM (after TC or CF) duty
000010 Read SW1_CS2 channel PWM (after TC or CF) duty
000011 Read SW1_CS3 channel PWM (after TC or CF) duty
000100 Read SW1_CS4 channel PWM (after TC or CF) duty
000101 Read SW1_CS5 channel PWM (after TC or CF) duty
000110 Read SW1_CS6 channel PWM (after TC or CF) duty
000111 Read SW1_CS7 channel PWM (after TC or CF) duty
001000 Read SW1_CS8 channel PWM (after TC or CF) duty
001001 Read SW1_CS9 channel PWM (after TC or CF) duty
001010 Read SW1_CS10 channel PWM (after TC or CF) duty
001011 Read SW1_CS11 channel PWM (after TC or CF) duty
001100 Read SW1_CS12 channel PWM (after TC or CF) duty
001101 Read SW1_CS13 channel PWM (after TC or CF) duty
001110 Read SW1_CS14 channel PWM (after TC or CF) duty
001111 Read SW1_CS15 channel PWM (after TC or CF) duty
010000 Read SW1_CS16 channel PWM (after TC or CF) duty
010001 Read SW1_CS17 channel PWM (after TC or CF) duty
010010 Read SW1_CS18 channel PWM (after TC or CF) duty
100001 Read SW2_CS1 channel PWM (after TC or CF) duty
100010 Read SW2_CS2 channel PWM (after TC or CF) duty
100011 Read SW2_CS3 channel PWM (after TC or CF) duty
100100 Read SW2_CS4 channel PWM (after TC or CF) duty
100101 Read SW2_CS5 channel PWM (after TC or CF) duty

100110	Read SW2_CS6 channel PWM (after TC or CF) duty
100111	Read SW2_CS7 channel PWM (after TC or CF) duty
101000	Read SW2_CS8 channel PWM (after TC or CF) duty
101001	Read SW2_CS9 channel PWM (after TC or CF) duty
101010	Read SW2_CS10 channel PWM (after TC or CF) duty
101011	Read SW2_CS11 channel PWM (after TC or CF) duty
101100	Read SW2_CS12 channel PWM (after TC or CF) duty
101101	Read SW2_CS13 channel PWM (after TC or CF) duty
101110	Read SW2_CS14 channel PWM (after TC or CF) duty
101111	Read SW2_CS15 channel PWM (after TC or CF) duty
110000	Read SW2_CS16 channel PWM (after TC or CF) duty
110001	Read SW2_CS17 channel PWM (after TC or CF) duty
110010	Read SW2_CS18 channel PWM (after TC or CF) duty
Other	invalid

Table 55 EDh~EEh Read PWM_L duty after Temperature Compensation or crossfade (Read only), select by ECh (PWM_RD_SEL[5:0]) Register

EDh: Read PWM_L duty after Temperature Compensation or crossfade

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	D7	D6	D5	D4	D3	D2	D1	D0
Default	0	0	0	0	0	0	0	0

EEh: Read PWM_H duty after Temperature Compensation or crossfade

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	D15	D14	D13	D12	D11	D10	D9	D8
Default	0	0	0	0	0	0	0	0

Table 56 EFh PWM data update Register (Write only)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	-	-	UPDATE
Default	0	0	0	0	0	0	0	0

When writing 0x01 to EFh register, update the PWM register values to all channels.

Table 57 F0h Reset Register (Write only)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	-	-	-
Default	1	1	1	1	1	1	1	1

When writing 0xC5 to F0h register, reset all Page 0 registers and Page1 registers to default values, excluding the PWR bit in F4h.

Table 58 F1h OTP Control Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	p1	p0	OTP_CMD		OTP_SEL			
Default	1	0	0	0	0	0	0	0

There are select 3 OTP Zone$_X$ bits, two OTP operation bits and two parity bits.
The parity bits for the OTP control byte are calculated with the equations below:

p[1] = ~(OTP_SEL [1] ^ OTP_SEL [3] ^ OTP_CMD [0] ^ OTP_CMD [1])
p[0] = OTP_SEL [0] ^ OTP_SEL [1] ^ OTP_SEL [2] ^ OTP_CMD [0]

OTP_CMD	OTP Operation Command
01	OTP write operation
11	OTP read operation
Other	No allowed

OTP_SEL	OTP Zone Selection
0010	Select OTP Zone B
0100	Select OTP Zone C
0101	Select OTP Zone D
Other	No operation

Table 59 F2h Read PWM_L active output duty after update (PWM_L, Read only), select by 81h (CSLT_PWMAT _SEL[5:0]) register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	D7	D6	D5	D4	D3	D2	D1	D0
Default	0	0	0	0	0	0	0	0

Table 60 F3h Read PWM_H active output duty after update (PWM_H, Read only), select by 81h (CSLT_PWMAT _SEL[5:0]) register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	D15	D14	D13	D12	D11	D10	D9	D8
Default	0	0	0	0	0	0	0	0

Table 61 F4h PWRST Power Status and Communication Configuration Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	ACKSEL [1:0]		PWR
Default	0	0	0	0	0	0	0	0

PWR	Power Reset
0	A power cycle has occurred since the last write to a “1”
1	No power cycle has occurred since the last write to a “1”

This bit is reset to 0 upon power-up (released from UVLO). It may be written to a “1” by the host MCU. Reading this bit allows the host MCU to detect if there has been a power cycle. Note that the Registers Reset Command cannot reset this bit.

ACKSEL	Acknowledge Data Select
00	Disable, No acknowledge is transmitted following successful received writes (default)
01	Return 0x7F, D3 =1: 1 byte acknowledge
10	Return ACK_DATA, D3=1: 1 byte acknowledge
11	Return ACK_DATA+CRC byte, D3=0: 2 bytes acknowledge

ACKSEL	ACK_DATA				
[1:0]	D7:D4	D3	D2	D1	D0
10	0111	1	-	0: Normal 1: One of Fault Flag Register 2 occurred (Page 1:02h)	0: Normal 1: One of Fault Flag Register 1 occurred (Page 1:01h)
11		0			

D1=0, D0=0 Normal
D1=0, D0=1 One of Fault Flag Register 1 occurred (Page 1:01h)

D1=1, D0=0 One of Fault Flag Register 2 occurred (Page 1:02h)
D1=1, D0=1 One of Fault Flag Register 1 or 2 occurred
Other Invalid

10.2.2 PAGE 1 (01H~22H): FAULT FLAG REGISTER MAPPING

Table 62 01h Fault Flag Register 1 (Read and Write, Clear after write "0")

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	TSDF	UVLEDF	-	SWOCF	SWSHF	SHORTF	OPENF
Default	0	0	0	0	0	0	0	0

TSDF **Thermal Shutdown Flag (Clear after write "0")**
1 Thermal shutdown occurred
0 Normal
When a fault occurs, current source is shut off until fault condition is removed.

UVLEDF **VLED under-voltage detected (Clear after write "0")**
1 VLED under-voltage occurred
0 Normal

SWOCF **SW over current occurred (Clear after write "0")**
1 SW1 or SW2 over current occurred
0 Normal

SWSHF **SW short to VLED occurred (Clear after write "0")**
1 SW1 or SW2 short to VLED occurred
0 Normal

SHORTF **LED Short Flag (Clear after write "0")**
1 At least one out of LEDs is short
0 Normal

OPENF **LED Open Flag (Clear after write "0")**
1 At least one out of LEDs is open
0 Normal

Table 63 02h Fault Flag Register 2 (Read and Write, Clear after write "0")

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	WDTF2	WDTF1	CRCF	INCKF	SWLTF	CSLTF	VFWDF	IMONF
Default	0	0	0	0	0	0	0	0

WDTF2 **Watch dog timer 2 time out (Clear after write "0")**
1 watch dog timer 2 timer out flag
0 Normal

WDTF1 **Communication Watch dog timer time out (Clear after write "0")**
1 Communication watch dog timer timed out flag
0 Normal

CRCF **CRC error Flag (Clear after write "0")**

1 Communication checksum error occurred

0 Normal

When bandwidth allowed, check this flag after writing operation to ensure correct transmission of data.

INCKF **Internal PWM Clock Monitoring Fail (Clear after write "0")**

1 Internal PWM clock has no frequency output

0 Normal

SWLTF **SW Loop Back Test Fail (Clear after write "0")**

1 At least one switch's loop back test fail

0 Normal

CSLTF **CS Channel Loop Back Test Fail (Clear after write "0")**

1 At least one channel's loop back test fail

0 Normal

VFWDF **LED VF Monitoring Fail (Clear after write "0")**

1 At least one channel's LED VF voltage out of monitor limit

0 Normal

IMONF **Output Current Monitoring Fail (Clear after write "0")**

1 At least one channel's output current out of monitor limit

0 Normal

Table 64 03h~07h Open/Short Detect and SW short Result Register (Read Only)

03h

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SW1_CS8_OPEN	SW1_CS7_OPEN	SW1_CS6_OPEN	SW1_CS5_OPEN	SW1_CS4_OPEN	SW1_CS3_OPEN	SW1_CS2_OPEN	SW1_CS1_OPEN
Default	0	0	0	0	0	0	0	0

04h

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SW1_CS16_OPEN	SW1_CS15_OPEN	SW1_CS14_OPEN	SW1_CS13_OPEN	SW1_CS12_OPEN	SW1_CS11_OPEN	SW1_CS10_OPEN	SW1_CS9_OPEN
Default	0	0	0	0	0	0	0	0

05h

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SW2_CS6_OPEN	SW2_CS5_OPEN	SW2_CS4_OPEN	SW2_CS3_OPEN	SW2_CS2_OPEN	SW2_CS1_OPEN	SW1_CS18_OPEN	SW1_CS17_OPEN
Default	0	0	0	0	0	0	0	0

06h

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SW2_CS14_OPEN	SW2_CS13_OPEN	SW2_CS12_OPEN	SW2_CS11_OPEN	SW2_CS10_OPEN	SW2_CS9_OPEN	SW2_CS8_OPEN	SW2_CS7_OPEN
Default	0	0	0	0	0	0	0	0

07h

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	SW2_CS18_OPEN	SW2_CS17_OPEN	SW2_CS16_OPEN	SW2_CS15_OPEN
Default	0	0	0	0	0	0	0	0

SW1_CSy_ OPEN	SW1_CSy Channel Open result
0	normal
1	SW1_CSy is open

SW2_CSy_ OPEN	SW2_CSy Channel Open result
0	normal
1	SW2_CSy is open

Table 65 08h~0Ch Short Detect Result Register (Read Only)

08h

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SW1_CS8_SHORT	SW1_CS7_SHORT	SW1_CS6_SHORT	SW1_CS5_SHORT	SW1_CS4_SHORT	SW1_CS3_SHORT	SW1_CS2_SHORT	SW1_CS1_SHORT
Default	0	0	0	0	0	0	0	0

09h

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SW1_CS16_SHORT	SW1_CS15_SHORT	SW1_CS14_SHORT	SW1_CS13_SHORT	SW1_CS12_SHORT	SW1_CS11_SHORT	SW1_CS10_SHORT	SW1_CS9_SHORT
Default	0	0	0	0	0	0	0	0

0Ah

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SW2_CS6_SHORT	SW2_CS5_SHORT	SW2_CS4_SHORT	SW2_CS3_SHORT	SW2_CS2_SHORT	SW2_CS1_SHORT	SW1_CS18_SHORT	SW1_CS17_SHORT
Default	0	0	0	0	0	0	0	0

0Bh

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SW2_CS14_SHORT	SW2_CS13_SHORT	SW2_CS12_SHORT	SW2_CS11_SHORT	SW2_CS10_SHORT	SW2_CS9_SHORT	SW2_CS8_SHORT	SW2_CS7_SHORT
Default	0	0	0	0	0	0	0	0

0Ch

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SW1_OC	SW2_OC	SW1_SH	SW2_SH	SW2_CS18_SHORT	SW2_CS17_SHORT	SW2_CS16_SHORT	SW2_CS15_SHORT
Default	0	0	0	0	0	0	0	0

SW1_OC	SW1 over current result
0	normal
1	SW1 over current occurred

SW2_OC	SW2 over current result
0	normal
1	SW2 over current occurred

SW1_SH	SW1 short to VLED result
0	normal
1	SW1 short to VLED occurred

Please set the PWM duty at first, then read this result, otherwise this detection is unavailable.

SW1_SH	SW2 short to VLED result
0	normal
1	SW2 short to VLED occurred

Please set the PWM duty at first, then read this result, otherwise this detection is unavailable.

SW1_CSy_ SHORT	SW1_CSy Channel Short Occurred
0	normal
1	SW1_CSy is short

SW2_CSy_SHORT	SW2_CSy Channel Short Occurred
0	normal
1	SW2_CSy is short

Table 66 0Dh~11h SW and CS Loop Back Test Result Register (Read Only)

0Dh

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SW1_CS8_LT	SW1_CS7_LT	SW1_CS6_LT	SW1_CS5_LT	SW1_CS4_LT	SW1_CS3_LT	SW1_CS2_LT	SW1_CS1_LT
Default	0	0	0	0	0	0	0	0

0Eh

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SW1_CS16_LT	SW1_CS15_LT	SW1_CS14_LT	SW1_CS13_LT	SW1_CS12_LT	SW1_CS11_LT	SW1_CS10_LT	SW1_CS9_LT
Default	0	0	0	0	0	0	0	0

0Fh

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SW2_CS6_LT	SW2_CS5_LT	SW2_CS4_LT	SW2_CS3_LT	SW2_CS2_LT	SW2_CS1_LT	SW1_CS18_LT	SW1_CS17_LT
Default	0	0	0	0	0	0	0	0

10h

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SW2_CS14_LT	SW2_CS13_LT	SW2_CS12_LT	SW2_CS11_LT	SW2_CS10_LT	SW2_CS9_LT	SW2_CS8_LT	SW2_CS7_LT
Default	0	0	0	0	0	0	0	0

11h

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	SW2_LT	SW1_LT	SW2_CS18_LT	SW2_CS17_LT	SW2_CS16_LT	SW2_CS15_LT
Default	0	0	0	0	0	0	0	0

SW1_CSy_ LT **SW1_CSy Channel Loop back Test Result**

0 SW1_CSy loop back test result is passed

1 SW1_CSy loop back test result is failed

SW2_CSy_ LT **SW2_CSy Channel Loop back Test Result**

0 SW2_CSy loop back test result is passed

1 SW2_CSy loop back test result is failed

SW1_LT **SW1 Loop back Test Result (Clear after write "0")**

0 SW1's test result is passed

1 SW1's test result is failed

SW2_LT **SW2 Loop back Test Result (Clear after write "0")**

0 SW2's test result is passed

1 SW2's test result is failed

Table 67 12h~16h VF Voltage Monitor Result Register (Read Only)

12h

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SW1_CS8_VFMD	SW1_CS7_VFMD	SW1_CS6_VFMD	SW1_CS5_VFMD	SW1_CS4_VFMD	SW1_CS3_VFMD	SW1_CS2_VFMD	SW1_CS1_VFMD
Default	0	0	0	0	0	0	0	0

13h

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SW1_CS16_VFMD	SW1_CS15_VFMD	SW1_CS14_VFMD	SW1_CS13_VFMD	SW1_CS12_VFMD	SW1_CS11_VFMD	SW1_CS10_VFMD	SW1_CS9_VFMD
Default	0	0	0	0	0	0	0	0

14h

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SW2_CS6_VFMD	SW2_CS5_VFMD	SW2_CS4_VFMD	SW2_CS3_VFMD	SW2_CS2_VFMD	SW2_CS1_VFMD	SW1_CS18_VFMD	SW1_CS17_VFMD
Default	0	0	0	0	0	0	0	0

15h

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SW2_CS14_VFMD	SW2_CS13_VFMD	SW2_CS12_VFMD	SW2_CS11_VFMD	SW2_CS10_VFMD	SW2_CS9_VFMD	SW2_CS8_VFMD	SW2_CS7_VFMD
Default	0	0	0	0	0	0	0	0

16h

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	SW2_CS18_ VFMD	SW2_CS17_ VFMD	SW2_CS16_ VFMD	SW2_CS15_ VFMD
Default	0	0	0	0	0	0	0	0

SW1_CSy_ VFMD	SW1_CSy Channel VF Voltage Monitor Result
0	normal
1	SW1_CSy VF voltage monitor result is failed

SW2_CSy_ VFMD	SW2_CSy Channel VF Voltage Monitor Result
0	normal
1	SW2_CSy VF voltage monitor result is failed

Table 68 17h~1Bh Output Current Monitor Result Register (Read Only)

17h

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SW1_CS8_ IM	SW1_CS7_ IM	SW1_CS6_ IM	SW1_CS5_ IM	SW1_CS4_ IM	SW1_CS3_ IM	SW1_CS2_ IM	SW1_CS1_IM
Default	0	0	0	0	0	0	0	0

18h

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SW1_CS16_ IM	SW1_CS15_ IM	SW1_CS14_ IM	SW1_CS13_ IM	SW1_CS12_IM	SW1_CS11_ IM	SW1_CS10_ IM	SW1_CS9_ IM
Default	0	0	0	0	0	0	0	0

19h

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SW2_CS6_ IM	SW2_CS5_ IM	SW2_CS4_ IM	SW2_CS3_ IM	SW2_CS2_ IM	SW2_CS1_ IM	SW1_CS18_ IM	SW1_CS17_ IM
Default	0	0	0	0	0	0	0	0

1Ah

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SW2_CS14_ IM	SW2_CS13_ IM	SW2_CS12_ IM	SW2_CS11_ IM	SW2_CS10_ IM	SW2_CS9_ IM	SW2_CS8_ IM	SW2_CS7_ IM
Default	0	0	0	0	0	0	0	0

1Bh

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	SW2_CS18_ IM	SW2_CS17_ IM	SW2_CS16_ IM	SW2_CS15_ IM
Default	0	0	0	0	0	0	0	0

SW1_CSy_ IM	SW1_CSy Channel Output Current Monitor Result
0	normal
1	SW1_CSy Output Current monitor result is failed

SW2_CSy_ IM	SW2_CSy Channel Output Current Monitor Result
0	normal
1	SW2_CSy Output Current monitor result is failed

Table 69 1Ch Self-check Status and Result Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	VFSC_BUSY	IMONSC_BUSY	Lbist_fail	Lbist_finish	-	-	VF_SC_F	IM_SC_F
Default	0	0	0	0	0	0	0	0

VFSC_BUSY **LED VF monitor Self-check Status Flag**
0 VF monitor self-check finished
1 VF monitor self-check in progress

IMONSC_BUSY **Output Current monitor Self-check Status Flag**
0 IOUT monitor self-check finished
1 IOUT monitor self-check in progress

Lbist_fail **Digital Self-check Status Flag (Clear after write "0")**
0 No failure
1 Failure

Lbist_finish **Digital Self-check Status Flag**
0 Digital Self-check in progress
1 Digital Self-check finished

VF_SC_F **LED VF Monitor Self-Check Result (Clear after write "0")**
0 No failure
1 Failure

IM_SC_F **Output Current Monitor Self-Check Result (Clear after write "0")**
0 No failure
1 Failure

Table 70 1Dh CRC Error Count Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CRCCNT[7:0]							
Default	0	0	0	0	0	0	0	0

The CRCCNT default value of is 0x00, when there is a CRC error in a communication frame, CRCCNT will increase by 1 and when it is increased to more than 255, it will remain 255.
If the host writes any value to the CRC Error Count register, the CRC Error Count will be cleared to 0x00.

Table 71 1Eh OTP Status register, read only

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						FAIL	FINISH	BUSY
Default	-	-	-	-	-	-	-	-

Table 72 21h ECC Status (1Err_Ecc Status), read only

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	1Err_eccC	1Err_eccC	1Err_eccB	-
Default	-	-	-	-	-	-	-	-

Table 73 22h ECC Status (2Err_Ecc Status), read only

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	2Err_eccD	2Err_eccC	2Err_eccB	-
Default	-	-	-	-	-	-	-	-

FAIL OTP write fail

FINISH OTP write finish

BUSY OTP operation in progress

1Err_eccX ECC detected 1bit error in zone X (X= B, C, D)

2Err_eccX ECC detected 2bits error in zone X (X= B, C, D)

10.2.3 PAGE 2 (08H~1FH): OTP REGISTER MAPPING

Zone B:

Table 74 08h~10h Save PWM State for SW1 Register

08h (OTPCRB1): SW1_CS1 and SW1_CS2 Save PWM State Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SA1_PWM_H_CS2[3:0]				SA1_PWM_H_CS1[3:0]			
Default	0	0	0	0	0	0	0	0

09h (OTPCRB2): SW1_CS3 and SW1_CS4 Save PWM State Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SA1_PWM_H_CS4[3:0]				SA1_PWM_H_CS3[3:0]			
Default	0	0	0	0	0	0	0	0

0Ah (OTPCRB3): SW1_CS5 and SW1_CS6 Save PWM State Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SA1_PWM_H_CS6[3:0]				SA1_PWM_H_CS5[3:0]			
Default	0	0	0	0	0	0	0	0

0Bh (OTPCRB4): SW1_CS8 and SW1_CS7 Save PWM State Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SA1_PWM_H_CS8[3:0]				SA1_PWM_H_CS7[3:0]			
Default	0	0	0	0	0	0	0	0

0Ch (OTPCRB5): SW1_CS10 and SW1_CS9 Save PWM State Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SA1_PWM_H_CS10[3:0]				SA1_PWM_H_CS9[3:0]			
Default	0	0	0	0	0	0	0	0

0Dh (OTPCRB6): SW1_CS12 and SW1_CS11 Save PWM State Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SA1_PWM_H_CS12[3:0]				SA1_PWM_H_CS11[3:0]			
Default	0	0	0	0	0	0	0	0

0Eh (OTPCRB7): SW1_CS14 and SW1_CS13 Save PWM State Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SA1_PWM_H_CS14[3:0]				SA1_PWM_H_CS13[3:0]			
Default	0	0	0	0	0	0	0	0

0Fh (OTPCRB8): SW1_CS16 and SW1_CS15 Save PWM State Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SA1_PWM_H_CS16[3:0]				SA1_PWM_H_CS15[3:0]			
Default	0	0	0	0	0	0	0	0

10h (OTPCRB9): SW1_CS18 and SW1_CS17 Save PWM State Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SA1_PWM_H_CS18[3:0]				SA1_PWM_H_CS17[3:0]			
Default	0	0	0	0	0	0	0	0

SA1_PWM_H_CSy sets SW1_CSy channels PWM data (only high 4 bits) in the case of loss communication.

Table 75 11h (OTPCRB10) ECC_B for Zone B

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	ECC_B [7:0]							
Default	0	0	0	0	0	0	0	0

ECC_B: ECC bit of zone B

Table 76 12h (OTPCRB11) Protection bit for Zone B

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PT_B	-						
Default	0	0	0	0	0	0	0	0

PT_B: protection bit of zone B

Zone C:

Table 77 13h~1Dh Save PWM State for SW2 Register

13h (OTPCRC1): SW2_CS1 and SW2_CS2 Save PWM State Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SA2_PWM_H_CS2[3:0]				SA2_PWM_H_CS1[3:0]			
Default	0	0	0	0	0	0	0	0

14h (OTPCRC2): SW2_CS3 and SW2_CS4 Save PWM State Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SA2_PWM_H_CS4[3:0]				SA2_PWM_H_CS3[3:0]			
Default	0	0	0	0	0	0	0	0

15h (OTPCRC3): SW2_CS5 and SW2_CS6 Save PWM State Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SA2_PWM_H_CS6[3:0]				SA2_PWM_H_CS5[3:0]			
Default	0	0	0	0	0	0	0	0

16h (OTPCRC4): SW2_CS8 and SW2_CS7 Save PWM State Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SA2_PWM_H_CS8[3:0]				SA2_PWM_H_CS7[3:0]			
Default	0	0	0	0	0	0	0	0

17h (OTPCRC5): SW2_CS10 and SW2_CS9 Save PWM State Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SA2_PWM_H_CS10[3:0]				SA2_PWM_H_CS9[3:0]			
Default	0	0	0	0	0	0	0	0

18h (OTPCRC6): SW2_CS12 and SW2_CS11 Save PWM State Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SA2_PWM_H_CS12[3:0]				SA2_PWM_H_CS11[3:0]			
Default	0	0	0	0	0	0	0	0

19h (OTPCRC7): SW2_CS14 and SW2_CS13 Save PWM State Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SA2_PWM_H_CS14[3:0]				SA2_PWM_H_CS13[3:0]			
Default	0	0	0	0	0	0	0	0

1Ah (OTPCRC8): SW2_CS16 and SW2_CS15 Save PWM State Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SA2_PWM_H_CS16[3:0]				SA2_PWM_H_CS15[3:0]			
Default	0	0	0	0	0	0	0	0

1Bh (OTPCRC9): SW1_CS18 and SW1_CS17 Save PWM State Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SA2_PWM_H_CS18[3:0]				SA2_PWM_H_CS17[3:0]			
Default	0	0	0	0	0	0	0	0

SA2_PWM_H_CSy sets SW1_CSy channels PWM data (only high 4 bits) in the case of loss communication.

Table 78 1Ch (OTPCRC10) ECC_C for Zone C

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	ECC_C [7:0]							
Default	0	0	0	0	0	0	0	0

ECC_C: ECC bit of zone C

Table 79 1Dh (OTPCRC11) Watchdog Fail Safe Mode Trigged Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PT_C	-				-	WDT_FS2	WDT_FS1
Default	0	0	0	0	0	0	0	0

WDT_FS2	**Watchdog Timer 2 Trigged Safe Mode**
0	Disable (Default)
1	Enable, when watchdog timer 2 time out, enter to fail safe mode

WDT_FS1	**Communication Watchdog Timer Trigged Fail Safe Mode**
0	Disable (Default)
1	Enable, when communication watchdog time out, enter to fail safe mode

PT_C: protection bit of zone C

Zone D:

Table 80 1Eh (OTPCRD1) SNPD address Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SNPD [7:0]							
Default	0	0	0	0	0	0	0	0

SNPD NAD[7:0]: SNPD address

Table 81 1Fh (OTPCRD2) PT_D and ECC_D for Zone D

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PT_D				ECC_D [4:0]			
Default	0	0	0	0	0	0	0	0

ECC_D: ECC bit of zone D

PT_D: protection bit of zone D

11 CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

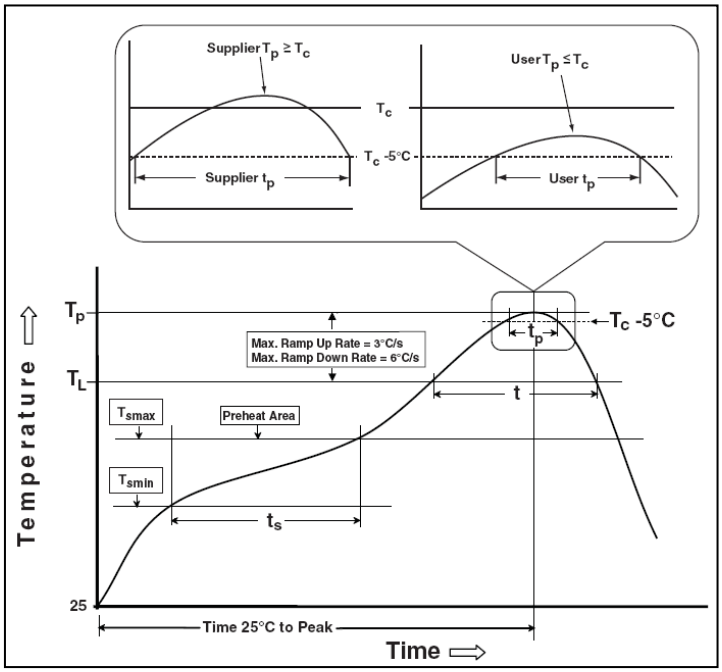
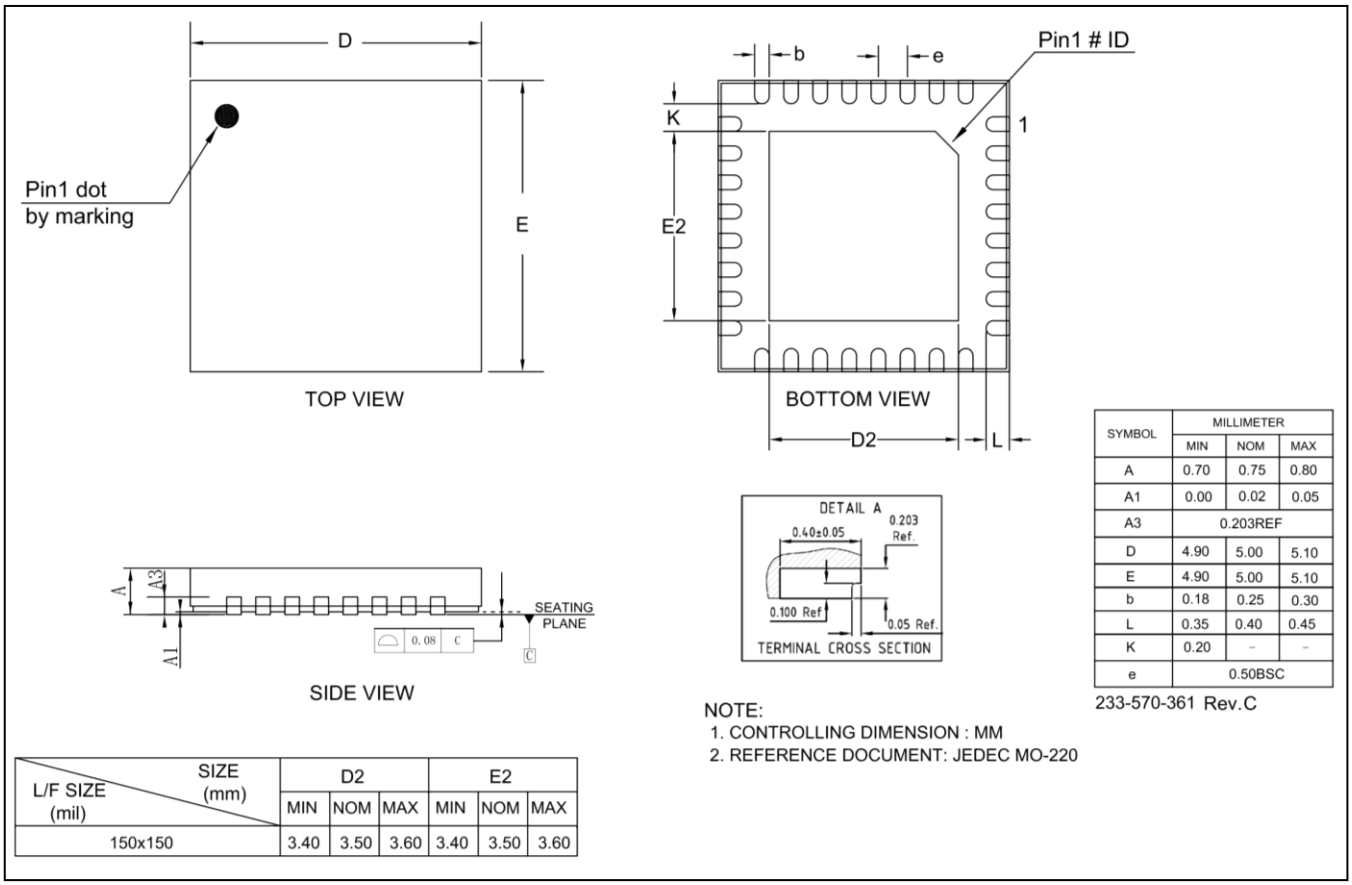


Figure 23 Classification Profile

12 PACKAGE INFORMATION

WFQFN-32



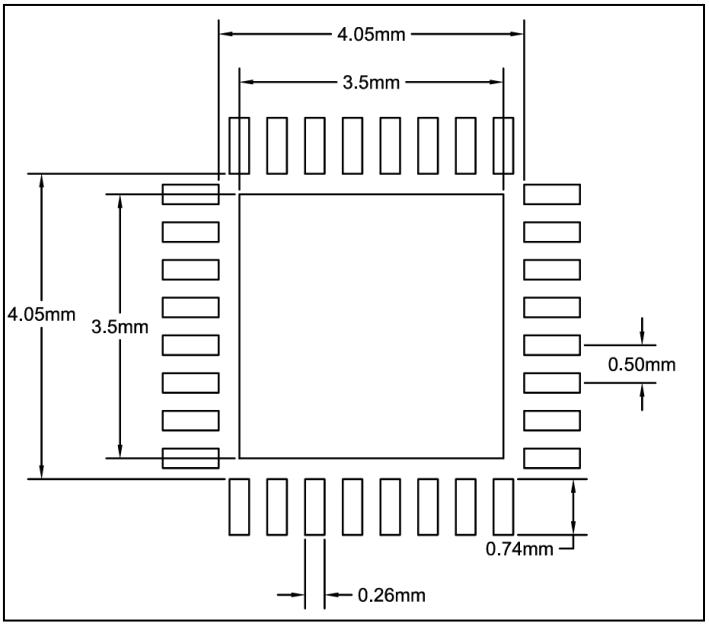
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203REF	
D	4.90	5.00	5.10
E	4.90	5.00	5.10
b	0.18	0.25	0.30
L	0.35	0.40	0.45
K	0.20	-	-
e		0.50BSC	

233-570-361 Rev.C

L/F SIZE (mil) \ SIZE (mm)	D2			E2		
	MIN	NOM	MAX	MIN	NOM	MAX
150x150	3.40	3.50	3.60	3.40	3.50	3.60

13 RECOMMENDED LAND PATTERN

WFQFN-32



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. User's board manufacturing specs), user must determine suitability for use.

14 REVISION HISTORY

Revision	Detail Information	Date
0A	Initial Release	2025.05.07
A	1. Update EC table format and conditions. 2. Update the corresponding EC data. 3. Update the formulas for Mismatch and Accuracy. 4. Update ABSOLUTE MAXIMUM RATINGS's θ_{JP} to θ_{JC_BOT}. 5. Update IOUT Channel to Channel Parameter of Features. 6. Add Rohs/TCAS items to Feature. 7. Update Application Schematic and add note 3 to introduce RFBO Resistor. 8. Update EC Data. 9. Update CANH & CANL Voltage of AMR. 10.Update OFS: OSC Frequency Setting for PWM. 11. Add Direct Address Recommended Resistor Description. 12. Update Note5 Description.	2026.05.09