IS31PM3510

HIGH VOLTAGE ASYNCHRONOUS MULTI-TOPOLOGY DC-DC PWM CONTROLLER

March 2024

GENERAL DESCRIPTION

The IS31PM3510 is an asynchronous multi-topology PWM controller that employs a single inductor to provide excellent voltage regulation. In a Buck-Boost topology regulated output voltage is maintained when the input voltage is either less or greater than the desired output voltage. With a 150kHz to 650kHz programmable operating frequency that can be either adjusted with an external resistor or synchronized with an external clock, optimum inductor and capacitor (s) size can be achieved while maintaining high efficiency. The controller integrates spread spectrum function that effectively reduces overall EMI profile.

The IS31PM3510 can also be configured for either Buck or Boost operation with a single switch, and features robust protection functions with power good signal output, PGOOD, for MCU fault flag reporting.

The IS31PM3510 is available in an eTSSOP-16 package with an exposed thermal pad for enhanced thermal dissipation.

FEATURES

- Wide input voltage: 4.5V to 55V
- Supports buck, boost and buck-boost topologies
- ±1.5% feedback voltage accuracy over -40°C ~ +150°C
- Adjustable operating frequency: 150kHz-650kHz
  - Spread spectrum for EMI profile optimization
  - External clock synchronization capability
- Internally fixed soft start to avoid inrush current
- Power good signal output
- Integrated bootstrap diode
- 1.5μA shutdown supply current
- Built-in robust protections with fault reporting:
  - Input over current protection
  - Output over voltage protection
  - Output over current protection
  - FS/SYNC resistor open/short protection
  - Thermal shutdown
- Operating temperature range from -40°C ~ +150°C junction temperature
- RoHS & Halogen-Free Compliance
- TSCA Compliance

APPLICATIONS

- Lighting system
- General voltage regulator

TYPICAL APPLICATION CIRCUIT

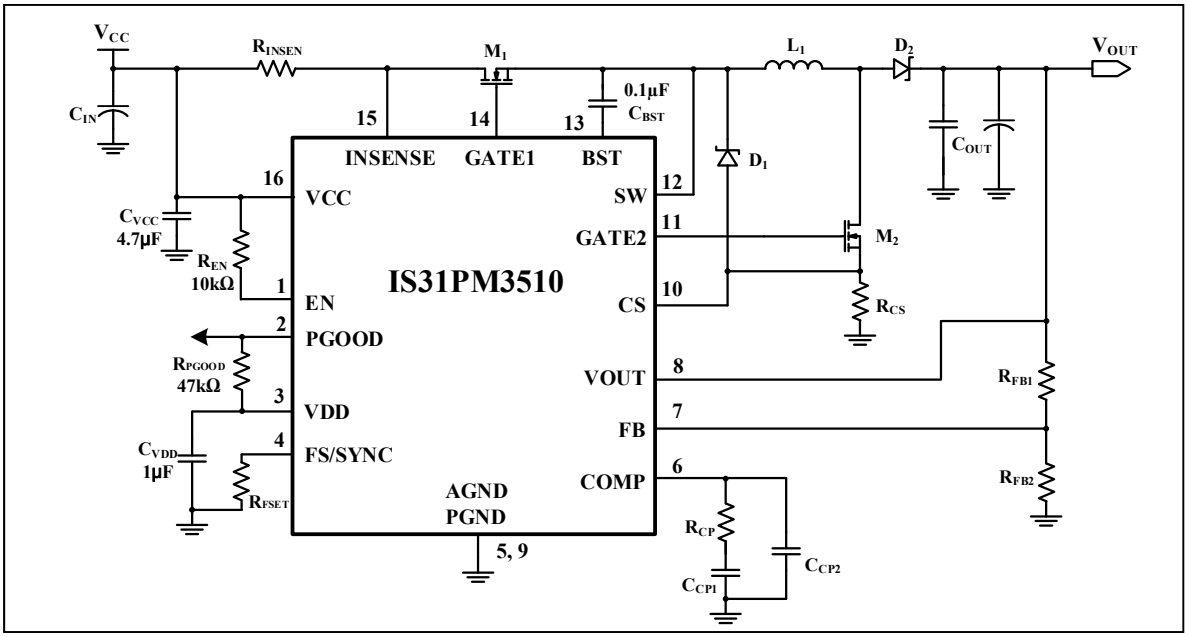


Figure 1 Typical Application Circuit (Buck-Boost Topology)

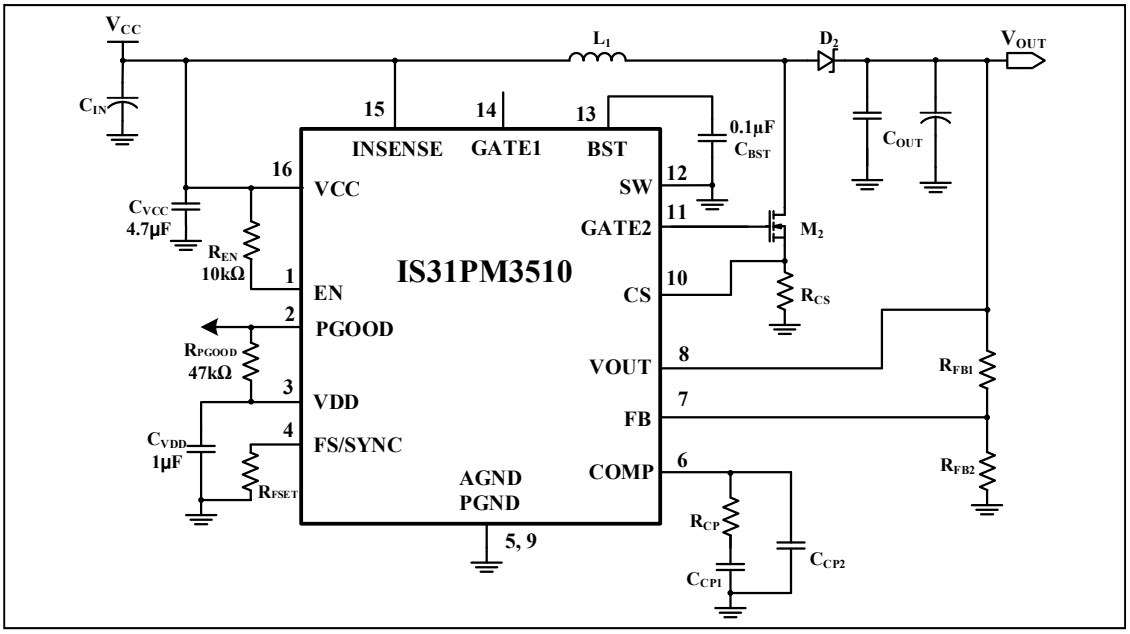


Figure 2 Typical Application Circuit (Boost Topology)

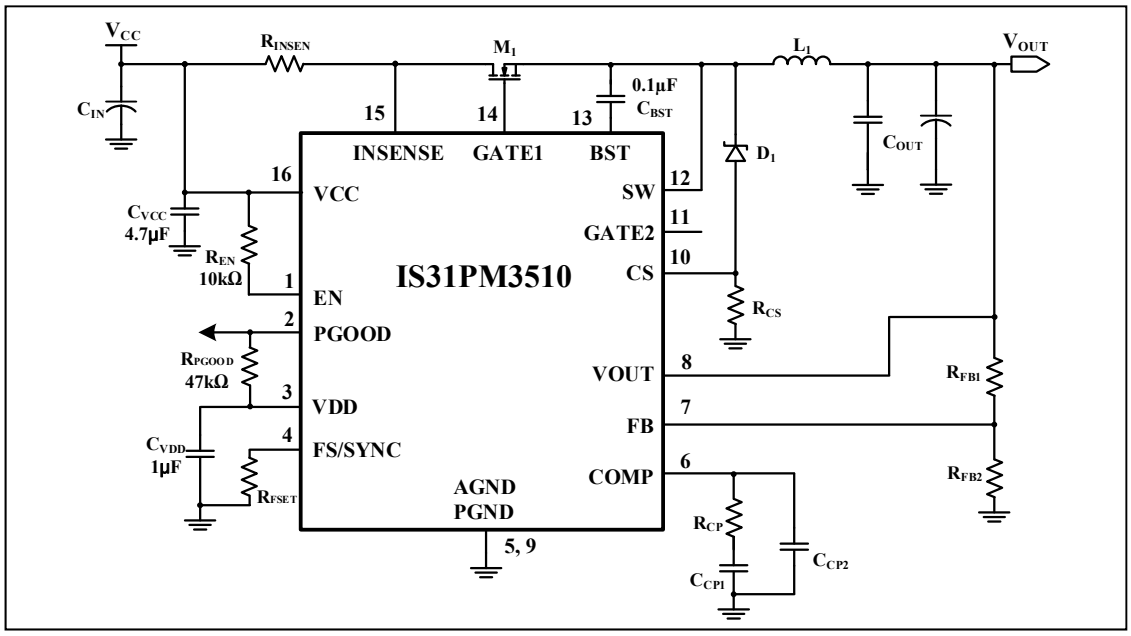
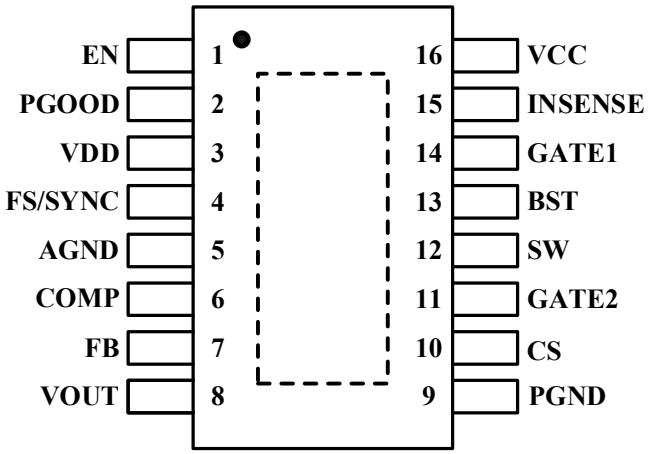


Figure 3 Typical Application Circuit (Buck Topology)

PIN CONFIGURATION

Package	Pin Configurations (Top view)
eTSSOP-16	

PIN DESCRIPTION

No.	Pin	Function
1	EN	Enable pin. It's internally pulled down by a 200kΩ resistor. Pulling down below 0.8V will shut down the IC. If shut down mode is unused, please connect EN pin to V_{CC} via a 10kΩ resistor.
2	PGOOD	The open drain power good output pin to indicate power good state. Connect to suitable voltage source through pull-up resistor. High=good. Low=fault.
3	VDD	Internal LDO 6V output. Needs an external capacitor (1μF) to GND. This capacitor must be placed as close to this pin as possible.
4	FS/SYNC	External resistor sets the operating frequency (150kHz-650kHz). It also can be used to synchronize the operating frequency with an external clock signal.
5	AGND	Analog ground.
6	COMP	Loop compensation pin.
7	FB	Output voltage feedback pin. Feedback voltage divider resistor network must be placed close to this pin.
8	VOUT	Output supply pin. This pin must be tied to the power output to determine the Buck, Boost or Buck-boost operating mode.
9	PGND	Driver and current sense ground. It must be directly connected to the ground terminal of the current sense resistor, R_{CS}, to ensure precise sensing.
10	CS	Low-side NMOS current sense and over current detect pin.
11	GATE2	Gate drive to the external low-side NMOS.
12	SW	High-side NMOS source pin.
13	BST	High-side NMOS bootstrap floating driver supply. The BST pin has an integrated bootstrap Schottky diode from an internal 5.5V (Typ.) linear regulator and requires an external bootstrap capacitor (0.1μF) to the SW pin. The BST pin swings from a diode voltage drop below 5.5V to (V_{SW} + 5.5V).
14	GATE1	Gate drive to the external high-side NMOS.
15	INSENSE	Input current sense pin.
16	VCC	Power supply pin.
	Thermal Pad	Connected to large PCB ground plane using multiple vias for good thermal performance.

ORDERING INFORMATION

Industrial Range: -40°C to +125°C

Order Part No.	Package	QTY
IS31PM3510-ZLS4-TR	eTSSOP-16, Lead-free	2500/Reel
IS31PM3510-ZLS4		96/Tube

ABSOLUTE MAXIMUM RATINGS

Voltage at VCC, INSENSE, GATE1, SW, PGOOD, VOUT and EN pins	-0.3V~+60V
Voltage at GATE2, VDD, COMP, FS/SYNC, FB and CS pins	-0.3V~+6.6V
Voltage at BST pin	-0.3V~+66V
Operating temperature, T_A=T_J	-40°C ~ +150°C
Junction temperature, T_{JMAX}	+150°C
Device storage temperature, T_{STG}	-65°C ~ +150°C
Maximum power dissipation, $P_{D(MAX)}$	2.64W
Package thermal resistance, junction to ambient (4-layer standard test PCB based on JESD 51-2A), θ_{JA}	47.4°C/W
Package thermal resistance, junction to thermal PAD (4-layer standard test PCB based on JESD 51-8), θ_{JP}	1.62°C/W
ESD (HBM) ESD (CDM)	±2kV ±750V

Note 1: Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Valid are at V_{CC}= 12V, T_J= T_A= 25°C, unless otherwise noted.
Limits apply over the junction temperature (T_J) range of -40°C ~ +150°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation (Note 2).

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Input voltage range		4.5		55	V
I_{CC}	Quiescent current	Gate switch off			4.5	mA
I_{SD}	Shutdown current	EN= Low		1.5	8	μA
V_{UVLO}	VCC under voltage lock out threshold	V_{CC} falling	3.8	4	4.2	V
V_{UVLO_HY}	VCC under voltage lock out hysteresis			200		mV
V_{DD}	Regulator output voltage	I_{VDD}= 5mA	5.8	6	6.2	V
I_{VDD_LM}	VDD output current limit	V_{CC}= 8V and V_{DD}= 4V	25	45		mA
V_{DD_UV}	VDD under voltage lock out	Voltage falling		3.5		V
V_{DD_UVHY}	VDD under voltage lock out hysteresis			0.5		V
t_{SS}	Internal soft-start time		3.5	5		ms
f_{SW}	Operating frequency	R_{FSET}= 125kΩ	360	400	440	kHz
f_{SYNC}	Frequency synchronization range		150		650	kHz
$V_{FS/SYNC}$	FS/SYNC pin voltage			1		V
V_{IH_SYNC}	FS/SYNC input high threshold		2.0			V
V_{IL_SYNC}	FS/SYNC input low threshold				0.4	V
t_{ON_SYNC}	Synchronization input minimum on-time		300			ns
t_{OFF_SYNC}	Synchronization input minimum off-time		300			ns
SS	Spread spectrum range	(Note 3)		±10		%
f_{SS}	Spread spectrum frequency	(Note 3)		500		Hz

ELECTRICAL CHARACTERISTICS (CONTINUED)

Valid are at V_{CC}= 12V, T_J= T_A= 25°C, unless otherwise noted.

Limits apply over the junction temperature (T_J) range of -40°C ~ +150°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation (Note 2).

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{BK_MINON}	Buck minimum ON-Time		120	160	200	ns
t_{BK_MINOFF}	Buck minimum OFF-Time		120	160	200	ns
t_{BT_MINON}	Boost minimum ON-Time		120	160	200	ns
t_{BT_MINOFF}	Boost minimum OFF-Time		100	145	180	ns
V_{CS_TH1}	Current limit threshold	Buck Valley	-77	-67	-57	mV
		Boost Peak	67	77	87	
V_{CS_TH2}	Secondary current limit threshold	Buck Peak	-125	-110	-95	mV
		Boost Peak	95	110	125	
$I_{INSENSE}$	INSENSE pin bias current	V_{CC}= $V_{INSENSE}$= 12V		110		uA
V_{IN_OCTH}	Input over current protection threshold (V_{CC}-$V_{INSENSE}$)		60	80	100	mV
t_{SKIP}	Fault protection reset time (Hiccup time)		115	128	145	ms
R_{PU_GATE}	GATE1/2 pins pull up resistance			3.5		Ω
R_{PD_GATE}	GATE1/2 pins pull down resistance			2.5		Ω
t_{R_GATE}	GATE1/2 turn on rising time	C_L= 3.3nF		40		ns
t_{F_GATE}	GATE1/2 turn off falling time	C_L= 3.3nF		30		ns
V_{FB_TH}	Feedback voltage		1.182	1.2	1.218	V
V_{OVP_OUT}	OVP protection via VOUT pin			58		V
V_{OVPHY_OUT}	OVP protection hysteresis			5		V
PG_H	PGOOD high threshold	Voltage rising, measured with respect to V_{FB_TH} reference	108%	111%	114%	V_{FB_TH}
PG_{H_HY}	PGOOD high hysteresis	measured with respect to V_{FB_TH} reference		3.33%		V_{FB_TH}
PG_L	PGOOD low threshold	Voltage falling, measured with respect to V_{FB_TH} reference	87%	90%	93%	V_{FB_TH}
PG_{L_HY}	PGOOD low hysteresis	measured with respect to V_{FB_TH} reference		3.33%		V_{FB_TH}
t_{PG_RP}	PGOOD report delay time			17		μs
t_{PG_RC}	PGOOD recover delay time			250		μs
V_{PG_LOW}	PGOOD pin pull low voltage	I_{PGOOD}= 1mA		100	200	mV
I_{PG}	PGOOD pin leakage current				1	μA
V_{IH}	High threshold on EN pin		2			V
V_{IL}	Low threshold on EN pin				0.8	V
V_{BTUV}	BST-SW under voltage lockout	Voltage rising, GATE1 start switching		3.6		V
V_{BTUV_HY}	BST-SW under voltage lockout hysteresis			300		mV

ELECTRICAL CHARACTERISTICS (CONTINUED)

Valid are at V_{CC}= 12V, T_J= T_A= 25°C, unless otherwise noted.

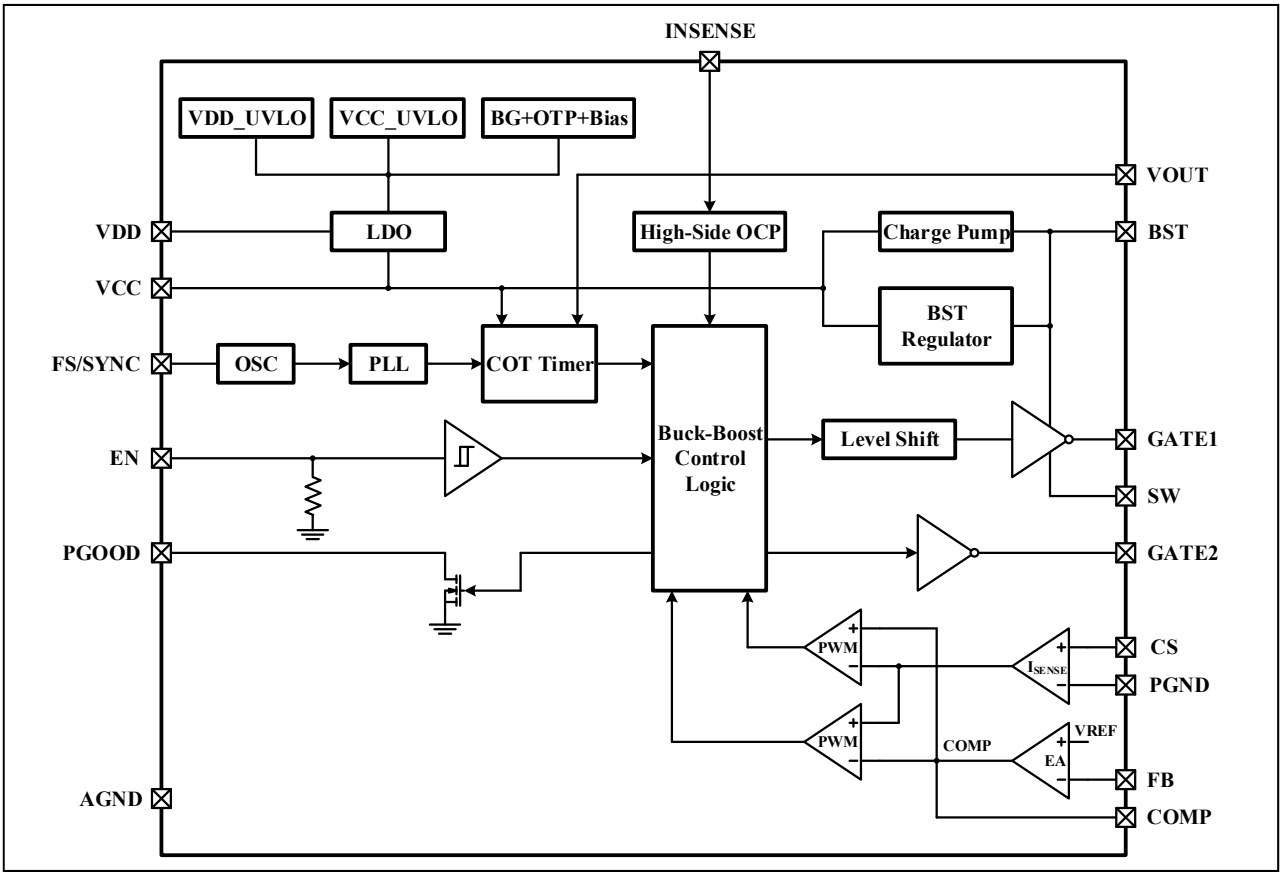
Limits apply over the junction temperature (T_J) range of -40°C ~ +150°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation (Note 2).

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{BT_REFR}	BST-SW refresh voltage	BOOT start refresh pulse at BOOST mode		3.9		V
R_{PD}	EN pin internal pull-down resistor			200		kΩ
gm_{EA}	Transconductance Amplifier gm			455		μS
G_{CS}	The gain from CS to EA COMP out	BUCK		30		
		BOOST		27.5		
V_{OUT}/V_{CC}	Mode transfer from buck to buck-boost		0.745	0.775	0.805	
	Mode transfer from buck-boost to buck		0.67	0.7	0.73	
	Mode transfer from buck-boost to boost		1.27	1.3	1.33	
	Mode transfer from boost to buck-boost		1.195	1.225	1.255	
T_{SD}	Thermal shutdown protection	(Note 3)		170		°C
T_{SD_HY}	Thermal shutdown hysteresis	(Note 3)		20		°C

Note 2: Limits are 100% production tested at 25°C. Limits over the operating temperature range verified through either bench and/or tester testing and correlation using statistical methods.

Note 3: Guaranteed by design.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL PERFORMANCE CHARACTERISTICS

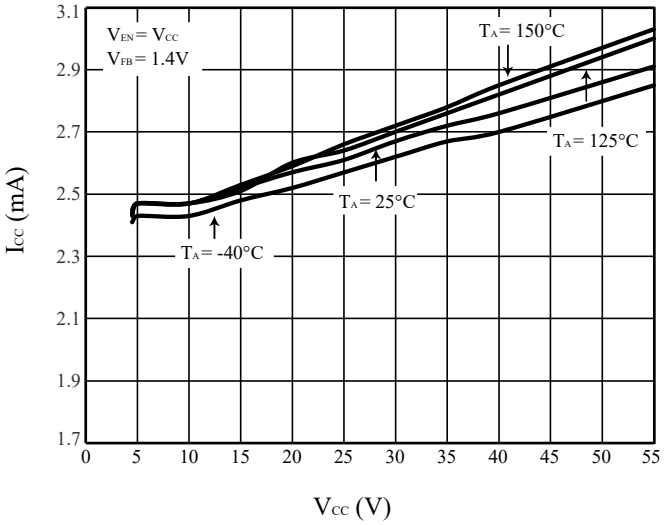


Figure 4 I_{CC} vs. V_{CC}

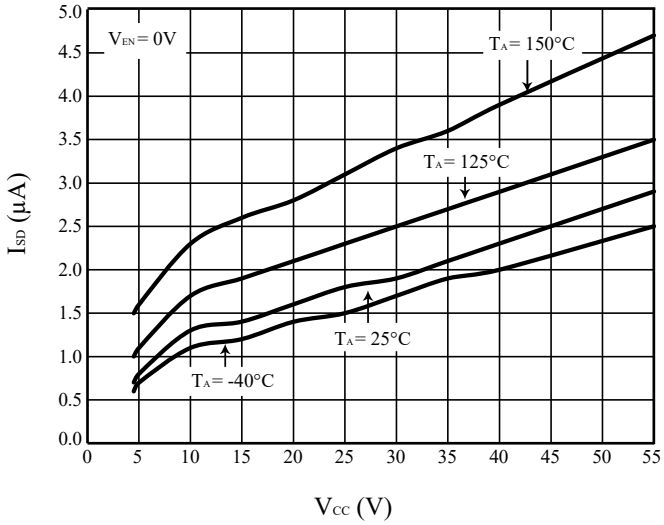


Figure 5 I_{SD} vs. V_{CC}

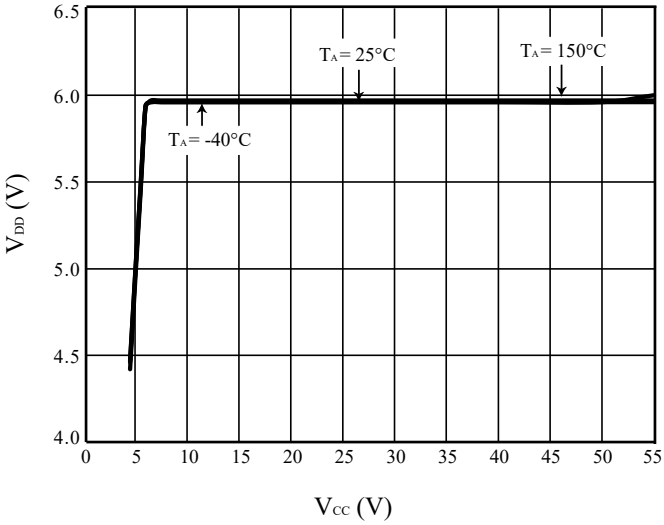


Figure 6 V_{DD} vs. V_{CC}

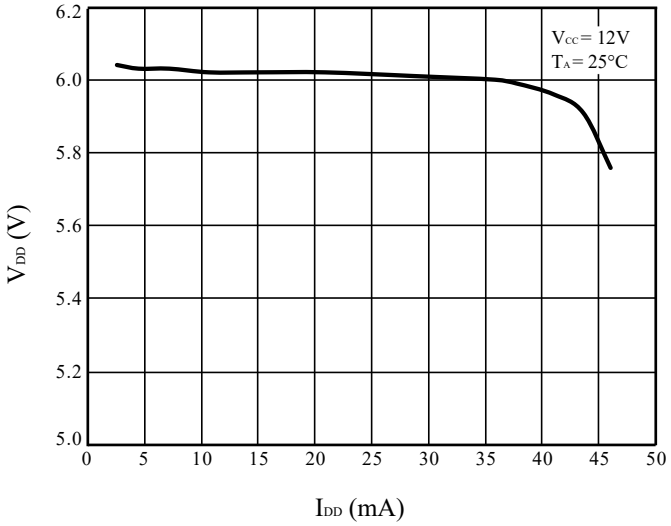


Figure 7 V_{DD} vs. I_{DD}

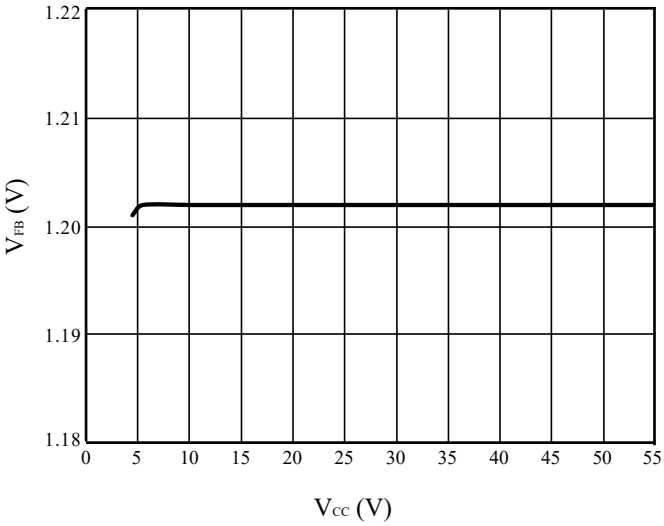


Figure 8 V_{FB} vs. V_{CC}

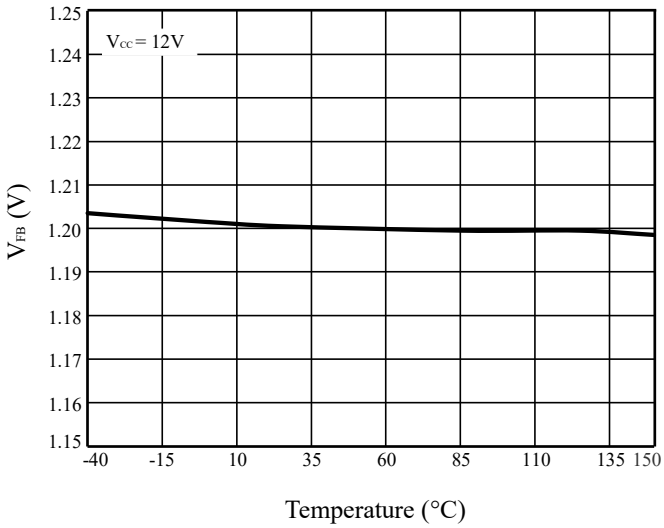


Figure 9 V_{FB} vs. Temperature

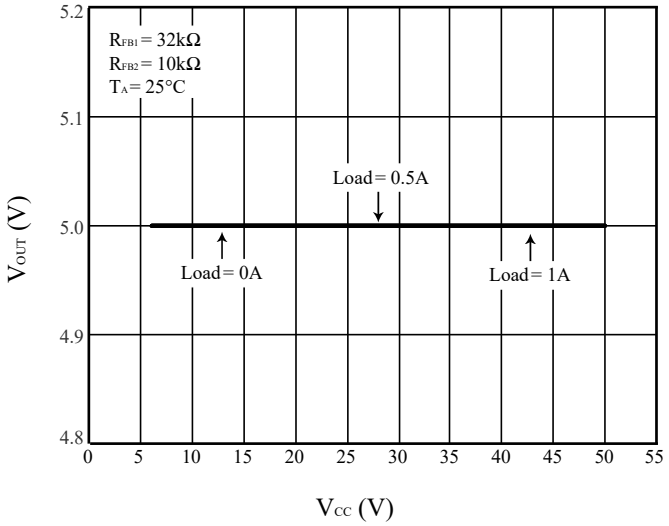


Figure 10 V_{OUT} vs. V_{CC}

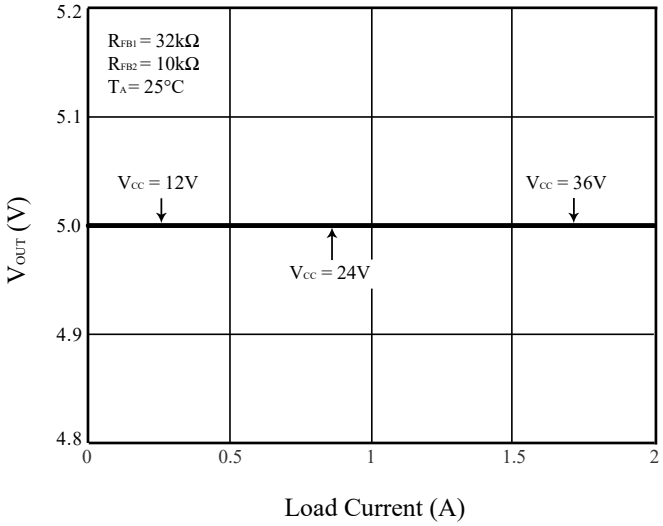


Figure 11 V_{OUT} vs. Load Current

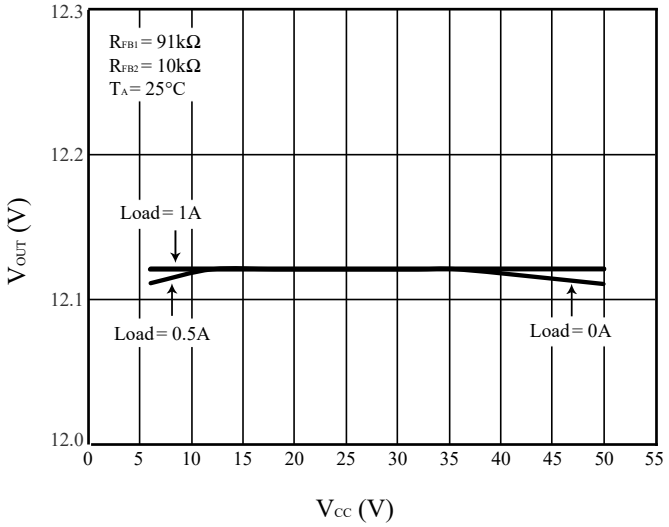


Figure 12 V_{OUT} vs. V_{CC}

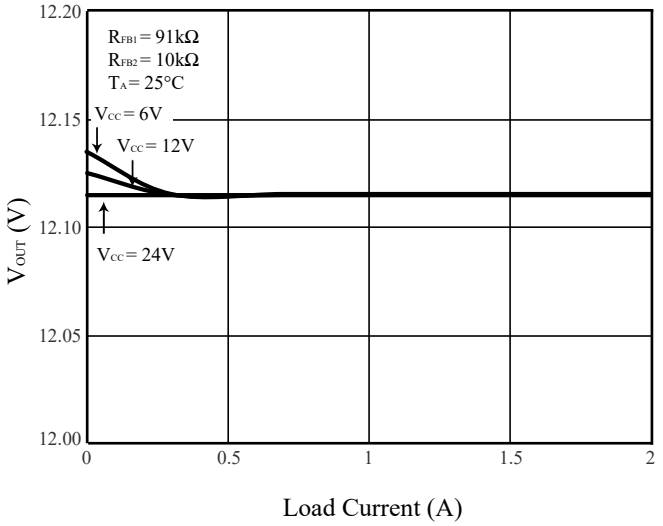


Figure 13 V_{OUT} vs. Load Current

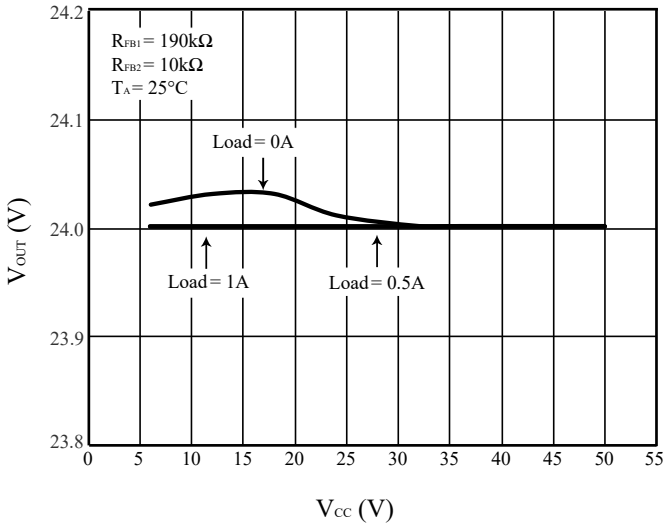


Figure 14 V_{OUT} vs. V_{CC}

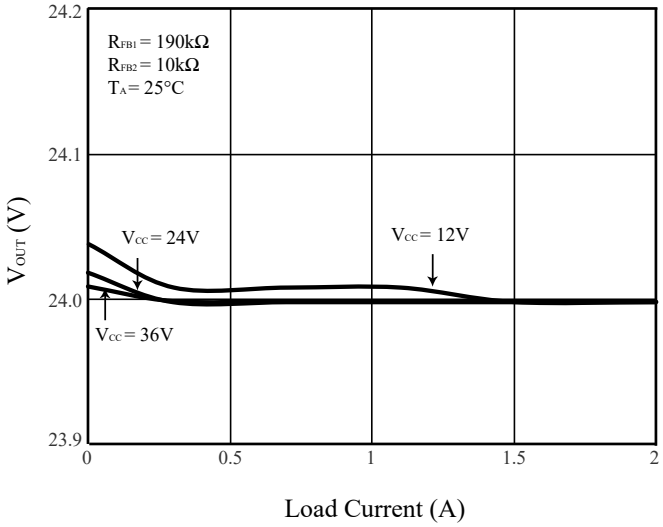


Figure 15 V_{OUT} vs. Load Current

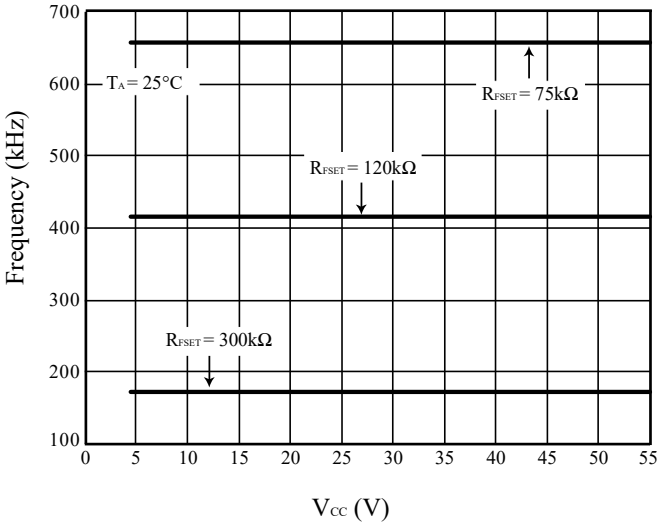


Figure 16 Frequency vs. V_{CC}

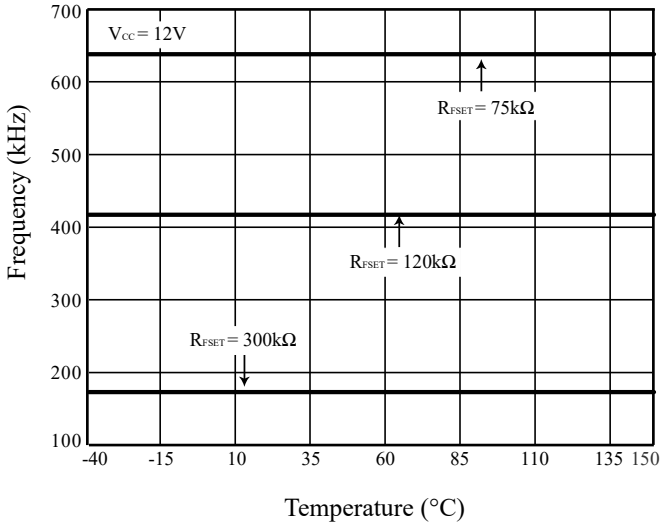


Figure 17 Frequency vs. Temperature

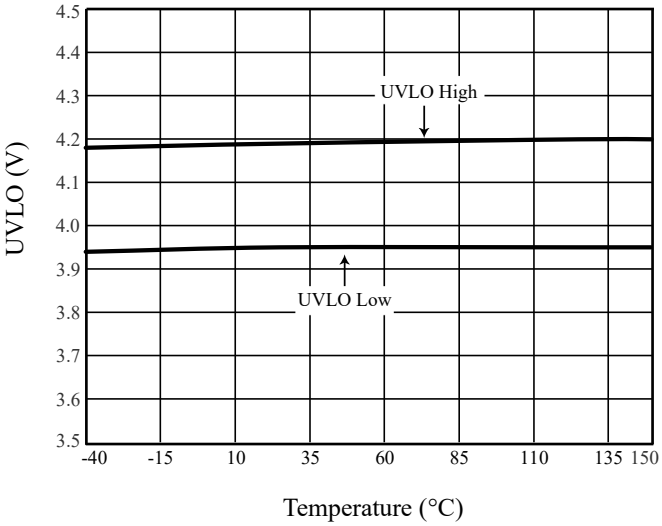


Figure 18 UVLO vs. Temperature

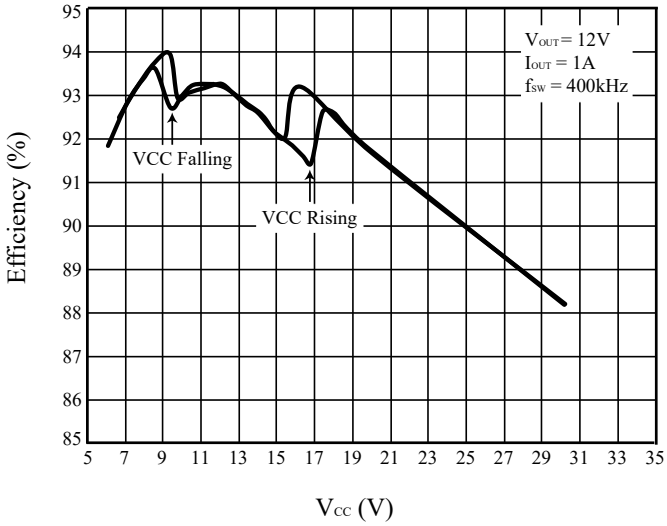


Figure 19 Efficiency vs. V_{CC}

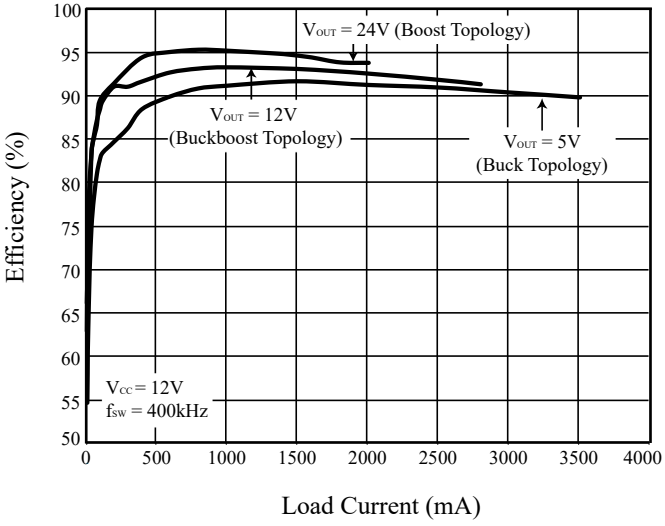


Figure 20 Efficiency vs. Load Current

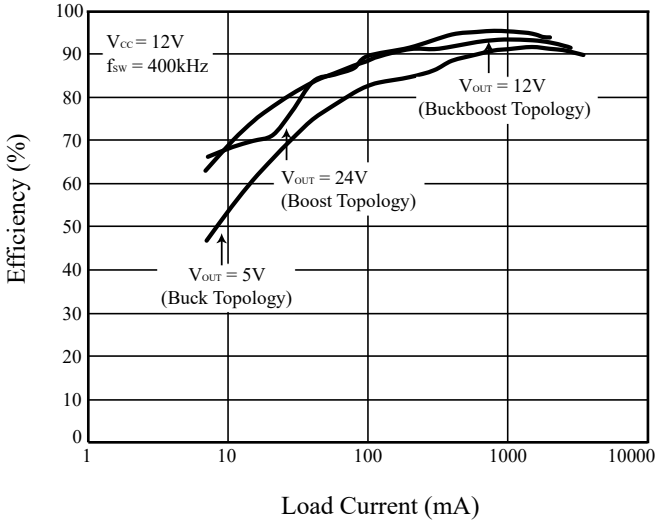


Figure 21 Efficiency vs. Load Current

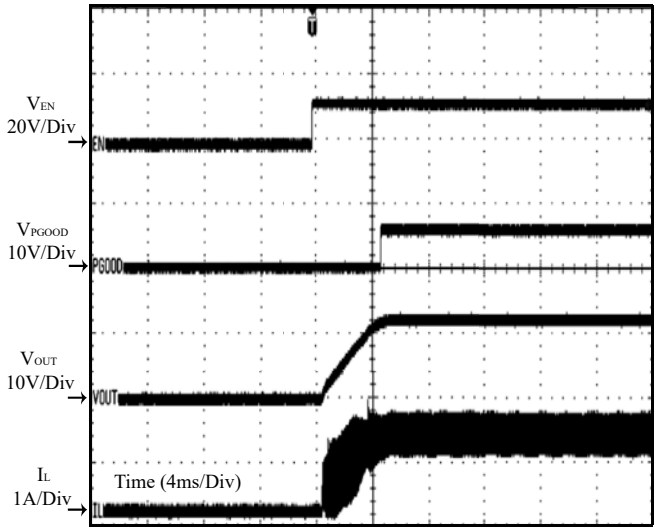


Figure 22 Enable Waveform

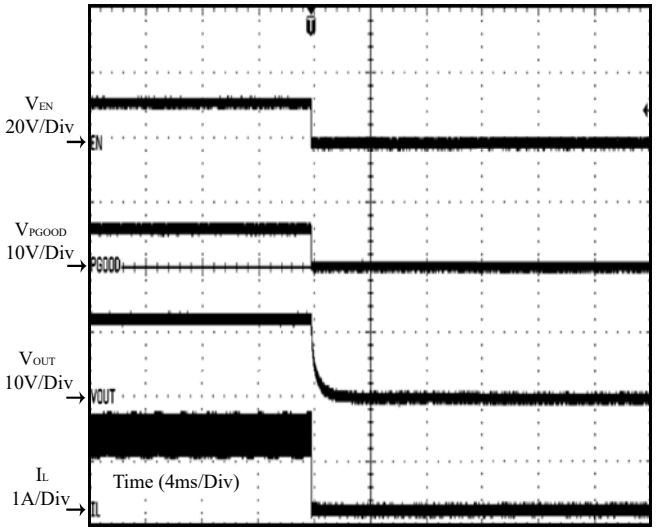


Figure 23 Disable Waveform

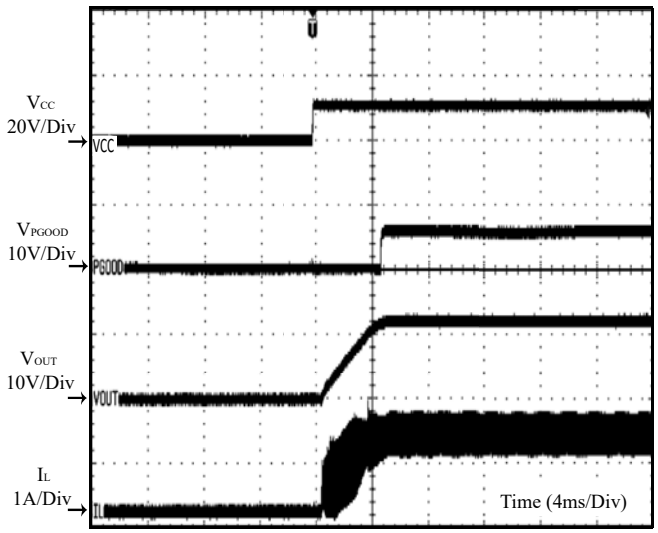


Figure 24 Power On

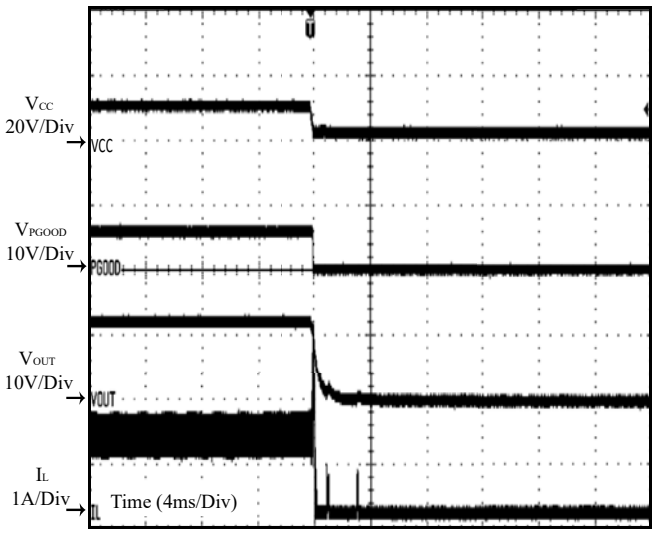


Figure 25 Power Off

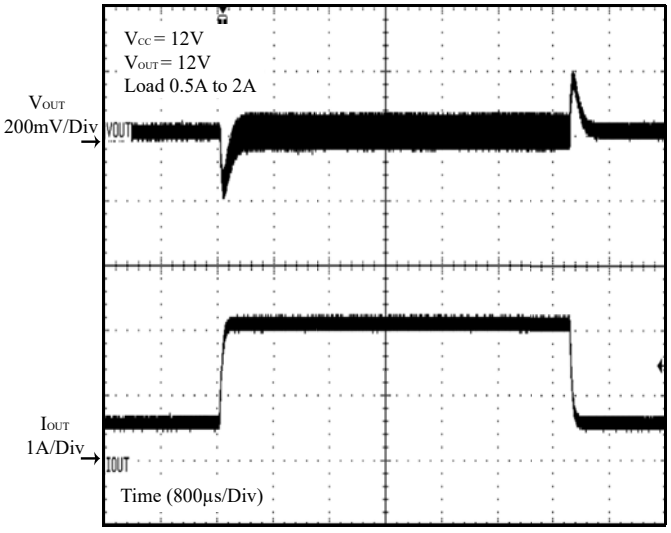


Figure 26 Load Transient

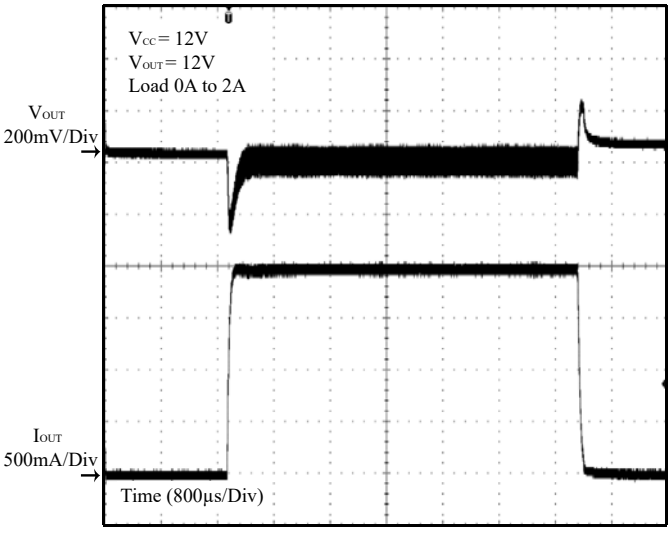


Figure 27 Load Transient

APPLICATION INFORMATION

The IS31PM3510 is a multi-topology DC-DC PWM controller with constant ON-Time Buck and constant OFF-Time Boost combination control scheme. It is able to regulate the output voltage set in between the input voltage operating range, with a single inductor while providing seamless transition between Buck, Buck-Boost, and Boost operating modes.

For the Buck-Boost topology, the IS31PM3510 needs two external power switches and two power Schottky diodes, as Figure 1.

Figure 28 shows a simplified diagram of how the two switches and two Schottky diodes are connected to the inductor L_1, the peak/valley current sense resistor R_{CS}, input over current sense resistor R_{INSEN}, power supply input V_{CC}, power output V_{OUT}, and ground. The current sense resistor R_{CS} connected to CS pin provides inductor current information for both peak current detection of Boost control loop and reverse valley current detection of Buck control loop. The input current sense resistor R_{INSEN} connected to VCC and INSENSE pins is a secondary protection to protect input over current fault. The operation region is decided by the V_{OUT}/V_{CC} voltage ratio. The power switches are properly controlled to smoothly transition between regions. The hysteresis is added to prevent jittering between regions. As Figure 29.

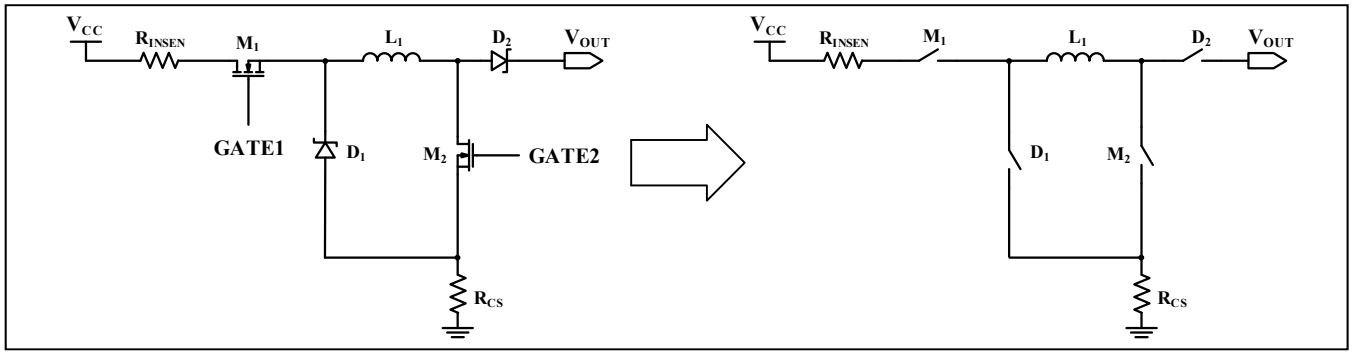


Figure 28 Simplified Diagram of Buck-boost Topology

As Figure 29, there are three operating states decided by the V_{OUT}/V_{CC} voltage ratio: (1) the operation mode is in constant ON-Time Buck region, (2) and (3) the operation mode is in constant ON-Time Buck and peak current Boost combination control Buck-Boost region, (4) the operation mode is in constant OFF-Time Boost region. The following sections give detailed description for each state with waveforms.

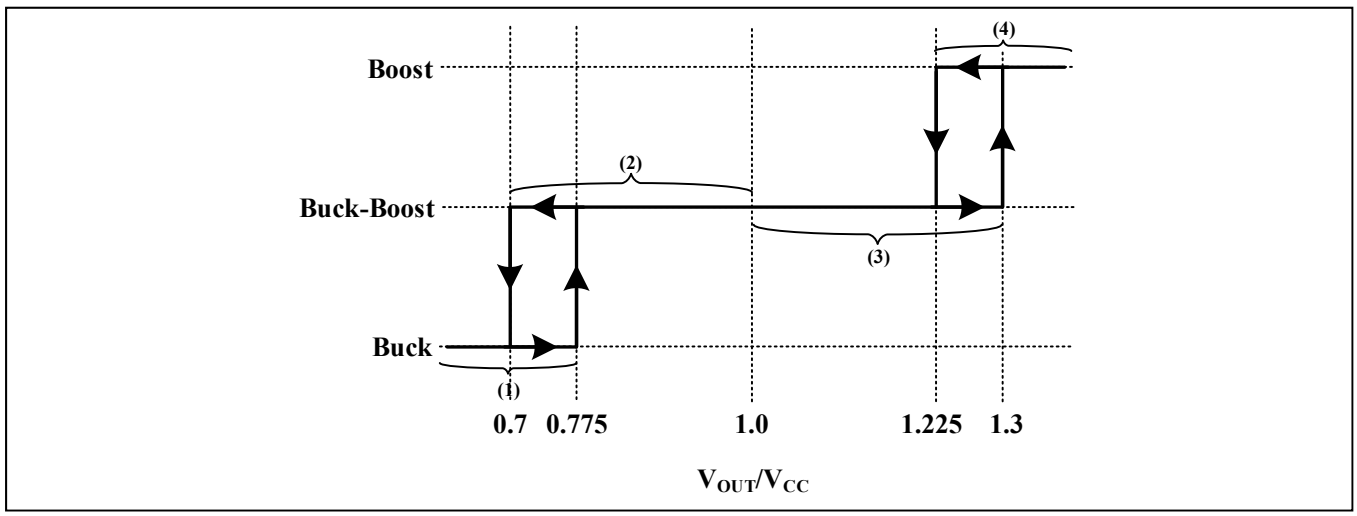


Figure 29 Operation Regions vs. V_{OUT}/V_{CC} Voltage Ratio

BUCK REGION (V_{CC} >> V_{OUT})

When the power supply voltage V_{CC} is much higher than the output voltage V_{OUT}, the IS31PM3510 uses constant ON-Time and valley current control in Buck region (Figure 30). The switch M_2 is always off and the Schottky diode D_2 is always active. At the beginning of each cycle, the switch M_1 is turned on and the current ramps up through the switch M_1, the inductor L_1 and the Schottky diode D_2 into output loading. When the constant ON-Time of the Buck control loop is expired, the switch M_1 is turned off and the recirculating Schottky diode D_1 is active. So the current ramps down through the current sense resistor R_{CS}, the recirculating Schottky diode D_1, the inductor L_1 and the Schottky diode D_2 into the output loading. Once the current hits the valley current threshold of the Buck control loop, detected by the current sense resistor R_{CS} in series with D_1, the switch M_1 is turned on again. The next cycle starts and repeats the above control.

In Buck region, since the switch M_2 is always off and the Schottky diode D_2 is always active, both of M_2 and D_2 can be omitted. It behaves like a typical asynchronous Buck regulator. As Figure 3 configuration.

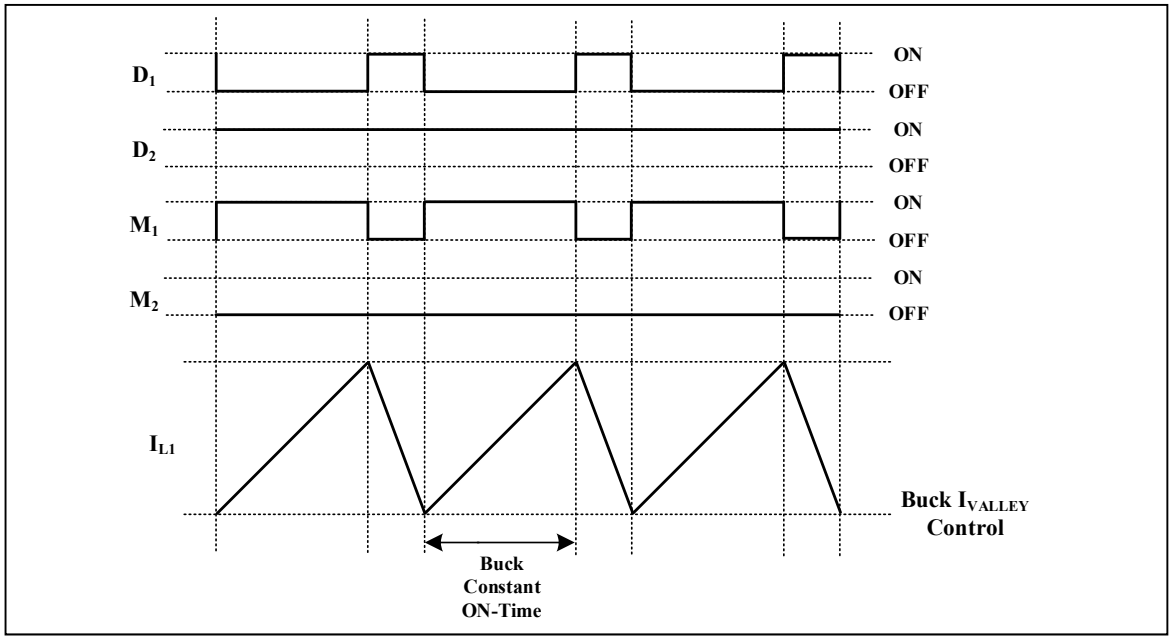


Figure 30 Buck Region (V_{CC} >> V_{OUT} Region)

BUCK-BOOST REGION (V_{CC} ~> V_{OUT})

When the power supply voltage V_{CC} is slightly higher than the output voltage V_{OUT}, the IS31PM3510 uses constant ON-Time Buck and peak current Boost combination control in Buck-Boost region (Figure 31). At the beginning of each cycle, both of the switches M_1 and M_2 are turned on and both of the Schottky diodes D_1 and D_2 are in off state. The current ramps up through the switch M_1, the inductor L_1, the switch M_2 and the current sense resistor R_{CS} to ground. When the current hits the peak current threshold of the Boost control loop, detected by the current sense resistor R_{CS} in series with the switch M_2, the switch M_2 is turned off and the Schottky diode D_2 is active. The current keeps slowly ramping up through the switch M_1, the inductor L_1 and the Schottky diode D_2 into the output loading until the constant ON-Time of the Buck control loop being expired and the switch M_1 is turned off. Then the recirculating Schottky diode D_1 is active. The current fast ramps down through the current sense resistor R_{CS}, the Schottky diode D_1, the inductor L_1, and the Schottky diode D_2 into the output loading. Once the current hits the valley current threshold of the Buck control loop, detected by the current sense resistor R_{CS} in series with D_1, both of the switches M_1 and M_2 are turned on again. The next cycle starts and repeats the above control.

Note that there is a 100ns (Typ.) dead-time control at the beginning of each cycle. The switch M_2 is delayed for 100ns (Typ.) to be turned on after the switch M_1 being turned on, that is helpful to minimize the switching noise. The dead-time is ignored in Figure 31 waveform.

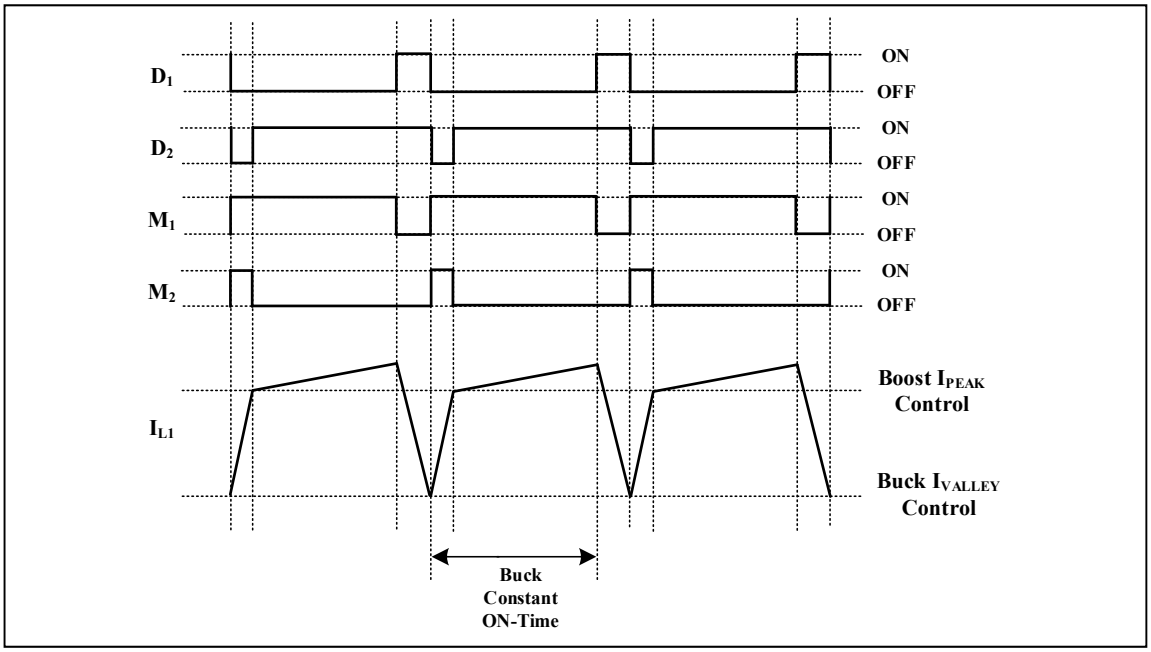


Figure 31 Buck-Boost Region (V_{CC} ~> V_{OUT} Region)

BUCK-BOOST REGION (V_{CC} <~ V_{OUT})

When the power supply voltage V_{CC} is slightly lower than the output voltage V_{OUT}, the IS31PM3510 uses constant ON-Time Buck and peak current Boost combination control in Buck-Boost region (Figure 32). At the beginning of each cycle, both of the switches M_1 and M_2 are turned on and both of the Schottky diodes D_1 and D_2 are in off state. The current ramps up through the switch M_1, the inductor L_1, the switch M_2 and the current sense resistor R_{CS} to ground. When the current hits the peak current threshold of the Boost control loop, detected by the current sense resistor R_{CS} in series with the switch M_2, the switch M_2 is turned off and the Schottky diode D_2 is active. The current starts to slowly ramp down through the switch M_1, the inductor L_1 and the Schottky diode D_2 into the output loading until the constant ON-Time of the Buck control loop being expired and the switch M_1 is turned off. Then the recirculating Schottky diode D_1 is active. The current fast ramps down through the current sense resistor R_{CS}, the Schottky diode D_1, the inductor L_1, and the Schottky diode D_2 into the output loading. Once the current hits the valley current threshold of the Buck control loop, detected by the current sense resistor R_{CS} in series with D_1, both of the switches M_1 and M_2 are turned on again. The next cycle starts and repeats the above control.

Note that there is a 100ns (Typ.) dead-time control at the beginning of each cycle. The switch M_2 is delayed for 100ns (Typ.) to be turned on after the switch M_1 being turned on, that is helpful to minimize the switching noise. The dead-time is ignored in Figure 32 waveform.

BOOST REGION (V_{CC} << V_{OUT})

When the power supply voltage V_{CC} is much lower than the output voltage V_{OUT}, the IS31PM3510 uses constant OFF-Time and peak current control in Boost region (Figure 33). The switch M_1 is always on and the Schottky diode D_1 is always in off state. At the beginning of each cycle, the switch M_2 is turned on and the current ramps up through the switch M_1, the inductor L_1, the current sense resistor R_{CS} and the switch M_2 to ground. When the current hits the peak current threshold of the Boost control loop, detected by the current sense resistor R_{CS} in series with M_2, the switch M_2 is turned off and the recirculating Schottky diode D_2 is active. So the current ramps down through the switch M_1, the inductor L_1 and the Schottky diode D_2 into the output loading. The switch M_2 keeps off until the constant OFF-Time of the Boost control loop being expired and it turns on again. The next cycle starts and repeats the above control.

In Boost region, since the switch M_1 is always on and the Schottky diode D_1 is always in off state, both of M_1 and D_1 can be omitted. It behaves like a typical asynchronous Boost regulator. As Figure 2 configuration.

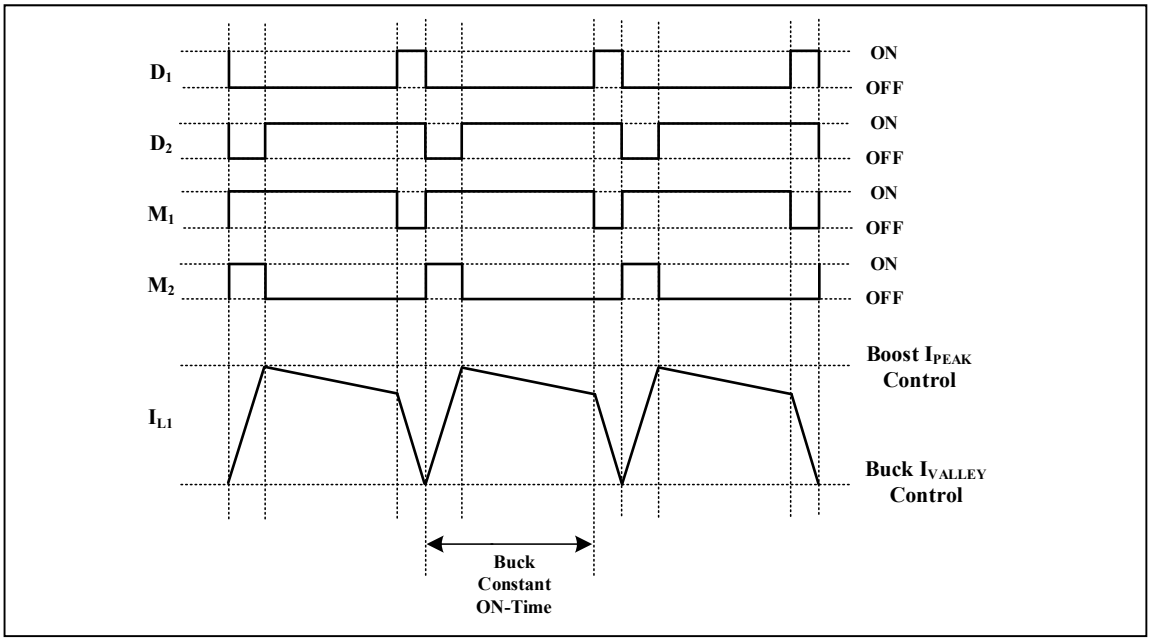


Figure 32 Buck-Boost Region (V_{CC} <~ V_{OUT} Region)

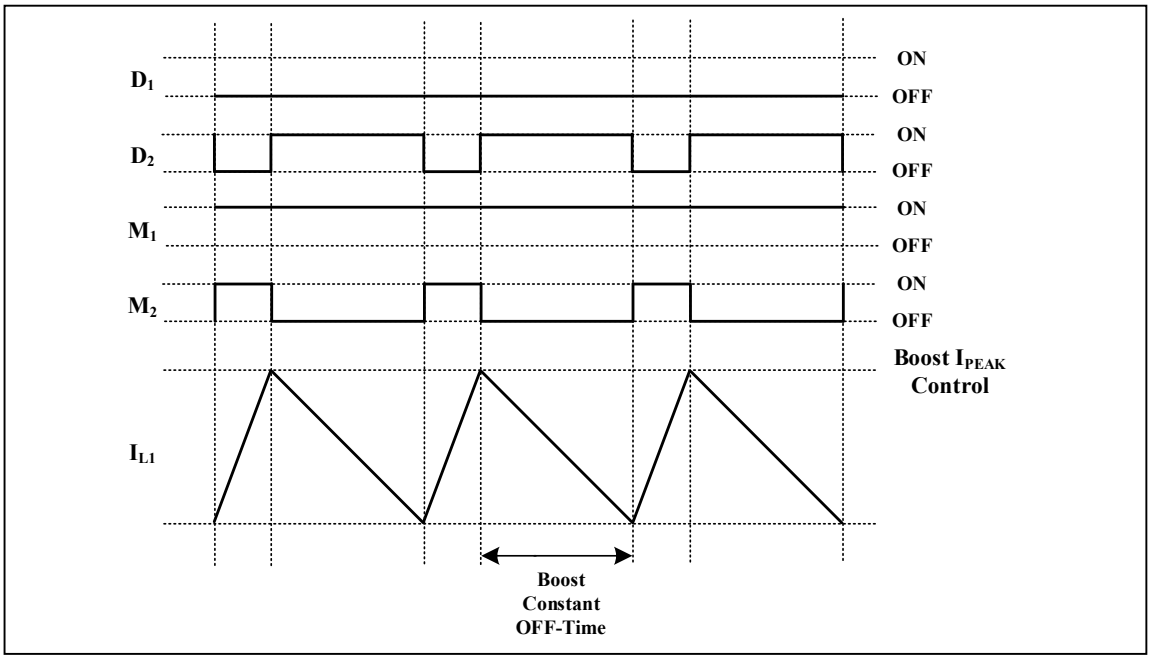


Figure 33 Boost Region (V_{CC} << V_{OUT} Region)

VCC UNDER VOLTAGE LOCKOUT (UVLO)

IS31PM3510 features an under voltage lockout (UVLO) function on the VCC pin to prevent unintended operation at too low input voltages. UVLO threshold is an internally fixed value and cannot be adjusted. The device disables the output when the V_{CC} voltage drops below V_{UVLO} (Typ. 4.0V), and resumes normal operation when the V_{CC} voltage rises above (V_{UVLO}+V_{UVLO_HY}) (Typ. 4.2V).

INTERNAL LINEAR REGULATORS

The device integrates a linear regulator (VDD) with 6.0V (Typ.) and I_{VDD_LM} current capability to power internal circuitry and low-side NMOS gate driver (GATE2) in the IS31PM3510. During operation, the external low-side NMOS will draw transient high current from this linear regulator. Therefore, a 1μF low ESR, X7R type ceramic capacitor is necessary from VDD pin to GND; it must be placed as close to VDD pin as possible. This regulator also has the UVLO feature. The device disables the output when the V_{DD} voltage drops below V_{DD_UV} (Typ. 3.5V), and resumes normal operation with soft-start process when the V_{DD} voltage rises above (V_{DD_UV}+V_{DD_UVHY}) (Typ. 4.0V). This helps protect the external low-side NMOS from excessive power consumption due relatively higher $Rds_{(ON)}$ at such condition. An I_{VDD_LM} current limit on VDD pin

protects the IS31PM3510 from excessive power dissipation at high input voltage.

VDD can be used to bias external low current circuitry requiring a reference supply, such as pulling up bias voltage for PGOOD pin. However, to ensure stable operation of the IS31PM3510, do not recommend to power high current external device with VDD pin.

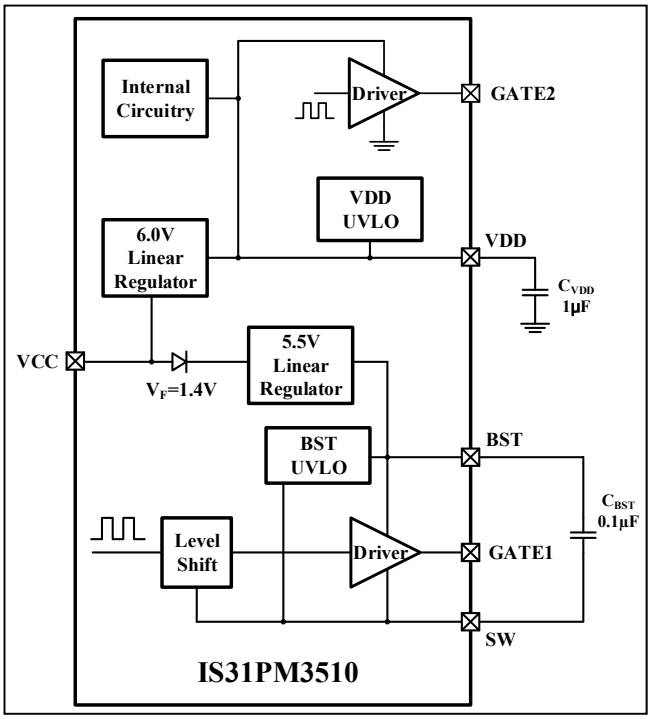


Figure 34 Linear Regulator

Beside the 6.0V linear regulator, there is another internal 5.5V linear regulator for high-side NMOS driver (GATE1). During operation, the external high-side NMOS will draw transient high current from this linear regulator. Therefore, a 0.1µF low ESR, X7R type ceramic, floating bootstrap capacitor is necessary from BST pin to SW; it must be placed as close to BST and SW pins as possible. This regulator is monitored by a separate under voltage lockout circuit, BST UVLO, whose threshold voltage refers to SW pin. The device stops switching when the (V_{BST}-V_{SW}) voltage drops below (V_{BTUV}-V_{BTUV_HY}) (Typ. 3.3V), and resumes normal operation when the (V_{BST}-V_{SW}) voltage rises above V_{BTUV} (Typ. 3.6V). This helps protect the external high-side NMOS from excessive power consumption due to relatively higher $Rds_{(ON)}$ resulting from insufficient gate drive voltage.

These two linear regulators will be supplied to the GATE1/2 pins to drive power NMOSs. The driving current can be calculated from the following Equation (1):

$$I_{GATE} = f_{SW} \times (Q_{G1} + Q_{G2}) \qquad (1)$$

Where f_{SW} is operating frequency of IS31PM3510 and Q_{G1} and Q_{G2} are the total gate charge of power switches, M_1 and M_2.

Choosing power NMOSs with lower Q_G will improve the efficiency and allow higher switching frequency. It is important to consider the NMOS threshold voltage when operating in the dropout region when the input voltage (V_{CC}) is below the regulation level of these two regulators. If the device is required to operate at an input voltage less than 7V, recommend power NMOSs with a threshold voltage ($V_{GS(th)}$) below 3V and add an external BST diode from the VDD pin to BST pin which can enhance the high-side NMOS driving and improve the efficiency. The recommended external BST diode is 1N4148.

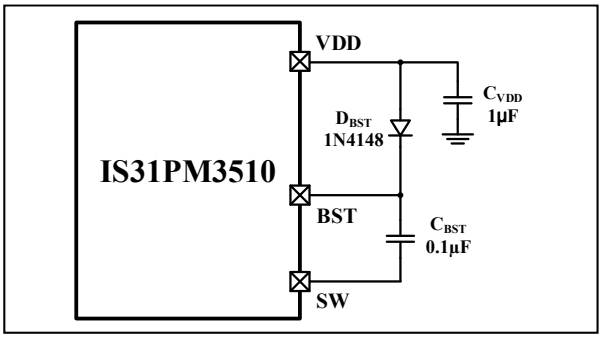


Figure 35 External BST Diode

ENABLE AND SHUTDOWN

The EN pin is an enable input for the device, pull it higher than V_{IH} to enable the device; pull it lower than V_{IL} to force the device into shutdown mode with an ultra-low quiescent current. EN pin has an internal 200kΩ (Typ.) pull-down resistor to ground. If the shutdown mode is unused, connect the EN pin to the VCC pin via a 10kΩ resistor.

SOFT-START

The IS31PM3510 provides a built-in soft-start function. The function of soft-start is made for the regulator to gradually reach the steady state operating point, thus dampening the inrush current to an acceptable value at startup. When the device starts, the internal circuitry generates a soft-start voltage ramping from 0V to V_{DD}. When it is lower than the internal reference of error amplifier (EA), the soft-start voltage overrides EA's reference so the EA uses the soft-start voltage as the reference. Once the soft-start voltage exceeds EA's reference, EA's reference regains loop control. The soft-start period time is internally fixed at 5ms (Typ.) and not adjustable.

OPERATING FREQUENCY

The operating frequency of the device is programmable from 150kHz to 650kHz range using a single resistor R_{FSET} connected between FS/SYNC pin to ground. Selection of the operating frequency is a tradeoff between overall conversion efficiency and component size. Higher frequency operating results in smaller component size but increases the switching losses and power NMOS gate driving current, and may not allow sufficiently high or low duty cycle due to minimum ON-Time and minimum OFF-Time limitation. Lower

frequency gives better efficiency performance but results in larger component size. In applications, an operating frequency of 400kHz is a good compromise between component size and efficiency. It makes the system easier to filter switching noise from sensitive frequency bands and pass the EMI test.

To set a desired frequency, the resistor value can be calculated by following Equation (2):

$$R_{FSET} = \frac{5\times10^4}{f_{SW}-12} - 3.5 \qquad (2)$$

(74.9kΩ ≤ R_{FSET} ≤ 358.8kΩ)

Where R_{FSET} is in kΩ. f_{SW} is the operating frequency in kHz.

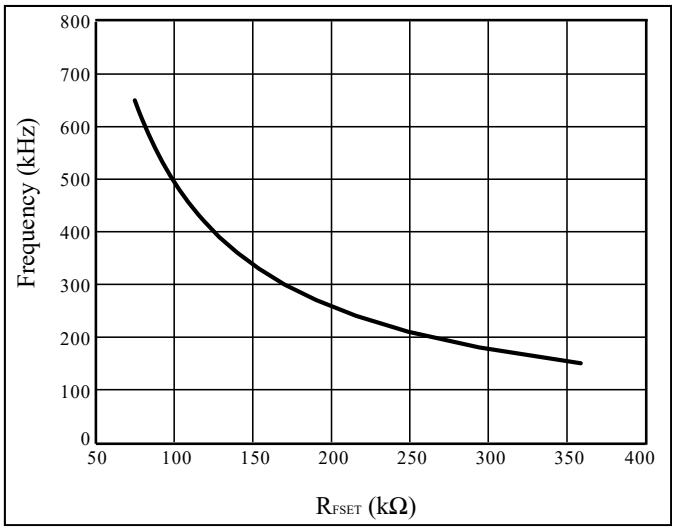


Figure 36 f_{SW} vs. R_{FSET}

If the FS/SYNC pin is connected to an extremely low or high value resistor, equivalent to an open or shorted to ground condition, the operating frequency will be clamped by internal 400kHz oscillator.

FREQUENCY SYNCHRONIZATION

The FS/SYNC pin can also be used as a synchronization input, allowing the IS31PM3510 to operate with an external clock in the range of 150kHz to 650kHz as long as its pulse width satisfies the requirements of t_{ON_SYNC} and t_{OFF_SYNC}, and its voltage level satisfies V_{IH_SYNC} and V_{IL_SYNC}. When an external synchronization clock is applied to the FS/SYNC pin, the internal oscillator is over-driven so that each switching cycle begins at the rising edge of external clock. When an external synchronization clock is detected, Figure 37 shows the timing for a synchronization clock into the IS31PM3510 at 500kHz. Any pulse with a duty cycle of 15% to 85% at 500kHz can be used to synchronize the IC. However, driving FS/SYNC pin with a 50% duty cycle waveform is always a good choice.

Table 1 Synchronization Duty Cycle Range

SYNC Clock Frequency(kHz)	Duty Cycle Range (%)
650	19.5 ~ 80.5
500	15 ~ 85
400	12 ~ 88
300	9 ~ 91
250	7.5 ~ 92.5
150	4.5 ~ 95.5

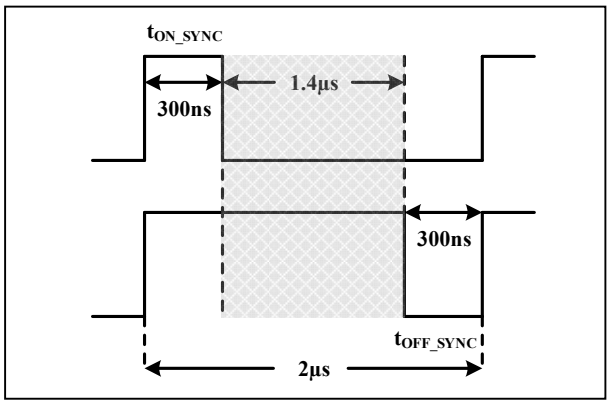


Figure 37 SYNC Pulse On And Off Time Requirements

SPREAD SPECTRUM

In switching topologies, EMI is a major concern. To optimize the EMI performance, the IS31PM3510 includes a spread spectrum feature, which is a 500Hz (Typ.) with ±10% (Typ.) operating frequency jitter. Spread spectrum effectively spreads the total electromagnetic emitting energy from a narrow band to a wide band lowering in the process the peak energy of EMI profile. Spread spectrum, reduces filter size and cost to pass EMI regulatory test. Note that when FS/SYNC pin is open or shorted to ground, spread spectrum function is disabled.

OUTPUT VOLTAGE SETTING

The output voltage is set by selecting the values of the FB resistor divider, R_{FB1} and R_{FB2}, according to the following equation:

$$V_{OUT} = V_{FB\_TH} \times \frac{R_{FB1} + R_{FB2}}{R_{FB2}} \qquad (3)$$

In order to have an accurate output voltage, precision resistors are preferred (±1% recommended). The R_{FB1} and R_{FB2} resistors should be placed as close as possible to the IS31PM3510 device with minimal trace length to FB and AGND pins.

MAXIMUM AND MINIMUM INPUT VOLTAGE

With a given output voltage, the maximum input voltage is limited by minimum ON-Time of high-side NMOS in Buck region and the minimum input voltage is limited by minimum OFF-Time of low-side NMOS in Boost

region.

In Buck region, the operating duty cycle is approximately given as below:

$$D_{BK} = \frac{V_{OUT}}{V_{CC}} = \frac{t_{ON}}{t_{ON} + t_{OFF}} = t_{ON} \times f_{SW} \quad (4)$$

$$V_{CC} = \frac{V_{OUT}}{t_{ON} \times f_{SW}} \quad (5)$$

Where D_{BK} is the operating duty cycle in Buck region. t_{ON} and t_{OFF} are the turn-on and turn-off time of high-side NMOS.

According to above equation, the allowable input voltage depends on the operating frequency and the high-side NMOS turn-on time. When the frequency is set, the maximum input voltage is limited by the minimum ON-Time of the high-side NMOS, Typ. 160ns. Due to the spread spectrum, the f_{SW} should choose the maximum of the operating frequency. For example, if the output voltage is set at 5V and the operating frequency is 650kHz, the maximum input voltage is:

$$V_{CC\_MAX} = \frac{V_{OUT}}{t_{BK\_MINON} \times f_{SW\_MAX}} = \frac{5V}{160ns \times (650kHz \times 110\%)} = 43.7V \quad (6)$$

In Boost region, the operating duty cycle is approximately given as below:

$$D_{BT} = \frac{V_{OUT} - V_{CC}}{V_{OUT}} = \frac{t_{ON}}{t_{ON} + t_{OFF}} = 1 - t_{OFF} \times f_{SW} \quad (7)$$

$$V_{CC} = t_{OFF} \times f_{SW} \times V_{OUT} \quad (8)$$

Where D_{BT} is the operating duty cycle in Boost region. t_{ON} and t_{OFF} are the turn-on and turn-off time of low-side NMOS.

According to above equation, the allowable input voltage depends on the operating frequency and the low-side NMOS turn-off time. When the frequency is set, the minimum input voltage is limited by the minimum OFF-Time of the low-side NMOS, Typ. 145ns. Due to the spread spectrum, the f_{SW} should choose the maximum of the operating frequency. For example, if the output voltage is set at 48V and the operating frequency is 650kHz, the minimum input voltage is:

$$V_{CC\_MIN} = t_{BT\_MINOFF} \times f_{SW\_MAX} \times V_{OUT} = 145ns \times (650kHz \times 110\%) \times 48V = 4.98V \quad (9)$$

Note that the maximum and minimum input voltage is affected by other operating parameters, such as the output current, the R_{DS_ON} of the NMOSs, the R_{DC} of the inductor L_1, the parasitic resistance of the PCB traces, the forward voltage of the Schottky diodes, and so on. Therefore, the maximum and minimum input voltage could slightly vary from above calculation.

To achieve wider input voltage range, a lower operating frequency could be considered.

INDUCTOR SELECTION

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor value. If the operating frequency is decided, inductor value involves trade-offs in performance. Larger inductance reduces inductor current ripple resulting in smaller output current ripple, however it also brings in unwanted parasitic resistance that degrades performance. The inductor value is determined based upon the operating frequency, output current, allowable current ripple, and input voltage and output voltage. Use the following equations to estimate the approximate inductor value:

For Boost:

$$L_{BOOST} \geq \frac{V_{CC\_MIN} \times (V_{OUT} - V_{CC\_MIN})}{f_{SW} \times \Delta I_L \times V_{OUT}} \quad (10)$$

For Buck:

$$L_{BUCK} \geq \frac{V_{OUT} \times (V_{CC\_MAX} - V_{OUT})}{f_{SW} \times \Delta I_L \times V_{CC\_MAX}} \quad (11)$$

Where V_{CC_MIN} is the minimum input voltage in volts, V_{CC_MAX} is the maximum input voltage in volts, V_{OUT} is the output voltage in volts, f_{SW} is the operating frequency in hertz. ΔIL is allowable inductor peak to peak ripple current in Amp. The inductor value has a direct effect on ripple current. In the Boost region, to keep the circuit in Continuous Conductive Mode (CCM), the maximum inductor current ripple ΔI_L should be chosen less than twice the input average current at the minimum input voltage. In the Buck region, to keep the circuit in Continuous Conductive Mode (CCM), the maximum inductor current ripple ΔI_L should be chosen less than twice the output LED current. The highest current ripple happens in the Buck region at maximum input voltage. If the application requires all operation regions, choose the inductor value based on the Buck's Equation.

For high efficiency, choose an inductor with low core loss. The inductor should have low DC resistance to reduce the I^2R losses, and its rating current must be greater than the maximum input average current and saturation current greater than maximum inductor peak current with some safety margin. To minimize radiated EMI noise, a shielded inductor is always a good choice.

MAXIMUM OUTPUT CURRENT AND CURRENT SENSE RESISTOR R_{CS} SELECTION

When the input voltage is much lower than the output voltage, the IS31PM3510 operates in constant OFF-Time and inductor peak current control Boost mode. In

Boost operation, the switch M_1 is always on. In the switch M_2 on phase, the inductor current ramps up through the switch M_2 and the current sense resistor R_{CS} to ground. The inductor peak current control is detected by the current sense resistor R_{CS} connected in series with the switch M_2.

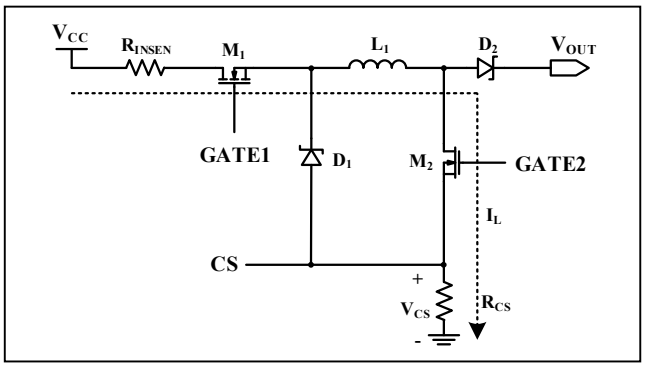


Figure 38 Boost Peak Current Detection in M_2 On Phase

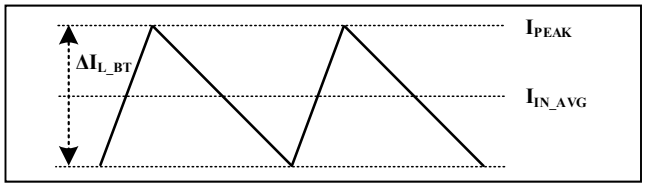


Figure 39 Boost Inductor Current

The inductor peak current limit protection threshold is set by the R_{CS} resistor, which determines the maximum output current of the Boost operation. So the maximum average load current at the minimum input voltage is:

$$I_{OUTBT\_MAX} = \frac{I_{IN\_AVG} \times V_{CC\_MIN}}{V_{OUT}}$$
$$= \left(I_{PEAK} - \frac{\Delta I_{L\_BT}}{2} \right) \times \frac{V_{CC\_MIN}}{V_{OUT}} \quad (12)$$
$$= \left(\frac{V_{CS\_TH1}}{R_{CS}} - \frac{\Delta I_{L\_BT}}{2} \right) \times \frac{V_{CC\_MIN}}{V_{OUT}}$$

Where, I_{IN_AVG} is the input average current at the minimum input voltage V_{CC_MIN}. V_{CS_TH1} is peak current limit threshold, typical 77mV for Boost operation. ΔI_{L_BT} is the inductor current ripple at minimum input voltage in Boost operation and can be calculated as:

$$\Delta I_{L\_BT} = \frac{V_{CC\_MIN} \times \left(V_{OUT} - V_{CC\_MIN} \right)}{f_{SW} \times L \times V_{OUT}} \quad (13)$$

The inductor peak current limit is cycle-by-cycle protection. Once the inductor peak current hits the current limit threshold, the GATE2 immediately pulls low to turn off the low-side power NMOS until the next switching cycle. If the output is over load, the inductor peak current keeps hitting the peak current limit and persists in longer than 2.5ms (Typ.) time frame, the IS31PM3510 will trigger hiccup protection, stop switching for t_{SKIP} and restart with the soft-start sequence. The hiccup will repeat until the peak current limit condition is removed. Besides the inductor peak current limit, the CS pin has a secondary peak current limit threshold, typical 110mV for Boost operation. Once the inductor peak current hits the secondary current limit, the hiccup protection is triggered directly.

When the input voltage is much higher than the output voltage, the IS31PM3510 operates in constant ON-Time and inductor valley current control Buck mode. In Buck operation, the switch M_2 is always off. In the switch M_1 off phase, the inductor current ramps down through the current sense resistor R_{CS} and the Schottky diode D_1, the inductor L_1 and the Schottky diode D_2 into the output loading. The inductor valley current control is detected by the current sense resistor R_{CS} connected in series with the Schottky diode D_1.

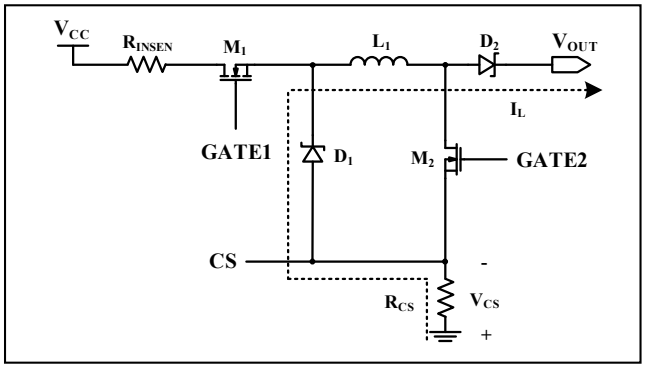


Figure 40 Buck Valley Current Detection in M_1 Off Phase

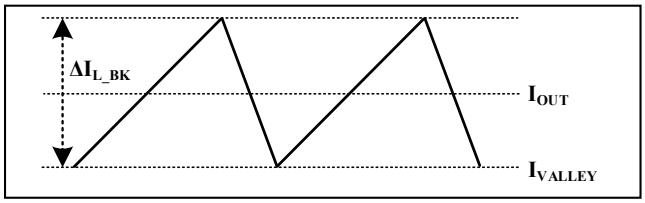


Figure 41 Buck Inductor Current

The inductor valley current limit protection threshold is set by the R_{CS} resistor, which determines the maximum output current of the Buck operation. So the maximum average load current is:

$$I_{OUTBK\_MAX} = I_{VALLEY} + \frac{\Delta I_L}{2} = \frac{\left| V_{CS\_TH1} \right|}{R_{CS}} + \frac{\Delta I_{L\_BK}}{2} \quad (14)$$

Where, V_{CS_TH1} is valley current limit threshold, typical -67mV for Buck. ΔI_{L_BK} is the inductor current ripple at minimum input voltage in Buck operation and can be calculated as:

$$\Delta I_{L\_BK} = \frac{V_{OUT} \times \left(V_{CC\_MIN} - V_{OUT} \right)}{f_{SW} \times L \times V_{CC\_MIN}} \quad (15)$$

The inductor valley current limit is cycle-by-cycle protection. In case of the output is over load and the inductor valley current exceeds the valley current limit, the high-side NMOS will keep off state to clamp the inductor valley current at the valley current limit threshold. If the inductor valley current persists at the

valley current limit for longer than 2.5ms (Typ.), the IS31PM3510 will trigger hiccup protection, stop switching for t_{SKIP} and restart with the soft-start sequence. The hiccup will repeat until the valley current limit condition is removed. Similar to the Boost operation, the CS pin has a secondary peak current limit threshold, typical -110mV for Buck operation. Once the inductor peak current hits the secondary current limit, the hiccup protection is triggered directly.

Therefore, the R_{CS} resistor value is chosen based on the required maximum output current.

If the maximum load current is given, I_{OUT_MAX}, the maximum current sense resistor R_{CS} value for the Boost operation is:

$$R_{CSBT\_MAX}=\frac{2\times V_{CS\_TH1}\times V_{CC\_MIN}}{2\times I_{OUT\_MAX}\times V_{OUT}+\Delta I_{L\_BT}\times V_{CC\_MIN}} \quad (16)$$

Where, V_{CS_TH1} is peak current limit threshold, typical 77mV for Boost.

With the same maximum load current, the maximum current sense resistor R_{CS} value for the Buck operation is:

$$R_{CSBK\_MAX}=\frac{2\times\left|V_{CS\_TH1}\right|}{2\times I_{OUT\_MAX}-\Delta I_{L\_BK}} \quad (17)$$

Where, V_{CS_TH1} is valley current limit threshold, typical -67mV for Buck.

If the application only requires Buck operation (Figure 3 topology), the final R_{CS} value should be lower than R_{CSBK_MAX}. Otherwise, the final R_{CS} value should be lower than R_{CSBT_MAX}. A 30% margin is usually recommended.

DIODES SELECTION

To select D_1 and D_2, the reserve recovery characteristics and forward voltage drop are particular important characteristics to be considered. To achieve high efficiency, Schottky type diode with low forward voltage drop and fast recovery time is good choice. Fast recovery time minimizes the peak instantaneous power during turn-on transition of the power switches. Low forward voltage drop has a significant impact on the conversion efficiency, especially for applications with low output voltage. The reverse breakdown voltage rating of both diodes should be selected to be greater than maximum of V_{CC} and V_{OUT}, plus some safety margin. The current rating of both diodes should be greater than the maximum output load current with some safety margin. A conservation design would at least two times of the maximum output load current.

POWER NMOS SELECTION

The IS31PM3510 requires two external power NMOSs, one for high-side switch (M_1) and another for low-side switch (M_2). Important parameters for the power NMOSs are the drain to source breakdown voltage $V_{(BR)DSS}$, the gate threshold voltage $V_{GS(TH)}$, drain to source on-resistance $R_{DS(ON)}$, and drain to source current capability.

The $V_{(BR)DSS}$ must be greater than the maximum of V_{CC} and V_{OUT} together with overshoot voltage due to the ringing caused by parasitic inductances and capacitances, therefore keeping 20% safety margin. The gate drive voltage is sourced from the internal linear regulator, 6.0V (Typ.) for the low-side NMOS and 5.5V (Typ.) for the high-side NMOS. Consequently, low gate threshold voltage type NMOSs should be chosen to make sure the internal linear regulator voltage is sufficient to drive the NMOSs into full saturation. The consideration of the $R_{DS(ON)}$ of power NMOSs is usually secondary because the switching loss dominates the power lost, especially at high operating frequency. Power NMOSs with lower Q_G and $R_{DS(ON)}$ achieves higher efficiency and lower power losses. The continuous current rating of the selected power NMOSs should be higher than the input average current of Boost operation and the maximum current rating should be higher than the peak current limit protection level of Boost operation.

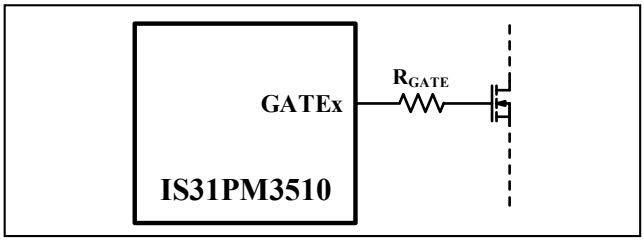


Figure 42 GATE Buffer Resistor

A buffer resistor can be considered to be added in series with the gate driving that slows down the switching rising and falling edge to minimize EMI. However, it increases the switching loss and degrades the efficiency at the same time. So the value should not be too large; a ten ohm is a good starting point. Please choose a proper value to compromise for both EMI test result and thermal performance.

INPUT AND OUTPUT CAPACITORS

Input and output capacitors are necessary to suppress voltage ripple caused by switched current. The use of low ESR capacitors is preferred to be used to efficiently reduce voltage ripple. Ceramic capacitors have excellent ESR characteristics and are good choice for input and output capacitors. A parallel combination of multiple ceramic capacitors is typically used to achieve ultra-low ESR and high capacitance. X7R type ceramic capacitors are recommended, as it retains the nominal capacitance value over wide voltage and temperature ranges. The ceramic capacitors should be placed near the regulator input and output. It's a good practice to put an additional 0.1μF~0.47μF ceramic capacitor on the input and output of the regulator to absorb high frequency switching spike. Ceramic capacitors, of at least 1μF, should also be placed from VCC to GND and

VOUT to GND as close to the IS31PM3510 pins as possible.

A typical regulator supply voltage has a large source impedance at the switching frequency. In the Buck operation, the input current is periodically interrupted with the on and off toggling of the high-side switch. When the high-side switch turns on, the input current into the high-side switch steps from zero to the valley of the inductor current waveform, then ramps up to the peak value, and then drops to the zero as the high-side switch turns off. The input capacitors must supply the most of the input current during the high-side switch on phase. Therefore, the input capacitors should be capable to handle the maximum RMS current in the Buck operation:

$$I_{INBK\_RMS} = I_{OUT\_MAX} \times \sqrt{(1-\frac{V_{OUT}}{V_{CC}}) \times \frac{V_{OUT}}{V_{CC}}} \qquad (18)$$

Where I_{OUT_MAX} is the maximum load current. The formula has a maximum at $V_{CC}=2\times V_{OUT}$, where $I_{INBK\_RMS}=I_{OUT\_MAX}/2$.

In the Boost operation, since the input current is uninterrupted, the demand for input capacitors is much less than in Buck mode. However the output current of the Boost mode is periodically interrupted with the on and off toggling of the low-side switch. When the low-side switch turns off, the output current through the output Schottky diode D_2 steps from zero to the peak of the inductor current waveform, then ramps down to the valley value, and then drops to the zero as the low-side switch turns on. The output capacitors must supply the entire output current during the low-side switch on phase. For this reason, the selection of the output capacitor is based on the Boost operation. Both bulk capacitance and ESR must be considered to ensure allowable output ripple voltage. The capacitance of the Boost mode can be estimated by:

$$C_{OUT\_MIN} = \frac{I_{OUT} \times (V_{OUT} - V_{CC\_MIN})}{\Delta V_{OUT\_RIP} \times f_{SW} \times V_{OUT}} \qquad (19)$$

$$ESR_{MAX} = \frac{\Delta V_{OUT\_RIP} \times V_{CC\_MIN}}{V_{OUT} \times I_{OUT\_MAX}} \qquad (20)$$

Where ΔV_{OUT_RIP} is allowable output ripple voltage. ESR_{MAX} is the maximum ESR of the output capacitors.

Note that the effective capacitance of ceramic capacitors decreases with DC bias. For larger bulk values of capacitance and lower cost, low ESR type electrolytic capacitors are usually used to be connected in parallel with the ceramic capacitors. However, electrolytic capacitors have poor tolerance, especially over temperature, and the selected value should be selected larger than the calculated value to allow for temperature variation.

LOOP COMPENSATION

The IS31PM3510 uses an internal transconductance error amplifier with COMP pin output that compensates the control loop. The external inductor, output capacitor and the compensation resistor and capacitor determine the loop stability. The inductor and output capacitor are chosen based on performance, size and cost. The compensation resistor and capacitor on the COMP pin are set to optimize control loop response and stability. Table 2 shows the recommended value for loop compensation of typical applications.

Table 2 Recommended Value for Loop Compensation

V_{CC} (V)	V_{OUT} (V)	R_{FB1} (kΩ)	R_{FB2} (kΩ)	R_{FSET} (kΩ)	L_1 (μH)	I_{OUT} (A)	C_{OUT} (μF)	R_{CS} (mΩ)	R_{CP} (kΩ)	C_{CP1} (nF)	C_{CP2} (pF)
8~24	5	32	10	120	10	3	77	20	47	10	50
8~24	12	91	10	120	6.8	3	77	13	20	10	200
8~24	16	124	10	120	10	3	77	10	20	22	300
8~24	24	190	10	120	15	2	77	10	27	22	300
8~24	48	390	10	120	22	1	77	10	62	22	200

LIGHT LOAD

The COMP pin voltage, V_{COMP}, is used to regulate the inductor current. The lighter load the lower V_{COMP}. If the load is too light which results in the V_{COMP} dropping to the internal PSM (Pulse Skipping Mode) threshold (around 1.1V), the IS31PM3510 will enter into PSM operation. When the V_{COMP} is below the PSM threshold, the IS31PM3510 stops switching for multiple cycles. Once the V_{COMP} rises above the PSM threshold, the IS31PM3510 recovers normal switching cycle. If the load is too light, the pulse skip switching period could be extended into audible noise frequency (>50μs), and the output voltage ripple may be higher than the normal switching operation. Choosing a larger output capacitor value will help minimize the output ripple. As the load increases from the light load condition, the operating resumes normal switching cycle.

INPUT CURRENT LIMIT

The IS31PM3510 has a standalone current sense monitor circuit which can be programmed with a current sense resistor R_{INSEN} connected in series with power supply, between VCC and INSENSE pins. When the voltage across R_{INSEN} hits the over current protection threshold V_{IN_OCTH} (Typ. 80mV), the high-side power switch M_1 will be turned off immediately. The input current limit must be set greater than the inductor peak current limit of the Boost operation, with a recommended 30% margin.

$$I_{IN\_LIM} = 1.3 \times \frac{V_{CS\_TH1}}{R_{CS}} \qquad (21)$$

So

$$R_{INSEN} = \frac{V_{IN\_OCTH} \times R_{CS}}{1.3 \times V_{CS\_TH1}} \qquad (22)$$

Where, V_{CS_TH1} is peak current limit threshold, typical 77mV for Boost.

In Boost topology (as Figure 2), when the high-side switch M_1 is omitted, the input current limit function will not be available. If the output is shorted to ground, the input power supply V_{CC} is shorted by the inductor L_1 and the Schottky diode D_2 to ground. The uncontrolled huge current I_{SHORT} may damage the components as well as power supply. As Figure 43.

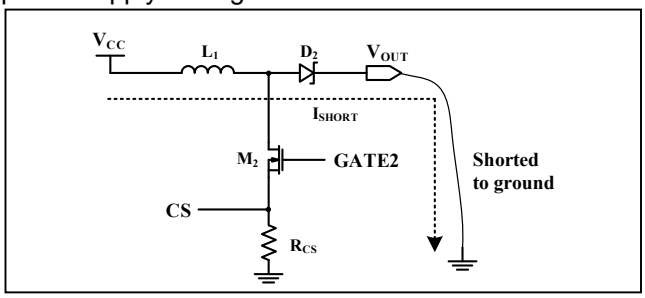


Figure 43 Output Shorted to Ground of Boost Topology

To avoid this fault condition, the Buck-Boost topology can be considered for the Boost applications.

If the application only requires Buck operation (Figure 3 topology), the input current limit can be set above 3 times of the maximum output current. So the R_{INSEN} value can be calculated by the following Equation (23):

$$R_{INSEN} = \frac{V_{IN\_OCTH}}{3 \times I_{OUT\_MAX}} \qquad (23)$$

If the application requires only Buck operation (Figure 3 topology), the R_{INSEN} value can be calculated by the Buck Equation (23). If the application requires other operating regions (Figure 1 or 2 topology), calculate R_{INSEN} value based on the Boost Equation (22).

If the input current limit function is unused, directly connect the INSENSE pin to the VCC pin.

OUTPUT OVER VOLTAGE PROTECTION

The IS31PM3510 provides Over Voltage Protection (OVP) through VOUT pin to avoid accidental IC damage, caused for example by an error on FB resistor value. The OVP protection is internally fixed threshold 58V (Typ.). In case the output voltage hits 58V (Typ.), the IS31PM3510 will stop switching immediately and will only resume operation once the output voltage drops below 53V (Typ.). This protection is provided to prevent catastrophic failures from accidental device over voltage breakdown.

THERMAL SHUTDOWN PROTECTION

The temperature of the die is monitored to protect the device from damage when the maximum junction temperature is exceeded. If the die temperature exceeds the thermal shutdown temperature of 170°C (Typ.) the device will stop switching and enter standby mode. After a thermal shutdown event, the IS31PM3510 will not try to restart when its die temperature has reduced to less than 150°C (Typ.).

POWER GOOD

The IS31PM3510 has a dedicated flag output pin, PGOOD, to indicate output power good state. The PGOOD pin is open drain structure which requires an external pull-up resistor connected to a voltage source. The recommended pull-up resistor is 47kΩ. The PGOOD pin goes high after a delay time t_{PG_RC} (Typ. 250μs) if the output voltage is within 90% to 111% of the nominal voltage; while it goes low after a delay time t_{PG_RP} (Typ. 17μs) if the output voltage is above 111% or below 90% of the nominal voltage. To prevent glitch both the upper and lower thresholds include 3.33% of hysteresis.

The PGOOD pin is also actively pulled low during several other conditions, including EN low, VCC/VDD UVLO protection, output OVP protection and thermal shutdown protection.

PCB LAYOUT CONSIDERATION

As for all switching power supplies, especially those providing high current and using high switching frequencies, PCB layout is a very critical design phase. If layout is not carefully done, operation instability as well as EMI problems may arise.

The high dV/dt surface and dI/dt loops are big noise emission sources. To optimize the EMI performance, keep the area size of all high switching frequency points with high voltage very compact. Meantime, keep all traces carrying high current as short as possible to minimize the loops.

Please design the PCB layout according to following considerations.

(1) Wide and short traces should be used for connection of the high current paths that helps to achieve better efficiency and EMI performance.

Such as the traces of power supply, inductor L_1, power switches M_1 and M_2, Schottky diodes D_1 and D_2, current sense resistor R_{CS} and R_{INSEN}, output to load, ground.

(2) Minimize the PCB area of the switching current loops. The input capacitors C_{IN}, inductor L_1, power switches M_1 and M_2, Schottky diodes D_1 and D_2, current sense resistor R_{CS}, and output capacitors C_{OUT} should be placed as close to each other as possible and the traces of connection between them should be as short and wide as possible.

(3) The (-) terminals of the input capacitors C_{IN} should be connected as close as possible to the (-) terminals of the output capacitors C_{OUT}.

(4) Connect the bootstrap capacitor, C_{BST}, closely to the BST and SW pins.

(5) The output voltage setting resistor divider, R_{FB1} and R_{FB2}, must be placed as close to FB and AGND pins as possible.

(6) The ground of the current sense resistor, R_{CS}, should be directly connected to PGND pin by a separate trace to prevent PGND plane jitter to ensure precise sensing.

(7) To avoid the ground jitter, the components of parameter setting should be placed close to the corresponding pins and return to the AGND pin, and keep the traces length to the pins as short as possible. On the other side, to prevent the noise coupling, the traces of these components should either be far away or be isolated from high-current paths and high-speed switching nodes. These practices are essential for better accuracy and stability.

(8) The capacitor C_{VCC} and C_{VDD} should be placed as close as possible to VCC and VDD pin for good filtering.

(9) Flood all unused areas on all layers with copper that reduces the temperature rise of the power components. Connect the copper areas to PGND.

(10) All thermal pads on the back of IS31PM3510, the Schottky diodes and the power NMOSs package must be soldered to a sufficient size of copper plane with sufficient vias to conduct the heat to opposite side PCB for adequate cooling.

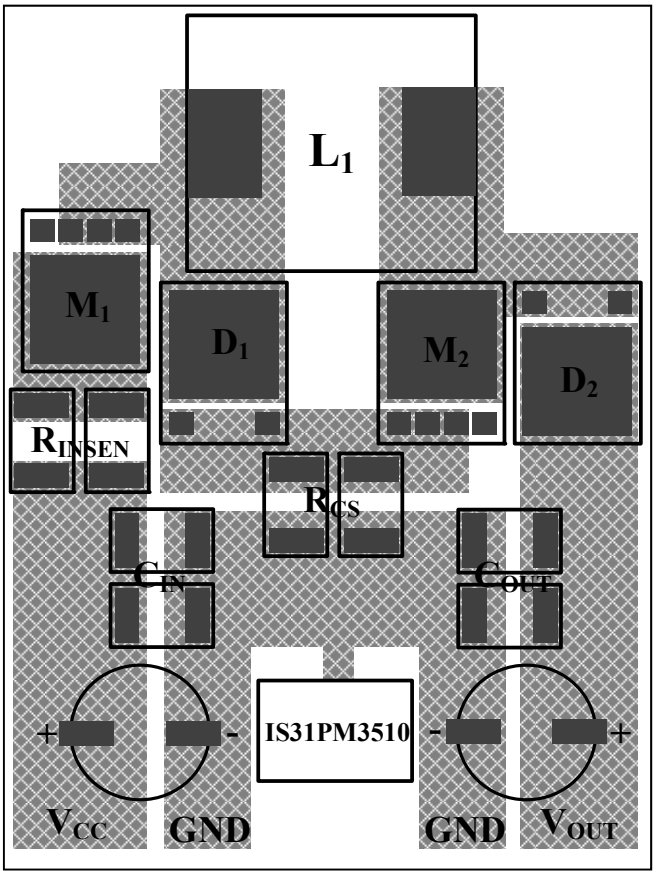


Figure 44 PCB Layout Example

THERMAL CONSIDERATIONS

The package thermal resistance, θ_{JA}, determines the amount of heat that can pass from the silicon die to the surrounding ambient environment. The θ_{JA} is a measure of the temperature rise created by power dissipation and is usually measured in degree Celsius per watt (°C/W). The junction temperature, T_J, can be calculated by the rise of the silicon temperature, ΔT, the power dissipation, PD, and the package thermal resistance, θ_{JA}, as in Equation (24):

$$P_D = V_{CC} \times (I_{CC} + f_{SW} \times (Q_{G1} + Q_{G2})) \quad (24)$$

And,

$$T_J = T_A + \Delta T = T_A + P_D \times \theta_{JA} \quad (25)$$

Where f_{SW} is operating frequency. Q_{G1} and Q_{G2} is the total gate charge of M_1 and M_2.

When operating the chip at high ambient temperatures, or when driving maximum load current, care must be taken to avoid exceeding the package power dissipation limits. The maximum power dissipation can be calculated using the following Equation (26):

$$P_{D(MAX)} = \frac{150°C - 25°C}{\theta_{JA}} \quad (26)$$

So,

$$P_{D(MAX)} = \frac{150\ °C - 25\ °C}{47.4\ °C/W} \approx 2.64\ W \qquad (27)$$

for eTSSOP-16 package.

Figure 45, shows the power derating of the IS31PM3510 on a JEDEC boards (in accordance with JESD 51-5 and JESD 51-7) standing in still air.

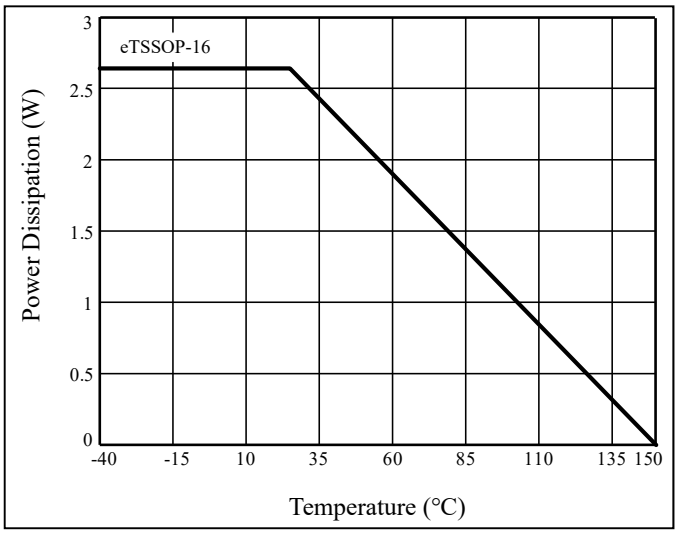


Figure 45 Dissipation Curve (eTSSOP-16)

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

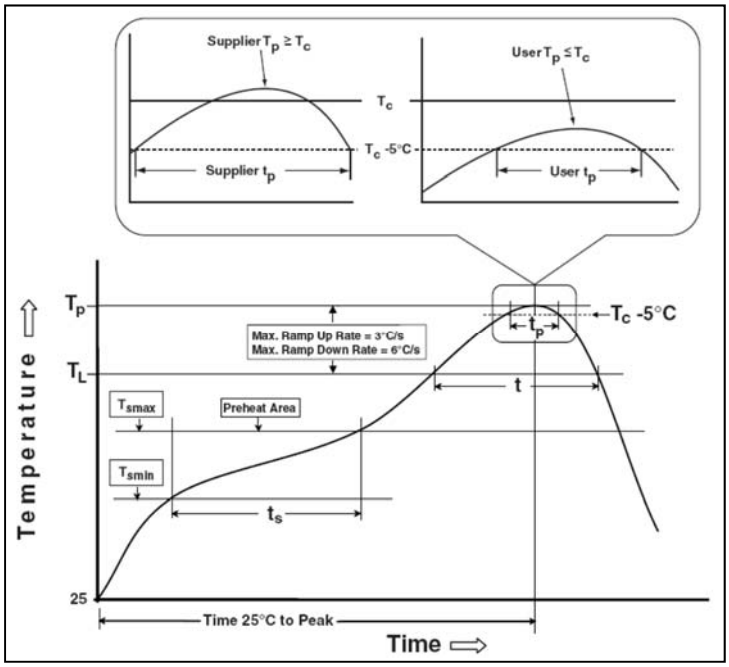
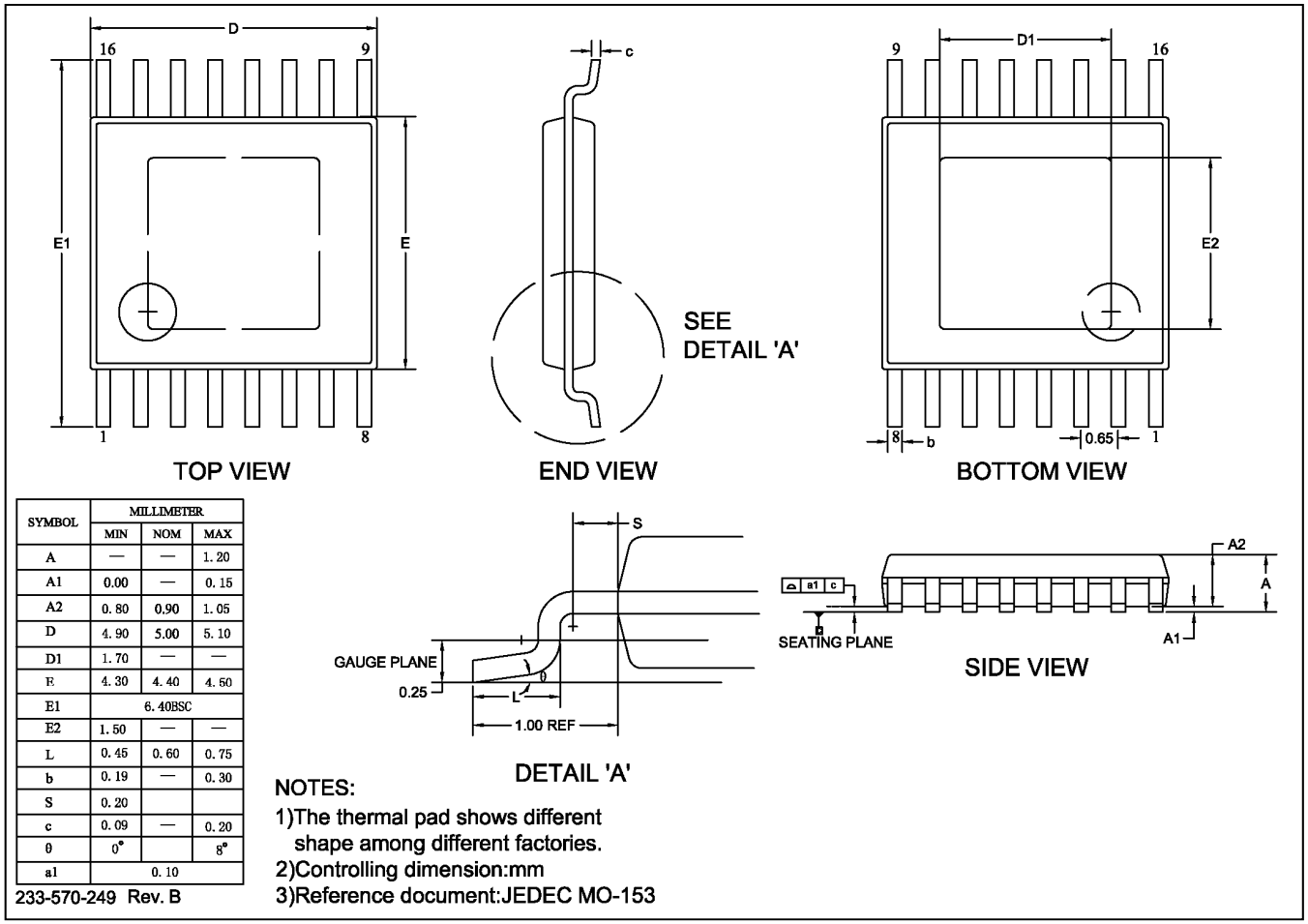


Figure 46 Classification Profile

PACKAGE INFORMATION

eTSSOP-16



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.00	—	0.15
A2	0.80	0.90	1.05
D	4.90	5.00	5.10
D1	1.70	—	—
E	4.30	4.40	4.50
E1	6.40BSC		
E2	1.50	—	—
L	0.45	0.60	0.75
b	0.19	—	0.30
S	0.20		
c	0.09	—	0.20
θ	0°		8°
a1	0.10		

233-570-249 Rev. B

NOTES:

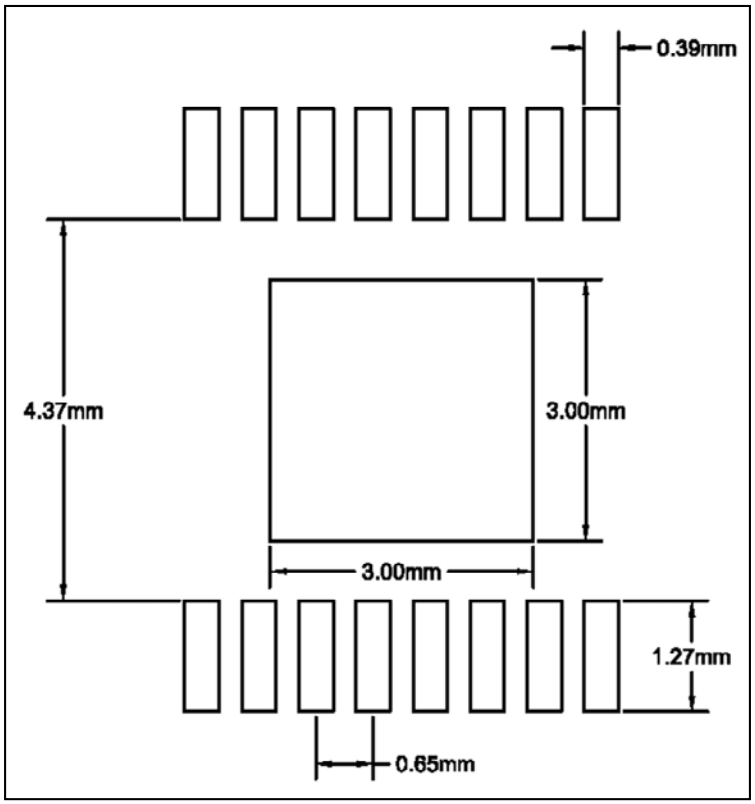
1)The thermal pad shows different shape among different factories.

2)Controlling dimension:mm

3)Reference document:JEDEC MO-153

RECOMMENDED LAND PATTERN

eTSSOP-16



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. user's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
A	Initial release	2021.10.26
B	1.Update to new Lumissil logo 2.Add RoHS	2024.03.22