IS31LT3957A

HIGH VOLTAGE LED LIGHTING CONTROLLER WITH FAULT PROTECTION

July 2024

GENERAL DESCRIPTION

The IS31LT3957A is a current mode PWM controller designed to drive a low side external NMOS FET for wide input/output voltage range and high LED current applications. An external resistor senses the high side output current of the LED string. A high side sense is the most flexible current sensing scheme, since it functions in either boost or buck-boost mode configurations. The controller can be configured with an external resistor to operate between 100kHz~1MHz frequency resulting in small external inductor and capacitors while maintaining high efficiency. A single capacitor is all that is required to set the spread spectrum dither frequency to reduce the radiated peak emission and optimize the system EMI performance.

The IS31LT3957A integrates circuity to detect output open/short, RT/SYNC pin short, VDD short, VCC under voltage lockout and over temperature fault conditions. These failure conditions can be reported by the open drain fault reporting FAULTB pin.

An MCU can be easily interfaced with the IS31LT3957A to perform dimming control and respond to fault report conditions. Dimming can be either analog and/or PWM input. An input DC voltage in the range of 0.1V ~ 1.1V on the ICTRL pin is required for analog dimming. A digital signal with varying duty cycle on the PWM/EN pin will achieve PWM dimming.

The IS31LT3957A is available in an eTSSOP-16 package with an exposed pad for enhanced thermal dissipation. It operates from 5V to 75V over the temperature range of -40°C to +125°C.

FEATURES

- Wide high voltage input range: 5V to 75V
- Supports boost, buck-boost, SEPIC and buck topology
- ±2% output current accuracy
- Adjustable operating frequency range of 100kHz~1MHz
- Programmable soft start to avoid inrush current
- Fixed under voltage lockout threshold
- EMI reduction capabilities
  - Programmable spread spectrum function
  - Operating frequency synchronization with external clock source
- Supports either analog or PWM dimming
- Fault protection with reporting:
  - VCC under voltage lockout (not reported)
  - Programmable output over voltage protection
  - Output short circuit protection
  - RT/SYNC pin short protection
  - VDD pin short protection
  - VDD under voltage lockout (not reported)
  - Over temperature protection
- RoHS & Halogen-Free Compliance
- TSCA Compliance

APPLICATIONS

- General high power LED
- Architecture lighting
- Motorcycle headlight
- Exit Signs and Emergency Lighting

TYPICAL APPLICATION CIRCUIT

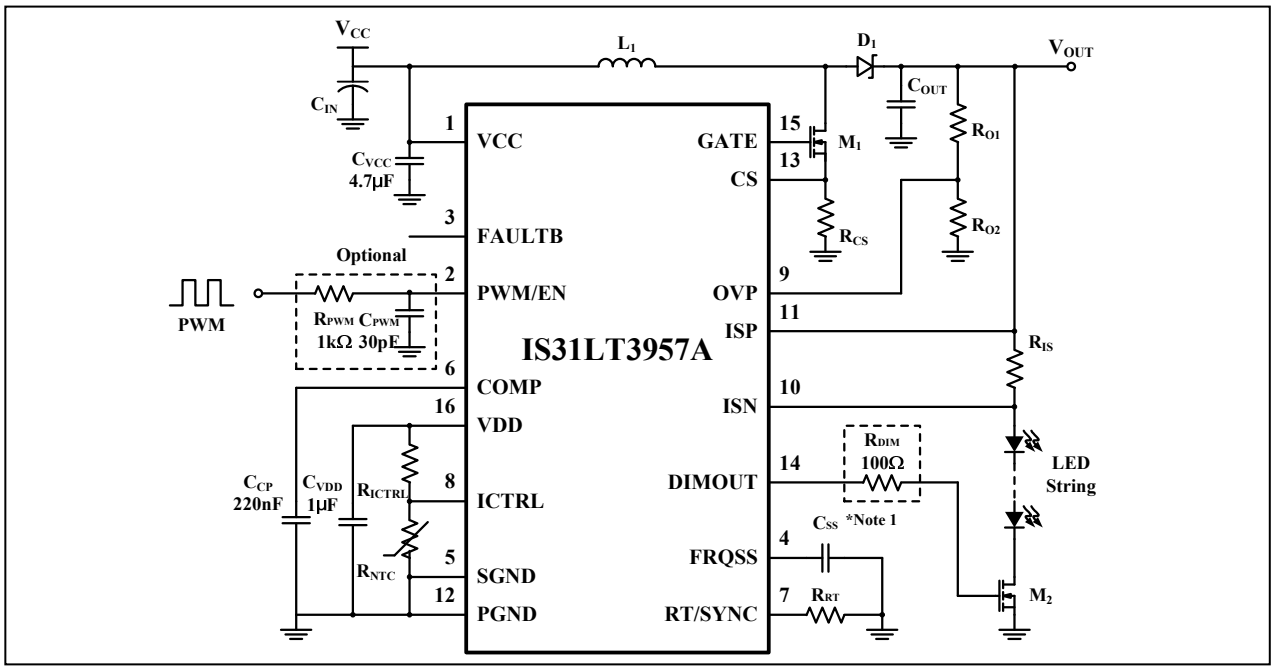


Figure 1 Typical Application Circuit (Boost Configuration)

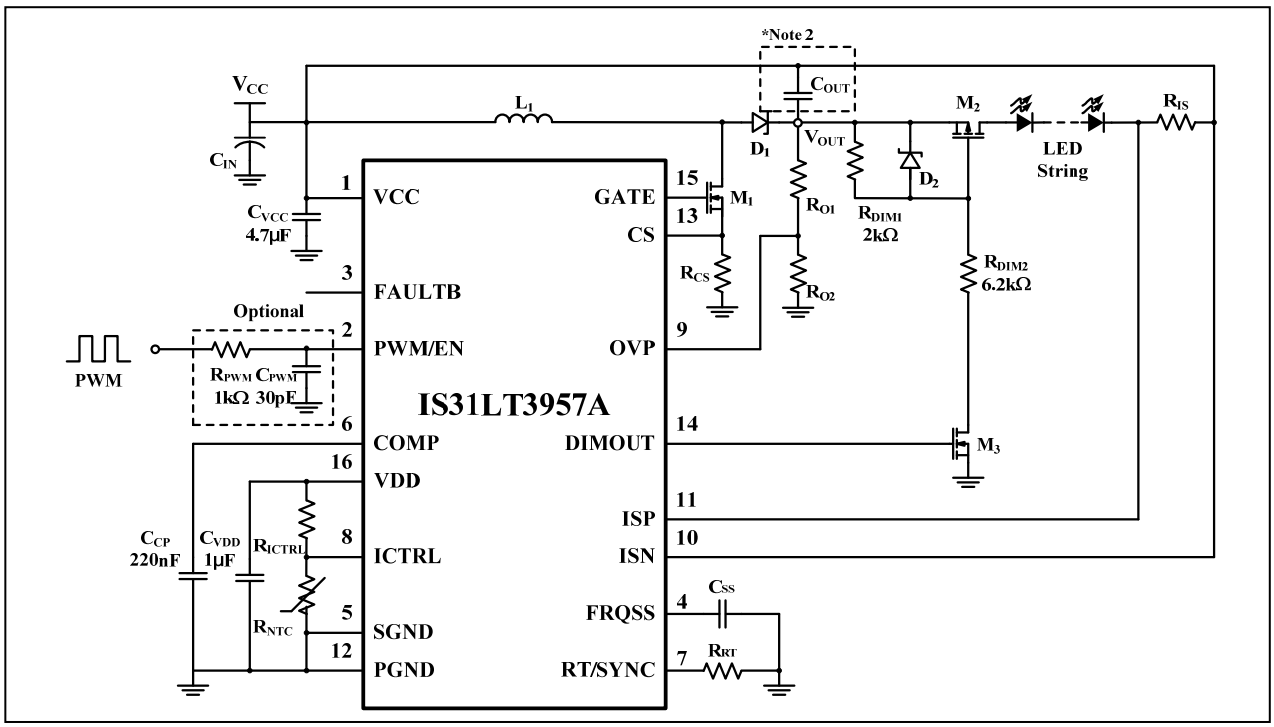


Figure 2 Typical Application Circuit (Buck-Boost Configuration)

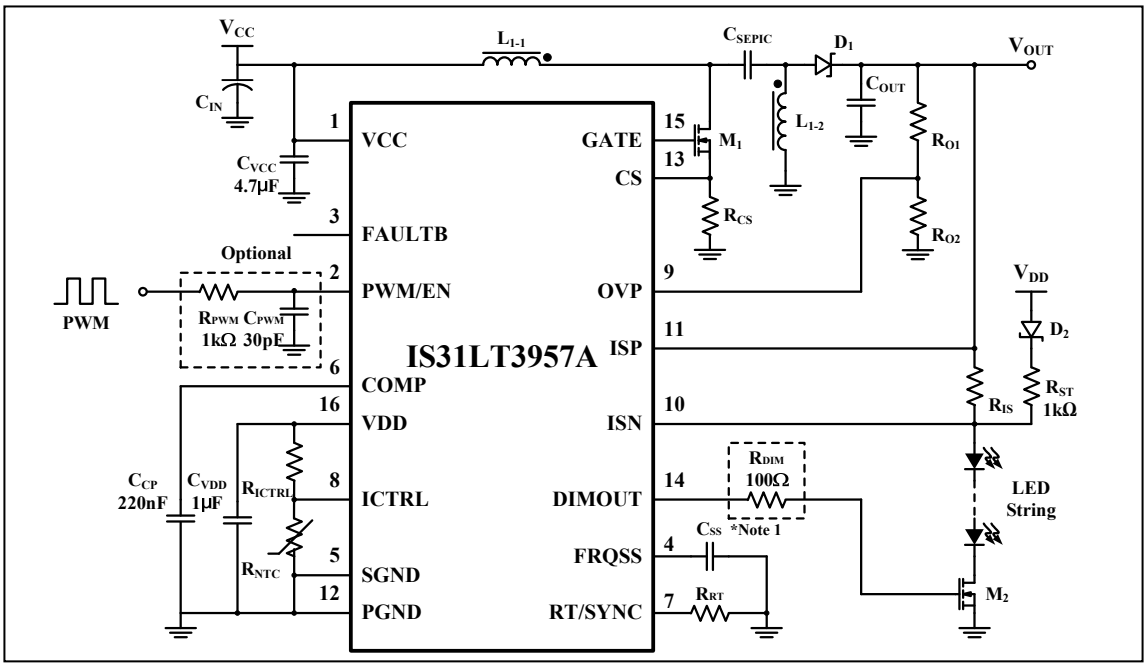


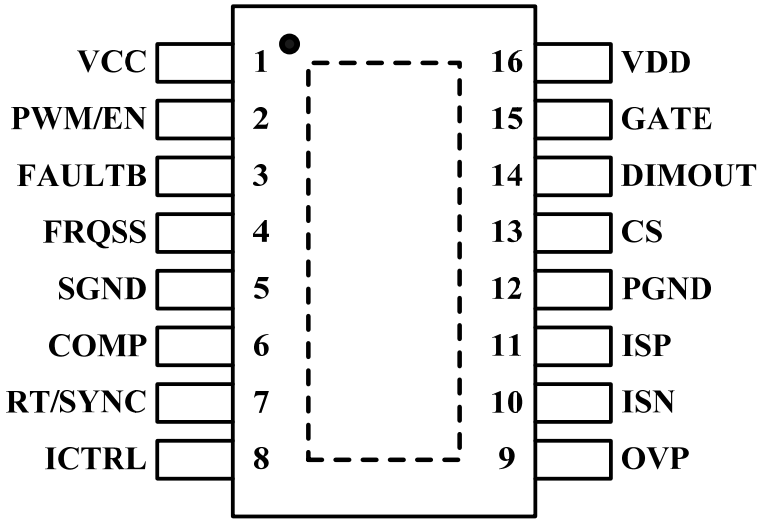
Figure 3 Typical Application Circuit (SEPIC Configuration)

Note 1: R_{DIM} is essential for boost and SEPIC configurations; it MUST be a fixed 100Ω, do not change this value.

Note 2: For buck-boost configuration, C_{OUT} MUST be placed close to C_{IN}.

Note 3: R_{PWM} and C_{PWM} are optional. If PWM dimming is not required, the PWM/EN pin should be tied to VCC or left floating. If PWM dimming is used, this RC filter is recommended and should be placed close to the PWM/EN pin to prevent noise coupling.

PIN CONFIGURATION

Package	Pin Configurations (Top View)
eTSSOP-16	

PIN DESCRIPTION

No.	Pin	Function
1	VCC	The power supply pin.
2	PWM/EN	PWM dimming and enable pin. Internally pulled up to 5V via a 500kΩ resistor. Pull high or leave floating (NC) to enable the IC. Apply an external PWM signal with high level over V_{IH} on this pin to achieve digital dimming. Pulling down below V_{IL} for over t_{DELAY} will force the IC into standby mode.
3	FAULTB	Open drain fault reporting pin. Active low to report a fault condition. Connect a 100kΩ resistor between this pin and the required logic level voltage.
4	FRQSS	Spread spectrum frequency setting pin. A capacitor from this pin to ground sets the dither frequency. Connect this pin directly to ground to disable this function.
5	SGND	Signal ground.
6	COMP	Error amplifier output for loop regulation. Connect a capacitor to ground to set the soft start speed.
7	RT/SYNC	An external resistor to ground on this pin sets the operating frequency. This pin can also be used to synchronize two or more IS31LT3957As in the system. Apply an external clock signal to this pin on two or more ICs for frequency synchronization.
8	ICTRL	Analog dimming voltage input. The analog dimming range is 0.1V~1.1V. The output is full current when the pin voltage is between 5V>V_{ADIM} >1.1V and zero current when V_{ADIM} <0.1V. Analog dimming is achieved when this pin voltage varies between 0.1V<V_{ADIM}<1.1V It cannot be left floating. Recommend a 10nF X7R type capacitor close to this pin for noise decoupling. When it's connected to VDD, a resistor divider is needed to keep the pin voltage below 5V.
9	OVP	Over voltage protect. The GATE pin will be pulled low when this pin voltage exceeds V_{OVP_TH} (1.34V Typ.). A resistor divider is used for monitoring the output voltage and keeping the pin voltage below V_{OVP_TH}.
10	ISN	The LED current sense amplifier negative input.
11	ISP	The LED current sense amplifier positive input.
12	PGND	Power ground.
13	CS	External NMOS switch peak current sense for control loop and over current protection. Connect a resistor from this pin to ground.
14	DIMOUT	Buffer of PWM signal for driving LED string disconnect NMOS to achieve better PWM dimming. High voltage level is determined by internal LDO VDD voltage. This pin also serves in the LED string shorted protection function. When (V_{ISP}-V_{ISN}) exceeds V_{SENSE_OC}, this pin will pull to ground to disconnect the circuit. Leave this pin unconnected if not used.
15	GATE	Gate drive to the external power NMOS. Switches between VDD and GND.
16	VDD	Internal LDO output, needs an external low ESR capacitor (fixed value 1μF) placed close to this pin. This pin is not meant to power any external circuit.
	Thermal Pad	MUST be soldered to a large size GND copper plane.

ORDERING INFORMATION
Industrial Range: -40°C to +125°C

Order Part No.	Package	QTY
IS31LT3957A-ZLS4-TR IS31LT3957A-ZLS4	eTSSOP-16, Lead-free	2500/Reel 96/Tube

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a.) the risk of injury or damage has been minimized;
b.) the user assume all such risks; and
c.) potential liability of Lumissil Microsystems is adequately protected under the circumstances

ABSOLUTE MAXIMUM RATINGS

VCC, PWM/EN, ISP, ISN, FAULTB pins	-0.3V ~ +80V
GATE, VDD, DIMOUT pins	-0.3V ~ +15V
COMP, RT/SYNC, ICTRL, OVP, CS pins	-0.3V ~ +7V
Operating temperature, T_A=T_J	-40°C ~ +125°C
Maximum operating junction temperature, T_{JMAX}	+150°C
Device storage temperature, T_{STG}	-65°C ~ +150°C
Maximum power dissipation, P_{DMAX}	2.5W
Package thermal resistance, junction to ambient (4-layer standard test PCB based on JESD 51-2A), θ_{JA}	46.4°C/W
Package thermal resistance, junction to thermal PAD (4-layer standard test PCB based on JESD 51-8), θ_{JP}	1.617°C/W
ESD (HBM) ESD (CDM)	±2kV ±750V

Note 4: Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

The specifications are at T_J= 25°C, V_{CC}= 12V, unless otherwise noted. (Note 5)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CC}	Input voltage range		5		75	V
I_{CC}	Supply current	V_{ICTRL}= 0V		2	3	mA
I_{STBY}	Supply current in standby mode	$V_{PWM/EN}$= 0V		1.2	1.5	mA
V_{UVLO_F}	Under voltage lock out falling threshold		3.8	4.25	4.8	V
V_{UVLO_R}	Under voltage lock out rising threshold				4.98	V
V_{UVLO_HY}	Under voltage lock out hysteresis			250		mV
V_{DD}	Internal regulator output voltage		6.05	6.60	7.05	V
I_{MAX_LDO}	VDD pin maximum drive current	VDD drops to less than 1V	20			mA
V_{CS_TH}	Power NMOS current limit threshold		160	200	230	mV
V_{SENSE}	Output current sense threshold (V_{ISP}-V_{ISN})	V_{ICTRL}=1.5V	245	250	255	mV
V_{SENSE_DIM}	Output current sense threshold (V_{ISP}-V_{ISN}) with analog dimming down to 10% level	V_{ICTRL} driven by resistor divider from VDD pin, V_{ICTRL}/V_{DD}=0.0303	22.5	25	27.5	mV
Fault Protection						
V_{FAULTB_LOW}	FAULTB pull low voltage	Fault condition, sink current I_{OL}= 1mA		200	400	mV
I_{FAULTB_LK}	FAULTB pin leakage current	No fault condition, FAULTB pin pulled up to 24V			1	μA
V_{SENSE_OC}	Output over current threshold (V_{ISP}-V_{ISN})	For boost architecture	400	475	550	mV
t_{SKIP}	Output over current reset time			16,000		f_{SW} cycles
V_{OVP_TH}	Over voltage protection threshold	OVP voltage rising	1.24	1.34	1.44	V
V_{OVP_HY}	Over voltage protection hysteresis			100		mV

ELECTRICAL CHARACTERISTICS (CONTINUE)

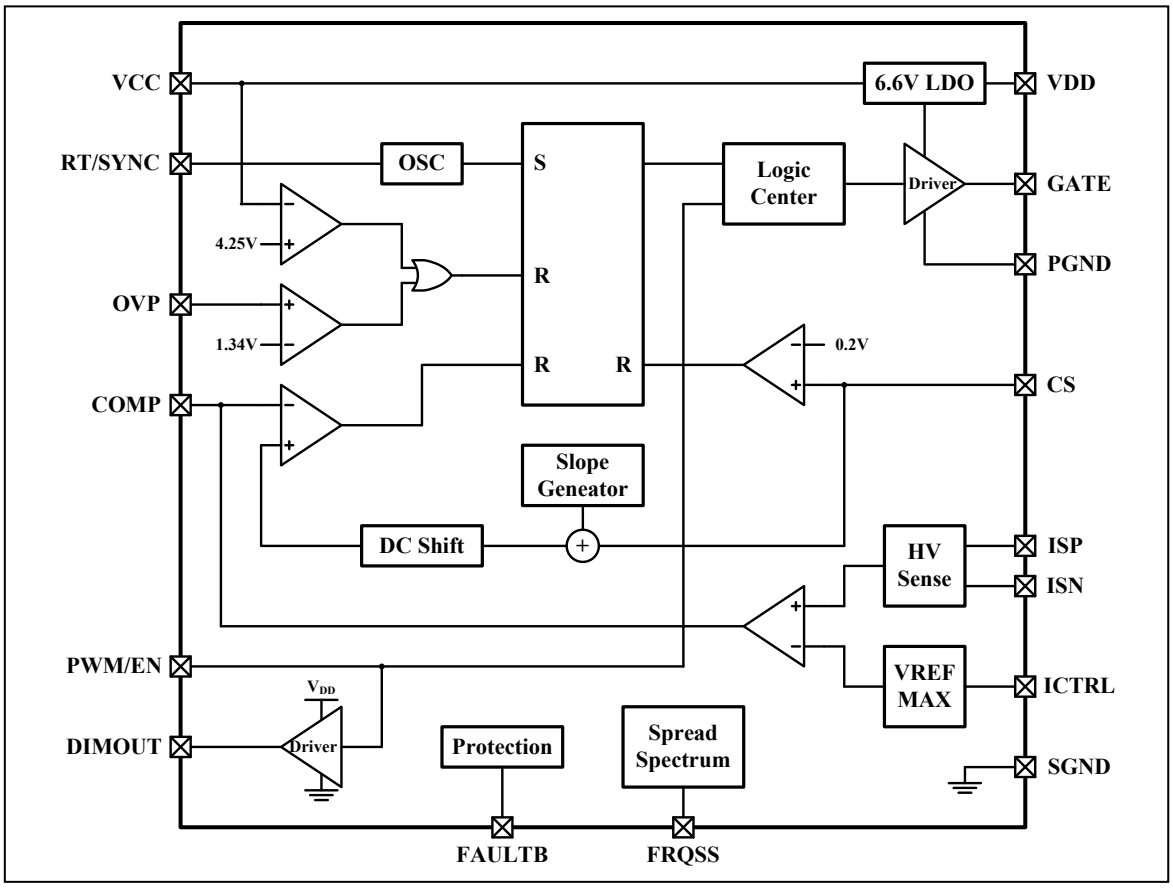
The specifications are at T_J= 25°C, V_{CC}= 12V, unless otherwise noted. (Note 5)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
T_{SD}	Thermal shutdown protection	(Note 6)		165		°C
T_{SD_HY}	Thermal shutdown hysteresis	(Note 6)		20		°C
Gate Driver						
t_{R_GATE}	GATE pin rise time	10%×V_{MAX} to 5V, C_{GATE}= 3.3nF		25	60	ns
t_{F_GATE}	GATE pin fall time	90%×V_{MAX} to 10%×V_{MAX}, C_{GATE}= 3.3nF		25	60	ns
t_{MIN_ON}	GATE minimum on time			150	230	ns
t_{R_DIMOUT}	DIMOUT pin rise time	10%×V_{MAX} to 5V, C_{DIMOUT}= 1nF		200	250	ns
t_{F_DIMOUT}	DIMOUT pin fall time	90%×V_{MAX} to 10%×V_{MAX}, C_{DIMOUT}= 1nF		120	180	ns
Oscillator						
f_{SWR}	Operating frequency range		100		1000	kHz
$V_{RT/SYNC}$	RT/SYNC pin voltage			1		V
f_{SW}	Operating frequency	R_{RT}= 430kΩ	80	100	110	kHz
		R_{RT}= 150kΩ	220	250	280	
		R_{RT}= 33kΩ	850	1000	1150	
D_{MAX}	Maximum operating duty cycle		88	90		%
f_{SY}	Synchronized PWM frequency		250		500	kHz
t_{SY_OFF}	Synchronization input minimum off-time		200			ns
t_{SY_ON}	Synchronization input minimum on-time		200			ns
V_{SY_H}	Synchronization input logic high	(Note 6)	2.5			V
V_{SY_L}	Synchronization input logic low	(Note 6)			0.8	V
I_{FRQSS}	FRQSS charging current	(Note 6)		10		μA
	FRQSS discharging current	(Note 6)		10		
R_{SS}	Spread spectrum frequency range	(Note 6)		±10		%
Inputs Parameter						
V_{IH}	PWM/EN input logic high		2.0			V
V_{IL}	PWM/EN input logic low				0.8	V
t_{DELAY}	The low voltage delay time on PWM/EN pin to enter into standby mode			32,000		f_{SW} cycles
$R_{PWM/EN}$	PWM/EN internal pull up resistor			500		kΩ
V_{ICTRL}	ICTRL analog dimming range	(Note 6)	0.1		1.1	V

Note 5: Production testing of the device is performed at 25°C. Functional operation of the device specified over -40°C to +125°C temperature range, is guaranteed by design, characterization and process control.

Note 6: Guaranteed by design.

INTERNAL FUNCTIONAL BLOCK DIAGRAM



TYPICAL OPERATING CHARACTERISTICS

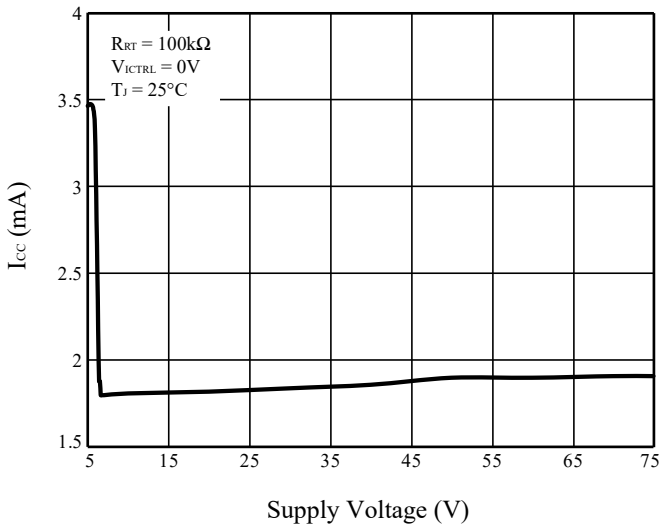


Figure 4 I_{CC} vs. Supply Voltage

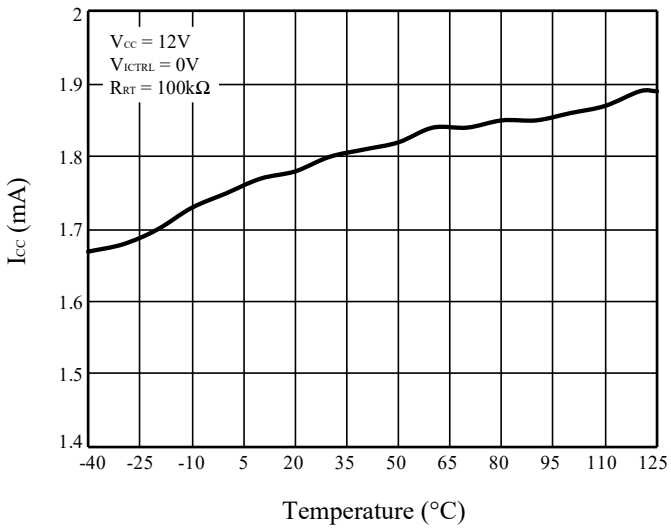


Figure 5 I_{CC} vs. T_J

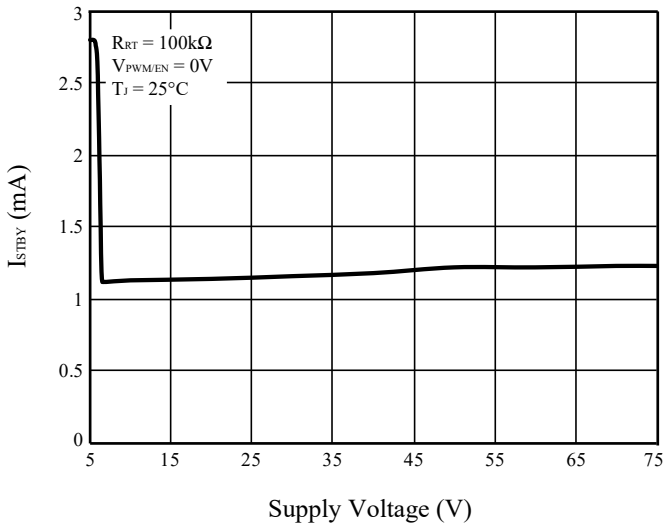


Figure 6 I_{STBY} vs. Supply Voltage

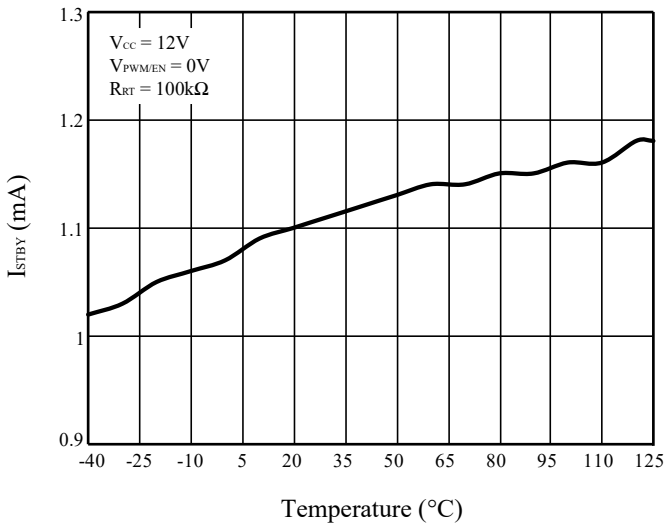


Figure 7 I_{STBY} vs. T_J

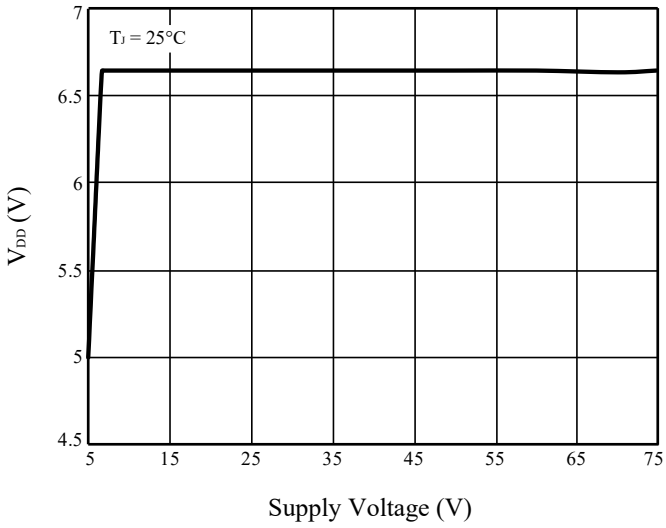


Figure 8 V_{DD} vs. Supply Voltage

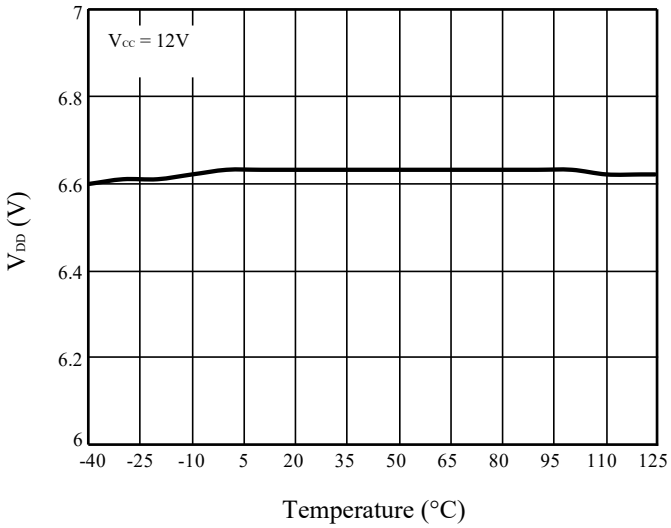


Figure 9 V_{DD} vs. T_J

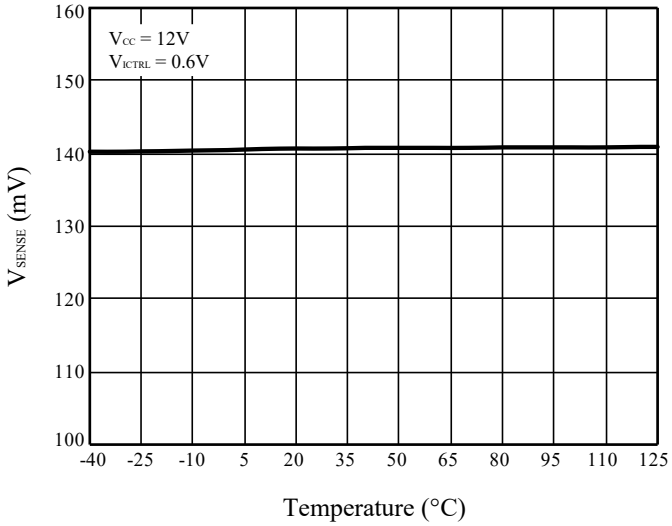


Figure 10 V_{SENSE} vs. T_J

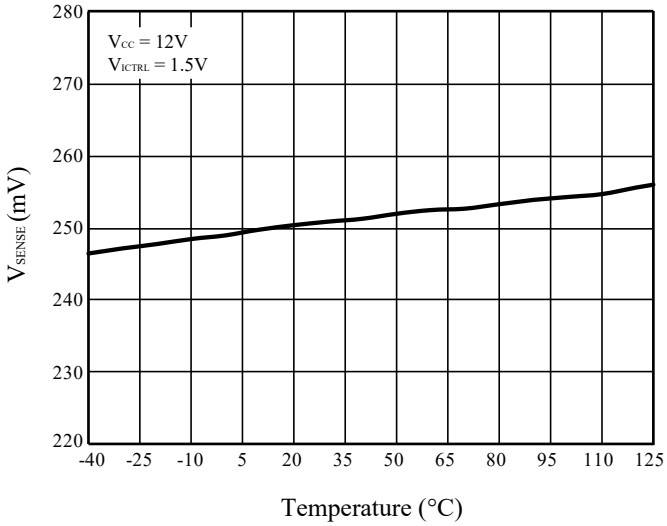


Figure 11 V_{SENSE} vs. T_J

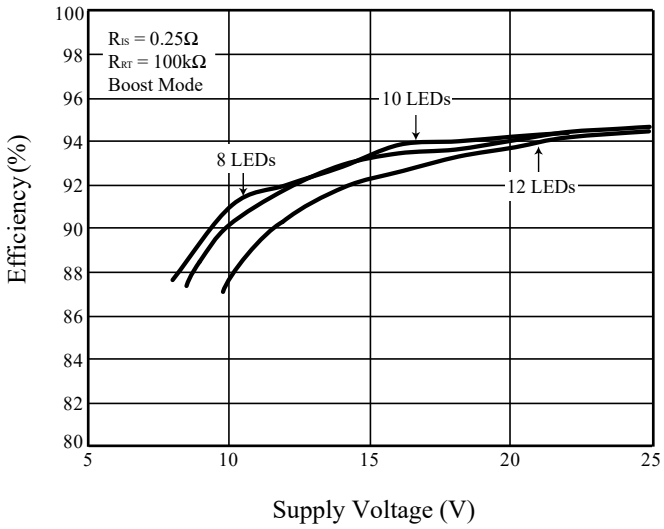


Figure 12 Efficiency vs. Supply Voltage

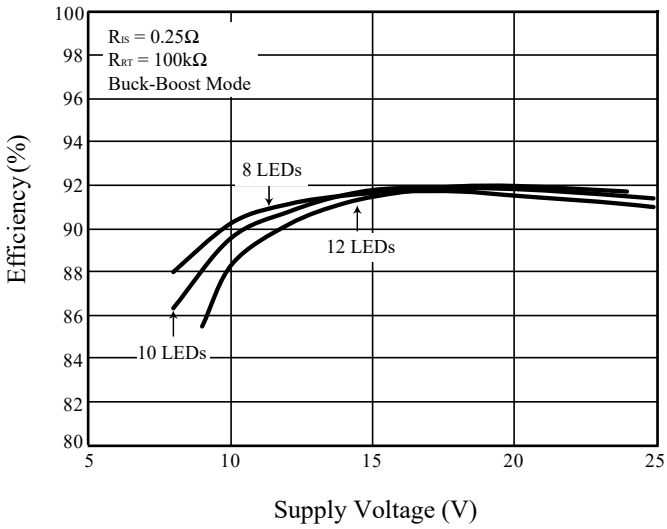


Figure 13 Efficiency vs. Supply Voltage

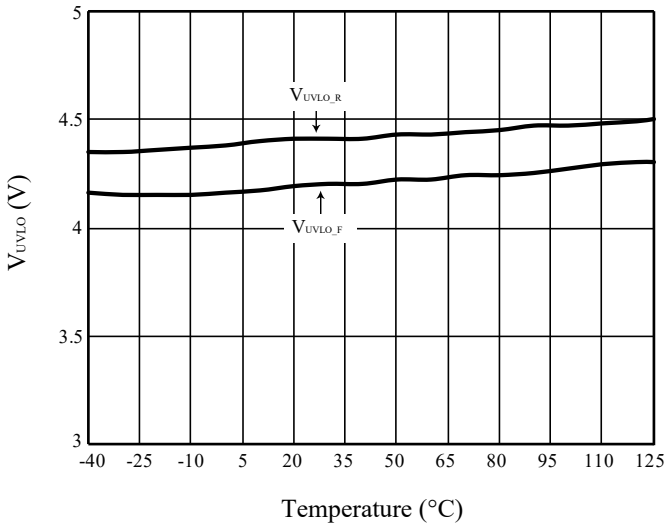


Figure 14 V_{UVLO} vs. T_J

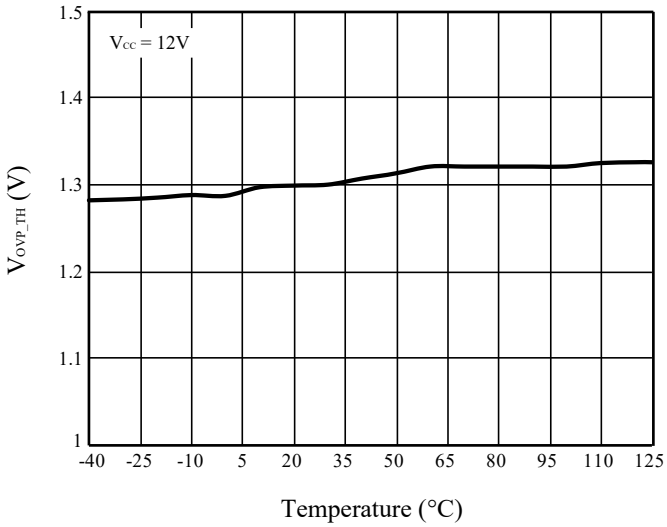


Figure 15 V_{OVP_TH} vs. T_J

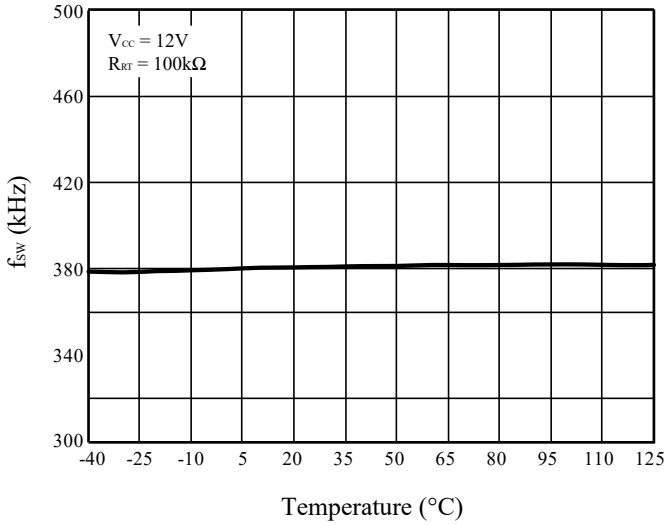


Figure 16 f_{SW} vs. T_J

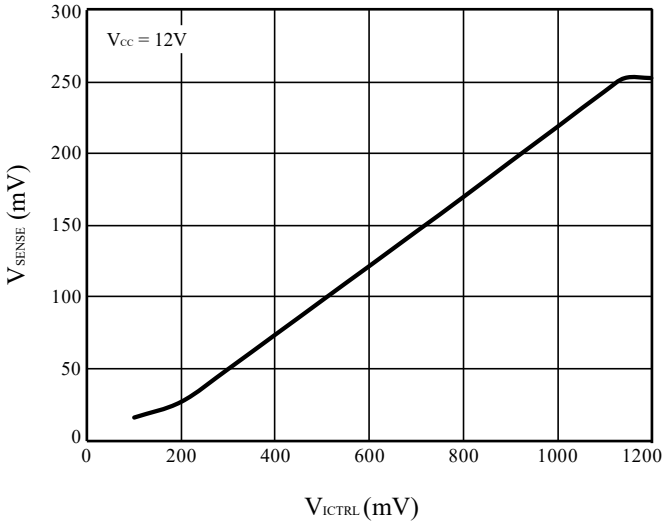


Figure 17 V_{SENSE} vs. V_{ICTRL}

APPLICATION INFORMATION

The IS31LT3957A is a constant frequency, current mode PWM controller designed for high current LED applications. The low side gate driver can drive the external NMOS in the 100kHz~1MHz frequency range, which is set by a single resistor connected to RT/SYNC pin. The frequency can be dithered for spread spectrum function by connecting a capacitor from FRQSS pin to GND. The LED current is programmable with one external current sense resistor between ISP and ISN pins. The device supports both analog and PWM dimming methods. The IS31LT3957A is ideal for boost, buck-boost, SEPIC and buck operation.

VCC UVLO

The device features the under voltage lockout (UVLO) function on VCC pin. It is an internally fixed value of 4.25V and cannot be adjusted. The device is enabled when the VCC voltage rises to exceed V_{UVLO_R}, and disabled when the VCC voltage falls below V_{UVLO_F}.

LINEAR REGULATOR VDD

The device integrates a linear regulator (VDD) with I_{MAX_LDO} current capability to power only the GATE and DIMOUT pins and drive the external low side NMOS switches with 6.6V (Typ.). During operation, the external NMOS will draw transient high current from this linear regulator. Therefore, a 1μF low ESR, X7R type ceramic capacitor is necessary from VDD pin to GND; it must be placed as close to VDD pin as possible. VDD is the output of the internal linear regulator and it's not recommended to be driven by an external power supply. This regulator also has the UVLO feature whose voltage threshold is identical with VCC UVLO. When the VDD voltage drops below V_{UVLO_F}, the GATE and DIMOUT will be turned off and will be turned on once the voltage exceeds V_{UVLO_R}. This helps protect the external NMOS from excessive power consumption due to insufficient gate driving voltage.

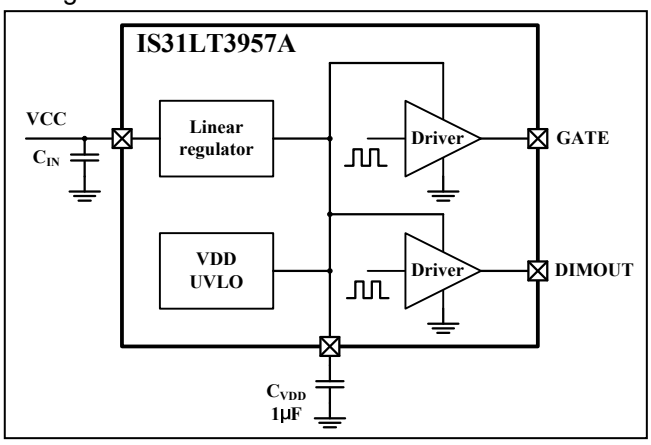


Figure 18 Linear Regulator

An I_{MAX_LDO} current limit on VDD pin protects the IS31LT3957A from excessive power dissipation at high input voltage. Should the VDD pin be externally pulled below 1.4V, the IS31LT3957A will be disabled and the FAULTB pin will be pulled low to report the fault condition until VDD rises above 1.4V. Most of the VDD current will be supplied to the GATE pin to drive power switching NMOS. The driving current can be calculated from the following Equation (1):

$$I_{GATE} = f_{SW} \times Q_G \qquad (1)$$

Where f_{SW} is operating frequency of IS31LT3957A and Q_G is the total gate charge of power NMOS.

Choosing a power NMOS with lower Q_G will improve the efficiency and allow higher switching frequency. It is important to consider the NMOS threshold voltage when operating in the dropout region when the input voltage (V_{CC}) is below the VDD regulation level. Recommend a logic level power NMOS with a threshold voltage below 3V when the device is required to operate at an input voltage less than 6V.

VDD can be used to bias external low current circuitry requiring a reference supply, such as in conjunction with the resistor divider to set voltage level for ICTRL pin. However, to ensure stable operation of the IS31LT3957A, please do not power any external device with VDD.

SOFT-START

The IS31LT3957A provides a built-in soft-start function. The function of soft-start is made for suppressing the inrush current to an acceptable value at startup and over voltage protection. During power up, an internal 6μA current source charges the capacitor (220nF Typ.) on the COMP pin causing the COMP pin voltage to gradually ramp up. The current through the external power NMOS depends on the COMP pin voltage, hence, the input peak current gradually ramps up following COMP pin voltage to the regulated level. The soft-start time can be roughly calculated by Equation (2):

$$t_{SS} = \frac{C_{CP} \times 1V}{6\mu A} \qquad (2)$$

The C_{CP} is the capacitor connected to COMP pin, whose value is in Farad.

OPERATION FREQUENCY

The internal oscillator of the device is programmable from 100kHz to 1MHz range using a single resistor R_{RT} at RT/SYNC pin. Higher frequency operation results in smaller component size but increases the switching losses and power NMOS gate driving current, and may not allow sufficiently high or low duty cycle. Lower frequency gives better performance but results in larger component size. To set a desired frequency, the resistor value can be calculated by following Equation (3):

$$R_{RT} = \frac{37.5\times10^9}{f_{SW}} \qquad (3)$$

Where R_{RT} is in ohm. f_{SW} is the operating frequency in Hertz.

If the RT/SYNC pin is connected to an extremely low value resistor or accidently shorted to ground, the internal oscillation frequency will be over 1MHz. If it exceeds 2.5MHz, the internal circuit will detect it and turn off the power NMOS for protection. When this fault condition is removed so the frequency drops below 2.5MHz, the operation will recovery.

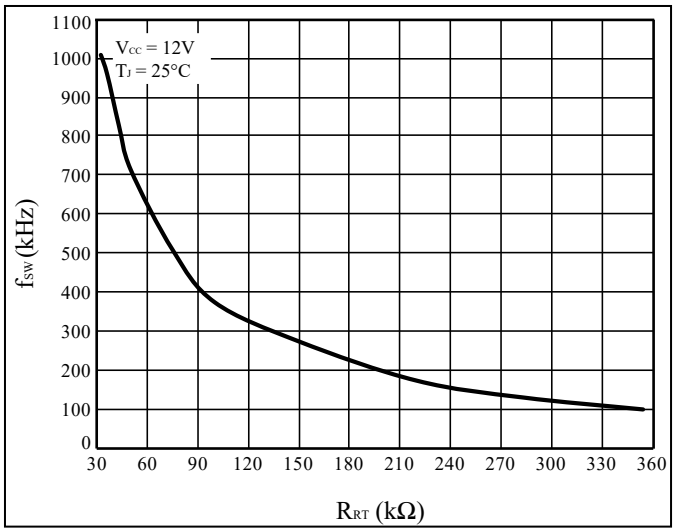


Figure 19 f_{SW} vs. R_{RT}

FREQUENCY SYNCHRONIZATION

The RT/SYNC pin can also be used as a synchronization input, allowing the IS31LT3957A to operate with an external clock in the range of 250kHz to 500kHz as long as it satisfies the requirements of t_{SY_ON} and t_{SY_OFF}. When an external synchronization clock is applied to the RT/SYNC pin, the internal oscillator is over-driven so that each switching cycle begins at the rising edge of external clock. The IS31LT3957A will not be enabled if the RT/SYNC pin is held low during power-up. The IS31LT3957A will start up only when the RT/SYNC pin is tri-stated and allowed to rise to about 1V, or when a synchronization clock is detected, Figure 20 shows the timing for a synchronization clock into the IS31LT3957A at 500kHz. Any pulse with a duty cycle of 10% to 90% at 500kHz can be used to synchronize the IC.

Table 1 Synchronization Duty Cycle Range

SYNC Clock Frequency(kHz)	Duty Cycle Range (%)
500	10 ~ 90
400	8 ~ 92
300	6 ~ 94
250	5 ~ 95

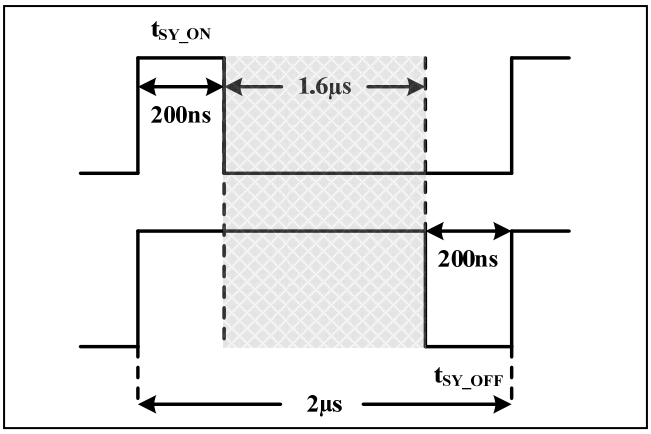


Figure 20 SYNC Pulse On And Off Time Requirements

SPREAD SPECTRUM

A switch mode controller can be particularly troublesome in applications where EMI is of concern. To optimize EMI performance, the IS31LT3957A includes a spread spectrum feature. The spread spectrum can spread the total electromagnetic emitting energy into a wider range to significantly degrade the peak EMI energy. With spread spectrum, the EMI test can pass with smaller size and lower cost filter circuit.

When a capacitor is connected to FRQSS pin, a triangle waveform is internally generated to modulate the internal oscillator in 90% to 110% of the base frequency which is set by R_{RT} resistor as Figure 21.

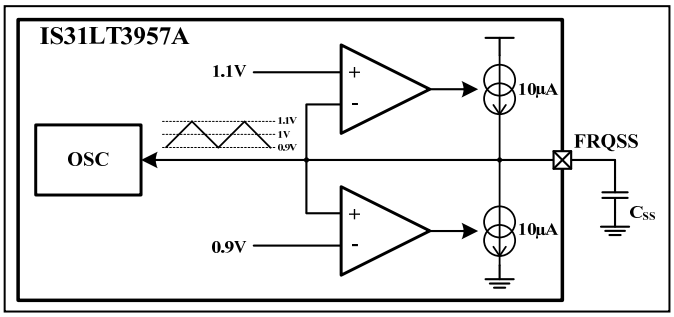


Figure 21 Spread Spectrum Operation

To set the desired modulation frequency, the C_{SS} capacitor can be calculated by the following Equation (4):

$$C_{SS} = \frac{10\mu A}{2\times f_{SS}\times 0.2V} \qquad (4)$$

The C_{SS} is in Farad. f_{SS} is the modulation frequency in Hertz. A 500Hz frequency is a good starting point to optimize EMI performance. Further adjust this frequency in the actual system to get best EMI performance. Connect FRQSS pin to GND to disable the spread spectrum function.

POWER NMOS CURRENT SENSE

CS is part of the current mode control loop. Connect a resistor R_{CS} from the CS pin to ground to regulate the internal oscillator duty cycle and power the NMOS

peak current and achieve input cycle-by-cycle peak current limit protection. In order to provide sufficient current to the external power NMOS for driving the load and prevent this current from exceeding current limit protection, the R_{CS} value should be set to a proper level.

The inductor peak current (I_{PEAK}) during normal operation is given by Equation (5):

$$I_{PEAK} = I_L + \frac{\Delta I_L}{2} \qquad (5)$$

Where I_L is the inductor average current in amp. ΔI_L is the current ripple of the inductor in amp.

To ensure a reasonable output current ripple and better operating stability, choose ΔI_L as follows range:

$$20\% \times I_L \le \Delta I_L \le 100\% \times I_L \qquad (6)$$

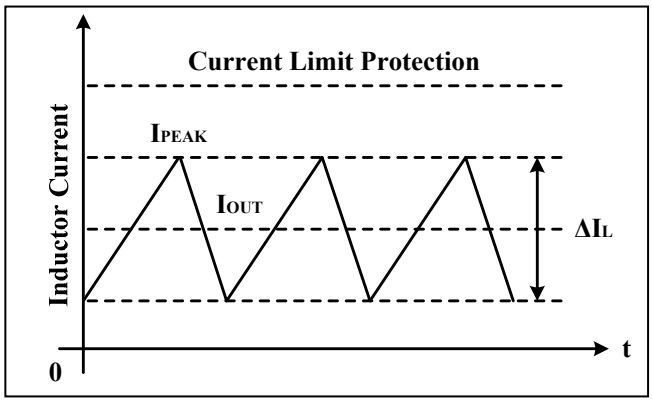


Figure 22 Inductor Current

The inductor ripple current ΔI_L involves trade-offs in performance. Lower ΔI_L requires a larger value and bigger size inductor that which will dissipate more power, however it also reduces the peak current in the external power NMOS and the recirculating diode that derate the power dissipation on them.

For boost application, the I_L is equal to the input average current, so

$$I_{PEAK_BOOST} = \frac{V_{LED} \times I_{LED}}{\eta \times V_{CC}} + \frac{\Delta I_L}{2} \qquad (7)$$

For buck-boost and SEPIC applications, the I_L is equal to the input average current plus LED average current, so

$$I_{PEAK_BUCK-BOOST} = \frac{(V_{LED} + V_{CC}) \times I_{LED}}{\eta \times V_{CC}} + \frac{\Delta I_L}{2} \qquad (8)$$

Where η is the assumed circuitry efficiency, choose 0.9 for it. V_{CC} uses the minimum input voltage in volts, V_{LED} is the maximum total forward voltage of LED string in volts. I_{LED} is the output LED current in amps.

The current limit protection should be at least 50% greater than the inductor peak current I_{PEAK}. The current sense resistor R_{CS} is calculated by the following Equation (9):

$$R_{CS} = \frac{V_{CS_TH}}{1.5 \times I_{PEAK}} \qquad (9)$$

Recommend use of ±1% precision type resistor for best accuracy.

The current limit protection is cycle-by-cycle detection. Once the CS pin voltage exceeds the current limit threshold, V_{CS_TH}, the GATE immediately pulls low to turn off the power NMOS until the next switching cycle. The current sense resistor should be placed as close as possible to IS31LT3957A device to ensure stable operation.

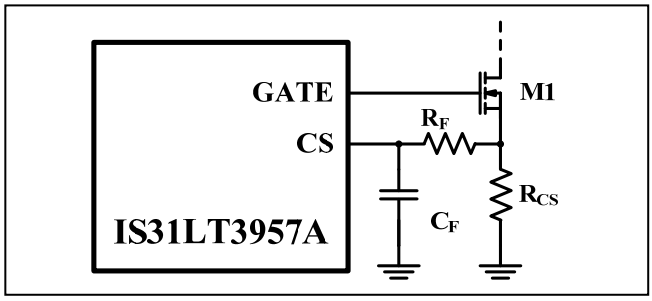


Figure 23 CS Filter

An internal blanking circuit prevents power NMOS switching current spike propagation and premature termination of duty cycle by internally shunting the CS input for 150ns after the beginning of the new switching period. For further noise suppression, the use of low pass RC filter on CS pin can be considered. The recommended value of R_F and C_F are 100Ω and 10pF.

INDUCTOR

Inductor value involves trade-offs in performance. Larger inductance reduces inductor current ripple resulting in smaller output current ripple, however it also brings in unwanted parasitic resistance that degrades performance. Select an inductor with a rating current greater than the input average current and a saturation current greater than the power NMOS current limit set by R_{CS}. Use the following equations to estimate the approximate inductor value:

For boost application:

$$L_{BOOST} = \frac{V_{CC} \times (V_{LED} - V_{CC})}{f_{SW} \times \Delta I_L \times V_{LED}} \qquad (10)$$

For buck-boost and SEPIC application:

$$L_{BUCK-BOOST} = \frac{V_{CC} \times V_{LED}}{f_{SW} \times \Delta I_L \times (V_{LED} + V_{CC})} \qquad (11)$$

Where V_{CC} uses the minimum input voltage in volts, V_{LED} is the maximum total forward voltage of LED string in volts, f_{SW} is the operation frequency in hertz. If

the SEPIC inductor is coupled, the equation's result can be used as is. If the SEPIC uses two uncoupled inductors, then each should have an inductance double the result of the equation.

POWER NMOS

A power NMOS must be chosen with its drain voltage rating V_{DS_MAX} greater than the over voltage protection voltage (V_{OVP}) together with overshoot voltage due to the ringing caused by parasitic inductances and capacitances, therefore keeping 20% safety margin voltage over V_{OVP} is necessary.

For boost and buck-boost:

$$V_{DS_MAX} \geq 1.2 \times V_{OVP} \qquad (12)$$

For SEPIC:

$$V_{DS_MAX} \geq 1.2 \times (V_{OVP} + V_{IN}) \qquad (13)$$

The gate drive current is sourced from the VDD pin whose current capability is limited to protect the device from excessive power dissipation at high input voltage. So low gate charge Q_G at 7V should be carefully considered (refer to Equation (1)). The consideration of the $R_{DS(ON)}$ of power NMOS is usually secondary because the switching loss dominates the power lost, especially at high operating frequency. A power NMOS with lower Q_G and $R_{DS(ON)}$ achieves higher efficiency and lower power losses. The continuous current rating of the selected power NMOS should be higher than the input average current and the maximum current rating should be higher than the current limit protection level.

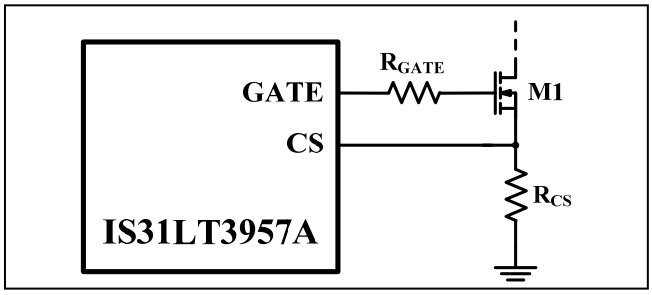


Figure 24 GATE Buffer Resistor

A buffer resistor can be considered to be added in series with the gate driving that slows down the switching rising and falling edge to minimize EMI. However, it increases the switching loss and degrades the efficiency at the same time. So the value should not be too large; several ten ohm is a good starting point. Please choose a proper value based on the EMI test result.

RECIRCULATING DIODE

The diode conducts the current during the interval when the power NMOS is turned off. To achieve high efficiency choose a Schottky diode with low forward voltage and fast switching speed. Ensure that the diode's continuous current rating exceeds the output LED current and peak current rating exceeds the current limit protection level. The diode's reverse breakdown voltage, V_{BD}, must be higher than the over voltage protection voltage (V_{OVP}) and keep a 20% safety margin.

$$V_{BD} \geq 1.2 \times V_{OVP} \qquad (14)$$

The leakage current of the diode is also a critical feature to consider, which increases with the temperature. High leakage current will degrade the efficiency and PWM dimming performance.

INPUT CAPACITOR

The input capacitor provides the transient current to the inductor of the converter. An X7R type ceramic capacitor is a good choice for the input bypass capacitor to handle the ripple current since it has a very low equivalent series resistance (ESR) and low equivalent series inductance (ESL) capacitor and good temperature performance. Use the following equation to estimate the approximate capacitance:

For boost application:

$$C_{IN} \geq \frac{\Delta I_L}{8 \times V_{RIPPLE} \times f_{SW}} \qquad (15)$$

For buck-boost and SEPIC application:

$$C_{IN} \geq \frac{I_{LED} \times V_{LED}}{V_{RIPPLE} \times f_{SW} \times (V_{LED} + V_{CC})} \qquad (16)$$

Where, V_{RIPPLE} is the acceptable input voltage ripple in volts. C_{IN} is in farads. This input capacitor must be placed close to the IS31LT3957A and the inductor to reduce the ripple. A higher value input capacitor is good for minimizing the input voltage deviation due to the large transient current. An aluminum electrolytic capacitor is recommended to be used in parallel with ceramic capacitors.

OUTPUT CAPACITOR

The output capacitor is used to filter the LED current ripple to an acceptable level. The equivalent series resistance (ESR), equivalent series inductance (ESL) and capacitance of the capacitor contribute to the output current ripple. Therefore, a low-ESR X7R type ceramic capacitor should be used. Use the following equation to estimate the approximate capacitance:

For boost application:

$$C_{OUT} \geq \frac{I_{LED} \times 2 \times (V_{LED} - V_{CC})}{V_{RIPPLE} \times f_{SW} \times V_{LED}} \qquad (17)$$

For buck-boost and SEPIC application:

$$C_{OUT} \geq \frac{I_{LED} \times 2 \times V_{LED}}{V_{RIPPLE} \times f_{SW} \times (V_{LED} + V_{CC})} \qquad (18)$$

Where, V_{RIPPLE} is the acceptable output voltage ripple

in volts. C_{OUT} is in farads. Based on the above equations, the higher operating frequency proportionally decreases the required output capacitor value which results in smaller capacitor size. The output ceramic capacitor should be placed close to the cathode of D1 for a better filter effect. An aluminum electrolytic capacitor can be used in parallel with the ceramic capacitors to provide bulk energy storage.

LED CURRENT CONTROL

The IS31LT3957A regulates the LED current by the external resistor, R_{IS}, in series with LED string and connecting to ISP and ISN. The internal current sense voltage threshold V_{SENSE}, which is equal to V_{ISP}-V_{ISN}, is 0.25V (Typ.). To get best output accuracy, sensing of the output current should be done on the top of the LED string. When the PWM/EN pin is tied to a DC voltage higher than 2.0V and ICTRL voltage is above 1.1V, will result in a full-scale current sense voltage threshold and the LED current can be calculated from Equation (19).

$$I_{LED} = \frac{V_{SENSE}}{R_{IS}} \qquad (19)$$

In order to have an accurate LED current, precision resistors are preferred (±1% recommended). The R_{IS} resistor should be placed as close as possible to the IS31LT3957A device with minimal trace length.

DIMMING CONTROL

IS31LT3957A can modulate the brightness of LEDs by controlling the PWM signal to the PWM/EN pin or the DC voltage on ICTRL pin.

PWM DIMMING AND ENABLING

IS31LT3957A offers a PWM/EN pin for pulse-width modulating of the output current.

The DIMOUT pin is a buffered output following the dimming signal on the PWM/EN pin which drives the gate of the dimming MOSFET. When the PWM/EN signal voltage is greater than logic high threshold V_{IH}, the device is enabled and the dimming MOSFET is turned on. When the PWM voltage is lower than the logic low threshold V_{IL}, the device is disabled and the dimming MOSFET is turned off. The LED string is dimmed by modulating the duty cycle of PWM signal to vary the LED average current. Apply a low PWM signal frequency with a higher device switching frequency will result in best dimming performance.

An external MOSFET driven by the DIMOUT pin (refer to Figure 1 and 2) is recommended for a precise PWM dimming function. The dimming MOSFET will disconnect the LED string during PWM low to prevent the V_{OUT} node from discharging which will minimize the recovery time when the PWM goes back high. This shorter recovery time results in better dimming linearity and stable loop regulation during low PWM duty cycles. Both are critical for ensuring control loop regulation during steady-state operation and to minimize LED current overshoot once PWM returns to high level.

Pulling the PWM/EN pin low for longer than 32,000 switching cycles (t_{DELAY}) will force the device into standby mode. There is a soft start when the PWM/EN is pulled high to enable the device after disabling.

Table 2 PWN/EN Disable Time

Operating Frequency(kHz)	t_{DELAY} (ms)
1000	32
600	53
400	80
250	128
100	320

An RC filter (1kΩ resistor and 30pF capacitor) in series with the PWM/EN input is recommended to avoid noise coupling during PWM dimming operation. The PWM/EN pin is internally pulled up to 5V via a 500kΩ resistor. If PWM dimming is not used, the PWM/EN pin can be either left floating or tied to VCC.

DIMMING MOSFET

A dimming NMOS (M2) in series with the LED string is essential for PWM dimming application while in boost mode (refer to Figure 1). The NMOS voltage rating should be as high as the power switching NMOS and its maximum continuous current rating should be higher than the maximum LED string current. Choose an NMOS with low total gate charge (Q_g) for high frequency turn on and off time to best PWM dimming contrast ratio. Another important NMOS selection parameter is low $R_{DS(ON)}$ for high operating efficiency and low power losses. If PWM dimming is not implemented, the dimming NMOS can be removed, the DIMOUT pin left floating and the LED cathode connected directly to GND. However, please note the LED short protection feature will not be functional. Therefore it's recommended to use a dimming NMOS for most applications.

In buck-boost mode (refer to Figure 2), an additional PMOS (M2), zener (D2), and resistors (R_{DIM2}, R_{DIM3}) are needed as a level shift to disconnect the output during PWM dimming operation. When the NMOS connected to the DIMOUT pin turns on, the R_{DIM2} resistor will pull low the PMOS gate to turn it on. When the dimming NMOS turns off, R_{DIM1} resistor will pull high the PMOS gate to turn it off. A 7V zener diode (D2) is needed to clamp the V_{SG} voltage and protect the PMOS. The PMOS selection should follow the same guideline as the dimming NMOS regarding voltage and current ratings in boost mode. However, the dimming NMOS (M3) in buck-boost mode can be a signal transistor which can be low current capability but the voltage rating should be the same as the power NMOS. If PWM dimming is not implemented, both dimming

PMOS and NMOS can be removed with the DIMOUT pin left floating and LED anode connected directly to V_{OUT}. The recommended value of R_{DIM1} and R_{DIM2} are 2kΩ and 6.2kΩ. Too large value of R_{DIM1} and R_{DIM2} slows down the turn on/off speed of the M2 that degrades the PWM dimming performance. While too low value discharges the output capacitor more quickly that extends the recovery time when the PWM goes back high and degrades the efficiency.

ANALOG DIMMING

The IS31LT3957A also offers an analog dimming input pin, ICTRL, whose dimming voltage range is 0.1V to 1.1V. The current sense voltage threshold, V_{SENSE}, can be regulated by the ICTRL pin voltage. If the ICTRL pin is pulled up above 1.1V, analog dimming is disabled and the output current is given by Equation (19). When the ICTRL voltage is driven below 1.1V, V_{ICTRL} will proportionally control the current sense voltage threshold V_{SENSE} resulting in a change in the output current as given by Equation (20):

$$I_{LED} = \frac{V_{ICTRL} - 0.1}{1V} \times \frac{V_{SENSE}}{R_{IS}} \qquad (20)$$

The output LED voltage will decrease when the output current decreases. Therefore, it must ensure the output voltage always higher than the input voltage during the dimming in the boost configuration.

Never leave the ICTRL pin floating. If the analog dimming function is not implemented, connect the ICTRL pin to a voltage level higher than 1.1V and lower than 5V. This voltage can be created with a resistor divider (R1, R2) from the VDD pin. The ICTRL pin cannot be connected directly to the VDD pin because the linear regulator VDD voltage (6.6V) exceeds the maximum voltage rating of the ICTRL pin.

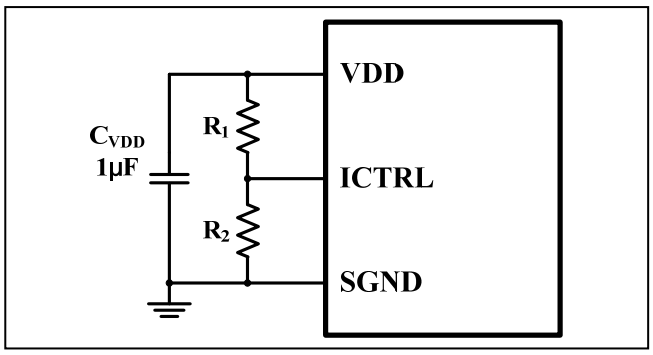


Figure 25 Analog Dimming Unused

The ICTRL can be used to dim the output current to zero, although the relative current accuracy decreases with the decreasing current sense voltage threshold due to the offset of the internal circuit. When the ICTRL voltage is below 0.1V, the output will be turned off. It is recommended to add a 10nF ceramic capacitor from the ICTRL pin to GND to bypass any high frequency noise, especially if the analog voltage level comes from a long copper trace. This 10nF capacitor should be placed as close to the ICTRL pin as possible.

The ICTRL pin can be used to fine tune the output current during mass-production. LEDs are typically sorted into various bins of different luminous intensity and forward voltage. To correct the brightness deviation during mass-production, the mean output current can be adjusted by adjusting the voltage level on the ICTRL pin. As shown in Figure 25, fix the R_2 value and vary the R_1 value to adjust and maintain the same lumen output across different LED bins.

The ICTRL pin can also be used in conjunction with a NTC thermistor to provide over temperature current roll off protection for the LED load or the system.

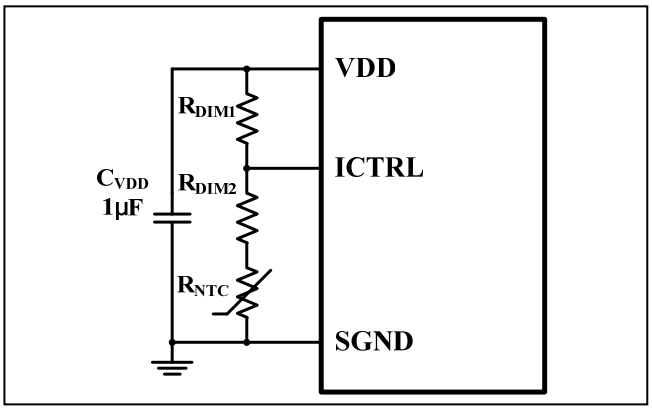


Figure 26 ICTRL Pin with Thermistor for Roll Off Protection

For example, assume the desired current roll off temperature threshold is T_R and the NTC thermistor resistance is R_{NTCR} at this temperature (R_{NTCR} can be found in the NTC thermistor datasheet), then R_{DIM1} and R_{DIM2} can be calculated by:

$$R_{DIM1} = \frac{(R_{NTCR} + R_{DIM2}) \times (V_{DD} - 1.1V)}{1.1V} \qquad (21)$$

For a given NTC thermistor, the R_{DIM1} resistor will adjust the current roll off temperature threshold. The larger R_{DIM1} the lower current roll off temperature threshold. The R_{DIM2} resistor is optional to be used to adjust current derating slope. The larger R_{DIM2} the flatter the current derating slope. If R_{DIM2} is not used, tie the NTC thermistor directly to ICTRL pin.

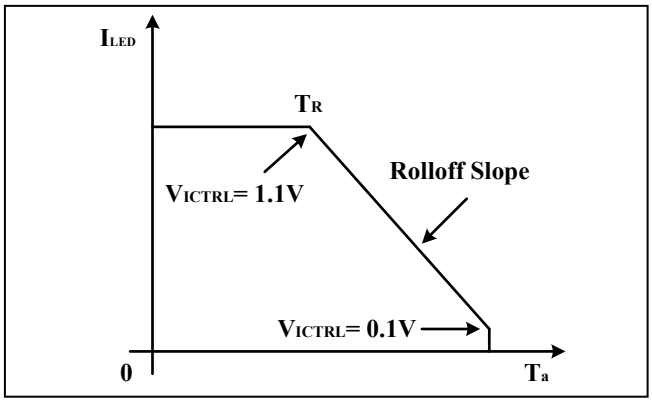


Figure 27 Roll Off Protection

SETTING THE OVER VOLTAGE PROTECTION

The open LED string protection is achieved using over voltage protection (OVP). In some cases, when the output voltage reaches the programmed OVP voltage (V_{OVP}), the GATE and DIMOUT pins are immediately pulled low and the FAULTB pin is also pulled low to report the fault condition. They remain low until the output voltage drops below the hysteresis voltage. To make sure the chip functions properly, the resistor divider (R_{O1}, R_{O2}) at the OVP pin must be set to 1.2x greater than the output voltage, V_{OUT}. For boost and SEPIC applications, V_{OUT} is equal to the LED string voltage. For buck-boost applications, V_{OUT} is equal to the input voltage (V_{CC}) plus the LED string voltage.

The OVP voltage is calculated using Equation (22).

$$V_{OVP} = \frac{V_{OVP_TH} \times (R_{O1} + R_{O2})}{R_{O2}} \geq 1.2 \times V_{OUT} \quad (22)$$

It is recommend to connect a 1nF ceramic capacitor from the OVP pin to GND to avoid unexpected noise coupling into this pin.

Note, the OVP voltage should not be set much higher than V_{OUT}, otherwise the power NMOS, the dimming MOS, the recirculating diode and the output capacitor would require higher voltage ratings.

SHORT CIRCUIT PROTECTION

In a boost configuration, the short circuit (LED string) protection is implemented by the R_{IS} over current detection. The ISP and ISN pins have an output over current threshold (V_{SENSE_OC}), which is higher than output current sense threshold (V_{SENSE}). If the LED string is shorted the total forward voltage (V_F) will be lower than the input voltage (V_{CC}), resulting in a current path from V_{CC} through the inductor, recirculating diode, R_{IS} and power NMOS (M2) to ground. If this fault occurs, the uncontrolled current of this path will rise rapidly. If there is no dimming MOS to disconnect this current path, the huge current may damage the components as well as the power source.

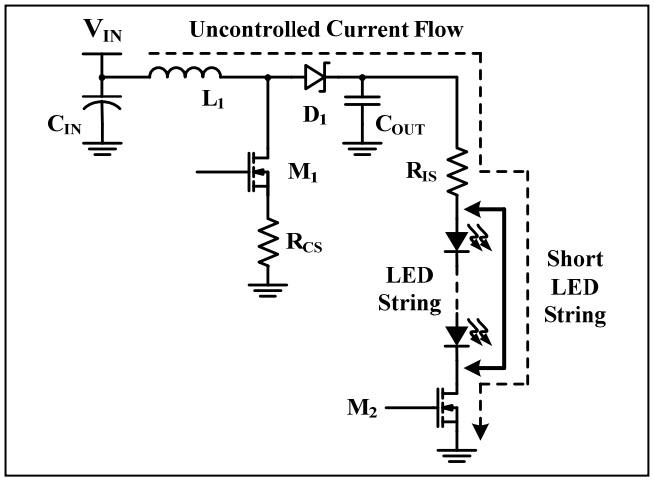


Figure 28 Boost Short LED String

With a dimming MOS, once the uncontrolled current results in the R_{IS} voltage reaching the threshold V_{SENSE_OC} over a delay time (about 2 f_{SW} cycles), the hiccup timer is started and the DIMOUT pin will pull low the gate of dimming MOS M2 for t_{SKIP}. When the timing is complete, the converter attempts to restart. If the fault condition still persists, the converter shuts down and goes through the cycle again. This on/off cycling of the uncontrolled current flow will result in a low average value. If the fault condition is cleared (due to a momentary output short) the converter will start regulating the output current normally. This prevents the circuitry and power supply from being damaged by an unwanted huge current.

In buck-boost and SEPIC configuration, when the LED string is shorted, there is no uncontrolled current path because in boost configuration the output current remains under control loop regulation. Therefore, an LED short circuit will not cause component damage.

THERMAL SHUTDOWN PROTECTION

To protect the IS31LT3957A from damage due to high power dissipation, the temperature of the die is monitored. If the die temperature exceeds the thermal shutdown temperature of 165°C (Typ.) the device will enter standby mode, and the FAULTB pin will be pulled low to report the fault. After a thermal shutdown event, the IS31LT3957A will not try to restart until its die temperature has reduced to less than 145°C (Typ.).

FAULT DETECTION AND REPORTING

For added system reliability, the IS31LT3957A integrates various fault detection and protection circuitry for LED string open/short circuit, VCC and VDD UVLO, power NMOS over current, RT/SYNC and VDD pins short circuit and over temperature conditions. The open drain pin FAULTB can be used as a fault condition flag. When it's monitored by a host, a pull up resistor from the FAULTB pin to the supply of the host is needed. It is pulled low to report the fault conditions. Table 3 briefly describes the typical protection trigger conditions and device behavior.

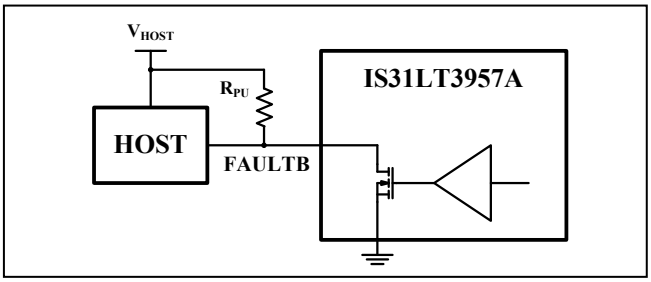


Figure 29 Host Monitors The Fault Reporting

The ideal value for the FAULTB R_{PU} range needs to take into account the number of IS31LT3957A devices connected to the same host. The resulting R_{PU} voltage level should not interfere with the V_{IH_HOST} and V_{IL_HOST} detection levels of the host. For no-fault detected operation, the sum of the leakage current(s) for the open drain (if more than one device interconnected)

multiplied with the value of R_{PU} must be greater than V_{IH_HOST}. For fault detected operation, the pull down voltage must be below V_{IL_HOST}. Then

$$R_{PU_MAX} = \frac{V_{HOST} - V_{IH_HOST}}{N \times I_{FAULTB_LK}} \quad (23)$$

$$R_{PU_MIN} = \frac{(V_{HOST} - V_{IL_HOST}) \times V_{FAULTB_LOW}}{N \times V_{IL_HOST} \times I_{OL}} \quad (24)$$

Where N is the number of IS31LT3957A devices connected to the same host. I_{OL} is the test condition of FAULTB pin pull down capability. It can be found in the EC table.

Table 3 Fault Actions

Fault Type	Fault Condition	Device Operation After Fault	FAULTB Pin	Fault Reset
VCC UVLO	$V_{CC}<V_{UVLO_F}$	GATE and DIMOUT pull low immediately. IC enters into standby mode and COMP resets to zero.	High Impedance	$V_{CC}>V_{UVLO_R}$
VDD UVLO	$V_{CC}<V_{UVLO_F}$	GATE pulls low immediately. IC enters into standby mode and COMP resets to zero.	High Impedance	$V_{CC}>V_{UVLO_R}$
VDD Pin Short	After startup and $V_{DD}<1.4V$	GATE pulls low immediately. IC enters into standby mode and COMP resets to zero.	Pull Low	$V_{DD}>1.4V$
Over Voltage (LED Open)	$V_{OUT}\geq V_{OVP}$	GATE pulls low immediately. IC enters into standby mode and COMP resets to zero.	Pull Low	$V_{OUT}<(V_{OVP}$-Hysteresis)
Power NMOS Current Limit	$V_{CS}>V_{CS_TH}$	GATE pulls low immediately until the next switching cycle.	High Impedance	$V_{CS}<V_{CS_TH}$
LED String Short (Boost Only)	$(V_{ISP}-V_{ISN})>V_{SENSE_OC}$	GATE and DIMOUT pull low immediately and COMP resets to zero. And retry after 16,000 f_{SW} cycles.	Pull Low	$(V_{ISP}-V_{ISN})<V_{SENSE_OC}$
RT/SYNC Pin Short	$f_{SW}>2.5MHz$	GATE pulls low immediately.	Pull Low	$f_{SW}<2.5MHz$
Thermal Shutdown	$T_J>165°C$	GATE pulls low immediately. IC enters into standby mode and COMP resets to zero.	Pull Low	$T_J<145°C$

PCB LAYOUT CONSIDERATION

As for all switching power supplies, especially those providing high current and using high switching frequencies, layout is an important design step. If layout is not carefully done, the operation could show instability as well as EMI problems.

The high dV/dt surface and dI/dt loops are big noise emission source. To optimize the EMI performance, keep the area size of all high switching frequency points with high voltage compact. Meantime, keep all traces carrying high current as short as possible to minimize the loops.

Please design the PCB layout according to following considerations.

(1) Wide and short traces should be used for connection of the high current paths that helps to achieve better efficiency and EMI performance. Such as the traces of power supply, inductor L1, power NMOS M1, recirculating diode D1, LED load, ground.

(2) Keep the traces of the switching points shorter. The inductor L1, power MOSFET M1 and current recirculating diode D1 should be placed as close to each other as possible and the traces of connection between them should be as short and wide as possible.

(3) To avoid the ground jitter, the components of parameter setting, especially the R_{IS}, R_{CS}, R_{RT}, R_{O2}, C_{CP} should be placed close to the device and keep the traces length to the device pins as short as possible. On the other side, to prevent the noise coupling, the traces of these components should either be far away or be isolated from high-current paths and high-speed switching nodes. These practices are essential for better accuracy and stability.

(4) The capacitor C_{VCC} and C_{VDD} should be placed as close as possible to VCC and VDD pin for good filtering.

(5) For the boost application, the output capacitor C_{OUT} must be placed close to the cathode of D1. For the buck-boost application, the C_{OUT} must be placed close to both of the anode of C_{IN} and the cathode of D1, otherwise the output current performance will be degraded.

(6) All thermal pads on the back of IS31LT3957A, the recirculating diode and the power NMOS package must be soldered to a sufficient size of copper plane with sufficient vias to conduct the heat to

opposite side PCB for adequate cooling.

THERMAL CONSIDERATIONS

The package thermal resistance, θ_{JA}, determines the amount of heat that can pass from the silicon die to the surrounding ambient environment. The θ_{JA} is a measure of the temperature rise created by power dissipation and is usually measured in degree Celsius per watt (°C/W). The junction temperature, T_J, can be calculated by the rise of the silicon temperature, ΔT, the power dissipation, PD, and the package thermal resistance, θ_{JA}, as in Equation (25):

$$P_D = V_{CC} \times (I_{CC} + f_{SW} \times Q_G) \qquad (25)$$

and,

$$T_J = T_A + \Delta T = T_A + P_D \times \theta_{JA} \qquad (26)$$

Where f_{SW} is operation frequency and Q_G is the total gate charge of power NMOS.

When operating the chip at high ambient temperatures, or when driving maximum load current, care must be taken to avoid exceeding the package power dissipation limits. The maximum power dissipation can be calculated using the following Equation (27):

$$P_{D(MAX)} = \frac{125°C - 25°C}{\theta_{JA}} \qquad (27)$$

So,

$$P_{D(MAX)} = \frac{125°C - 25°C}{46.4°C/W} = 2.16W \qquad (28)$$

for eTSSOP-16 package.

Figure 30, shows the power derating of the IS31LT3957A on a JEDEC boards (in accordance with JESD 51-5 and JESD 51-7) standing in still air.

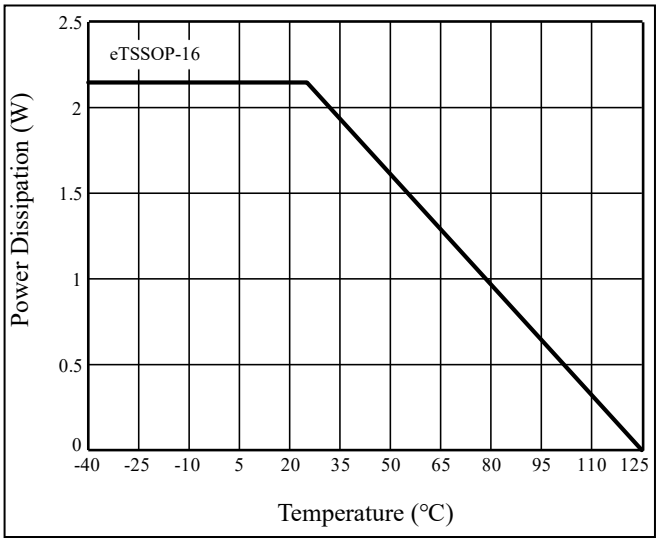


Figure 30 Dissipation Curve (eTSSOP-16)

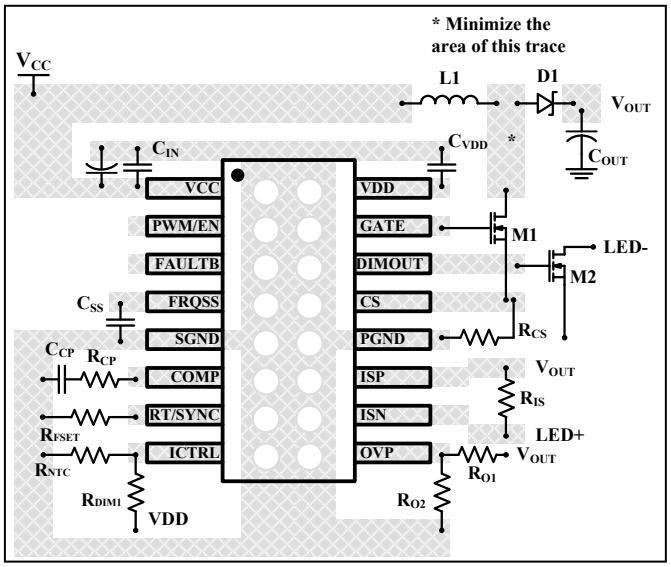


Figure 31 PCB Layout (Boost Configuration)

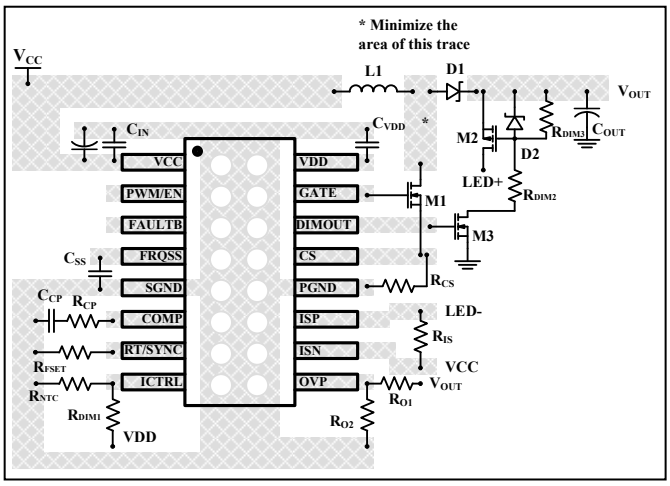


Figure 32 PCB Layout (Buck-Boost Configuration)

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

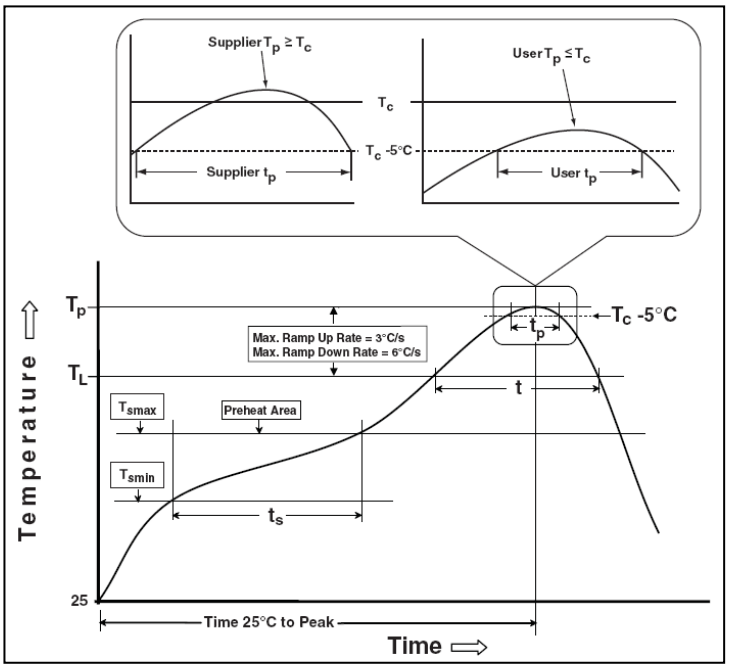
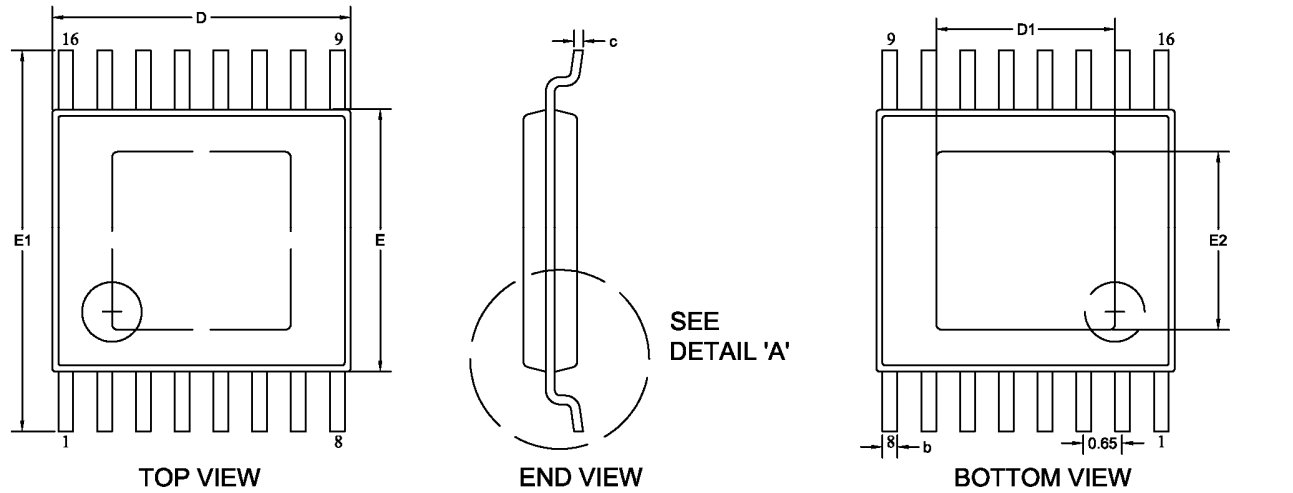


Figure 33 Classification Profile

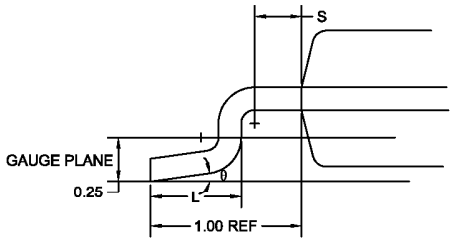
PACKAGE INFORMATION

eTSSOP-16

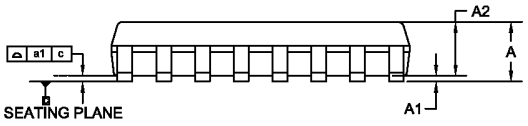


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.00	—	0.15
A2	0.80	0.90	1.05
D	4.90	5.00	5.10
D1	1.70	—	—
E	4.30	4.40	4.50
E1	6.40BSC		
E2	1.50	—	—
L	0.45	0.60	0.75
b	0.19	—	0.30
S	0.20		
c	0.09	—	0.20
θ	0°		8°
a1	0.10		

233-570-249 Rev. B



DETAIL 'A'



SIDE VIEW

NOTES:

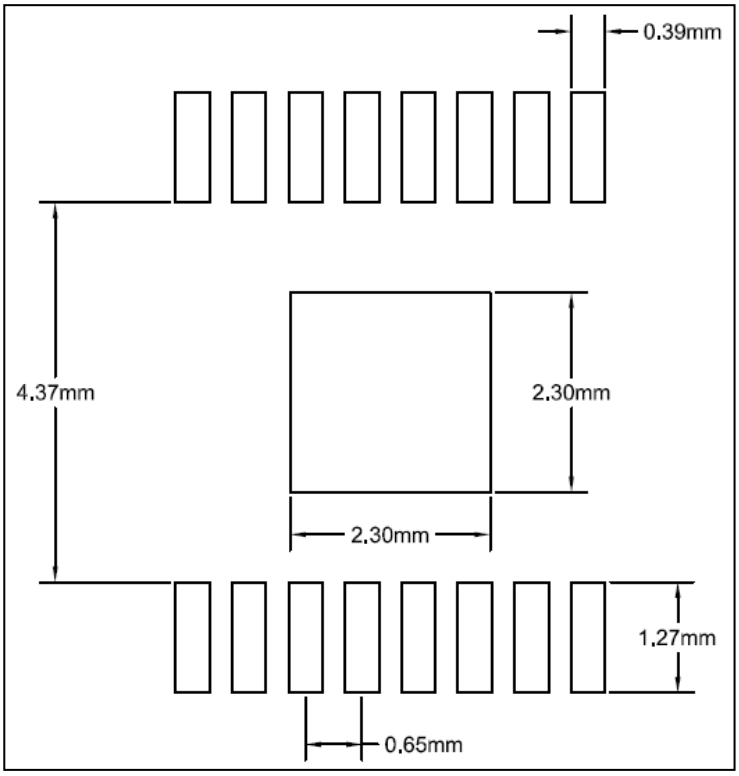
1)The thermal pad shows different shape among different factories.

2)Controlling dimension:mm

3)Reference document:JEDEC MO-153

RECOMMENDED LAND PATTERN

eTSSOP-16



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. user's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
0A	Initial release	2020.02.11
A	Update to final version	2020.03.12
B	1. Update to new Lumissil logo 2. Add RoHS	2024.06.20