IS31LT3505

1.0MHZ BOOST CONVERTER WITH 35V INTERNAL NMOS

December 2024

GENERAL DESCRIPTION

The IS31LT3505 is a constant current step-up converter with internal NMOS. The step-up converter topology allows series connection of the white LEDs so the LED currents are identical for uniform brightness as well as constant output voltage to drive other devices. The output current of each channel can be set by an external resistor and dimming the brightness of LEDs with the PWM signal or DC voltage. The IS31LT3505 operates with a switching frequency up to 1MHz. A low 0.3V feedback voltage minimizes power loss in the current setting resistor for better efficiency. With OVP circuit, the chip and the system can be safe even if the load is not connected.

IS31LT3505 is available in MSOP-10. It operates from 6V to 30V over the temperature range of -40°C to +85°C.

FEATURES

- 6V to 30V supply voltage
- High efficiency: 90% typical
- PWM dimming control
- Fast 1.0MHz switching frequency
- Internal high power 35V NMOS
- Internal soft start
- Adjustable LED Open Protection
- Over-temperature protection
- MSOP-10 package
- RoHS & Halogen-Free Compliance
- TSCA Compliance

APPLICATIONS

- TV monitor backlighting
- PDA, handheld computer
- GPS receiver

TYPICAL APPLICATION CIRCUIT

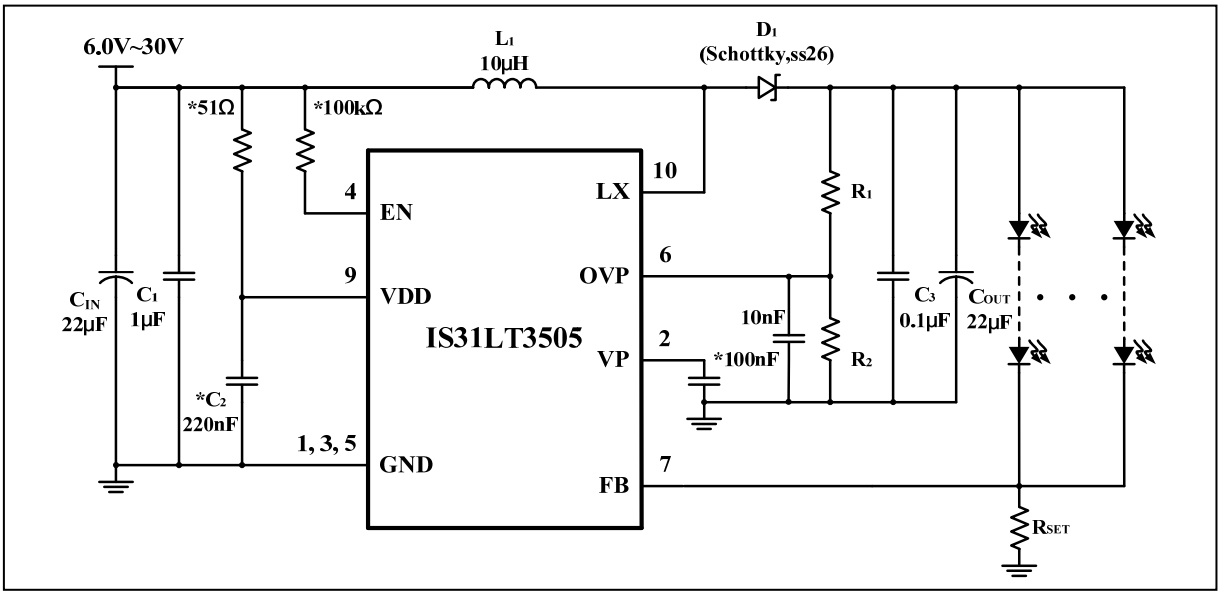
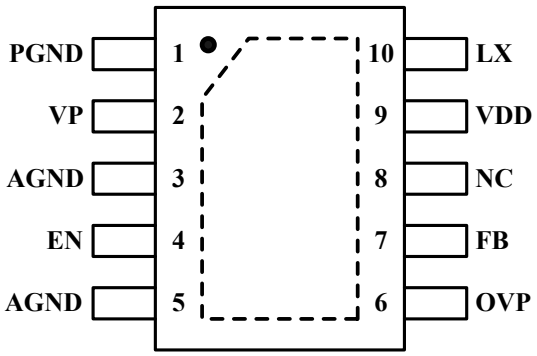


Figure 1 Typical Application Circuit (Constant Current to Drive White LEDs)

Note: These components with * symbol are recommended to fix the value. Or it will decrease the performance of whole system.

PIN CONFIGURATION

Package	Pin Configuration (Top View)
MSOP-10	

PIN DESCRIPTION

No.	Pin	Description
1	PGND	Power ground.
2	VP	Internal 5V regulator. A power supply for the internal NMOS gate driver and the internal control circuitry.
3,5	AGND	Signal ground. All external components ground must be connected to this pin.
4	EN	Enable control input. Do not let this pin floating.
6	OVP	Over-voltage protection of output.
7	FB	Feedback voltage of output.
8	NC	No connection.
9	VDD	Supply voltage.
10	LX	The drain of the internal NMOS.
	Thermal Pad	Connect to ground.

ORDERING INFORMATION
INDUSTRIAL RANGE: -40°C TO +85°C

Order Part No.	Package	QTY/Reel
IS31LT3505-SLS2-TR	MSOP-10, Lead-free	2500

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{DD}	-0.3V ~ +40V
Voltage at EN, LX pin	-0.3V ~ +40V
All other pins	-0.3V ~ +6.0V
Operate temperature range	-40°C ~ +85°C
Storage temperature range	-65°C ~ +150°C
Junction temperature range	-40°C ~ +150°C
θ_{JA}	60°C/W
ESD (HBM)	±2.5kV

Note: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{DD} = 12V, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage		6		30	V
UVLO	Undervoltage threshold	VP falling		2.9		V
ΔUVLO	Undervoltage threshold hysteresis			100		mV
I_{DD}	Supply current	Continuous switching		2		mA
		No switching		1.1		
I_{SD}	Shutdown current	V_{EN} = 0V		15		μA
V_P	Internal regulator	6V<V_{DD}<30V, C_{VP}=100nF	4.5	5	5.5	V
$V_{EN\ ON}$	EN on threshold	V_{EN} rising	1.4			V
$V_{EN\ OFF}$	EN off threshold	V_{EN} falling			0.4	V
f_{OSC}	Operation frequency			1		MHz
D_{MAX}	Maximum duty cycle			90		%
R_{DS_ON}	Internal NMOS on-resistance			0.8	1.2	Ω
I_{SW_LK}	Internal NMOS leakage current	V_{SW} = 35V			1	μA
I_{SW_LIMIT}	Internal NMOS current limit	Duty = 90%	1.8	2.1	2.4	A
V_{OVP_TH}	Over voltage threshold			0.9		V
V_{FB}	Feedback voltage		0.285	0.3	0.315	V
T_{OTP}	Over temperature threshold			150		°C
$T_{OTP-HYS}$	Over temperature threshold hysteresis			50		°C

TYPICAL OPERATING CHARACTERISTICS

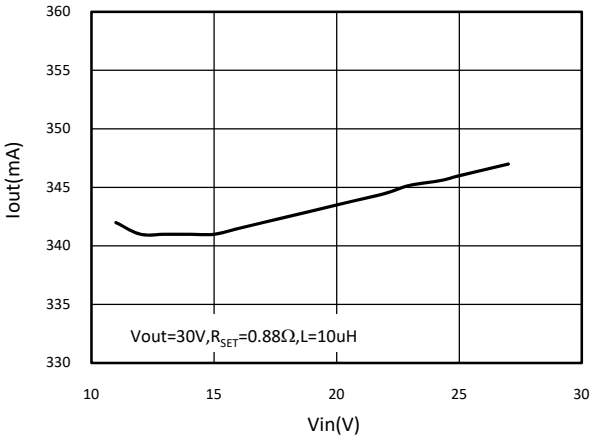


Figure 2 Iout vs. Vin

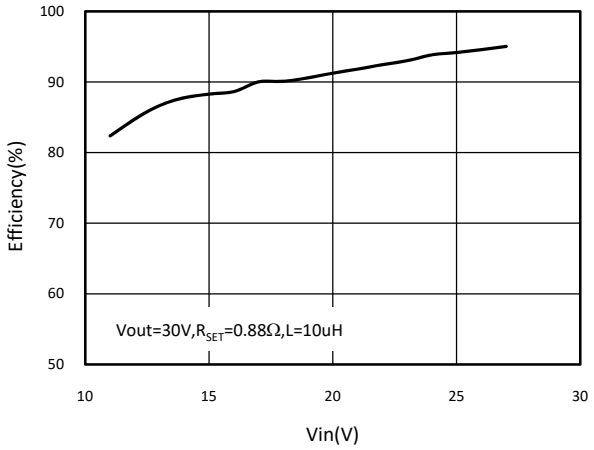


Figure 3 Efficiency vs. Vin

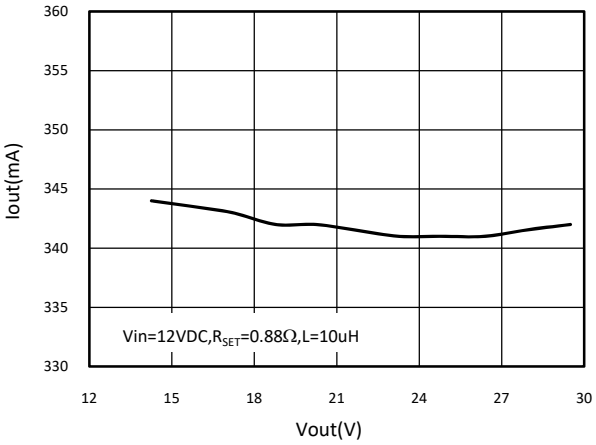


Figure 4 Iout vs. Vout

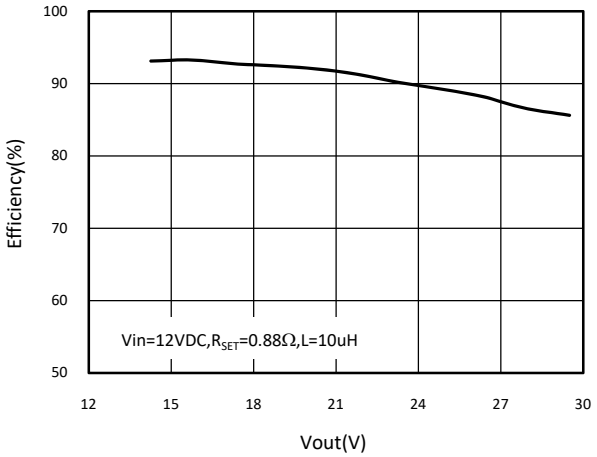


Figure 5 Efficiency vs. Vout

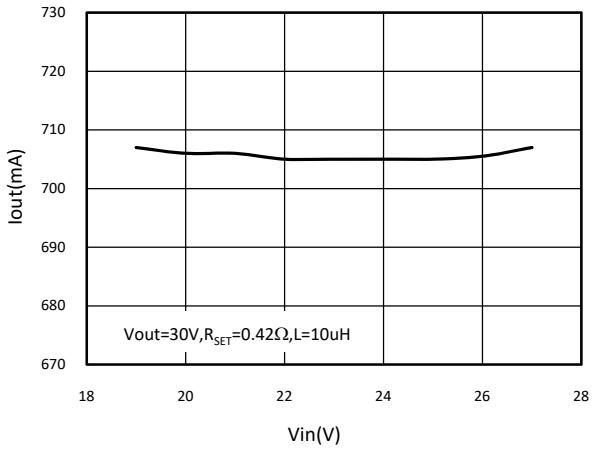


Figure 6 Iout vs. Vin

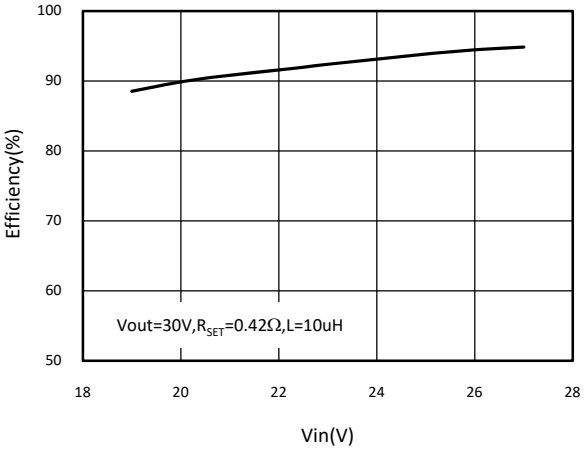


Figure 7 Efficiency vs. Vin

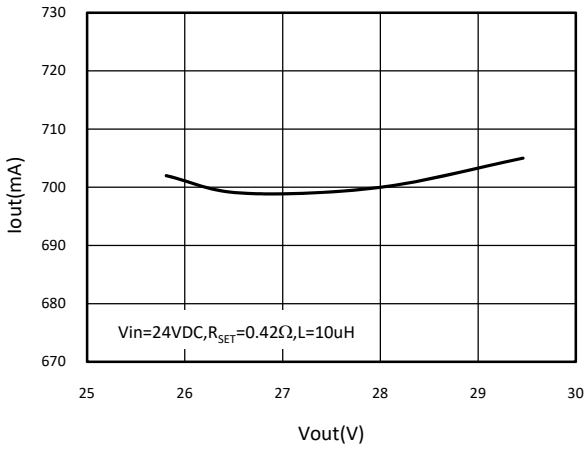


Figure 8 Iout vs. Vout

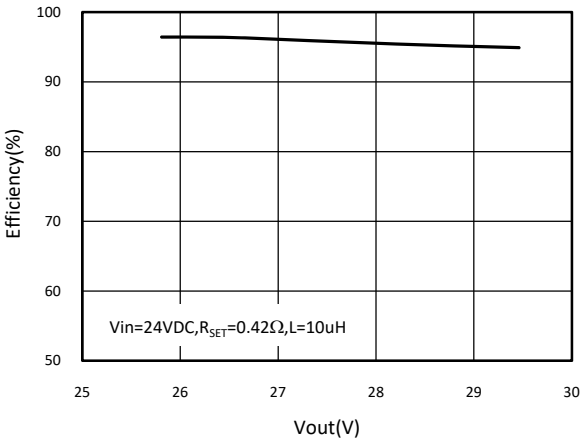


Figure 9 Efficiency vs. Vout

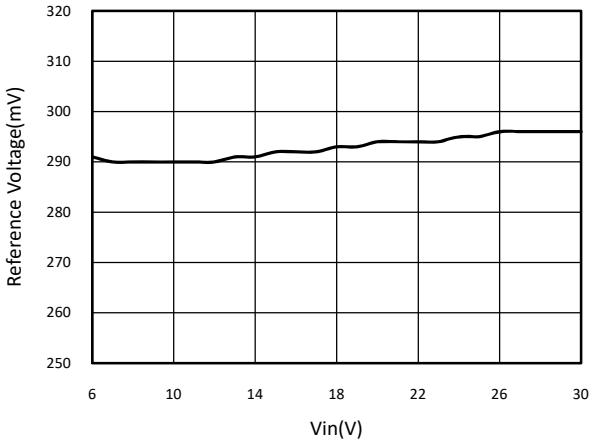


Figure 10 V_{FB} voltage vs. Vin

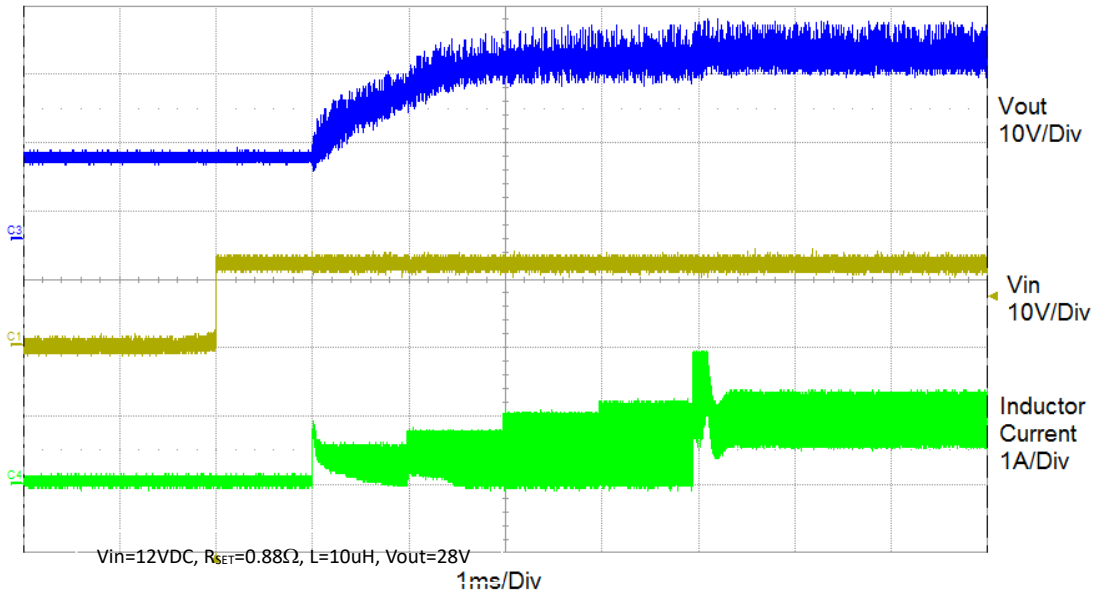


Figure 11 Soft-start waveform

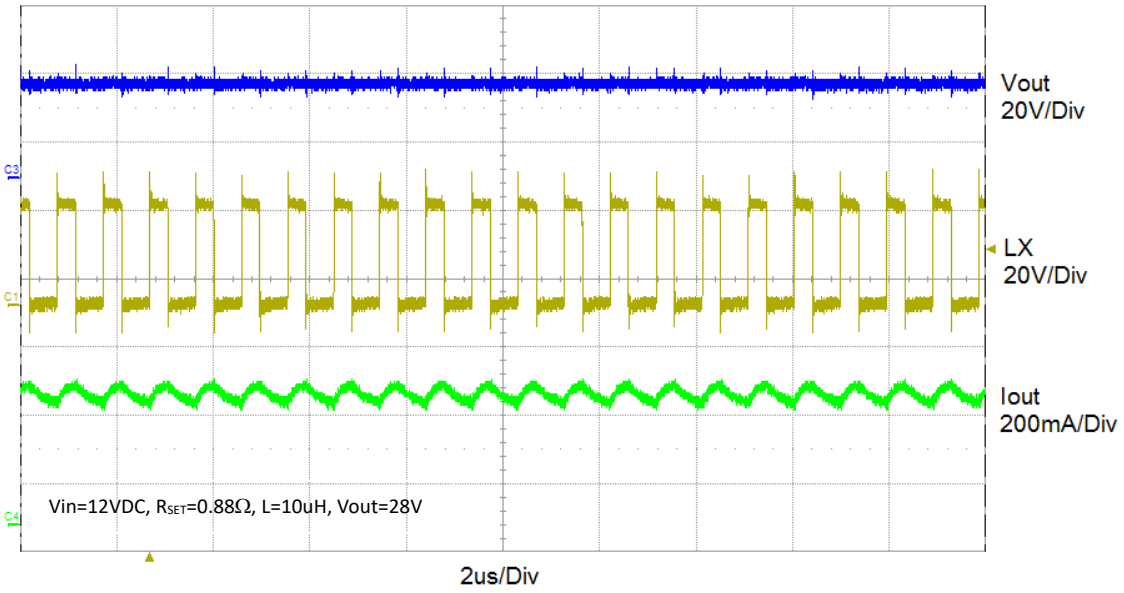


Figure 12 Operation waveform

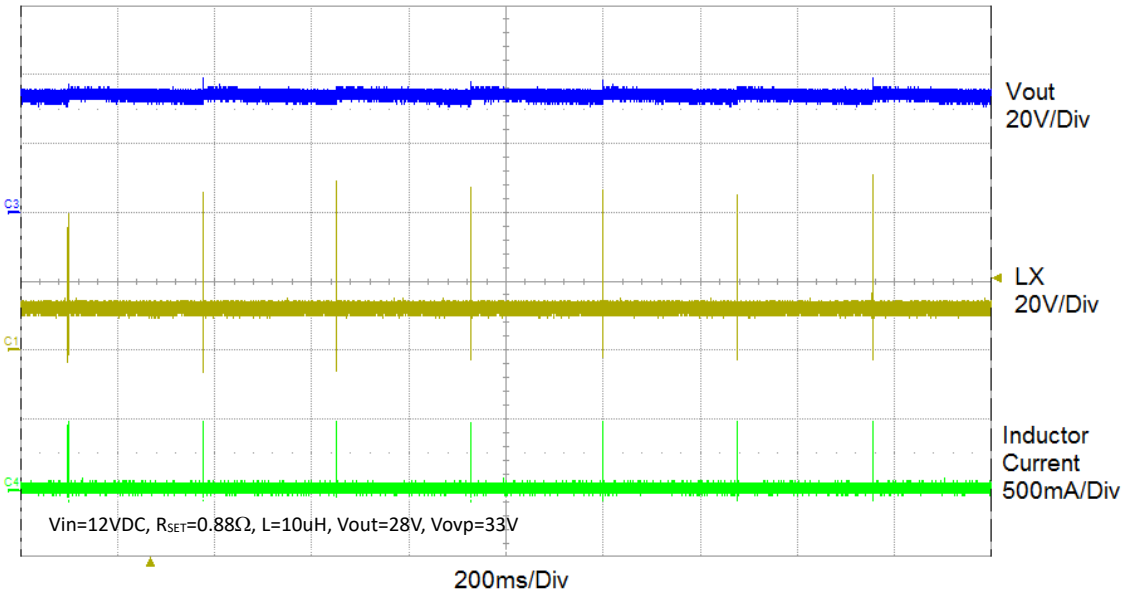
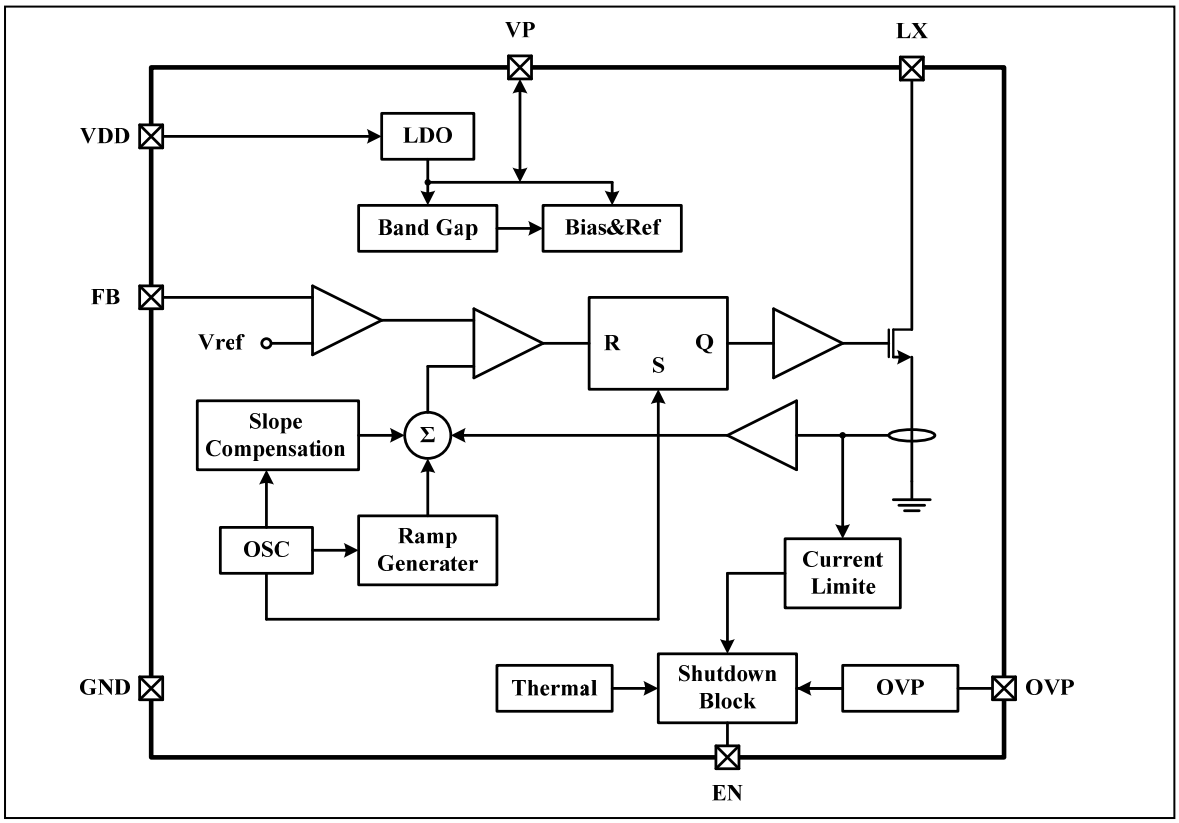


Figure 13 OVP waveform

FUNCTIONAL BLOCK DIAGRAM



APPLICATION INFORMATION

INPUT AND OUTPUT CAPACITOR

The output capacitor is decided by the output voltage ripple. A low ESR ceramic capacitor (recommended 22μF) and a 0.1μF/50V ceramic capacitor in parallel will provide sufficient output capacitance for most applications. The input capacitor is used to reduce the input voltage ripple and noise. A low ESR electric capacitor (22μF or larger) and a 1μF/50V ceramic capacitor in parallel as input capacitor is recommended. Place the input and output capacitors close to the IS31LT3505 to reduce the ripple.

INDUCTOR

Inductor value involves trade-offs in performance. Larger inductors reduce inductor ripple current and larger inductors also bring in unwanted parasitic resistor that degrade the performance. Select an inductor with a rating current over input average current and the saturation current over the Internal NMOS current limit. A 10μH inductor with saturation current over 2A is sufficient for the most applications.

DIODE

To achieve high efficiency, a Schottky diode must be used. Ensure that the diode's average and peak current rating exceed the output LED current and inductor peak current. The diode's reverse breakdown voltage must exceed the over voltage protection voltage (V_{OVP}). Therefore, A SS26 Schottky diode is sufficient for the most applications.

SOFT-START

The function of soft-start is made for suppressing the inrush current to an acceptable value at startup. The IS31LT3505 provides a built-in soft-start function by clamping the input current and increasing step-by-step so that the output voltage will rise gradually in the soft-start period.

LED CURRENT CONTROL

The IS31LT3505 regulates the LED current by setting the external resistor connecting to feedback and ground. The internal feedback reference voltage is 0.3V (Typ.). The LED current can be set from the Formula (1) easily.

$$I_{LED} = \frac{V_{FB}}{R_{SET}} \qquad (1)$$

In order to have an accurate LED current, precision resistors are preferred (1% is recommended).

DIMMING CONTROL

IS31LT3505 can modulate the brightness of LEDs by controlling the DC voltage or the PWM duty cycle (Figure 14, 15).

Note: The DC voltage (PWM duty cycle) is inversely proportional to the LED current. That is when DC voltage is maximum (the PWM signal is 100% duty cycle), the output current is minimum, ideally zero, and when DC voltage is minimum (the PWM signal is 0% duty cycle), the output current is maximum.

The output LED voltage will decrease when the output current becomes lower. Therefore, it must to ensure the output voltage always higher than the input voltage during the dimming.

DC VOLTAGE CONTROL

Figure 14 shows that the intensity of the LEDs can be adjusted by the DC voltage. As the DC voltage increases, the current pass through R3 increasingly and the voltage drop on R3 increase, i.e. the LED current decreases. The LED current can be calculated by the Formula (2). The internal feedback voltage V_{FB} is 0.3V (Typ.).

$$I_{LED} = \frac{V_{FB} - \frac{R_3 \times (V_{DC} - V_{FB})}{R_4}}{R_{SET}} \qquad (2)$$

When the DC voltage is from 0V to 5V, the value of R3 should be 10kΩ. Refer to Figure 14.

PWM SIGNAL CONTROL

A filtered PWM signal acts as the DC voltage to regulate the output current. The recommended application circuit is shown as Figure 15. In this circuit, the output ripple depends on the frequency of PWM signal. For smaller output voltage ripple, the recommended frequency of 5V PWM signal should be above 2kHz. To the fixed frequency of PWM signal and change the duty cycle of PWM signal can get different output current. The LED current can be calculated by the Formula (3). The internal feedback voltage V_{FB} is 0.3V (Typ.).

$$I_{LED} = \frac{V_{FB} - \frac{R_3 \times (V_{PWM} \times Duty - V_{FB})}{R_4 + R_5}}{R_{SET}} \qquad (3)$$

When it's the 5V PWM signal, the value of R3 should be 10kΩ. Refer to Figure 15.

SETTING THE OUTPUT VOLTAGE

When IS31LT3505 drives other devices (Figure 16) with the constant voltage, the output voltage is set through the Formula (4). The internal feedback voltage V_{FB} is 0.3V (Typ.).

$$V_{OUT} = \frac{V_{FB} \times (R_3 + R_{SET})}{R_{SET}} \qquad (4)$$

SETTING THE OVER VOLTAGE PROTECTION

The open string protection is achieved through the over voltage protection (OVP). In some cases, if the output voltage reaches the programmed OVP voltage (V_{OVP}), the protection will be triggered. To make sure the chip functions properly, the OVP setting resistor divider must be set with a proper value. The OVP voltage should be 3V higher than normal operation output voltage and the maximum should not exceed 35V. OVP pin should connect a 10nF ceramic capacitor to GND to avoid unexpected noise coupling into this pin and affecting the OVP function. The OVP threshold is calculated through the Formula (5).

$$V_{OVP} = \frac{0.9V \times (R_1 + R_2)}{R_2} \qquad (5)$$

SETTING OTHER COMPONENTS

There is an R, C between power supply positive terminal to VDD pin. 51Ω resistor for R and 220nF ceramic capacitor for C are the recommended.

The VP pin, output of the internal regulator, must be connected to a 100nF bypass capacitor.

If EN pin is not used to enable and disable the IS31LT3505, it should be connected to power supply positive through a 100kΩ resistor. The enable pin needs to be terminated and should not be left floating.

These components should be fixed the value as above description, or it will decrease the performance of whole system.

PCB LAYOUT CONSIDERATION

As for all switching power supplies, especially those providing high current and using high switching frequencies, layout is an important design step. If layout is not carefully done, the regulator could show instability as well as EMI problems.

- Wide traces should be used for connection of the high current loop.
- When laying out signal ground (pin 5), it is recommended to use the traces separate from power ground (pin1) traces and connect them together at the input capacitor negative terminal or the large ground plane that will avoid the signal ground shift. Both of signal and power ground should be as wide as possible. Other components ground must be connected to signal ground. Especially the R_{SET} ground to signal ground (pin 5) connection should be as short as possible to have an accurate LED current.
- The capacitor C_{VDD} and C_{VP} should be placed as close as possible to VDD and VP pin for good filtering. The ground of C_{VDD} and C_{VP} must be connected to the signal ground (pin 5).
- LX pin is a fast switching node. The inductor and diode should be placed as close as possible to the switch pin and the connection between this pin to the inductor and the schottky diode should be kept as short and wide as possible. Avoid other traces cross and routing too long in parallel with this node to minimum the noise coupling into these traces.
- The feedback network (FB, OVP) should be as short as possible and routed away from the inductor, the schottky diode and LX pin. The feedback pin and feedback network should be shielded with a ground plane or trace to minimize noise coupling into this circuit.
- The thermal pad on the back of package must be soldered to the large ground plane for ideal power dissipation.

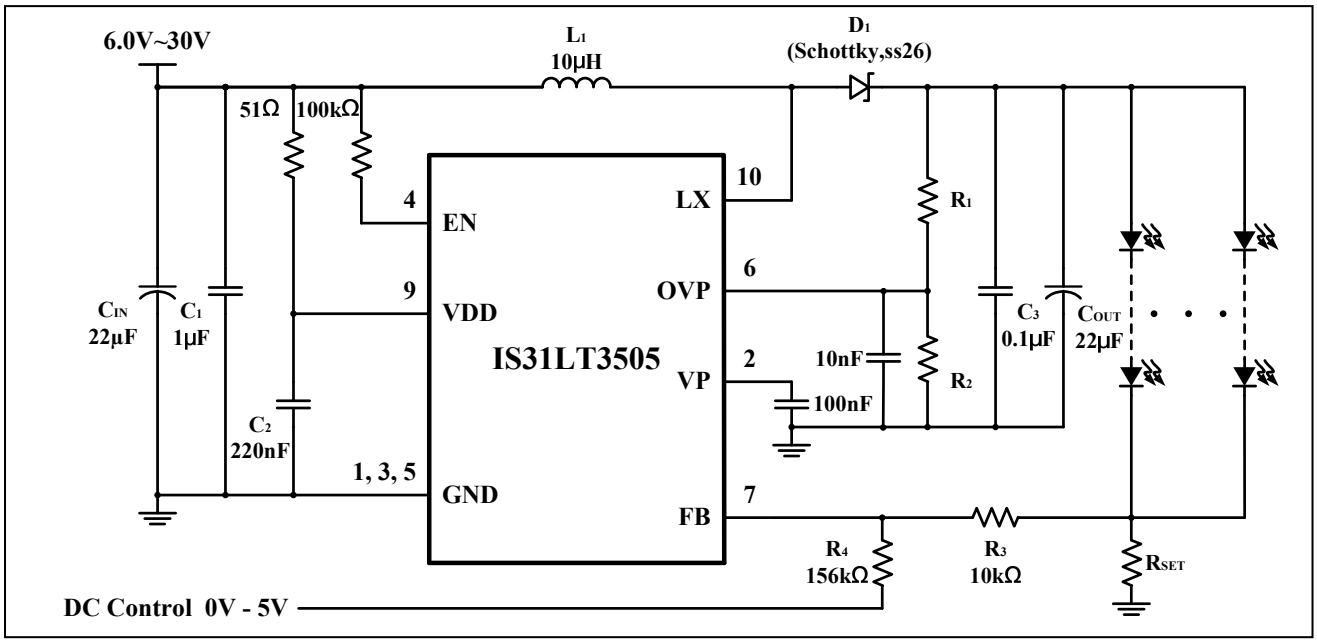


Figure 14 Application Circuit (Constant Current to Drive White LEDs With DC Dimming)

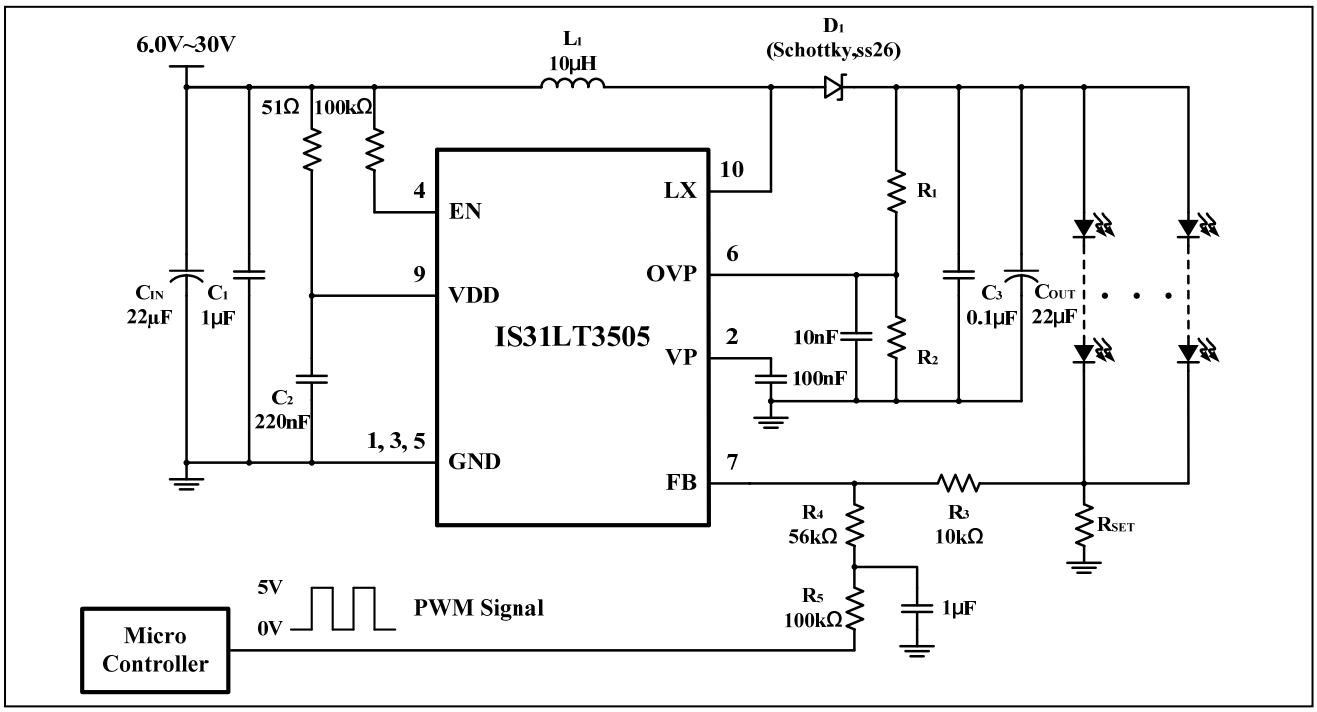


Figure 15 Application Circuit (Constant Current to Drive White LEDs With PWM Dimming)

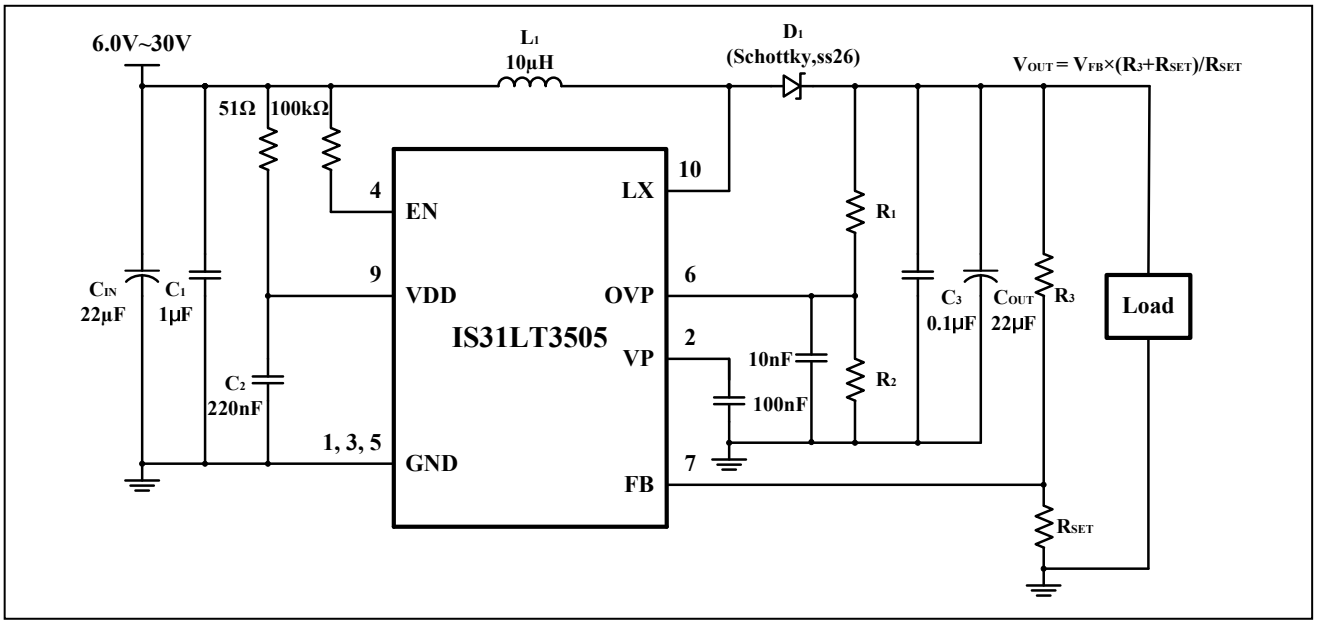


Figure 16 Application Circuit (Constant Voltage to Drive Other Devices)

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

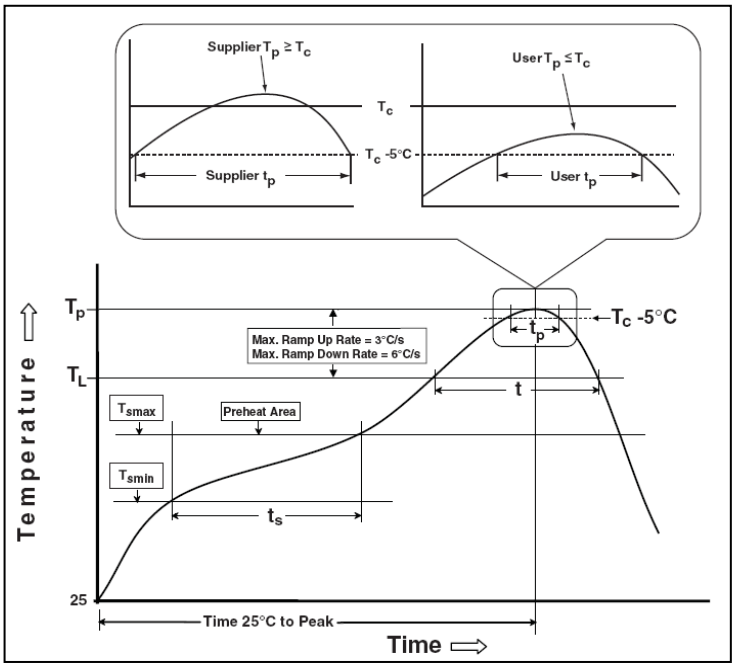
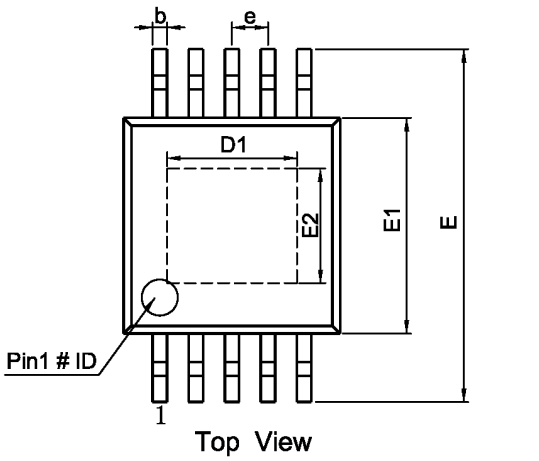
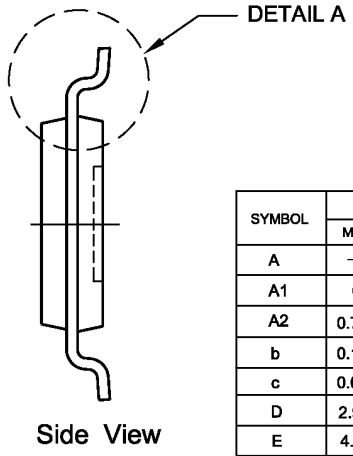


Figure 17 Classification Profile

PACKAGE INFORMATION

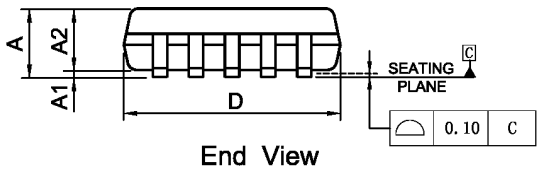
MSOP-10

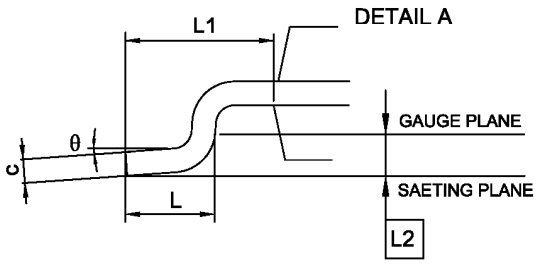




SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.10
A1	0	—	0.15
A2	0.75	0.85	0.95
b	0.17	—	0.33
c	0.08	—	0.23
D	2.90	3.00	3.10
E	4.70	4.90	5.10
E1	2.90	3.00	3.10
L	0.40	0.60	0.80
L1	0.95 REF		
e	0.50 BSC		
L2	0.25 BSC		
θ	0°	—	8°
D1	0.75	—	2.5
E2	0.75	—	2.5

233-570-317 Rev. A



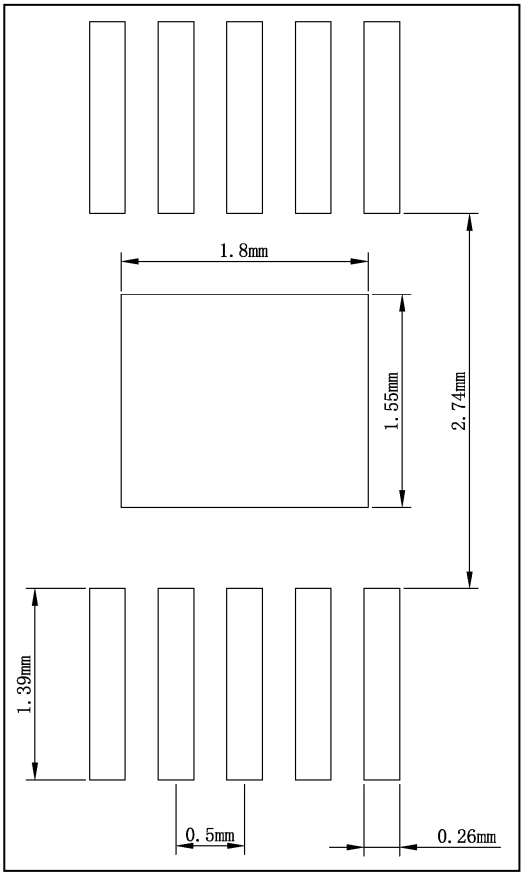


NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.
4. REFERENCE DOCUMENT: JEDEC MO-187F
5. THE SHAPE OF BODY AND THERMAL PAD SHOWE DIFFERENT SHAPE AMONG DIFFERENT FACTORIES.

RECOMMENDED LAND PATTERN

MSOP-10



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. user's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
A	Initial release	2011.09.08
B	The cap of Vp pin changes from 10uF to 100nF. The cap of VDD changes from 1uF to 220nF. The output cap changes from 1uF to 0.1uF.	2013.07.16
C	not release	2014.07.12
D	1.Update EC and ABSOLUTE MAXIMUM RATINGS 2.Add functional block	2014.07.16
E	1. Update to new Lumissil logo 2. Add RoHS	2024.06.07
F	Update land pattern	2024.12.04