IS31FL3758

48CH LED DRIVER WITH 40×9 MATRIX EXTEND

April 2025

GENERAL DESCRIPTIONS

IS31FL3758 is a 48ch LED driver with 48 constant current channels. It also supports from one to eight power scan to become a 48ch, 47×1, 46×2, 45×3…40×8, 40×9 matrix LED driver by control 9~2 external power PMOS. Each channel can be pulse width modulated (PWM) with maximum 8-bit/6+2-bit 256 steps precision for smooth LED brightness control. The maximum output current of each channel is designed to be 60mA, which can be adjusted by 8-bit ×3 global control registers. The maximum output current of each channel is designed to be 60mA, which can be adjusted by three 8-bit global control registers (GCCR for CS1, CS4, CS7 … CS46, GCCG for CS2, CS5, CS8 … CS47, and GCCB for CS3, CS6, CS9 … CS48). Proprietary algorithms are used in IS31FL3758 to minimize power bus noise caused by passive components on the power bus such as MLCC decoupling capacitor. All registers can be programmed via SPI (up to 12MHz) bus or I2C (1MHz) bus.

IS31FL3758 can be turned off with minimum current consumption by either pulling the SDB pin low or by using the software shutdown feature.

IS31FL3758 is available in QFN-60 (7mm×7mm) and can work over temperature range from -40°C to +125°C.

APPLICATIONS

- White good display panel with high brightness
- Gaming machine

FEATURES

- Operating voltage: 2.7V to 5.5V
- Support 48 constant current channels @ 60mA/ch
  - ±7% bit-to-bit output current accuracy @I_{OUT}=40mA,
  - ±6% device-to-device output current accuracy @I_{OUT}=40mA
  - Combined for higher current capability with same current accuracy
  - Minimum headroom voltage of 200mV(typ.) at 40mA
- Support to control the PMOS to become a matrix LED controller Support 48ch, 47×1, 46×2, 45×3, …, 40×8, 40×9, SW need external PMOS, OUT can control the SW timing
- Interface
  - SPI (12MHz)
  - I2C (1MHz)
- SDB pin rising edge reset the interface
- Support 8-bit and 6 + 2-bit dithering PWM
- 260kHz PWM Frequency (at 6+2-bit PWM mode)
- 8-bit ×3 global current adjustment: 1/255-255/255
- Group phase shift (180 degrees) and 6 groups delay reduce audible noise and power ripple
- Spread spectrum
- Open/Short detection Function
- For matrix scanning operation
  - Built-in de-ghosting circuit for CS pins
  - Reduced inactive LED reverse bias to improve LED reliability
- Other protection: over temperature, over current, under voltage
- Operating temperature: -40°C to 125°C
- Programmable detection of open/short, detected LED and store detected LED information in registers for ease of manufacturing/debugging.
- Thermal shutdown
- QFN-60 (7mm×7mm) package
- RoHS & Halogen-Free Compliance
- TSCA Compliance

TYPICAL APPLICATION CIRCUIT

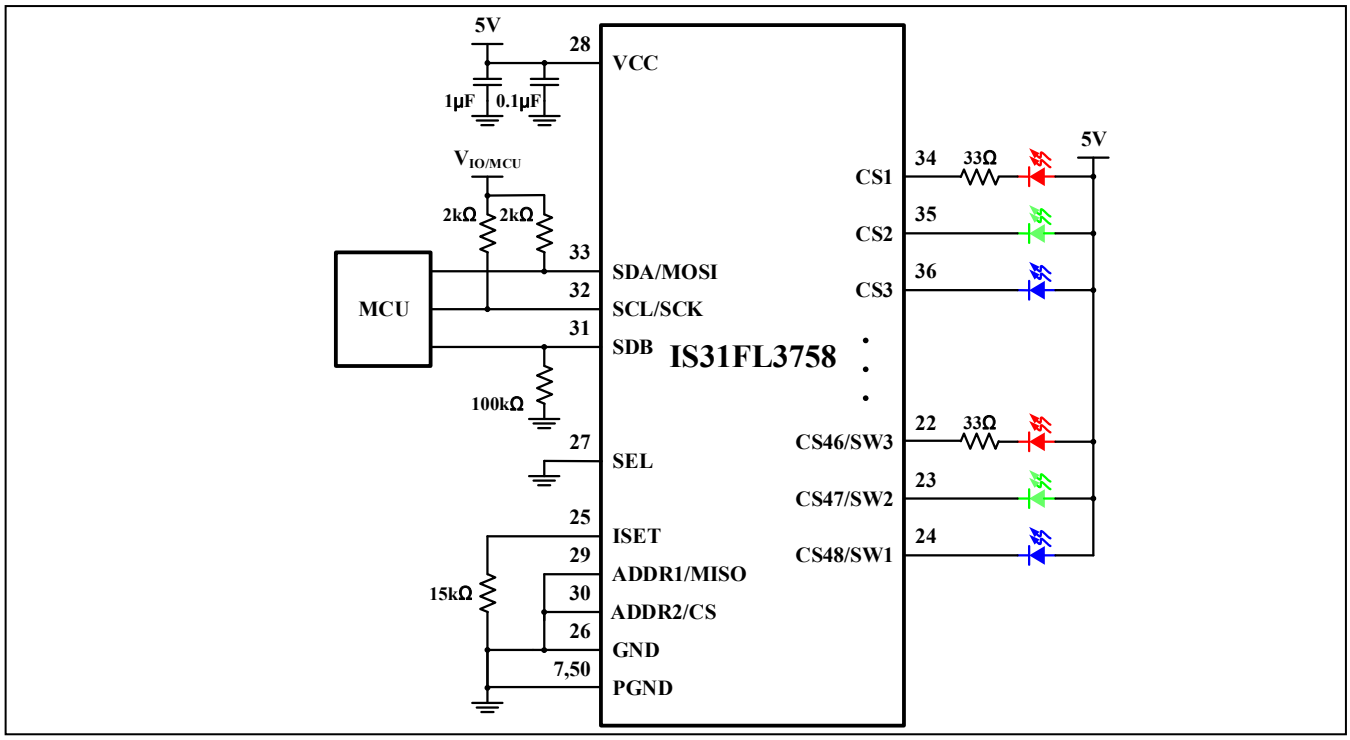


Figure 1 Typical Application Circuit-I2C, 48 channels (RGB)

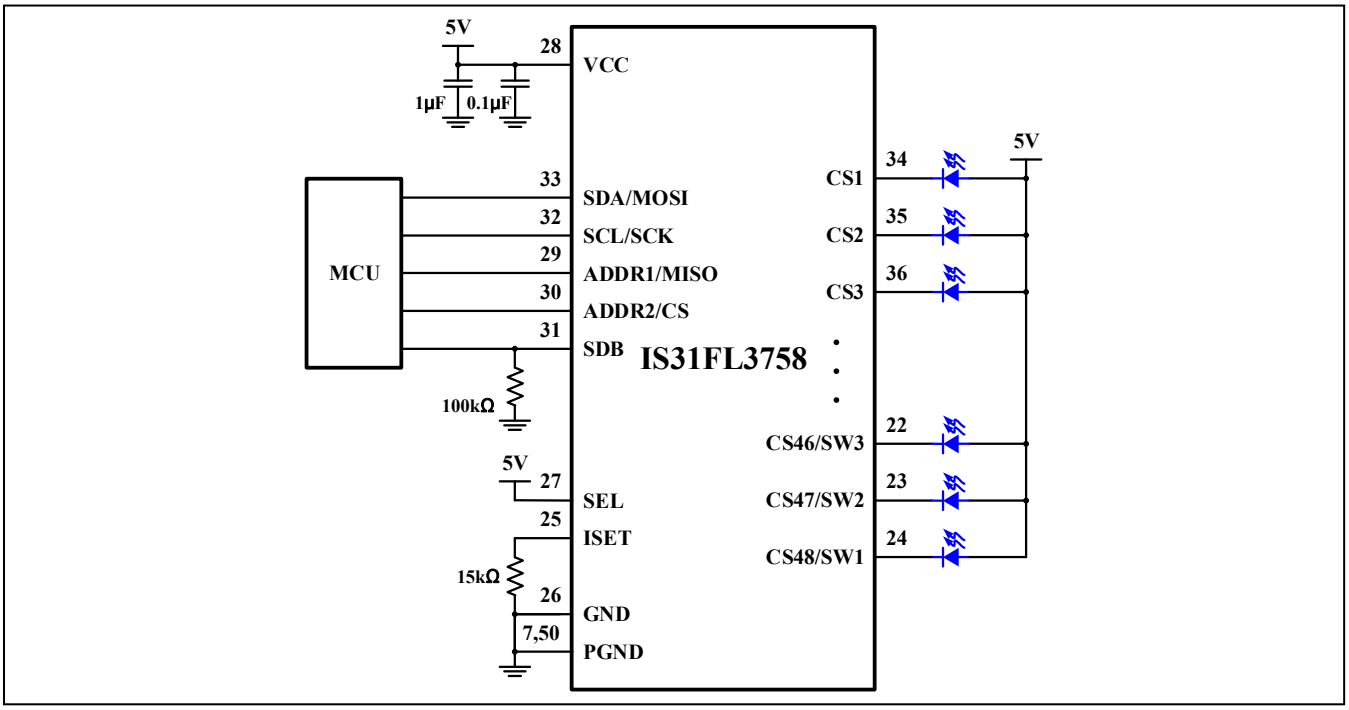


Figure 2 Typical Application Circuit-SPI, 48 Channels

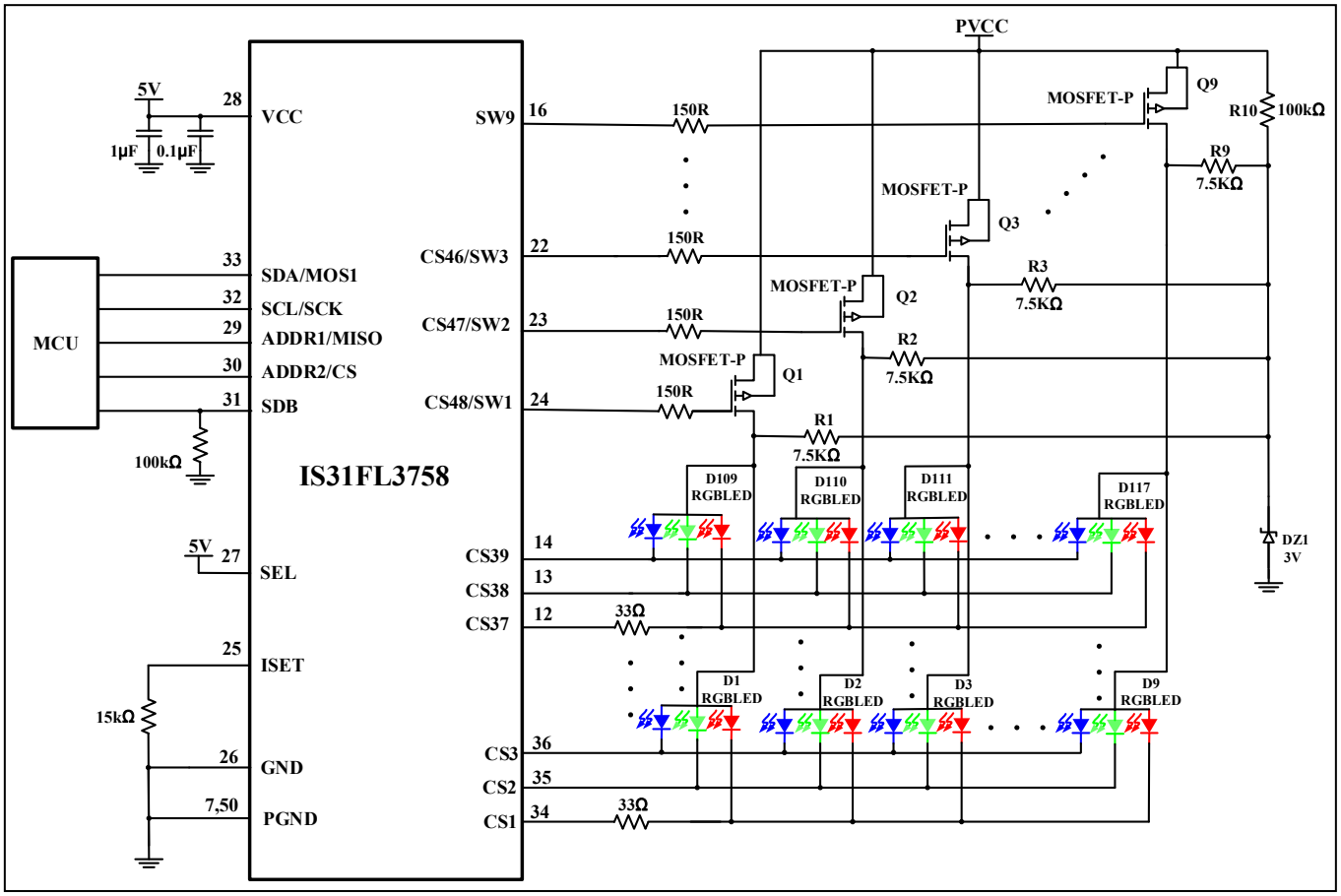
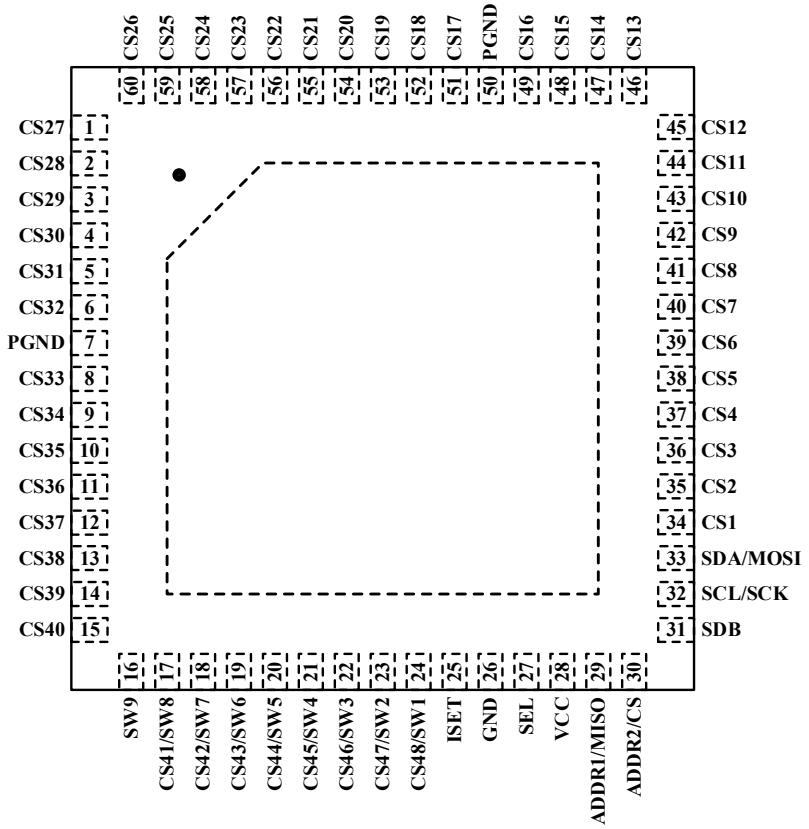


Figure 3 Typical Application Circuit-SPI, 9SW×39CS (Need To Work With PMOS)

PIN CONFIGURATION

Package	Pin Configuration (Top View)
QFN-60	

PIN DESCRIPTION

No.	Pin	Description
1~6,8~15,34~49,51~60	CS1~CS40	Current sink pins.
7,50	PGND	Power GND.
16	SW9	Power switches controllers.
17~24	CS41/SW8 ~ CS48/SW1	Power switches controllers / Current sink pins.
25	ISET	Set the maximum IOUT current.
26	GND	Analog GND.
27	SEL	Select SPI or I2C,SEL=L: I2C, SEL=H: SPI.
28	VCC	Analog and digital circuits.
29	ADDR1/MISO	Address select pin/MISO of SPI.
30	ADDR2/CS	Address select pin/CS of SPI.
31	SDB	Shutdown pin.
32	SCL/SCK	I2C clock / SPI clock.
33	SDA/MOSI	I2C input data / SPI input data.
	Thermal Pad	Connect to GND.

ORDERING INFORMATION

Industrial Range: -40°C to +125°C

Order Part No.	Package	QTY/Reel
IS31FL3758-QFLS4-TR	QFN-60, Lead-free	2500

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	-0.3V ~+6.0V
Voltage at any input pin	-0.3V ~ V_{CC}+0.3V
Maximum junction temperature, T_{JMAX}	+150°C
Storage temperature range, T_{STG}	-65°C ~+150°C
Operating temperature range, T_A=T_J	-40°C ~ +125°C
Package thermal resistance, junction to ambient (4-layer standard test PCB based on JESD 51-2A), θ_{JA}	32.6°C/W
ESD (HBM) ESD (CDM)	±7kV ±750V

Note 1: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

The following specifications apply for V_{CC}= 5V, T_A= 25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage		2.7		5.5	V
I_{CC}	Quiescent power supply current	V_{SDB}=V_{CC}, I_{OUT}=40mA (R_{ISET}=15kΩ), all LEDs off with PWM=0x00, GCC=0x00, PFS=8.3kHz@6+2bit mode, de-ghost disabled	0.5	1	1.5	mA
		V_{SDB}=V_{CC}, I_{OUT}=60mA (R_{ISET}=10kΩ), all LEDs off with PWM=0x00, PFS=260kHz@6+2bit mode, GCC=0x00, de-ghost disabled		3.56		
I_{SD}	Shutdown current	V_{SDB}=0V, Configuration Register written "0000 0001"		0.5	1.2	μA
		V_{SDB}= V_{CC}, Configuration Register written "0000 0000		0.5	1.2	
I_{OUT}	Maximum constant current of CSx	R_{ISET}=10kΩ, GCC=0xFF, PWM=0xFF		60		mA
		R_{ISET}=15kΩ, GCC=0xFF, PWM=0xFF	37	40	43	mA
ΔI_{MAT}	Output current error between outputs (Note 2)	I_{OUT}= 40mA	7		7	%
ΔI_{ACC}	Output current error between devices (Note 3)	I_{OUT}= 40mA	6		6	%
V_{HR}	Current sink headroom voltage CSx	I_{CS}=40mA, R_{ISET}=15kΩ, GCC=0xFF		200	400	mV
I_{LED}	Average current on each LED $I_{OUT(PEAK)}$/Duty (1/9.61)	V_{CC}=5V, R_{ISET}=10kΩ, PWM=0xFF, GCC=0xFF, n=9 (Note 4)		6.22		mA
t_{SCAN}	Period of SWx (SWx)	6+2 mode, Default frequency.	106	113	120	μs
t_{PERIOD}	SW1~SW9 overall time	6+2 mode, Default frequency.	1000	1086	1150	μs
t_{NOL1}	Non-overlap blanking time during scan, the SWx and CSy are all off during this time	PWM is 6+2 mode, default frequency	6.5	7.7	8.5	μs
t_{NOL2}	Delay total time for CS1 to CS 48, during this time, the SWx is on but CSx is not all turned on	PWM is 6+2 mode, default frequency (Note 4)		22		ns

ELECTRICAL CHARACTERISTICS (CONTINUE)

The following specifications apply for V_{CC}= 5V, T_A= 25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{OD}	CSx pin open detect threshold	R_{ISET}=10kΩ, I_{OUT}≥0.1mA, measured at OUTx	0.1	0.19		V
V_{SD}	LED short detect threshold	R_{ISET}=10kΩ, I_{OUT}≥0.1mA, measured at (V_{CC}-V_{OUTx})	1.0	1.2		V
T_{SD}	Thermal shutdown	(Note 4)		160		°C
T_{SD_HY}	Thermal shutdown hysteresis	(Note 4)		25		°C
Logic Electrical Characteristics (SCK, MISO, MOSI, CS, SDB)						
V_{IL}	Logic “0” input voltage	V_{CC}=2.7V~5.5V, SDB/SCL/SDA/ADDR Logic “0” input voltage			0.25× V_{CC}	V
V_{IH}	Logic “1” input voltage	V_{CC}=2.7V~5.5V, SDB/SCL/SDA/ADDR Logic “1” input voltage	0.5× V_{CC}			V
V_{OH}	H level MISO pin output voltage	I_{OH}= -8mA	V_{CC}-0.4V		V_{CC}	V
V_{OL}	L level MISO pin output voltage	I_{OL}= 8mA	0		0.4	V
V_{HYS}	Input Schmitt trigger hysteresis			0.2		V
I_{IL}	Logic “0” input current	SDB=L, V_{INPUT} = L (Note 4)		5		nA
I_{IH}	Logic “1” input current	SDB=L, V_{INPUT} = H (Note 4)		5		nA

Note 2: I_{OUT} mismatch (bit to bit) $\triangle I_{MAT}$ is calculated:

$$\Delta I_{MAT} = MAX\left(ABS\left(\frac{I_{OUTn}(n = 1\sim48)}{\frac{I_{OUT1}+I_{OUT2}+\cdots+I_{OUT48}}{48}} - 1 \right) \right) \times 100\%$$

Note 3: I_{OUT} accuracy (device to device) $\triangle I_{ACC}$ is calculated:

$$\Delta I_{OUT} = ABS\left(\frac{\frac{I_{OUT1}+I_{OUT2}+\cdots+I_{OUT48}}{48} - I_{OUT(TYP)}}{I_{OUT(TYP)}} \right) \times 100\%$$

Where $I_{OUT(IDEAL)}$= 60mA when R_{ISET}= 10kΩ.

Note 4: Guaranteed by design.

DIGITAL INPUT I2C SWITCHING CHARACTERISTICS (NOTE 5)

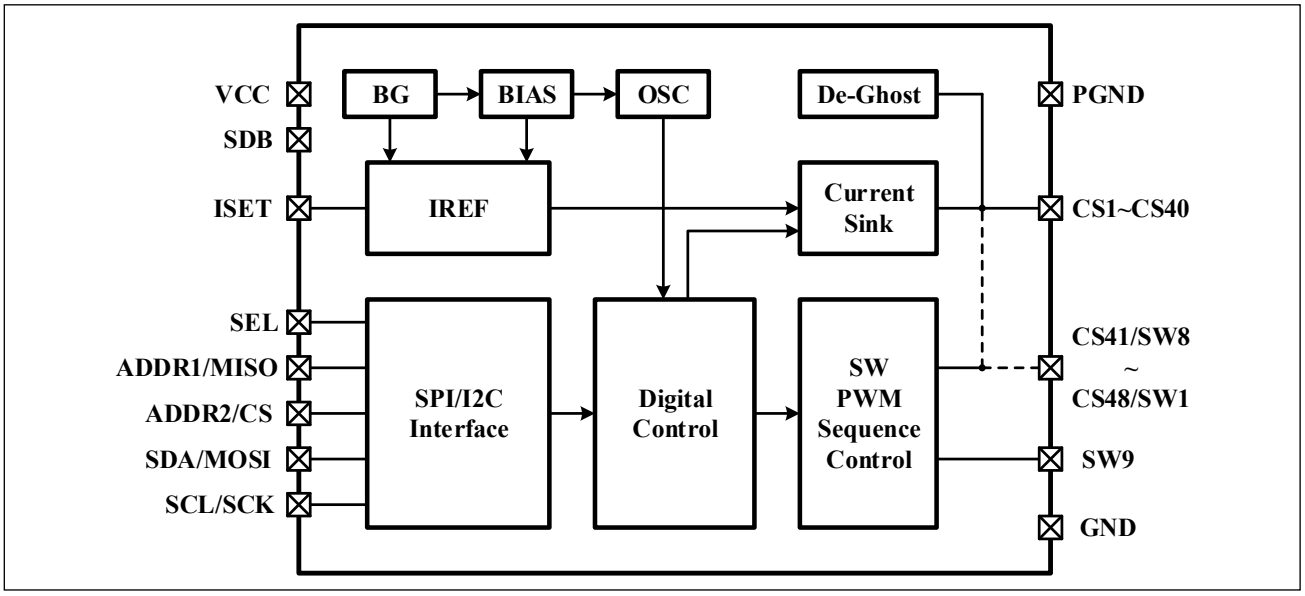
Symbol	Parameter	Fast Mode			Fast Mode Plus			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{SCL}	Serial-clock frequency	-		400	-		1000	kHz
t_{BUF}	Bus free time between a STOP and a START condition	1.3		-	0.5		-	μs
$t_{HD, STA}$	Hold time (repeated) START condition	0.6		-	0.26		-	μs
$t_{SU, STA}$	Repeated START condition setup time	0.6		-	0.26		-	μs
$t_{SU, STO}$	STOP condition setup time	0.6		-	0.26		-	μs
$t_{HD, DAT}$	Data hold time	-		-	-		-	μs
$t_{SU, DAT}$	Data setup time	100		-	50		-	ns
t_{LOW}	SCL clock low period	1.3		-	0.5		-	μs
t_{HIGH}	SCL clock high period	0.7		-	0.26		-	μs
t_R	Rise time of both SDA and SCL signals, receiving	-		300	-		120	ns
t_F	Fall time of both SDA and SCL signals, receiving	-		300	-		120	ns

DIGITAL INPUT SPI SWITCHING CHARACTERISTICS (NOTE 5)

Symbol	Parameter	Min.	Typ.	Max.	Units
f_C	Clock frequency	-		12	MHz
t_{SLCH}	CS active set-up time	34			ns
t_{SHCH}	CS not active set-up time	17			ns
t_{SHSL}	CS detect time	167			ns
t_{CHSH}	CS active hold time	34			ns
t_{CHSL}	CS not active hold time	17			ns
t_{CH}	Clock high time	34			ns
t_{CL}	Clock low time	34			ns
t_{CLCH}	Clock rise time			9	ns
t_{CHCL}	Clock fall time			9	ns
t_{DVCH}	Data in set-up time	7			ns
t_{CHDX}	Data in hold time	9			ns
t_{SHQZ}	Output disable time			34	ns
t_{CLQV}	Clock low to output valid			39	ns
t_{CLQX}	Output hold time	0			ns
t_{QLQH}	Output rise time			17	ns
t_{QLQH}	Output fall time			17	ns

Note 5: Guaranteed by design.

FUNCTIONAL BLOCK DIAGRAM



DETAILED DESCRIPTION

I2C INTERFACE

IS31FL3758 uses a serial bus, which conforms to the I2C protocol, to control the chip's functions with two wires: SCL and SDA. The IS31FL3758 has a 7-bit slave address (A7:A1), followed by the R/W bit, A0. Set A0 to "0" for a write command and set A0 to "1" for a read command. The value of bits A1 and A2 are decided by the connection of the ADDRx pin.

Table 1 Slave Address:

ADDR2	ADDR1	A7:A5	A4:A3	A2:A1	A0
GND	GND	001	00	00	0/1
GND	SCL		00	01	
GND	SDA		00	10	
GND	VCC		00	11	
SCL	GND		01	00	
SCL	SCL		01	01	
SCL	SDA		01	10	
SCL	VCC		01	11	
SDA	GND		10	00	
SDA	SCL		10	01	
SDA	SDA		10	10	
SDA	VCC		10	11	
VCC	GND		11	00	
VCC	SCL		11	01	
VCC	SDA		11	10	
VCC	VCC		11	11	

ADDR1/2 connected to GND, (A2:A1)/(A4:A3)=00;
ADDR1/2 connected to VCC, (A2:A1)/(A4:A3)=11;
ADDR1/2 connected to SCL, (A2:A1)/(A4:A3)=01;
ADDR1/2 connected to SDA, (A2:A1)/(A4:A3)=10;

The SCL line is uni-directional. The SDA line is bi-directional (open-drain) with a pull-up resistor (typically 400kHz I2C with 4.7kΩ, 1MHz I2C with 2kΩ). The maximum clock frequency specified by the I2C standard is 1MHz. In this discussion, the master is the microcontroller, and the slave is the IS31FL3758.

The timing diagram for the I2C is shown in Figure 4. The SDA is latched in on the stable high level of the SCL. When there is no interface activity, the SDA line should be held high.

The "START" signal is generated by lowering the SDA signal while the SCL signal is high. The start signal will alert all devices attached to the I2C bus to check the incoming address against their own chip address.

The 8-bit chip address is sent next, most significant bit first. Each address bit must be stable while the SCL level is high.

After the last bit of the chip address is sent, the master checks for the IS31FL3758's acknowledge. The master releases the SDA line high (through a pull-up resistor). Then the master sends an SCL pulse. If the IS31FL3758 has received the address correctly, then it holds the SDA line low during the SCL pulse. If the SDA line is not low, then the master should send a "STOP" signal (discussed later) and abort the transfer.

Following acknowledge of IS31FL3758, the register address byte is sent, most significant bit first. IS31FL3758 must generate another acknowledge indicating that the register address has been received.

Then 8-bit of data byte are sent next, most significant bit first. Each data bit should be valid while the SCL level is stable high. After the data byte is sent, the IS31FL3758 must generate another acknowledge to indicate that the data was received.

The "STOP" signal ends the transfer. To signal "STOP", the SDA signal goes high while the SCL signal is high.

ADDRESS AUTO INCREMENT

To write multiple bytes of data into IS31FL3758, load the address of the data register that the first data byte is intended for. During the IS31FL3758 acknowledge of receiving the data byte, the internal address pointer will increment by one. The next data byte sent to IS31FL3758 will be placed in the new address, and so on. The auto increment of the address will continue as long as data continues to be written to IS31FL3758 (Figure 7).

READING OPERATION

Most of the registers can be read.

To read the registers, after I2C start condition, the bus master must send the IS31FL3758 device address with the R/$\overline{W}$ bit set to "0", followed by the register address which determines which register is accessed. Then restart I2C, the bus master should send the IS31FL3758 device address with the R/$\overline{W}$ bit set to "1". Data from the register defined by the command byte is then sent from the IS31FL3758 to the master (Figure 8).

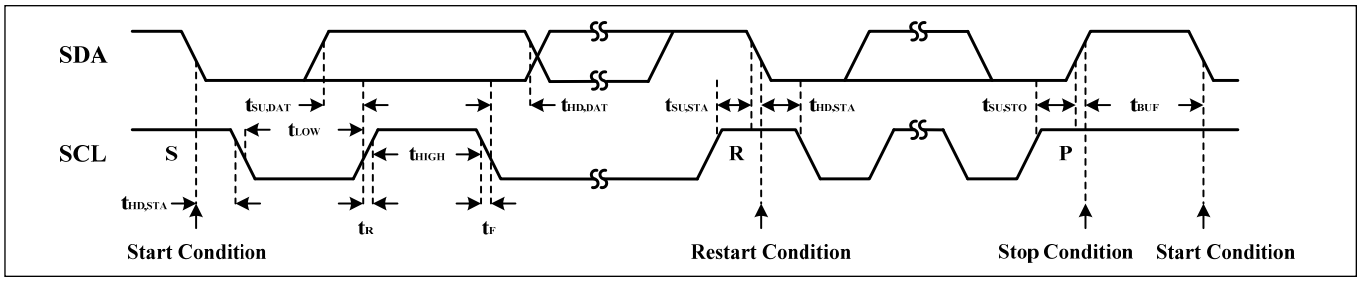


Figure 4 I2C Interface Timing

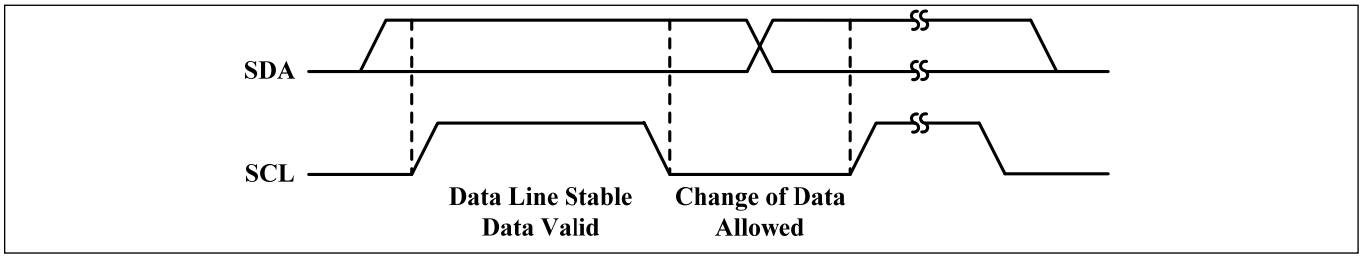


Figure 5 I2C Bit Transfer

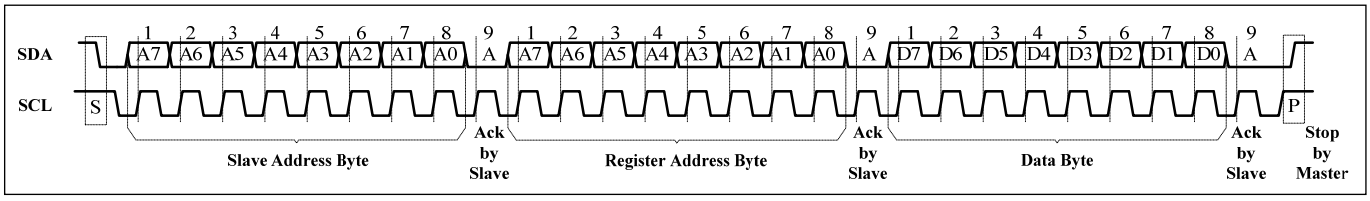


Figure 6 I2C Writing to IS31FL3758 (Typical)

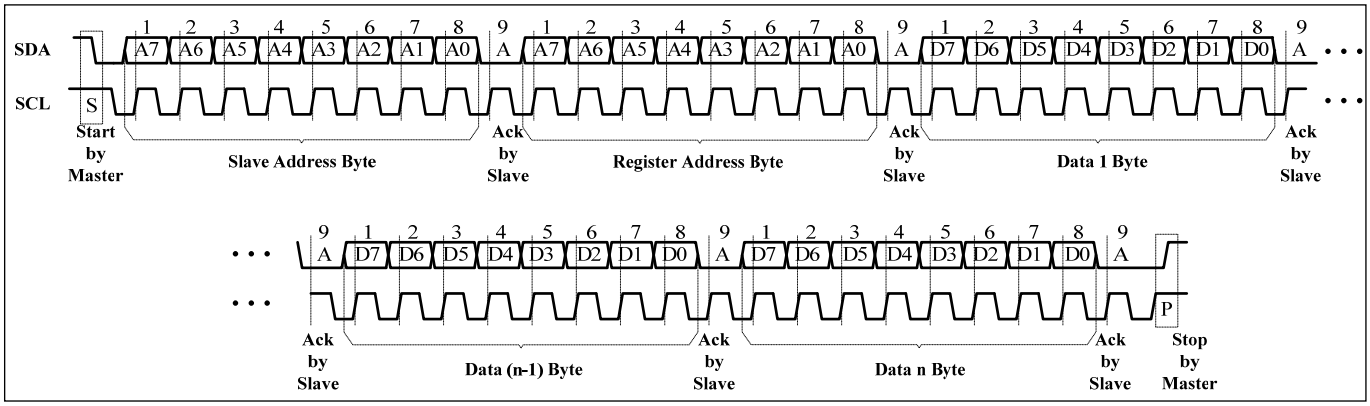


Figure 7 I2C Writing to IS31FL3758 (Automatic Address Increment)

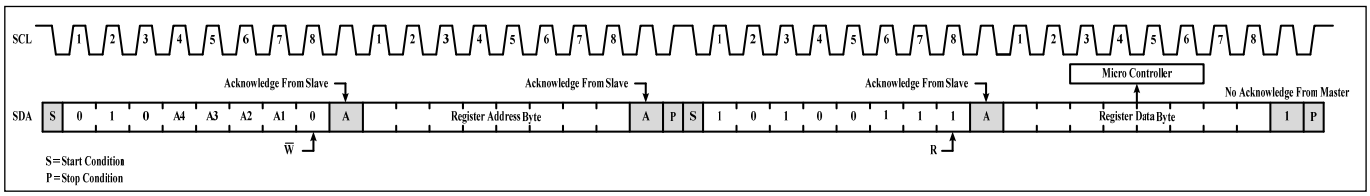


Figure 8 I2C Reading from IS31FL3758

SPI INTERFACE

IS31FL3758 uses a SPI protocol to control the chip's function with four wires: CS, SCK, MOSI and MISO. SPI transfer starts form CS pin from high to low controlled by Master (Microcontroller), and IS31FL3758 latches data when clock rising, that is mode 0, the SCLK is Low when idle, and the Master samples at the rising edge (CPOL=0, CPHA=0).

SPI data format is 8-bit length. The first command byte composite of 1-bit R/W bit, 3-bit chip ID bit and 4-bit page bit. The command byte must be sent first and is followed by register address byte then the register data. If the R/W bit is "0", it will be written operation and Master (Micro-controller) can write the register data into the register.

The maximum SCK frequency supported in IS31FL3758 is 12MHz.

Table 2 SPI Command Byte

Name	R/W	ID Bit	Page No.
Bit	D7	D6:D4	D3:D0
Value	0: Write 1: Read	001	0x00: Point to Page 0 0x01: Point to Page 1

ADDRESS AUTO INCREMENT

To write multiple bytes of data into IS31FL3758, load the address of the data register that the first data byte is intended for. During the 8th rising edge of receiving the data byte, the internal address pointer will increment by one. The next data byte sent to IS31FL3758 will be placed in the new address, and so on. The auto increment of the address will continue as long as data continues to be written to IS31FL3758 (Figure 12).

READING OPERATION

Page 0~Page 1 registers can be read by SPI.

To read the registers of Page 0 through Page 1, The D7 of the Command Byte needs to be set to "1" and select the page number. If read one register, as shown in Figure 13, read the MISO data after sending the command byte and register address. If read more registers, as shown in Figure 14, the register address will auto increase during the 8th rising edge of receiving the last bit of the previous register data.

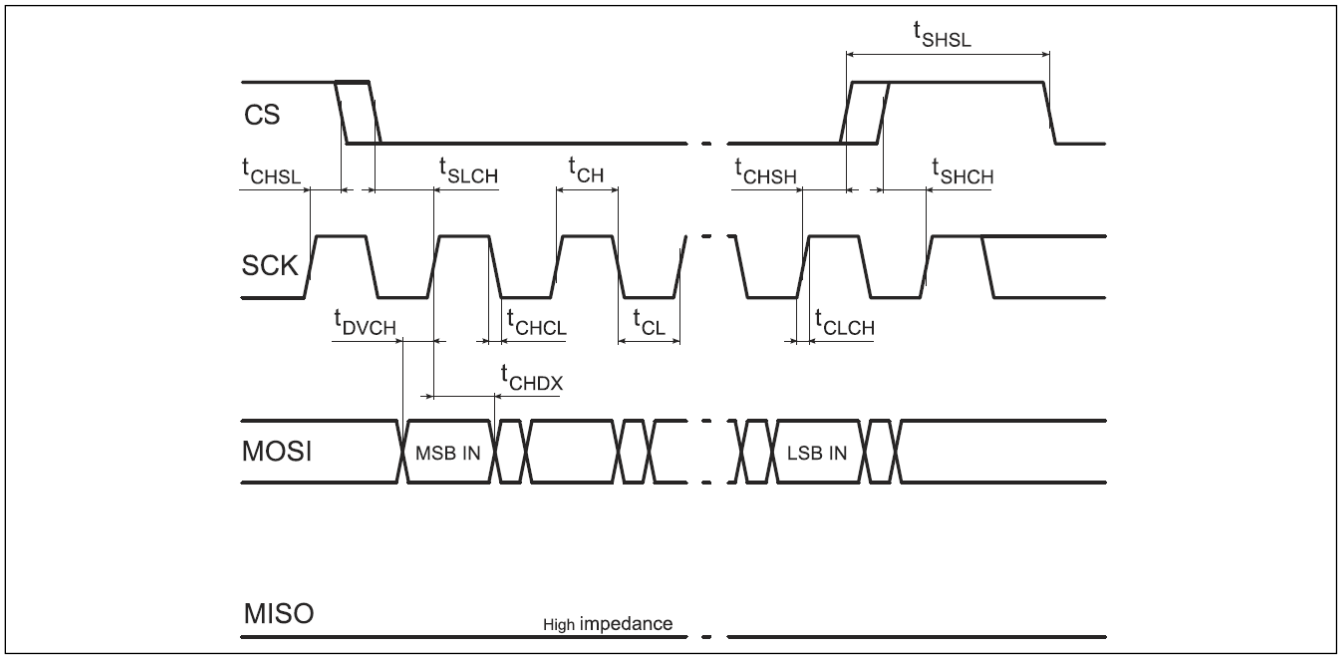


Figure 9 SPI Input Timing

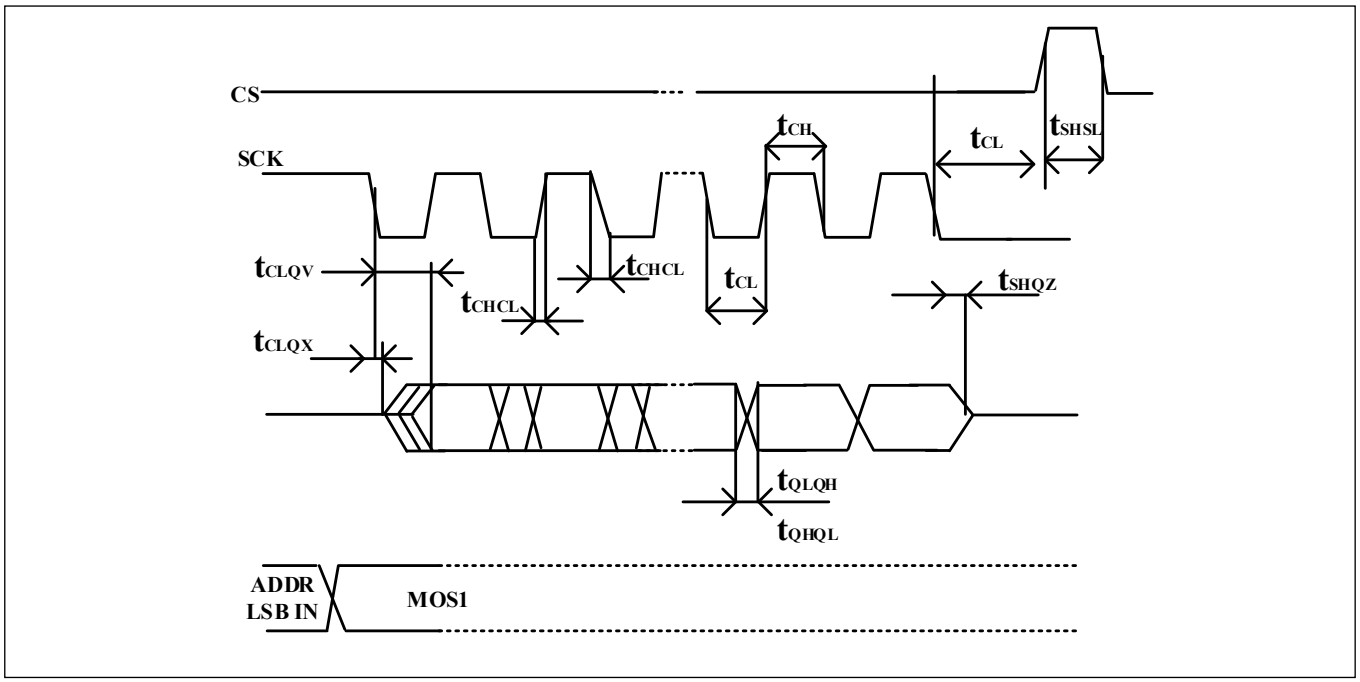


Figure 10 SPI Input Timing

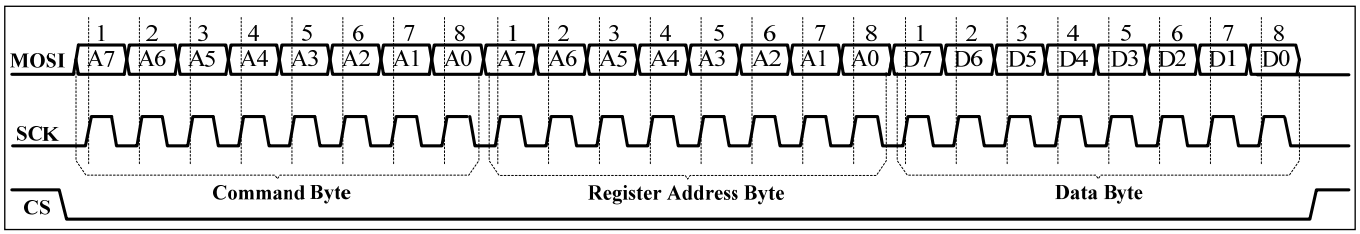


Figure 11 SPI writing to IS31FL3758 (Typical)

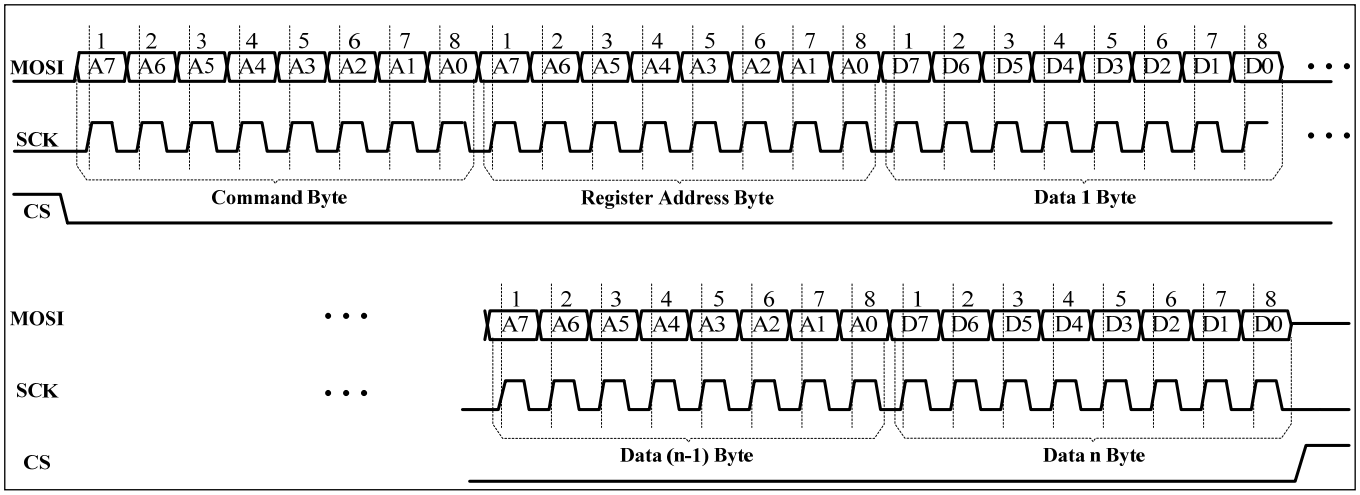


Figure 12 SPI writing to IS31FL3758 (Automatic address increment)

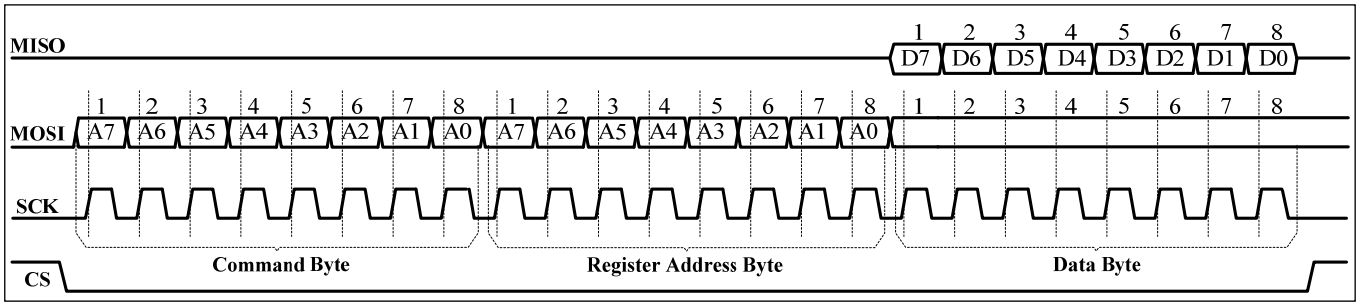


Figure 13 SPI Reading From IS31FL3758 (Typical)

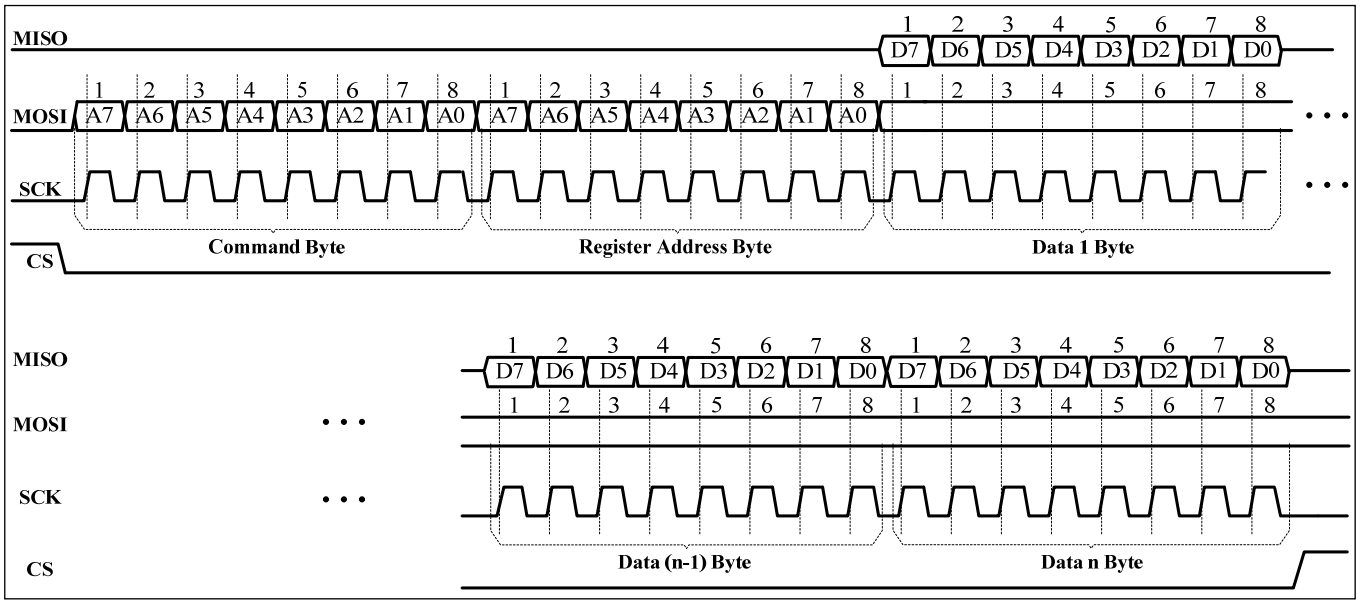


Figure 14 SPI Reading From IS31FL3758 (Automatic Address Increment)

REGISTER DEFINITIONS

Table 3 Command Register Definition

Address	Name	Function	Table	R/W	Default
E7h	Command Register	Available Page 0 to Page 1 Registers	4	W	0000 0000
E8h	Command Register Write Lock	To unlock Command Register	-	W	0000 0000

Note 6: For SPI mode only, the command already include the page information and it does not need to unlock the command register.

REGISTER PAGE CONTROL

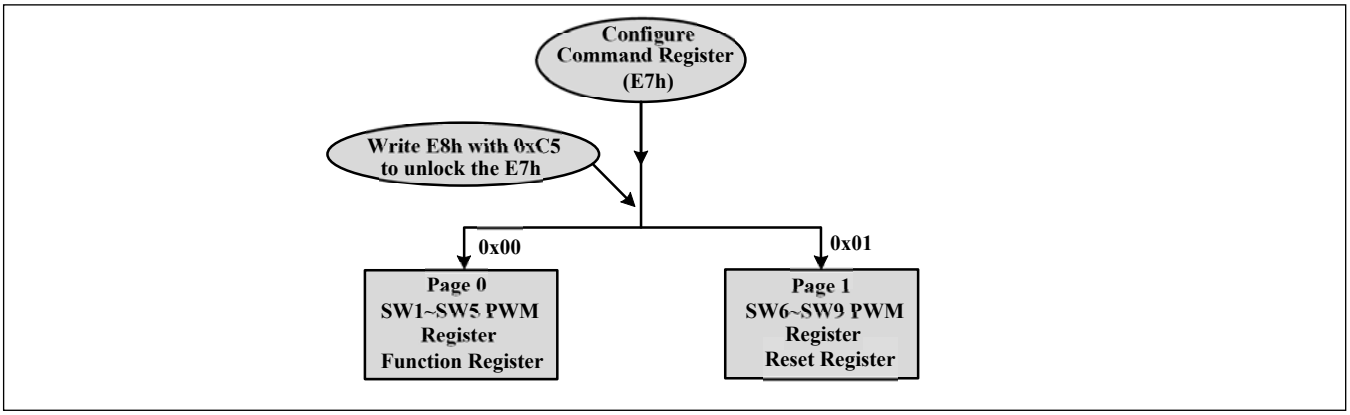


Figure 15 Register Pages (For I2C Mode Only)

Table 4 E7h Command Register

Data	Hex	Function
0000 0000	0x00	Point to Page 0(PG0): PWM and Function Register (SW1~SW5 PWM Register is available)
0000 0001	0x01	Point to Page 1(PG1): PWM and Reset Register (SW6~SW9 PWM Register is available)
Others	-	Not allowed

Note 7: Register E7h is not in any of above pages, and it can swap the pages at any time, when power up, default page is page 0(E7h=0x00), and all the writing will be stored in page 0, if it is not swapped to other pages. Follow the sequence above in table 4 to swap to a new page:

SPI mode: The SPI command already includes page information, see table 2 for detail information.

For example, when write “0000 0001” (0x01) in the Command Register (E7h), Note that E8h needs to be set to "0xC5" to unlock E7h first, the data written will be stored on page 1, the PWM data of SW6-SW9.

E8h Command Register Write Lock Register

To select the PG0~PG1, need to unlock this register first, with the purpose of avoiding mis-operation of this register. When E8h is written with 0xC5, E7h is allowed to modify once, after the E7h is modified the E8h will reset to be 0x00 at once.

Table 5 Register Definition

Address	Name	Function	Table	R/W	Default
Page 0, I2C: E7h=0x00, SPI page No.=0x00					
01h~ECh	PWM Register_SW1-SW5	Set SW1-SW5 PWM for each LED	6	R/W	0000 0000
EFh	Fault State Register	Set over temperature/current flag and LED open short flag.	7	R	0000 0000
F0h	Configuration Register	Configure the operation mode	8	R/W	0000 0000
F1h-F3h	Global Current Control Registers	Set the global current	9~11	R/W	0000 0000
F5h	Pull Up voltage Selection /De-ghost Enable Register	Set the pull up voltage for CSy as well as enables/disables de-ghost	12	R/W	0000 1000
F6h	PFS/Phase Enable Register	PFS and phase enable register	13	R/W	0000 0100
F7h	Spread Spectrum Register	SSP& OSC Enable Register	14	R/W	0010 0000
F8h	De-ghost /CS SW Timing	De-ghost Timing Select Register	15	R/W	0000 0000
F9h	Open/Short Enable Register	Open and short function enable	16	R/W	0000 0000
FAh~FFh	Open and short read registers	Store the open or short information	17~22	R	0000 0000
Page 1, I2C: E7h=0x01, SPI page No.=0x01					
01h~B1h	PWM Register_SW6-SW9	Set PWM for SW6-SW9	6	R/W	0000 0000
FFh	Reset Register	Reset the values to default	-	W	0000 0000

PWM Register Page 0/Page 1

SW1/CS48	SW2/CS47	SW3/CS46	SW4/CS45	SW5/CS44	SW6/CS43	SW7/CS42	SW8/CS41	SW9
47X1	46X2	45X3	44X4	43X5	42X6	41X7	40X8	40X9

	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	SW9
CS48	D0								
CS47	CF								
CS46	CE	D6							
CS45	CD	D5	DD						
CS44	CC	D4	DC	E4					
CS43	CB	D3	DB	E3	EB				
CS42	CA	D2	DA	E2	EA	A2			
CS41	C9	D1	D9	E1	E9	A1	A9		
CS40	28	50	78	A0	C8	28	50	78	A0
CS39	27	4F	77	9F	C7	27	4F	77	9F
CS38	26	4E	76	9E	C6	26	4E	76	9E
CS37	25	4D	75	9D	C5	25	4D	75	9D
CS36	24	4C	74	9C	C4	24	4C	74	9C
CS35	23	4B	73	9B	C3	23	4B	73	9B
CS34	22	4A	72	9A	C2	22	4A	72	9A
CS33	21	49	71	99	C1	21	49	71	99
CS32	20	48	70	98	C0	20	48	70	98
CS31	1F	47	6F	97	BF	1F	47	6F	97
CS30	1E	46	6E	96	BE	1E	46	6E	96
CS29	1D	45	6D	95	BD	1D	45	6D	95
CS28	1C	44	6C	94	BC	1C	44	6C	94
CS27	1B	43	6B	93	BB	1B	43	6B	93
CS26	1A	42	6A	92	BA	1A	42	6A	92
CS25	19	41	69	91	B9	19	41	69	91
CS24	18	40	68	90	B8	18	40	68	90
CS23	17	3F	67	8F	B7	17	3F	67	8F
CS22	16	3E	66	8E	B6	16	3E	66	8E
CS21	15	3D	65	8D	B5	15	3D	65	8D
CS20	14	3C	64	8C	B4	14	3C	64	8C
CS19	13	3B	63	8B	B3	13	3B	63	8B
CS18	12	3A	62	8A	B2	12	3A	62	8A
CS17	11	39	61	89	B1	11	39	61	89
CS16	10	38	60	88	B0	10	38	60	88
CS15	0F	37	5F	87	AF	0F	37	5F	87
CS14	0E	36	5E	86	AE	0E	36	5E	86
CS13	0D	35	5D	85	AD	0D	35	5D	85
CS12	0C	34	5C	84	AC	0C	34	5C	84
CS11	0B	33	5B	83	AB	0B	33	5B	83
CS10	0A	32	5A	82	AA	0A	32	5A	82
CS9	09	31	59	81	A9	09	31	59	81
CS8	08	30	58	80	A8	08	30	58	80
CS7	07	2F	57	7F	A7	07	2F	57	7F
CS6	06	2E	56	7E	A6	06	2E	56	7E
CS5	05	2D	55	7D	A5	05	2D	55	7D
CS4	04	2C	54	7C	A4	04	2C	54	7C
CS3	03	2B	53	7B	A3	03	2B	53	7B
CS2	02	2A	52	7A	A2	02	2A	52	7A
CS1	01(hex)	29	51	79	A1	01	29	51	79
PAGE	PAGE0					PAGE1			

Figure 16 PWM Register

Table 6
Page 0: 01h ~ ECh PWM Register
Page 1: 01h ~ B1h PWM Register

Bit	D7:D0
Name	PWM
Default	0000 0000

Each dot has a byte to modulate the PWM duty in 256 steps, the page 0 stores the SW1-SW5, the page 1 stores the SW6-SW9.

The value of the PWM Registers decides the average current of each LED noted I_{LED}.

I_{LED} computed by Formula (1):

$$I_{LED} = \frac{PWM}{256} \times I_{OUT(PEAK)} \times Duty \quad (1)$$

$$PWM = \sum_{n=0}^{7} D[n] \cdot 2^n$$

Where Duty is the duty cycle of SWx, see SCANING TIMING section for more information.

$$Duty = \frac{113\mu s}{(113\mu s + 7.7\mu s + 0.02\mu s)} \times \frac{1}{9} = \frac{1}{9.61} \quad (2)$$

Where 113μs is t_{SCAN}, the period of scanning and 7.7μs is t_{NOL}, the non-overlap time and 0.02μs is the CSy delay.

I_{OUT} is the output current of CSy (y=1~40),

$$I_{OUT(PEAK)} = \frac{603}{R_{ISET}} \times \frac{GCC}{255} \quad (3)$$

GCC is the Global Current Control register (PG0, F1~F3h) value, R_{ISET} is the external resistor of ISET pin. D[n] stands for the individual bit value, 1 or 0, in location n.

For example: if D7:D0=1011 0101 (0xB5, 181), GCC=1111 1111, R_{ISET}=10kΩ:

$$I_{LED} = \frac{603}{10k\Omega} \times \frac{GCC}{255} \times Duty \times \frac{PWM}{256}$$

Table 7 Page 0 EFh Fault State Register

Bit	D7:D4	D3	D2	D1	D0
Name	-	OTF	OCF	LSF	LOF
Default	0000	0	0	0	0

Fault State Register stores over temperature/current flag and LED open flag. After 0/S bits of F9h register are enabled, if LED open is detected, the LOF bit will be set to 1.

LOF LED open flag
0 no open
1 open happens

LSF LED short flag
0 No short Flag
1 Short Flag happens

OCF Over current flag
0 No over current
1 Over current flag happens

OTF Over temperature flag
0 No over temperature
1 Over temperature happens

Table 8 Page 0 F0h Configuration Register

Bit	D7:D4	D3	D2	D1	D0
Name	SWS	RP	PWMM	DEGM	SSD
Default	0000	0	0	0	0

The Configuration Register sets operating mode of IS31FL3758.

When SSD is "0", IS31FL3758 works in software shutdown mode and to normally operate the SSD bit should set to "1". SWS controls the duty cycle of the SWx, default mode is 1/9.

SSD Software Shutdown Control
0 Software shutdown
1 Normal operation

RP Reset Register Write Lock
0 Reset Register(Page 1 FFh) cannot be written
1 Reset Register(Page 1 FFh) Writes normally

DEGM De-ghost mode
0 in non-overlap time
1 PWM off

PWMM PWM mode
0 6+2-bit mode
1 8-bit mode

SWS SWx Setting
0000 SW1~SW9, 1/9 (All SWx are active)
0001 SW1~SW8, 1/8, SW9 (Not active)
0010 SW1~SW7, 1/7, SW8~SW9 (Not active)
0011 SW1~SW6, 1/6, SW7~SW9 (Not active)
0100 SW1~SW5, 1/5, SW6~SW9 (Not active)
0101 SW1~SW4, 1/4, SW5~SW9 (Not active)
0110 SW1~SW3, 1/3, SW4~SW9 (Not active)
0111 SW1~SW2, 1/2, SW3~SW9 (Not active)
1000 NA, 47x1, SW1 is still scanning
1001 SW1~SW3~SW5~SW7
1010 SW1~SW3~SW5
1011 SW1~SW3
1100 48CH are all CS, no-scanning

Table 9 Page 0 F1h Global Current Control Register 1

Bit	D7:D0
Name	GCC for R Channels
Default	0000 0000

Table 10 Page 0 F2h Global Current Control Register 2

Bit	D7:D0
Name	GCC for G Channels
Default	0000 0000

Table 11 Page 0 F3h Global Current Control Register 3

Bit	D7:D0
Name	GCC for B Channels
Default	0000 0000

The Global Current Control Registers modulates all CSy (x=1~48) DC current which is noted as I_{OUT} in 256 steps.

F1h is for R channels, GCCR, CS1, CS4, CS7…CS46

F2h is for G channels, GCCG, CS2, CS5, CS8…CS47

F3h is for B channels, GCCB, CS3, CS6, CS9…CS48.

For SPI and I2C mode, I_{OUT} is computed by the Formula (3):

$$I_{OUT(PEAK)} = \frac{603}{R_{ISET}} \times \frac{GCC}{255} \qquad (3)$$

$$GCC = \sum_{n=0}^{7} D[n] \cdot 2^n$$

Where D[n] stands for the individual bit value, 1 or 0, in location n.

Table 12 Page 0 F5h Pull Up Voltage Selection Register

Bit	D7:D6	D5	D4	D3:D0
Name	PCS	DES	DEN	CSPUV
Default	00	0	0	1000

F5h sets the pull up voltage for CSy. When DEN bit is "1" De-ghost function is enabled and CSy pull up Voltage Selection can be configured by the CSPUV bits.

PCS	Pre-charge Select, pull
00	Disable
01	20ns
10	40ns
11	80ns

DES	De-ghost setting
0	Normal
1	Stronger Driver

DEN	De-ghost Enable
0	Disable
1	Enable

CSPUV	CSy Pull up Voltage Selection Bit
0000	no pull
0001	V_{CC}-3.2V
0010	V_{CC}-3.0V
0011	V_{CC}-2.8V
0100	V_{CC}-2.6V
0101	V_{CC}-2.4V
0110	V_{CC}-2.2V
0111	V_{CC}-2.0V
1000	V_{CC}-1.8V
1001	V_{CC}-1.6V
1010	V_{CC}-1.4V
1011	V_{CC}-1.2V
1100	V_{CC}-1.0V
1101	V_{CC}-0.8V
1110	V_{CC}-0.6V
1111	V_{CC}

Table 13 Page 0 F6h PFS/Phase Enable Register

Bit	D7	D6	D5:D4	D3	D2:D0
Name	PHC	-	OC_SEL	-	PFS
Default	0	0	00	0	100

F6h register set the PWM frequency and phase delay. IS31FL3758 has 2 groups of phase delays, group 1 is CS1, CS3, CS5... CS47, group 2 is CS2, CS4, CS6... CS48. After phase delay is enabled, the delay between the two groups will be 180°; otherwise, it will be 0°. Enabling phase delay helps minimize the power ripple. It is recommended to set the PHC bit in the initial stage. If the PHC value is adjusted during work, the output will be updated immediately, which may cause a brief change in LED brightness. See the application information section for more details.

OC_SEL needs to be set to 0x00 before another set to enable Over current test.

After setting OC_SEL, The D1 of EFh can be read to understand the current overcurrent status. OC_SEL needs to be set to 0x00 before another set to enable Over current test.

PFS control PWM frequency setting bits. For example, if PWM Mode is 6+2-bit and PFS = "010", that the PWM frequency is 66kHz and the scan frequency is 1/9 namely SWS = "0000" is 7.3kHz.

PHC	Phase choice
0	0 degree phase delay
1	180 degree phase delay

OC_SEL	Over current setting
0x	disable
10	90mA
11	120mA

PFS	PWM frequency setting
000	Not allowed
001	260kHz for 6+2-bit mode 70kHz for 8-bit mode
010	66kHz for 6+2-bit mode 17.6kHz for 8-bit mode
011	16.6kHz for 6+2-bit mode 4.4kHz for 8-bit mode
100 (default)	8.3kHz for 6+2-bit mode 2.2kHz for 8-bit mode
101	4.1kHz for 6+2-bit mode 1.1kHz for 8-bit mode
110	2.1kHz for 6+2-bit mode (not allowed, when PWM=0x01, it is only 40+Hz) 0.55kHz for 8-bit mode (not allowed when n>4)
111	1kHz for 6+2-bit mode (not allowed, when PWM=0x01, it is only 20+Hz) 0.275 kHz for 8-bit mode (not allowed when n>2)

Table 14 Page 0 F7h Spread Spectrum Register

Bit	D7	D6	D5	D4
Name	EN_INC PRS	-	OSC_EN	SSP_EN
Default	1	0	1	0
Bit	**D3:D2**		**D1:D0**	
Name	-		SSP_RNG	
Default	00		00	

When SSP_EN bit is written as 1, the spread spectrum function will be enabled and the RNG bits will adjust the range of spread spectrum function.

SSP_EN	Spread spectrum function enable
0	Disable
1	Enable

SSP_RNG	Spread spectrum range
00	±5%
01	±15%
10	±20%
11	Not allowed

OSC_EN	OCS enable
0	Disable
1	Enable (Default)

EN_INC PRS	Enable increase current precision
0	no increase current precision when (CS <1V)
1	Yes

Table 15 Page 0 F8h De-ghost Timing Select Register

Bit	D7:D4	D3:D2	D1:D0
Name	-	DEG-Vref T	DEGT
Default	0000	00	00

F8h register sets the De-ghost timing.

DEG-Vref T	De-ghost -Time select
00	3/4 SW Time
01	1/2 SW Time
10	3/4 SW Time
11	SWx end position pull up

DEG-T	De-ghost -Time select
00	4CLK-256ns @ 16MHz
01	2CLK
10	8CLK
11	16CLK

Table 16 Page 0 F9h Open/Short Enable Register

Bit	D7:D6	D5:D4	D3:D0
Name	O/S	-	OS of SW
Default	00	00	0000

F9h enables/disables open/short detect information which can be detected by selecting the corresponding SW1~9.

When O/S is “01” or “10”, the Open short detect enable. If O/S is “01”, Open detect enable and if O/S is “10”, Short detect enable, and the result stored in FAh~FFh.

O/S	Select open or short
00	Disable
01	Open
10	Short
11	Scan, report to EFh flag only

OS of SW	Select which SW to detect
0001	SW1
0002	SW2
…	
1001	SW9

Note 8: It should be noted that it will not store both open/short detect information at the same time, either it will store open, or it will store short information. Open/short information can be read by the FAh~FFh registers.

Table17 Page 0 FAh Open Short Register 1

Bit	D7:D0
Name	CS08:CS01
Default	0000 0000

Table 18 Page 0 FBh Open Short Register 2

Bit	D7:D0
Name	CS16:CS09
Default	0000 0000

Table 19 Page 0 FCh Open Short Register 3

Bit	D7:D0
Name	CS24:CS17
Default	0000 0000

Table 20 Page 0 FDh Open Short Register 4

Bit	D7:D0
Name	CS32:CS25
Default	0000 0000

Table 21 Page 0 FEh Open Short Register 5

Bit	D7:D0
Name	CS40:CS33
Default	0000 0000

Table 22 Page 0 FFh Open Short Register 6

Bit	D7:D0
Name	CS48:CS41
Default	0000 0000

After setting F9h, FA~FFh can be read for the open or short information of each LED string. F9h needs to be set to 0x00 before another set to enable open or short test.

Page 1 FFh Reset Register

To perform a reset operation, it is necessary to unlock the register before writing to the Reset Register (FFh) to avoid incorrect operations on this register. When the RP bit of the Configuration Register(Page 0 F0h) is set to 1, writing to the Reset Register (FFh) is allowed. Once user writes the Reset Register with 0x00, IS31FL3758 will reset all the IS31FL3758 registers to their default value. On initial power-up, the IS31FL3758 registers are reset to their default values for a blank display.

Reset Register does not Reset Command Register(E7h), that is, Command Register(E7h) remains the original value (0x01) after Reset Register is written. The user can write it manually.

TYPICAL APPLICATION INFORMATION

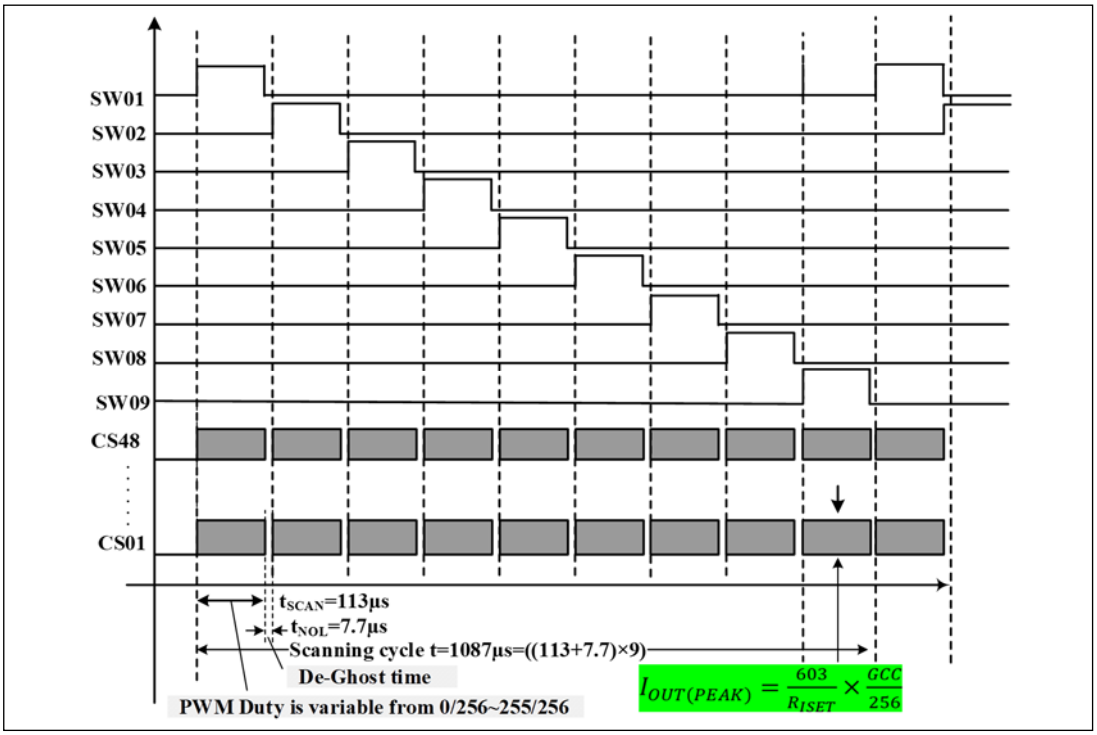


Figure 17 Scanning Timing

GENERAL DISCRIPTION

IS31FL3758 is a 48-channel LED driver with 48 constant current channels. It also supports from one to eight power scan to become a 48ch, 47×1, 46×2, 45×3…40×8, 40×9 matrix LED driver by control 9~2 external power PMOS.

SCANING TIME

The SW1~SW9 is turned on by serial as shown in figure 17, LED is driven 9 by 9 within the SWx (x=1~9) on time SWx, x=1~9 is source and it is high when LED on), including the non-overlap blanking time during scan, the duty cycle of SWx (active high, x=1~9) is:

$$Duty = \frac{113\mu s}{(113\mu s+7.7\mu s+0.02\mu s)} \times \frac{1}{9} = \frac{1}{9.61} \qquad (2)$$

Where 113μs is t_{SCAN}, the period of scanning and 7.7μs is t_{NOL}, the non-overlap time and 0.02μs is the CSy delay.

And the scan frequency is 1/n of PWM frequency, where n is SW scan number that can be choose by SWS of Page 0 F0h register and the number of select range as 1, 2, 3 … 9. For example, when n = 9, namely SWS = 0001, and the PWM frequency is 137kHz, the scan frequency is 1/9 of PWM frequency is 15.2kHz; or when n = 8, the scan frequency is 1/8 of PWM frequency is 17.1kHz…

PWM CONTROL

After setting the I_{OUT} and GCC, the brightness of each LEDs (LED average current (I_{LED})) can be modulated with 256 steps by PWM Register, as described in equation (1).

$$I_{LED} = \frac{PWM}{256} \times I_{OUT(PEAK)} \times Duty \quad (1)$$

GCC is the Global Current Control register (PG0, F1~F3h) value, R_{ISET} is the external resistor of ISET pin. D[n] stands for the individual bit value, 1 or 0, in location n.

For example: if D7:D0=1011 0101 (0xB5, 181), GCC=1111 1111, R_{ISET}=10kΩ:

$$I_{LED} = \frac{603}{10k\Omega} \times \frac{GCC}{255} \times Duty \times \frac{PWM}{256}$$

Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve a breathing effect

GAMMA CORRECTION

In order to perform a better visual LED breathing effect, we recommend using a gamma corrected PWM value to set the LED intensity. This results in a reduced number of steps for the LED intensity setting but causes the change in intensity to appear more linear to the human eye.

Gamma correction, also known as gamma compression or encoding, is used to encode linear luminance to match the non-linear characteristics of display. Since the IS31FL3758 can modulate the brightness of the LEDs with 256 steps, a gamma correction function can be applied when computing

each subsequent LED intensity setting such that the change in brightness matches the human eye's brightness curve.

Table 14 32 Gamma Steps with 256 PWM Steps

C(0)	C(1)	C(2)	C(3)	C(4)	C(5)	C(6)	C(7)
0	1	2	4	6	10	13	18
C(8)	C(9)	C(10)	C(11)	C(12)	C(13)	C(14)	C(15)
22	28	33	39	46	53	61	69
C(16)	C(17)	C(18)	C(19)	C(20)	C(21)	C(22)	C(23)
78	86	96	106	116	126	138	149
C(24)	C(25)	C(26)	C(27)	C(28)	C(29)	C(30)	C(31)
161	173	186	199	212	226	240	255

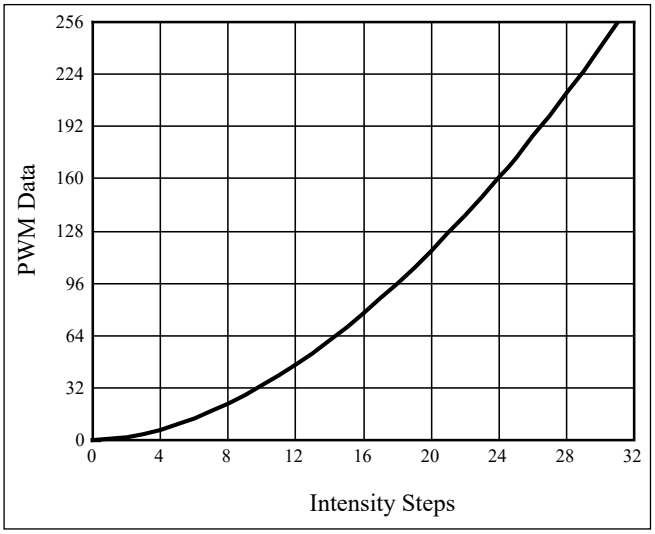


Figure 18 Gamma Correction (32 Steps)

Choosing more gamma steps provides for a more continuous looking breathing effect. This is useful for very long breathing cycles. The recommended configuration is defined by the breath cycle T. When T=1s, choose 32 gamma steps, when T=2s, choose 64 gamma steps. The user must decide the final number of gamma steps not only by the LED itself, but also based on the visual performance of the finished product.

Table 15 64 Gamma Steps with 256 PWM Steps

C(0)	C(1)	C(2)	C(3)	C(4)	C(5)	C(6)	C(7)
0	1	2	3	4	5	6	7
C(8)	C(9)	C(10)	C(11)	C(12)	C(13)	C(14)	C(15)
8	10	12	14	16	18	20	22
C(16)	C(17)	C(18)	C(19)	C(20)	C(21)	C(22)	C(23)
24	26	29	32	35	38	41	44
C(24)	C(25)	C(26)	C(27)	C(28)	C(29)	C(30)	C(31)
47	50	53	57	61	65	69	73
C(32)	C(33)	C(34)	C(35)	C(36)	C(37)	C(38)	C(39)
77	81	85	89	94	99	104	109
C(40)	C(41)	C(42)	C(43)	C(44)	C(45)	C(46)	C(47)
114	119	124	129	134	140	146	152
C(48)	C(49)	C(50)	C(51)	C(52)	C(53)	C(54)	C(55)
158	164	170	176	182	188	195	202
C(56)	C(57)	C(58)	C(59)	C(60)	C(61)	C(62)	C(63)
209	216	223	230	237	244	251	255

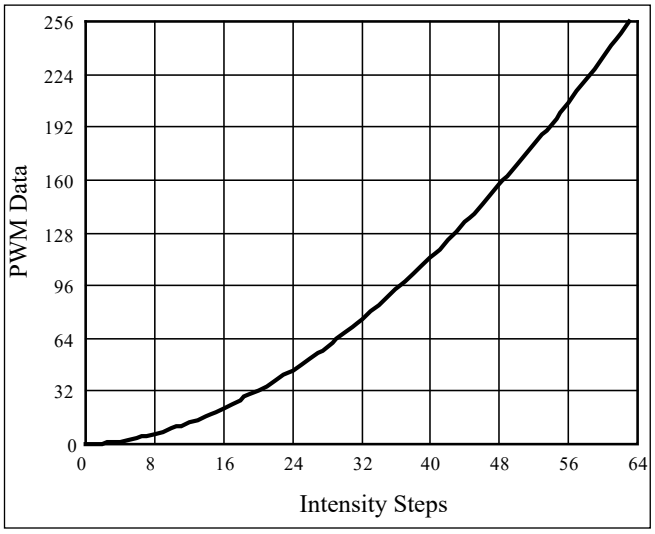


Figure 19 Gamma Correction (64 Steps)

Note 9: The data of 32 gamma steps is the standard value and the data of 64 gamma steps is the recommended value.

OPERATING MODE

IS31FL3758 can only operate in PWM Mode. The brightness of each LED can be modulated with 256 steps by PWM registers. For example, if the data in PWM Register is “0000 0100”, then the PWM is the fourth step. Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve a breathing effect.

6+2-BIT PWM MODE

When PWMM of the Control Register (F0h) is “0”, 6+2-bit PWM Mode is enabled. Then the final output PWM frequency is 6-bit, resolution is 8-bit. This is achieved through 6-bit PWM modulation and 2-bit dither control. For 2-bit dither, according to the 4-dither timing, each of the 4 PWM groups can add one PWM_H or no PWM_H.

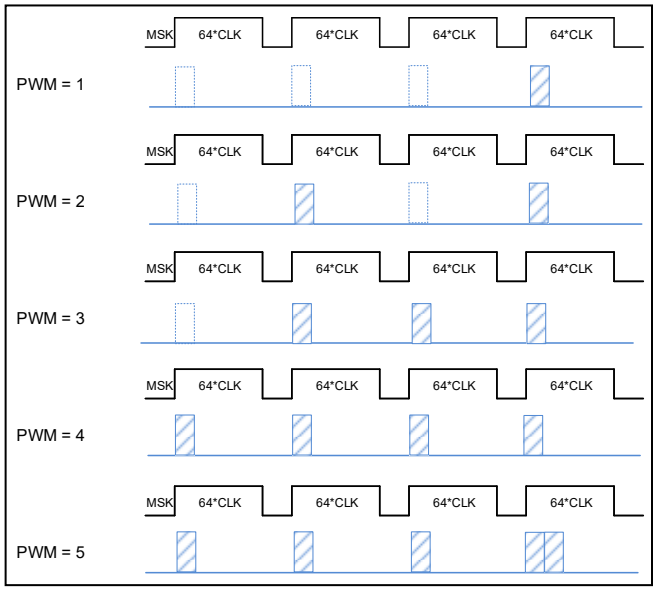


Figure 20 PWMM= "0", 6+2-bit PWM Mode Enable

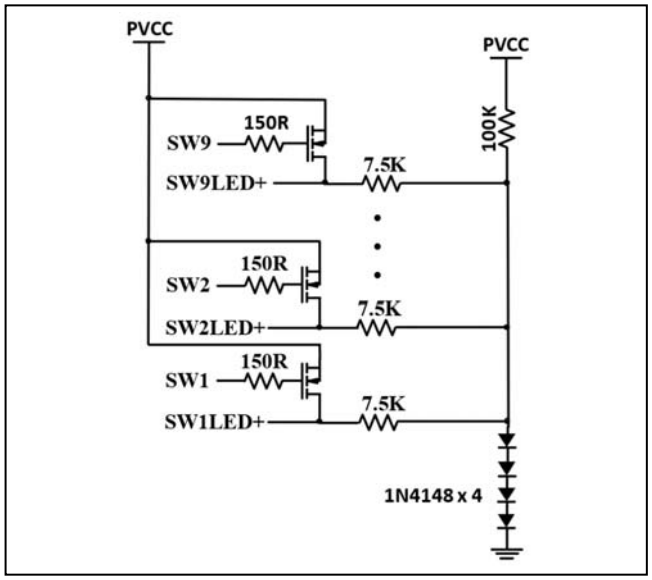


Figure 21 External Circuit to Remove De-ghost

OPEN SHORT DETECT FUNCTION

IS31FL3758 has an open and short detect bit for each LED. The open status register stores the open information of LED string. F9h needs to be set to 0x00 before another set to enable open or short test.

To get the correct open information, several configurations are recommended to set before setting the O/S bit (D3:D0 of F9h):

1. GCCx=0x10, too low or too high GCCx, like GCCx=0x01, may read out incorrect open information.

2. PWM>0x7F, too low PWM, like PWM=0x01, may read out incorrect open information.

DE-GHOST FUNCTION

The "ghost" term is used to describe the behavior of an LED that should be OFF but instead glows dimly when another LED is turned ON. A ghosting effect typically can occur when multiplexing LEDs. In matrix architecture any parasitic capacitance found in the constant-current outputs or the PCB traces to the LEDs may provide sufficient current to dimly light an LED to create a ghosting effect.

The ghost can be completely eliminated by adjusting the pull voltage of CS and combining it with the external SW drop-down. Typically, selecting the 7.5kΩ will be sufficient to eliminate the LED ghost phenomenon.

Note 10: To solve the ghosting issue, precise fine-tuning of the CS (Common Source) node's pull voltage, alongside the integration of an external SW (switch) pull-down circuit, is of utmost importance. Selecting a 7.5kΩ resistor at the default operational frequency represents a judicious choice, effectively nullifying the occurrence of LED ghosting while preserving the LED's negative voltage within the desired range. It is noteworthy that the four 1N4148 Schottky barrier diodes exhibit a forward voltage drop of approximately 2.2V. To optimize performance, it is prudent to substitute these diodes with Zener Diode featuring voltage characteristics similar to those depicted in Figure 21.

Furthermore, the introduction of resistance between the SW output and the PMOS G (Gate) electrode serves a critical purpose. This resistance mitigates voltage spikes resulting from parasitic inductance, a common consequence when the SW switch undergoes rapid activation. This precautionary measure strengthens system stability and reliability, ensuring seamless operation in demanding scenarios.

6-GROUPS DELAY FUNCTION

IS31FL3758 configuration involves the establishment of 6 distinct groups delay, each comprising eight channels. Specifically, channels CS1 through CS8 are allocated to Group 1, channels CS9 through CS16 to Group 2, channels CS17 through CS24 to Group 3, channels CS24 through CS32 to Group 4, channels CS33 through CS40 to Group 5 and channels CS41 through CS48 to Group 6. To mitigate the power ripple that may arise from concurrently activating numerous channels, a deliberate delay of one clock cycle is introduced between these groups. In 6+2Bit mode, the delay of each channel in the same group is 4nS, and the delay between groups is 2ns. In 8 Bit mode, the delay of each channel in the same group is 4nS. delay between groups 0.5 CLK, When PWMF is set to 2kHz(default), the delay time is 0.5/2k/256 ≈ 976ns. This temporal partition into groups, coupled with the adjusted delay, serves as an effective strategy to ameliorate power fluctuations associated with the simultaneous activation of multiple channels within the IS31FL3758 configuration. This delay might seem extremely short, almost like a quick blink of an eye, but it serves an important purpose. It helps to spread power consumption over time, reducing the chances of sudden, large spikes in power usage. This, in turn, helps maintain a more stable and consistent power supply, which can be crucial in various applications where precise control of lighting or display elements is necessary.

INTERFACE RESET

The SPI/I2C will be reset if the SDB pin is pull-high from 0V to logic high, at the operating SDB rising edge.

SHUTDOWN MODE

Shutdown mode can be used as a means of reducing power consumption. During shutdown mode all registers retain their data.

Software Shutdown

By setting SSD bit of the Configuration Register (PG0, F0h) to "0", the IS31FL3758 will operate in software shutdown mode. When the IS31FL3758 is in software shutdown, all current sources are switched off, so that the matrix is blanked. All registers can be operated. Typical current consumption is 0.5μA.

Hardware Shutdown

The chip enters hardware shutdown when the SDB pin is pulled low. All analog circuits are disabled during hardware shutdown, typical the current consume is 0.5μA.

The chip releases hardware shutdown when the SDB pin is pulled high.

If VCC has a risk drop below 1.75V but above 0.1V during SDB pulled low, please re-initialize all Function Registers before SDB pulled high.

LAYOUT

As described in external resistor (R_{ISET}), the chip consumes lots of power. Please consider below factors when layout the PCB.

1. The V_{CC} (PVCC) capacitors need to be close to the chip and the ground side should be well connected to the GND of the chip.

2. R_{ISET} should be close to the chip and the ground side should connect well to the GND of the chip.

3. The thermal pad should connect to ground pins and the PCB should have the thermal pad too, usually this pad should have 16 or 25 via through the PCB to other side's ground area to help radiate the heat. About the thermal pad size, please refer to the land pattern of each package.

4. The CSy pins maximum current is 60mA (R_{ISET}=10kΩ).

Thermal Consideration

The over temperature of the chip may result in deterioration of the properties of the chip. IS31FL3758 has a thermal pad but the chip could be very hot if the power is very large. So do consider the ground area connects to the GND pins and thermal pad. Other traces should keep away and ensure the ground area below the package is integrated, and the back layer should be connected to the thermal pad thru 9 or 16 vias to be maximized the area size of ground plane.

The package thermal resistance, θ_{JA}, determines the amount of heat that can pass from the silicon die to the surrounding ambient environment. The θ_{JA} is a measure of the temperature rise created by power dissipation and is usually measured in degree Celsius per watt (°C/W).

When operating the chip at high ambient temperatures, or when driving maximum load current, care must be taken to avoid exceeding the package power dissipation limits. The maximum power dissipation can be calculated using the following Formula (6):

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}} \quad (6)$$

So,

$$P_{D(MAX)} = \frac{125°C - 25°C}{32.6°C/W} \approx 3.07W$$

Figure 22 shows the power derating of the IS31FL3758 on a JEDEC boards (in accordance with JESD 51-5 and JESD 51-7) standing in still air.

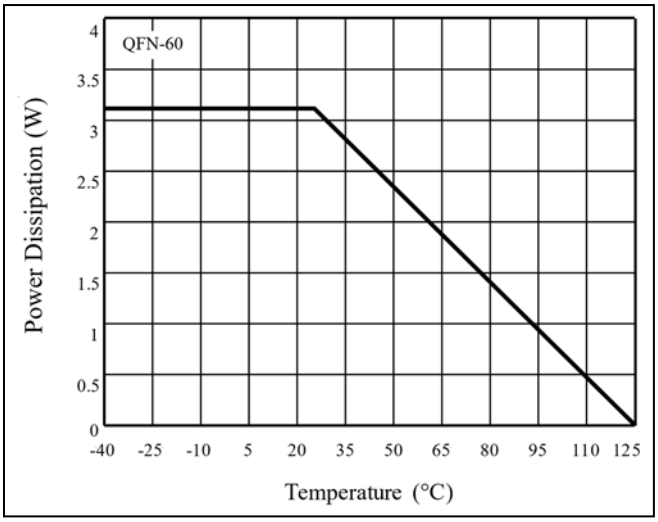


Figure 22 Dissipation Curve

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

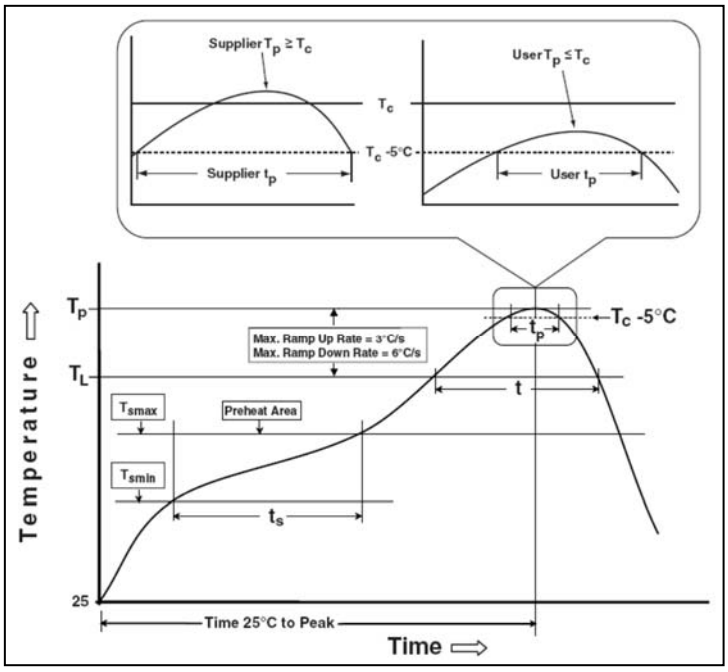
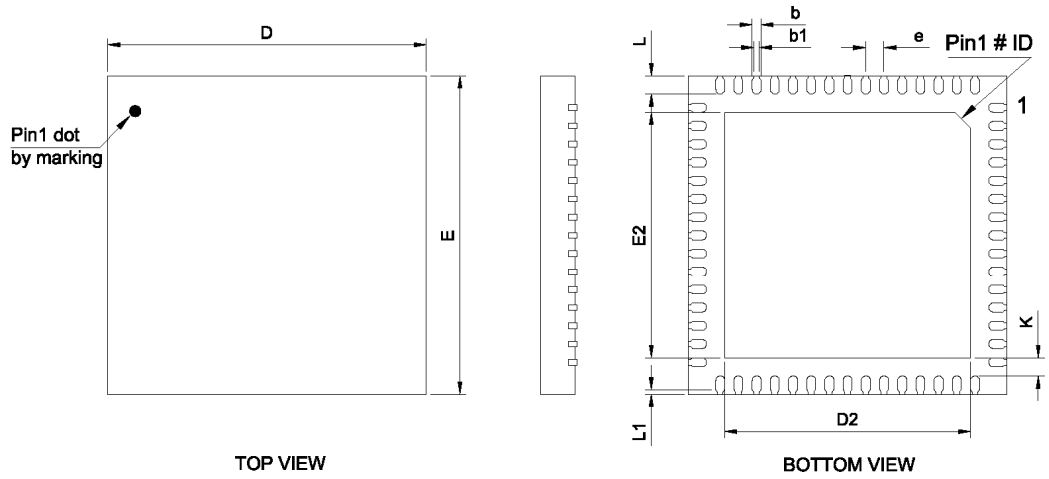


Figure 23 Classification Profile

PACKAGE INFORMATION

QFN-60



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20REF	
b1		0.125REF	
b	0.15	0.20	0.25
D	6.90	7.00	7.10
E	6.90	7.00	7.10
D2	4.95	-	5.55
E2	4.95	-	5.55
L	0.30	0.40	0.50
L1		0.10REF	
e		0.40BSC	
K	0.20	-	-

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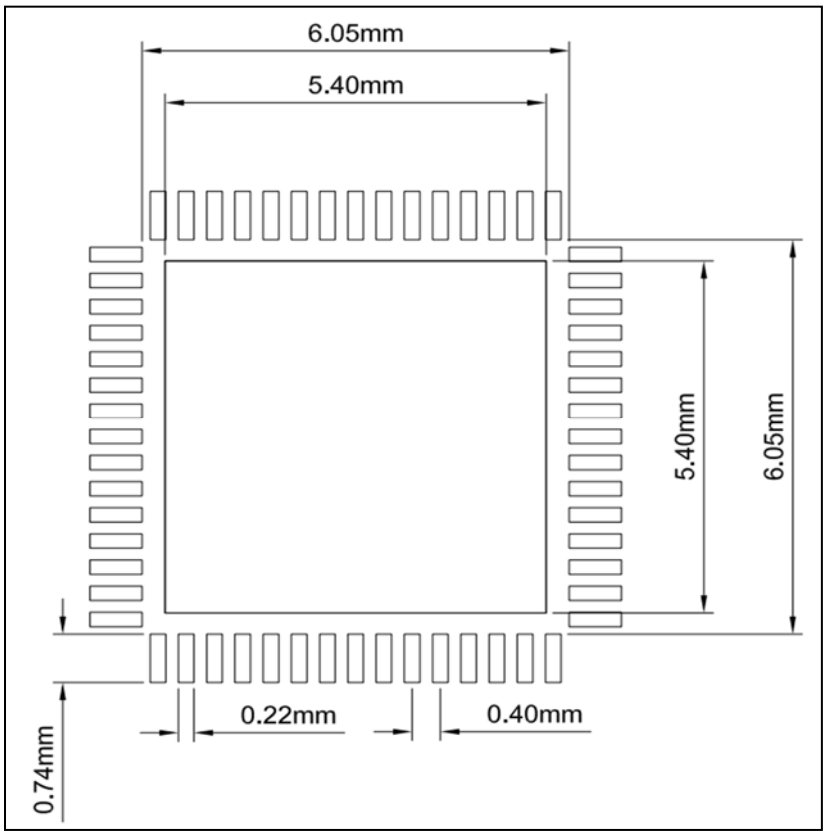
NOTE:
1. CONTROLLING DIMENSION : MM
2. REFERENCE DOCUMENT: JEDEC MO-220
3. THE PIN'S SHARP AND THERMAL PAD SHOWS DIFFERENT SHAPE AMONG DIFFERENT FACTORIES.

RECOMMENDED LAND PATTERN

QFN-60



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. User's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
0A	Initial Release	2023.10.10
0B	1. Modify EC table data and information. 2. Modify the Figure 3 Typical Application Circuit-SPI, 9SW×39CS (Need To Work With PMOS), add De-ghost circuit. 3. FEATURES update.	2023.11.10
0C	1. Modify EC table data and information. 2. Modify SRS to PFS (PWM frequency select) and change scan frequency to PWM frequency. 3. Increase SW scan frequencies introduce and calculate method in scan timing of APPLICATION INFORMATION.	2024.04.15
A	1. Added frequency gear support for PFS=001. 2. Added Reset Register Write Lock bit(RP). 3. Modify EC table data. 4. Application circuit DIAGRAM, Pin Configuration, BLOCK DIAGRAM to optimize the pin order. 5. Release to Mass-Production.	2025.03.25