IS31FL3748A

24 × 4 DOTS MATRIX LED DRIVER

July 2021

GENERAL DESCRIPTION

IS31FL3748A is a matrix LED driver with 24 high voltage (28V) constant current channels. It supports from one to four power scan to become a 24×n (n=1~4) matrix LED driver. Each channel can be pulse width modulated (PWM) with 8-bit precision for smooth LED brightness control. In addition, each channel can be controlled by an 8-bit output current control register (Dot correction, current scale, SL), which allows fine tuning the current for rich RGB color mixing, e.g., a pure white color LED application. The maximum output current of each channel is designed to be 40mA, which can be adjusted by three 8-bit global control registers (one group for R for channels 3×I, one group for G for channels 3×I+1, and one group for B for channels 3×I+2, where I= 0 to 7). Proprietary algorithms are used in IS31FL3748A to minimize power bus noise caused by passive components on the power bus such as MLCC decoupling capacitor. All registers can be programmed via I2C (1MHz) interface.

IS31FL3748A can be turned off with minimum current consumption by either pulling the SDB pin low or by using the software shutdown feature. It internally generates 4.8V V_{OUT} to power the internal logic operation, which can also be external powered from 3V to 5.5V.

IS31FL3748A is available in QFN-48 (6mm×6mm) package and can work over temperature range from -40°C to +125°C.

FEATURES

- Support 24 constant current channels
- 4 PMOS high side switches
- Tolerate up to 30V, nominal operation voltage between 4.5V to 28V
- Optional built-in LDO to generate 4.8V supply for internal logic
- 1MHz I2C Interface
- SDB pin rising edge reset the interface
- Built-in PWM generator: 8-bit/dot
- Built-in Dot correction, current scale, SL: 8-bit/dot
- 8-bit × 3 global current adjustment
- Power noise reduction method
  - 4 groups delay to minimize the power ripple
  - Channel to channel timing skew (one sys-clock skew to reduce transient noise)
- Spread spectrum
- LED open detection and fault reporting
- Over temperature protection, over voltage protection, under voltage protection
- Operating temperature: -40°C to 125°C
- QFN-48 (6mm×6mm) package

APPLICATIONS

- White good display panel
- Pachinko
- Gaming machine

TYPICAL APPLICATION CIRCUIT

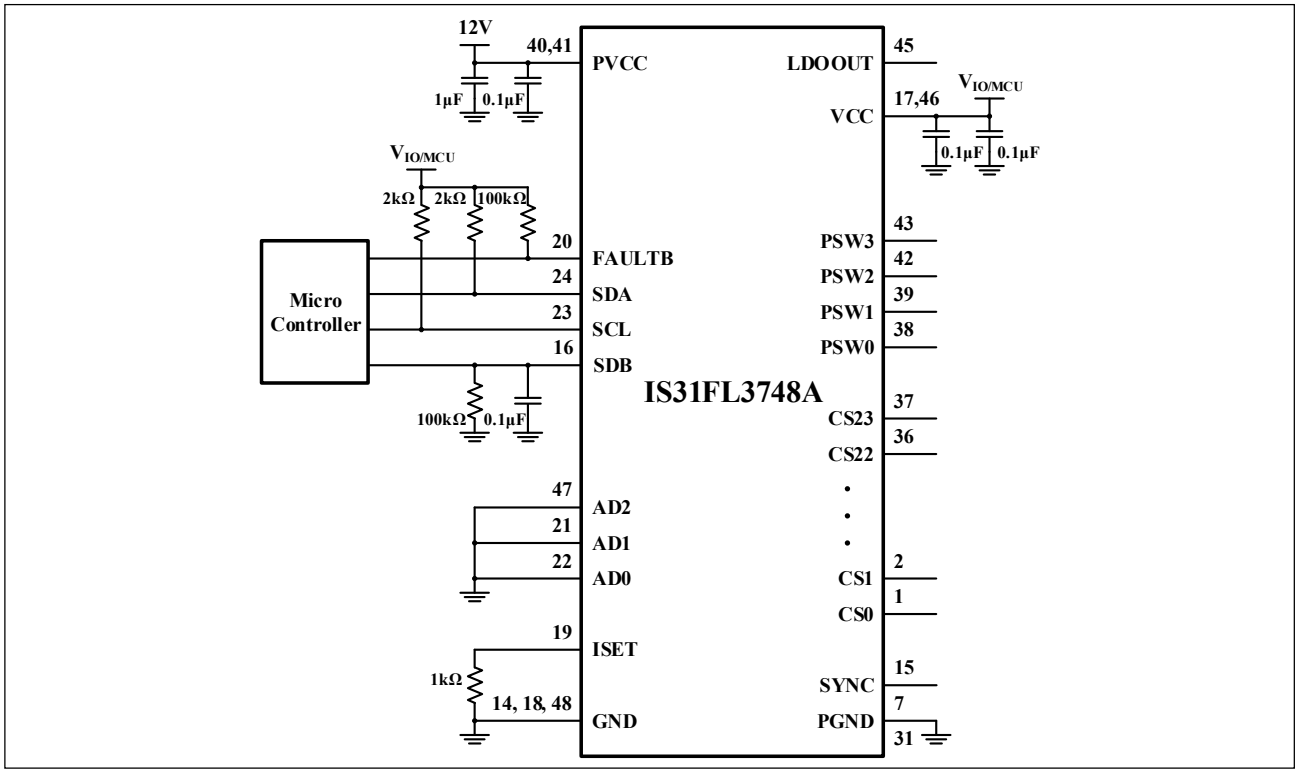


Figure 1 Typical Application Circuit

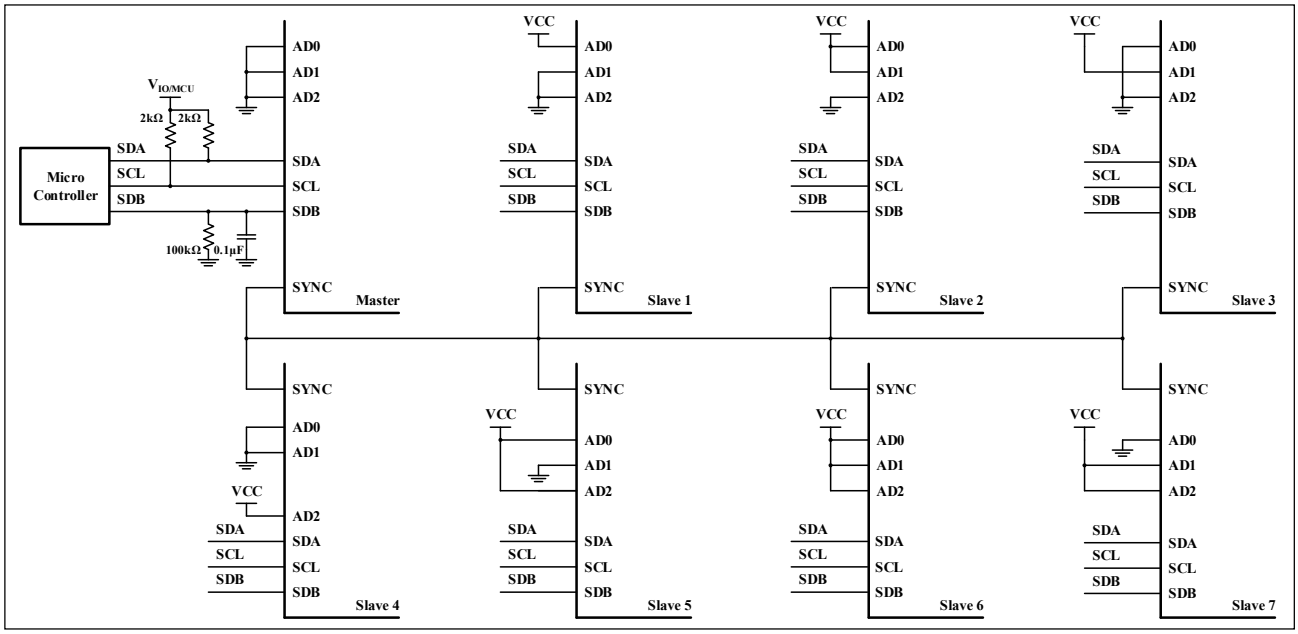


Figure 2 Typical Application Circuit: More Than One Slave in System

TYPICAL APPLICATION CIRCUIT (CONTINUED)

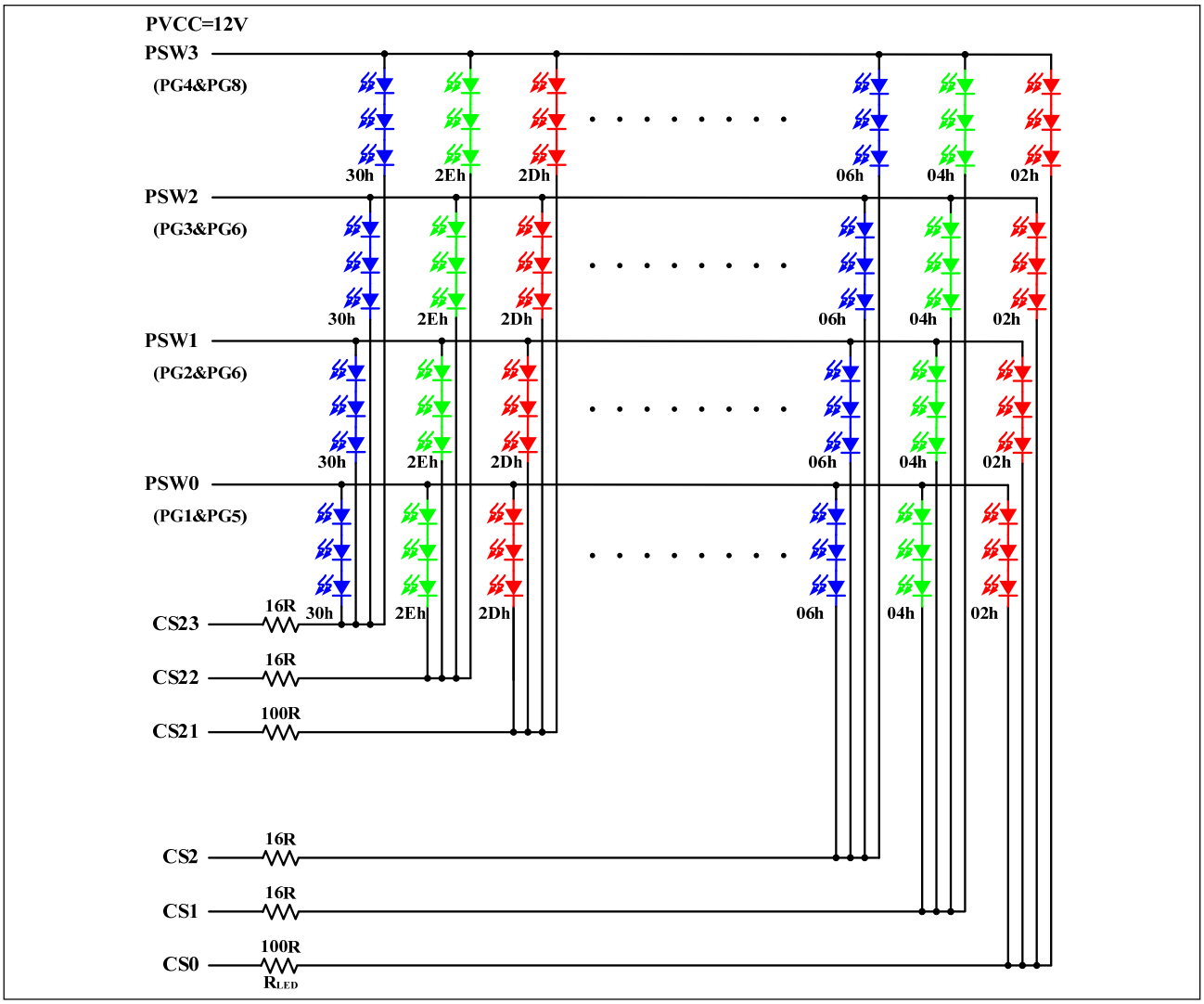


Figure 3 LED Circuit: 24×4

TYPICAL APPLICATION CIRCUIT (CONTINUED)

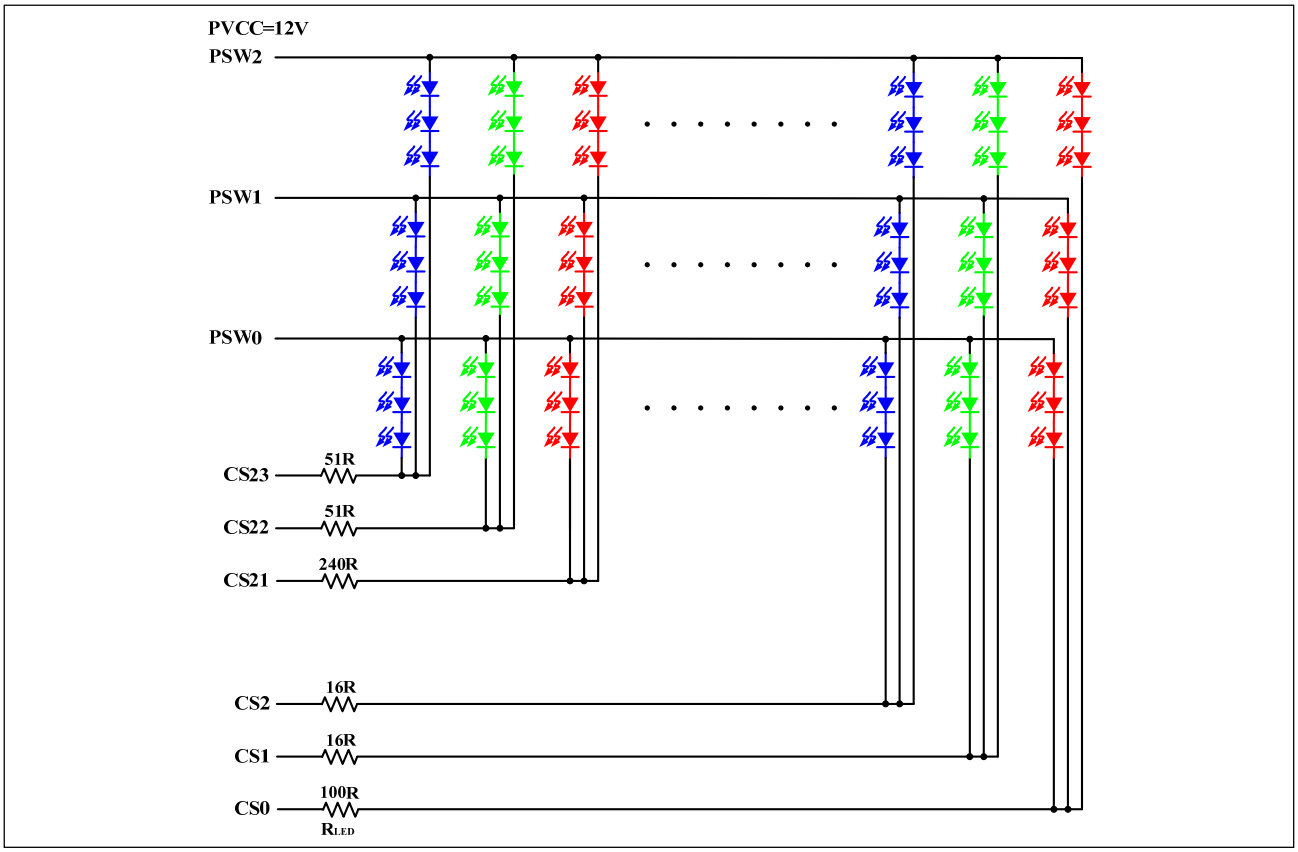


Figure 4 LED Circuit: 24×3

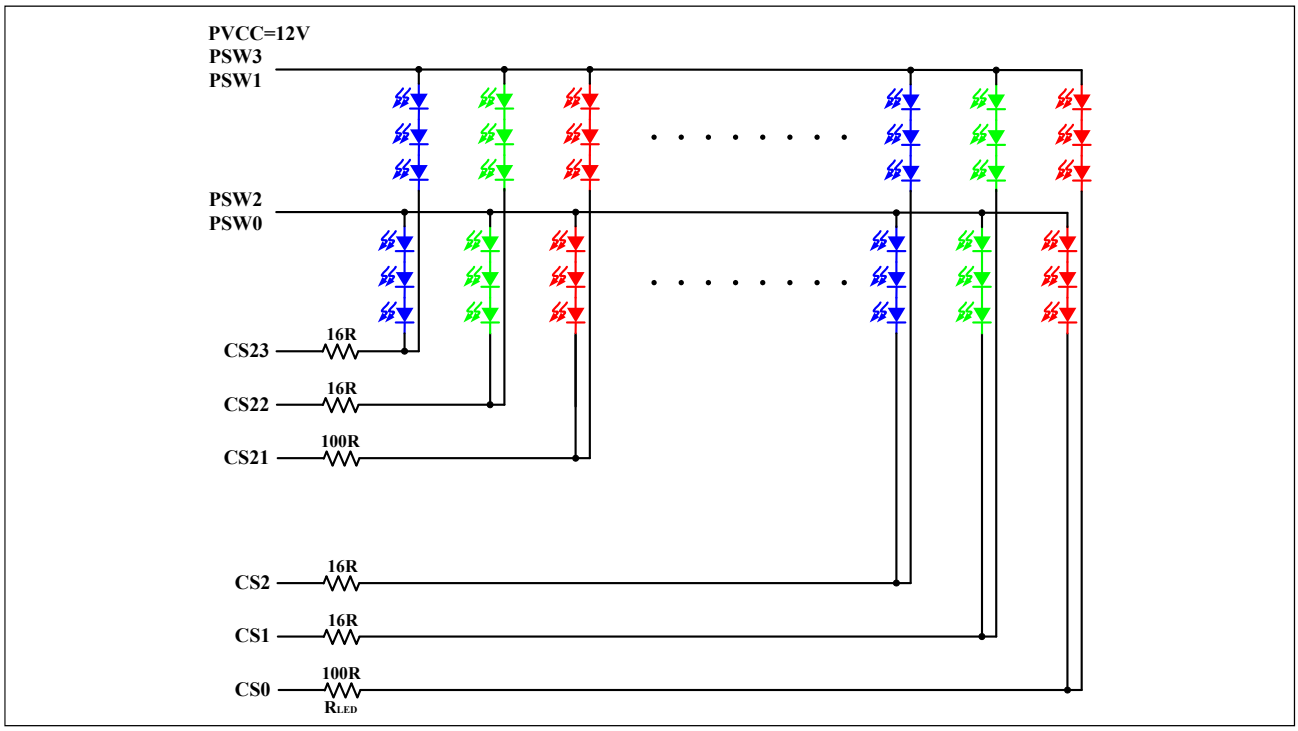
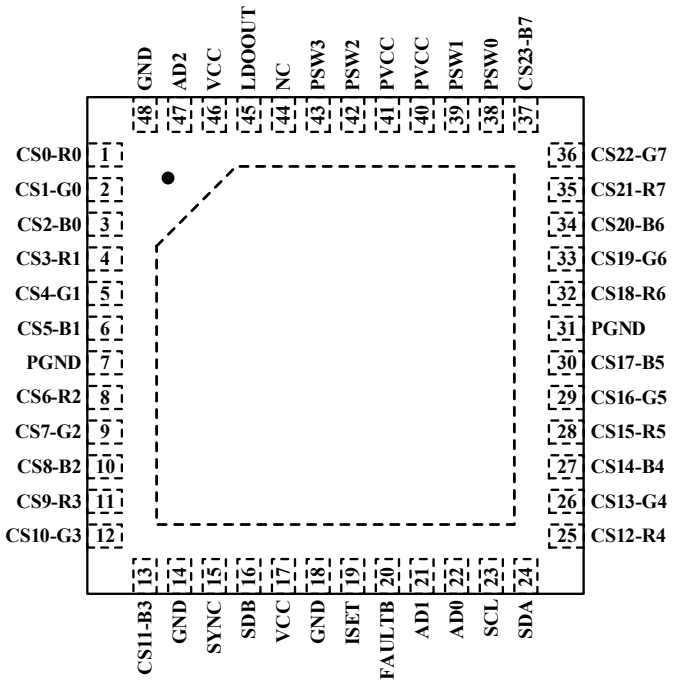


Figure 5 LED Circuit: 24×2

PIN CONFIGURATION

Package	Pin Configuration (Top View)
QFN-48	

PIN DESCRIPTION

No.	Pin	Description
1~6,8~13, 25~30,32~37	CS[23:0]	Current sink pin for LED matrix.
7,31	PGND	Power GND.
14,18, 48	GND	Analog GND.
15	SYNC	Synchronization.
16	SDB	Shutdown pin.
17,46	VCC	Analog and digital circuits.
19	ISET	Set the maximum IOUT current.
20	FAULTB	Fault report pin.
21	AD1	Address select pin.
22	AD0	Address select pin.
23	SCL	Bus serial clock
24	SDA	Bus serial data
38,39,42,43	PSW[3:0]	Power SW.
40, 41	PVCC	Power for current source PSWx.
44	NC	Not connect.
45	LDOOUT	LDO output, 4.8V typical.
47	AD2	Address select pin.
	Thermal Pad	Connect to GND.

ORDERING INFORMATION

Industrial Range: -40°C to +125°C

Order Part No.	Package	QTY/Reel
IS31FL3748A-QFLS4-TR	QFN-48, Lead-free	2500

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	-0.3V ~ +6.0V
Supply voltage, PV_{CC}	-0.3V ~ +30V
Voltage at CSx pin	-0.3V ~ +30V
Voltage at any input pin	-0.3V ~ PV_{CC}+0.3V
Maximum junction temperature, T_{JMAX}	+150°C
Storage temperature range, T_{STG}	-65°C ~+150°C
Operating temperature range, T_A=T_J	-40°C ~ +125°C
Package thermal resistance, junction to ambient (4 layer standard test PCB based on JESD 51-2A), θ_{JA}	37.3°C/W
ESD (HBM) ESD (CDM)	±7kV ±750V

Note 1: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

The following specifications apply for PV_{CC}= 12V, V_{CC}= 5V, T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
PV_{CC}	Power supply voltage		4.5		28	V
V_{CC}	Supply voltage		3.0		5.5	V
$I_{CC}(PV_{CC})$	Quiescent power supply current	R_{ISET} =1.0kΩ, V_{SDB}=V_{CC}=5V, all LEDs off		2.2	3	mA
$I_{CC}(V_{CC})$		R_{ISET} =1.0kΩ, V_{SDB}=V_{CC}=5V, all LEDs off		11.6	15	mA
$I_{SD}(PV_{CC})$	Shutdown current	V_{SDB}=0V		10	12	μA
$I_{SD}(V_{CC})$				0.8	1.4	
$I_{SD}(PV_{CC})$		V_{SDB}=V_{CC}=5V, Configuration Register written "0000 0000"		2.6	3.5	mA
$I_{SD}(V_{CC})$				7.2	10	
I_{OUT}	Maximum constant current of CSx	R_{ISET}=1kΩ, GCCR= GCCG= GCCB= 0xFE	37	39.6	43	mA
ΔI_{MAT}	Output current error between outputs (Note 2)	R_{ISET}=1kΩ, GCCR= GCCG= GCCB= 0xFE	-5		5	%
ΔI_{ACC}	Output current error between devices (Note 3)	R_{ISET}=1kΩ, GCCR= GCCG= GCCB= 0xFE	-8		8	%
V_{HR}	Current switch headroom voltage PSWx	R_{ISET}= 1kΩ, I_{SWITCH}= 800mA		700	1100	mV
	Current sink headroom voltage CSx	R_{ISET}= 1kΩ, I_{SINK}= 40mA		350	550	
t_{SCAN}	Period of scanning 1		27	31	35	μs
t_{NOL1}	Non-overlap blanking time during scan, the PSWx and CSy are all off during this time			0.75		μs
t_{NOL2}	Delay total time for CS1 to CS 24, during this time, the PSWx is on but CSx is not all turned on	(Note 4)		0.375		μs

ELECTRICAL CHARACTERISTICS (CONTINUED)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Logic Electrical Characteristics (DATA/DIN/MOSI, CLK/DOUT/MISO, CS, MODE[1:0], AD[2:0])						
V_{IL}	Logic "0" input voltage (not include SDB pin)	V_{CC}= 3.0V			0.3V_{CC}	V
V_{IH}	Logic "1" input voltage (not include SDB pin)	V_{CC}= 5.5V	0.7V_{CC}			V
V_{HYS}	Input Schmitt trigger hysteresis (not include SDB pin)	V_{CC}= 3.6V		0.2		V
V_{AD}	Input for AD[2:0], AD= VCC	V_{CC}= 3.0V~5.5V	V_{CC}-0.3		V_{CC}	V
	Input for AD[2:0], AD= Open	V_{CC}= 3.0V~5.5V	GND+1.6		V_{CC}-0.6	V
	Input for AD[2:0], AD= ISET	V_{CC}= 3.0V~5.5V	ISET-0.3		ISET+0.3	V
	Input for AD[2:0], AD= GND	V_{CC}= 3.0V~5.5V	GND		GND+0.3	V
V_{IL_SDB}	Logic "0" input voltage	V_{CC}= 3.0V			0.6	V
V_{IH_SDB}	Logic "1" input voltage	V_{CC}= 5.5V	2			V
V_{HYS_SDB}	Input schmitt trigger hysteresis	V_{CC}= 3.6V		0.2		V
I_{IL}	Logic "0" input current	V_{INPUT}= L (Note 4)		5		nA
I_{IH}	Logic "1" input current	V_{INPUT}= H (Note 4)		5		nA

Note 2: I_{OUT} mismatch (bit to bit) $\triangle I_{MAT}$ is calculated:

$$\Delta I_{MAT} = \pm \left(\frac{I_{OUT(MAX)} - I_{OUT(MIN)}}{\left(\frac{I_{OUT0} + I_{OUT1} + ... + I_{OUT23}}{24} \right) \times 2} - 1 \right) \times 100\%$$

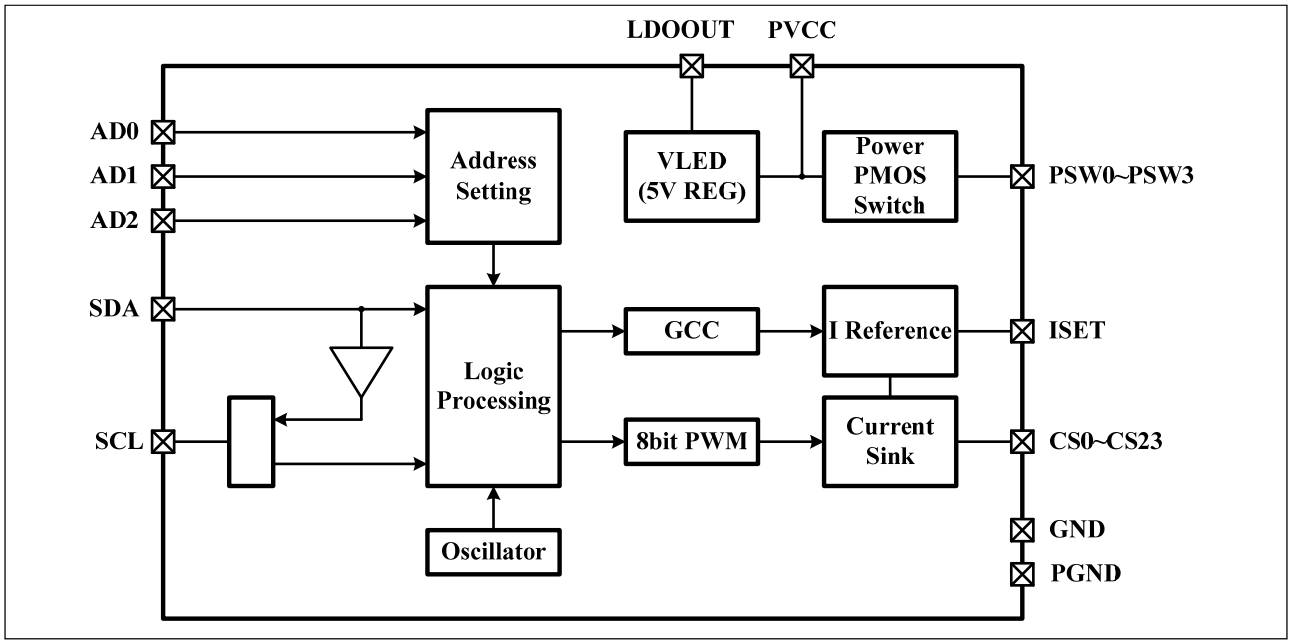
Note 3: I_{OUT} accuracy (device to device) $\triangle I_{ACC}$ is calculated:

$$\Delta I_{ACC} = \left(\frac{I_{OUT(MIN)} - I_{OUT(IDEAL)}}{I_{OUT(IDEAL)}} \right) \times 100\% \sim \left(\frac{I_{OUT(MAX)} - I_{OUT(IDEAL)}}{I_{OUT(IDEAL)}} \right) \times 100\%$$

Where $I_{OUT(IDEAL)}$= 39.6mA when R_{ISET}= 1kΩ.

Note 4: Guaranteed by design.

FUNCTIONAL BLOCK DIAGRAM



DETAILED DESCRIPTION

I2C INTERFACE

IS31FL3748A uses a serial bus, which conforms to the I2C protocol, to control the chip's functions with two wires: SCL and SDA. The IS31FL3748A has a 7-bit slave address (A7:A1), followed by the R/W bit, A0. Set A0 to "0" for a write command and set A0 to "1" for a read command. The value of bits from A6 to A1 is decided by the connection of the ADx pins.

Input voltages and logic states of the AD2, AD1 and AD0 pins are determined as follows.

Table 1 Slave Address

A7	A6:A5	A4:A3	A2:A1	A0	Remark
1	AD2	AD1	AD0	0	ADx=VCC, ISET, Open or GND, "10000000" ~ "11111100" AD[2:0] must not all connect to VCC
1	AD2	AD1	AD0	1	Read address
1	1	1	1	0	Broadcast address, all slaves will ack

ADx connected to VCC, ADx = 11;

ADx connected to ISET, ADx = 01;

ADx is open, ADx = 10;

ADx connected to GND, ADx = 00;

Total support "10000000"~"11111100", 63 addresses.

When A7:A0= "1111 1110" all slave device are selected, include 4 PWM pages in each single part.

The SCL line is uni-directional. The SDA line is bi-directional (open-collector) with a pull-up resistor (typically 2kΩ). The maximum clock frequency specified by the I2C standard is 1MHz. In this discussion, the master is the microcontroller and the slave is the IS31FL3748A.

The timing diagram for the I2C is shown in Figure 6. The SDA is latched in on the stable high level of the SCL. When there is no interface activity, the SDA line should be held high.

The "START" signal is generated by lowering the SDA signal while the SCL signal is high. The start signal will alert all devices attached to the I2C bus to check the incoming address against their own chip address.

The 8-bit chip address is sent next, most significant bit first. Each address bit must be stable while the SCL level is high.

After the last bit of the chip address is sent, the master checks for the IS31FL3748A's acknowledge. The master releases the SDA line high (through a pull-up resistor). Then the master sends an SCL pulse. If the IS31FL3748A has received the address correctly, then it holds the SDA line low during the SCL pulse. If the SDA line is not low, then the master should send a "STOP" signal (discussed later) and abort the transfer.

Following acknowledge of IS31FL3748A, the register address byte is sent, most significant bit first. IS31FL3748A must generate another acknowledge indicating that the register address has been received.

Then 8-bit of data byte are sent next, most significant bit first. Each data bit should be valid while the SCL level is stable high. After the data byte is sent, the IS31FL3748A must generate another acknowledge to indicate that the data was received.

The "STOP" signal ends the transfer. To signal "STOP", the SDA signal goes high while the SCL signal is high.

ADDRESS AUTO INCREMENT

To write multiple bytes of data into IS31FL3748A, load the address of the data register that the first data byte is intended for. During the IS31FL3748A acknowledge of receiving the data byte, the internal address pointer will increment by one. The next data byte sent to IS31FL3748A will be placed in the new address, and so on. The auto increment of the address will continue as long as data continues to be written to IS31FL3748A (Figure 9).

READING OPERATION

Most of the registers can be read.

To read the register, after I2C start condition, the bus master must send the IS31FL3748A device address with the R/$\overline{W}$ bit set to "0", followed by the register address which determines which register is accessed. Then restart I2C, the bus master should send the IS31FL3748A device address with the R/$\overline{W}$ bit set to "1". Data from the register defined by the command byte is then sent from the IS31FL3748A to the master (Figure 10).

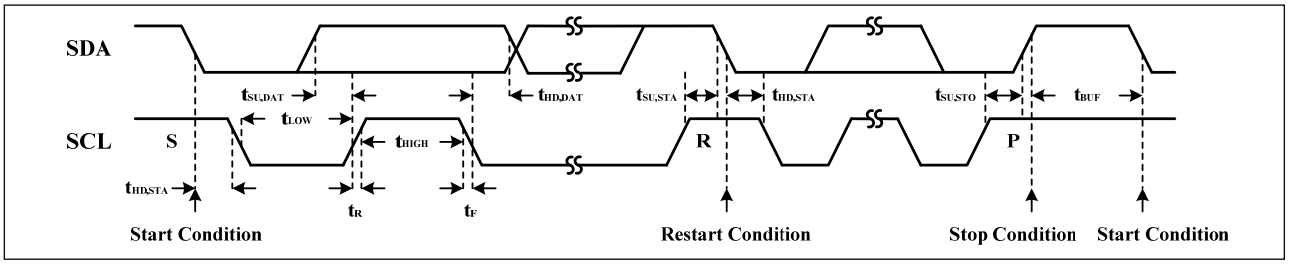


Figure 6 I2C Interface Timing

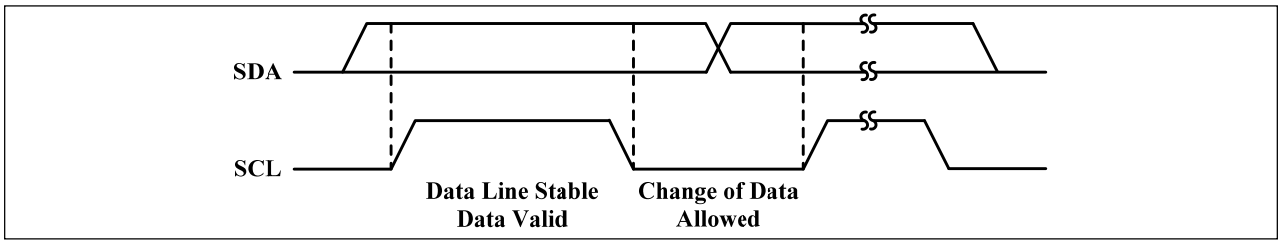


Figure 7 I2C Bit Transfer

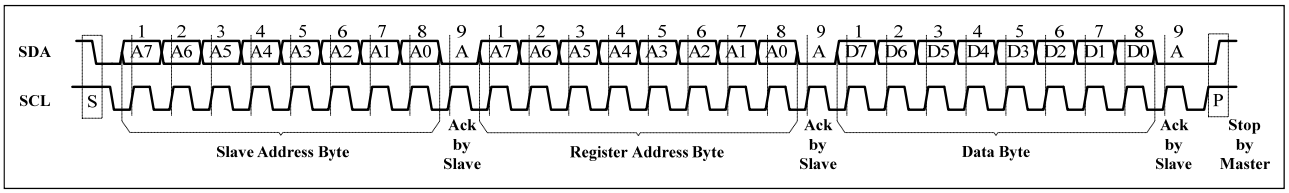


Figure 8 I2C Writing to IS31FL3748A (Typical)

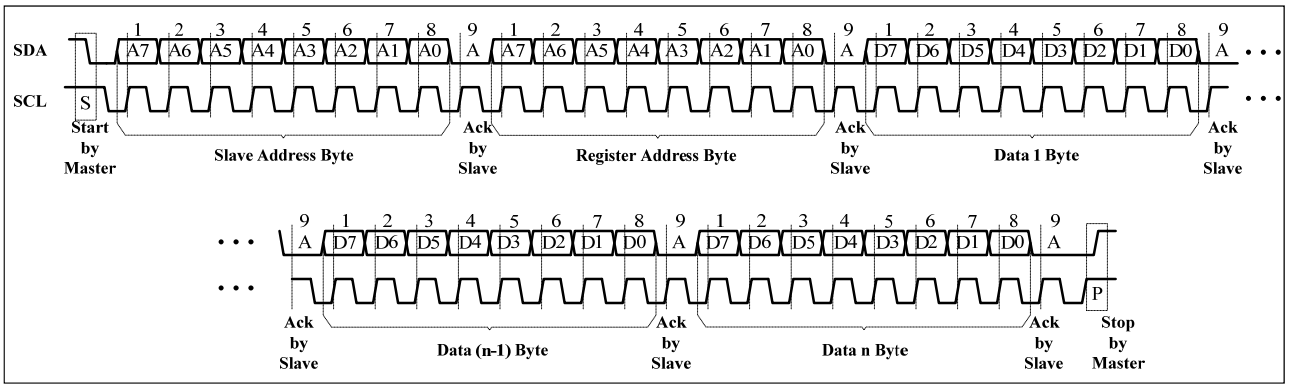


Figure 9 I2C Writing to IS31FL3748A (Automatic Address Increment)

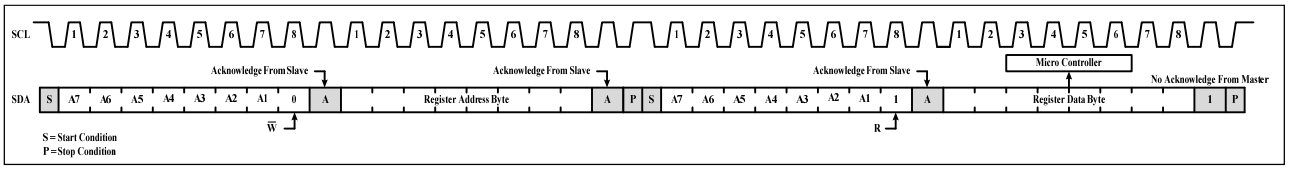


Figure 10 I2C Reading from IS31FL3748A

REGISTER DEFINITIONS

Table 4 Command Register Definition

Address	Name	Function	Table	R/W	Default
7Eh	Command Register Write Lock	To unlock Command Register	-	W	0000 0000
7Ah	Command Register	Available Page 1 to Page 9 Registers	5	W	0101 0110

REGISTER PAGE CONTROL

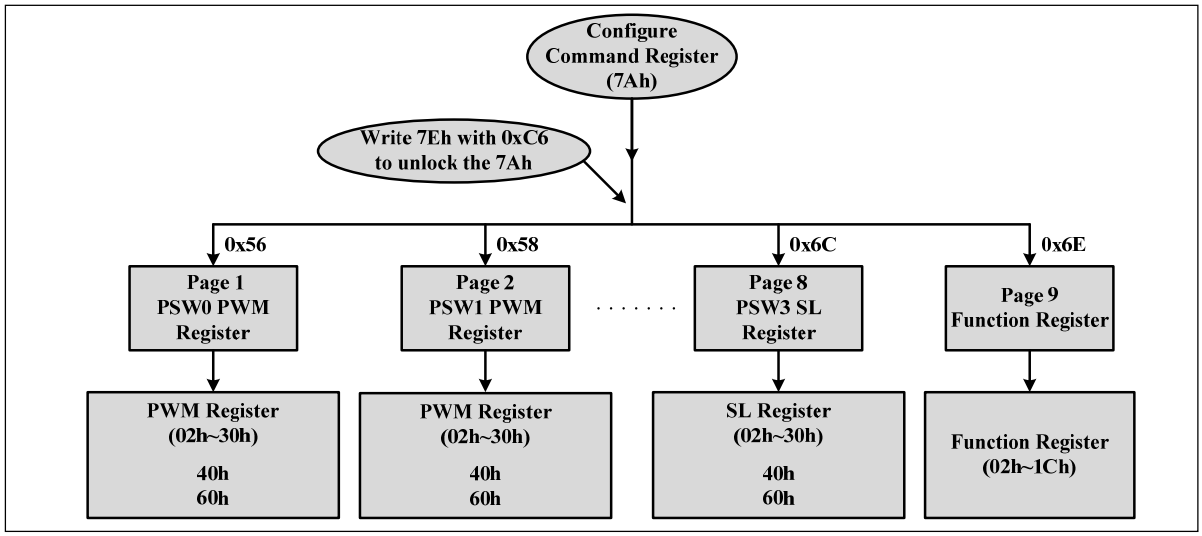


Figure 11 Register Pages

Table 5 7Ah Command Register

Data	Hex	Function
0101 0110	0x56	Point to Page 1(PG1): PSW0-PWM (PSW0 page PWM Register is available)
0101 1000	0x58	Point to Page 2(PG2): PSW1-PWM (PSW1 page PWM Register is available)
0101 1010	0x5A	Point to Page 3(PG3): PSW2-PWM (PSW2 page PWM Register is available)
0101 1100	0x5C	Point to Page 4(PG4): PSW3-PWM (PSW3 page PWM Register is available)
0110 0110	0x66	Point to Page 5(PG5): PSW0-SL (PSW0 page Current Scaling Register is available)
0110 1000	0x68	Point to Page 6(PG6): PSW1-SL (PSW1 page Current Scaling Register is available)
0110 1010	0x6A	Point to Page 7(PG7): PSW2-SL (PSW2 page Current Scaling Register is available)
0110 1100	0x6C	Point to Page 8(PG8): PSW3-SL (PSW3 page Current Scaling Register is available)
0110 1110	0x6E	Point to Page 9(PG9): Function Register Page
Others	-	Not allowed

Note 5: Register 7Ah is not in any of above pages and it can swap the pages at any time, when power up, default page is page 1(7Ah=0x56), and all the writing is in page 1 if not swap to other pages. Follow the sequence can swap to new page:

For example, when write “0110 0110” (0x66) in the Command Register (7Ah), the data which writing after will be stored in page 5, PSW0-SL page, the White balance Scaling Register of PSW0.

For example, when write “0110 1110” (0x6E) in the Command Register (7Ah), the data which writing after will be stored in page 9, Function Register page.

Table 6 Register Definition

Address	Name	Function	Table	R/W	Default
PG1 (0x56): PWM Register of PSW0					
02h~30h	PWM Register	Set PWM value for PSW0	7	W	0000 0000
40h	All Channel Select	Set global channel		W	0000 0000
60h	Special Mode	Set special mode		W	0000 0000
PG2 (0x58): PWM Register of PSW1					
02h~30h	PWM Register	Set PWM value for PSW1	7	W	0000 0000
40h	All Channel Select	Set global channel		W	0000 0000
60h	Special Mode	Set special mode		W	0000 0000
PG3 (0x5A): PWM Register of PSW2					
02h~30h	PWM Register	Set PWM value for PSW2	7	W	0000 0000
40h	All Channel Select	Set global channel		W	0000 0000
60h	Special Mode	Set special mode		W	0000 0000
PG4 (0x5C): PWM Register of PSW3					
02h~30h	PWM Register	Set PWM value for PSW3	7	W	0000 0000
40h	All Channel Select	Set global channel		W	0000 0000
60h	Special Mode	Set special mode		W	0000 0000
PG5 (0x66): SL Register of PSW0					
02h~30h	SL Register	Set SL value for PSW0	9	W	1111 1110
40h	All Channel Select	Set global channel		W	1111 1110
60h	Special Mode	Set special mode		W	1111 1110
PG6 (0x68): SL Register of PSW1					
02h~30h	SL Register	Set SL value for PSW1	9	W	1111 1110
40h	All Channel Select	Set global channel		W	1111 1110
60h	Special Mode	Set special mode		W	1111 1110
PG7 (0x6A): SL Register of PSW2					
02h~30h	SL Register	Set SL value for PSW2	9	W	1111 1110
40h	All Channel Select	Set global channel		W	1111 1110
60h	Special Mode	Set special mode		W	1111 1110
PG8 (0x6C): SL Register of PSW3					
02h~30h	SL Register	Set SL value for PSW3	9	W	1111 1110
40h	All Channel Select	Set global channel		W	1111 1110
60h	Special Mode	Set special mode		W	1111 1110

Table 6 Register Definition (Continued)

Address	Name	Function	Table	R/W	Default
PG9 (0x6E): Function Register					
02h	Configuration Register	Set operating mode	11	W	0000 0010
04h	Global Current Control Register	Set global current for R channels	12	W	1111 1110
06h		Set global current for G channels		W	
08h		Set global current for B channels		W	
0Ah	Spread Spectrum Register	Set spread spectrum and SYNC function	13	W	0000 0000
0Eh	Power Noise Reduction (PNR) Register	Power noise reduction setting	14	W	1001 0000
10h	Temperature Status Register	Temperature thermal roll off setting	15	W	0000 0000
12h~28h	Open Detect Register	Store the open information of LED	16~18	R	0000 0000
30h	Pull Down Voltage Selection Register 1	Set de-ghost option: pull down voltage for PSW0 and PSW1	19	W	0000 0000
32h	Pull Down Voltage Selection Register 2	Set de-ghost option: pull down voltage for PSW2 and PSW3	20	W	0000 0000
34h	Pull Up Voltage Selection Register 1	CSx pull up voltage selection	21	W	0000 0000
36h	Pull Up Voltage Selection Register 2	CSx pull up voltage selection and PSW pull 1.5x mode enable	22	W	0000 0000
3Eh	Software Reset Register	Enable software reset function	-	W	0000 0000

Table 7 PWM Register: PG1~PG4 (7Ah=0x56~0x5C): PWM Register of PSW0~PSW3
Data bytes set PWM value.

HEX	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register	Remark
02h	0	0	0	0	0	0	1	0	/CS00	
04h	0	0	0	0	0	1	0	0	/CS01	
06h	0	0	0	0	0	1	1	0	/CS02	
…									…	
30h	0	0	1	1	0	0	0	0	/CS23	
40h	0	1	0	0	0	0	0	0	Global	Default Local

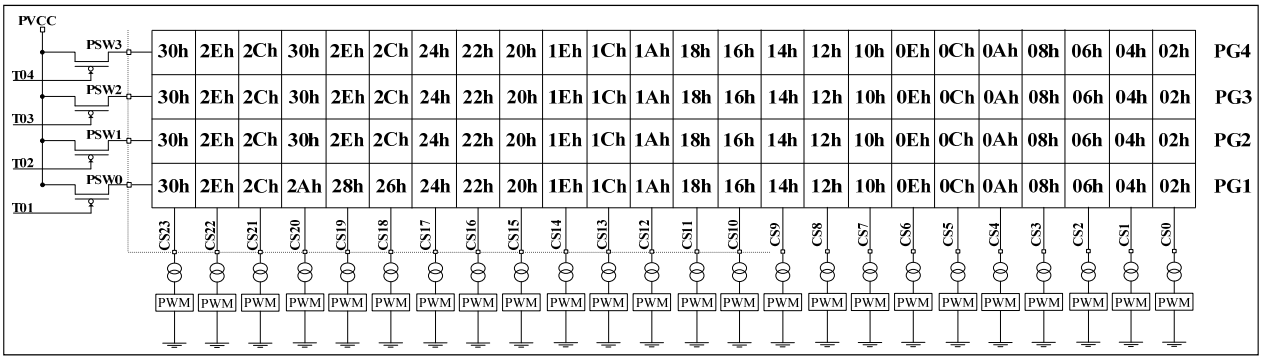


Figure 12 PWM Register

Table 8 Data Bytes: PWM Value
Data bytes set PWM value.

HEX	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	PWM Dimming (for reference only)
00	0	0	0	0	0	0	0	0	0/256, OFF (Default)
01	0	0	0	0	0	0	0	1	1/256
02	0	0	0	0	0	0	1	0	2/256
… …									
FE	1	1	1	1	1	1	1	0	254/256
FF	1	1	1	1	1	1	1	1	255/256

Table 9 Register: PG5~PG8 (7Ah= 0x66~0x6C): SL Register of PSW0~PSW3

Data bytes set dot correction (SL) value.

HEX	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register	Remark
02	0	0	0	0	0	0	1	0	/CS00	
04	0	0	0	0	0	1	0	0	/CS01	
06	0	0	0	0	0	1	1	0	/CS02	
…									…	
30	0	0	1	1	0	0	0	0	/CS23	
40	0	1	0	0	0	0	0	0	Global	Default Local

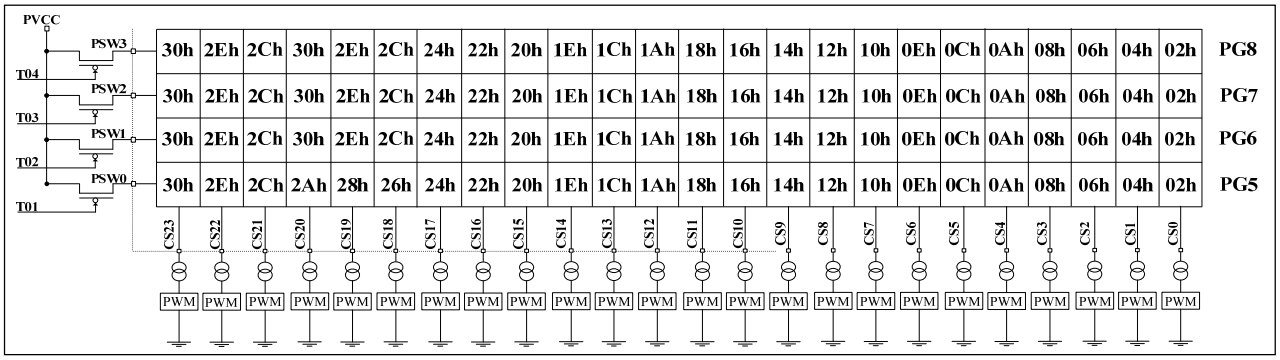


Figure 13 SL Register

Data bytes set current scale value.

HEX	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	SL current (of maximum, for reference only)
00	0	0	0	0	0	0	0	0	0/256, OFF
01	0	0	0	0	0	0	0	1	1/256
02	0	0	0	0	0	0	1	0	2/256
03	0	0	0	0	0	0	1	1	3/256
… …									
FE	1	1	1	1	1	1	1	0	254/256
FF	1	1	1	1	1	1	1	1	255/256 (Default)

Function Register: PG9 (7Ah= 0x6E)

Table 11 02h Configuration Register

Bit	D7	D6:D4	D3:D2	D1	D0
Name	-	SWS	PWMF	SSD	-
Default	-	000	00	1	0

The Configuration Register sets operating mode of IS31FL3748A. When SSD is "0", IS31FL3748A works in software shutdown mode. When SSD is set to "1", IS31FL3748A works in normal operate mode.

SWS control the duty cycle of the PSWx, default mode is 1/4.

SWS	PSWx Scan Setting
000	PSW0~PSW3 scan, 1/4
001	PSW0~PSW2 scan, PSW3 no-active
010	PSW0~PSW1 scan, PSW2 and PSW3 no-active
011	Only PSW0 scan, PSW1~PSW3 no-active
100	PSW0~PSW1 scan, PSW2=PSW0, PSW3=PSW1

PWMF	PWM Frequency
00	25.6kHz (default)
01	51.2kHz
10	800Hz
11	400Hz

SSD	Software Shutdown Control
0	Software shutdown
1	Normal operation

Table 12 04h/06h/08h Global Current Control Register

Bit	D7:D1	D0
Name	GCCx	-
Default	1111 111	0

The Global Current Control Registers modulate all CSy (x=0~23) SL current which is noted as IOUT in 128 steps.

04h is for R channels, GCCR, CS0, CS3, CS6 … CS21

06h is for G channels, GCCG, CS1, CS4, CS7 … CS22

08h is for B channels, GCCB, CS2, CS5, CS8 … CS23

I_{OUT} is computed by the Formula (1):

$$I_{OUT(PEAK)} = \frac{40}{R_{ISET}} \times \frac{GCC}{256} \times \frac{SL}{256} \qquad (1)$$

$$GCC = \sum_{n=0}^{7} D[n] \cdot 2^n$$

$$SL = \sum_{n=0}^{7} D[n] \cdot 2^n$$

Where D[n] stands for the individual bit value, 1 or 0, in location n.

Table 13 0Ah Spread Spectrum Register

Bit	D7:D6	D5:D4	D3:D2	D1	D0
Name	-	CLT	SYNC	SSP	-
Default	00	00	00	0	0

Spread Spectrum Register set the spread spectrum (SSP) and synchronization function of IS31FL3748A. The spread spectrum range is ±5%. When SSP enable, the spread spectrum function will be enabled and the CLT bits will adjust the cycle time of spread spectrum function.

CLT	Spread Spectrum Cycle Time
00	1980μs
01	1200μs
10	820μs
11	660μs

SYNC	Enable of SYNC Function
0x	Disable SYNC function, 30kΩ pull-low
10	Slave, clock input
11	Master, clock output

SSP	Spread Spectrum Function Enable
0	Disable
1	Enable

Table 14 0Eh Power Noise Reduction (PNR) Register

Bit	D7:D6	D5:D4	D3:D2	D1:D0
Name	PNR_B	PNR_G	PNR_R	-
Default	10	01	00	00

IS31FL3748A implemented a proprietary PWM algorithm which is to spread PWM rising and falling edges of each channel to minimize power line disturbance, hence to minimize power rail noise. Traditionally, all channels start PWM cycle at the same time, creating a large LED current switching transient on the power bus. Using this Power Noise Reduction (PNR) method, some LED rising and falling edges can be cancelled, some are spread at different time point, minimizing simultaneously switching

power transient noise. The timing and definition is shown in the following Figure 14.

Between each adjacent channel with the same starting PWM cycles, an internal clock delay is inserted to further spread the edges.

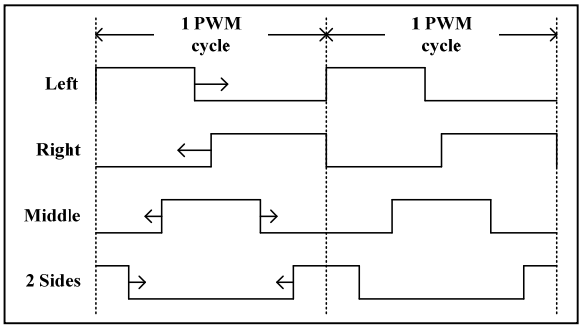


Figure 14 PWM Counting Position Definition

The PWM counting direction is programmable for each color group, for all R channel, G channel and B channel, defined by PNR[7:0]. Select different direction for R, G and B can minimize the power rail noise.

The default value of PNR_B is “10”, default value of PNR_G is “10’”, but before writing any value to 0Eh, if read out the 0Eh, the read result is always 0x00. After writing 0Eh with correct value, the reading result will be same as 0Eh is written.

PNR_B	PNR for blue channels
00	Left
01	Right
10	Middle (default)
11	Two sides

PNR_G	PNR for green channels
00	Left
01	Right (default)
10	Middle
11	Two sides

PNR_R	PNR for red channels
00	Left (default)
01	Right
10	Middle
11	Two sides

Table 15 10h Temperature Status Register

Bit	D7:D6	D5:D4	D3	D2	D1	D0
Name	TS	TROF	ODE	GOFF	GON	-
Default	00	00	0	0	0	0

TS store the temperature point of the IC. If the IC temperature reaches the temperature point the IC will trigger the thermal roll off and will decrease the current as TROF set percentage.

TS	Temperature Point, Thermal Roll Off start point
00	140°C
01	120°C
10	100°C
11	90°C

TROF	Percentage Of Output Current
00	100%
01	75%
10	55%
11	30%

ODE	Open Detect Enable
0	Disable
1	Enable

GOFF	All PWM off, if GON= “1”, GOFF will reset GON to “0”
0	Function off (default)
1	All channel’s PWM= 0x00

GON	All PWM On
0	Function off (default)
1	All channel’s PWM= 0xFE

Table 16 12h/18h/1Eh/24h R Open Status Register of PSW0/PSW1/PSW2/PSW3

Bit	D7:D0
Name	OPR7: OPR0
Default	0000 0000

Table 17 14h/1Ah/20h/26h G Open Status Register of PSW0/PSW1/PSW2/PSW3

Bit	D7:D0
Name	OPG7: OPG0
Default	0000 0000

Table 18 16h/1Ch/22h/28h B Open Status Register of PSW0/PSW1/PSW2/PSW3

Bit	D7:D0
Name	OPB7: OPB0
Default	0000 0000

The open status register stores the open information of LED string. PSW0 is 12h, 14h, 16h; PSW1 is 18h 1Ah 1Ch; PSW2 is 1Eh 20h 22h; PSW3 is 24h 26h 28h.

To get the correct open and short information, several configurations are recommended to set before setting the ODEN bit (D3 of 10h):

1 SL=0xFF. LSB of SL register should be set to “1”. For example, if set SL= “0xFE”, can’t read correct open and short information. If set SL= “0xFF”, can read correct open and short information. Recommend to set SL registers to 0xFF. Notice the default value of SL is 0xFE.
2 GCCx=0x10, too low or too high GCCx, like GCCx=0x01, may read out incorrect open or short information.
3 PWM=0xFE, too low PWM, like PWM=0x01, may read out incorrect open or short information.
4 Disable PSWx Pull Down Voltage and CSy Pull Up Voltage. 30h=0x00, 32h=0x00, 34h=0x00, 36h=0x00.

Table 19 30h Pull Down Voltage Selection Register 1

Bit	D7	D6:D4	D3:D1	D0
Name	-	PSW0PD	PSW1PD	-
Default	0	000	000	0

The “ghost” term is used to describe the behavior of an LED that should be OFF but instead glows dimly when another LED is turned ON. In matrix architecture any parasitic capacitance found in the constant-current outputs or the PCB traces to the LEDs may provide sufficient current to dimly light an LED to create a ghosting effect.

To prevent this LED ghost effect, the IS31FL3748A has integrated Pull down voltage for each PSWx (x=0~3) and Pull up voltage for each CSy (y=0~23). Select the right PSWx Pull down voltage (30h, 32h) and CSy Pull up voltage (34h, 36h) which eliminates the ghost LED for a particular matrix layout configuration.

The PSWx pull down voltage and CSy pull up voltage are active only when the CSy/PSWx output working the OFF state and therefore no power is lost through these voltages setting.

When IS31FL3748A works in hardware shutdown mode, the de-ghost function should be disabled.

PSWxPD PSWx Pull Down Voltage Selection Bit, 1x Mode, PSWVS= “0” in 36h
000 No pull down
001 0V
010 1.4V
011 2.8V
100 4.2V
101 5.6V
110 7.0V
111 8.4V

PSWxPD PSWx Pull Down Voltage Selection Bit, 1.5x Mode, PSWVS= “1” in 36h
000 No pull down
001 0V
010 2.1V
011 4.2V
100 6.3V
101 8.4V
110 10.5V
111 12.6V

Table 20 32h Pull Down Voltage Selection Register 2

Bit	D7	D6:D4	D3:D1	D0
Name	-	PSW2PD	PSW3PD	-
Default	0	000	000	0

PSWxPD PSWx Pull Down Voltage Selection Bit, 1x Mode, PSWVS= “0” in 36h
000 No pull down
001 0V
010 1.4V
011 2.8V
100 4.2V
101 5.6V
110 7.0V
111 8.4V

PSWxPD PSWx Pull Down Voltage Selection Bit, 1.5x Mode, PSWVS= “1” in 36h
000 No pull down
001 0V
010 2.1V
011 4.2V
100 6.3V
101 8.4V
110 10.5V
111 12.6V

Table 21 34h Pull Up Voltage Selection Register 1

Bit	D7	D6:D4	D3:D1	D0
Name	-	CSRPUV	CSGPUV	-
Default	0	000	000	0

CSxPUV CSx Pull up Voltage Selection Bit
000 No pull up
001 PVCC
010 PVCC-7.0V
011 PVCC-5.6V
100 PVCC-4.2V
101 PVCC-2.8V
110 PVCC-1.4V
111 PVCC-1.0V

Table 22 36h Pull Up Voltage Selection Register 2

Bit	D7	D6:D4	D3	D2	D1	D0
Name	-	CSBPUV	-	PSWVS	PSWTS	-
Default	0	000	0	0	0	0

CSxPUV	CSx Pull up Voltage Selection Bit
000	No pull up
001	PVCC
010	PVCC-7.0V
011	PVCC-5.6V
100	PVCC-4.2V
101	PVCC-2.8V
110	PVCC-1.4V
111	PVCC-1.0V

PSWVS	PSW Pull Down Voltage 1.5x Selection Bit
0	Disable
1	Enable

PSWTS	PSW Pull Down Only During the Interval Time
0	SW pull down in PSWx off time
1	SW pull down in t_{NOL}

3Eh Software Reset Register

Write Software Reset Register with 0x00 will reset all the register to default value.

APPLICATION INFORMATION

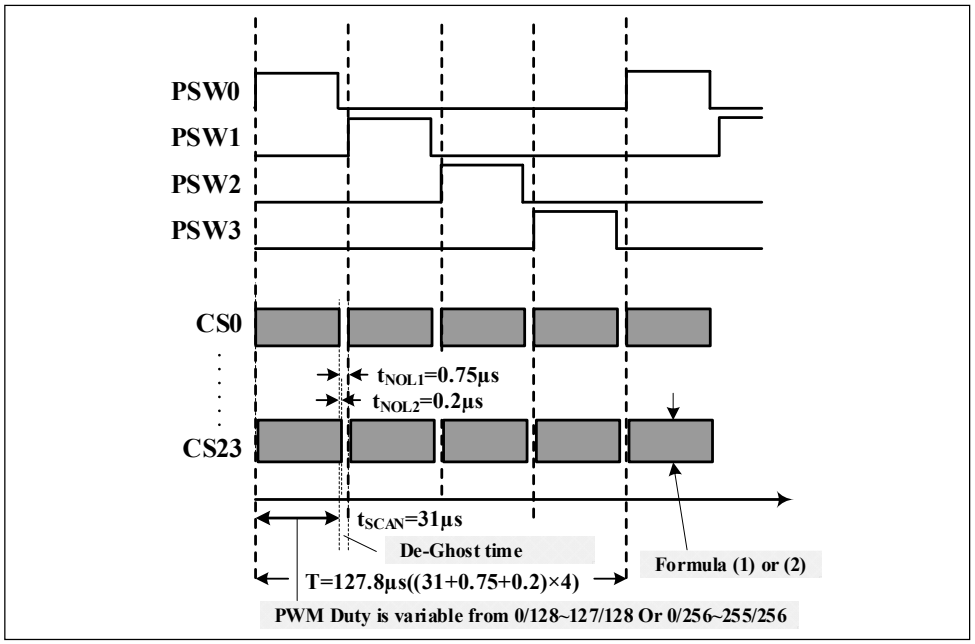


Figure 15 Scanning Timing

SCANING TIMING

As shown in Figure 15, the PSW0~PSW3 is turned on by serial, LED is driven 4 by 4 within the PSWx (x= 0~3) on time (PSWx, x= 0~3 is source and it is high when LED on), including the non-overlap blanking time during scan, the duty cycle of PSWx (active high, x= 0~3, SWS= "000") is:

$$Duty=\frac{31\mu s}{(31\mu s+0.75\mu s+0.2\mu s)}\times\frac{1}{4}=\frac{1}{4.12} \quad (2)$$

Where 31µs is t_{SCAN}, the period of scanning, 0.75µs is t_{NOL1}, 0.2µs is t_{NOL2}, the non-overlap time and CSy (y= 0~23) delay time.

If SWS= "001", the duty cycle is:

$$Duty=\frac{31\mu s}{(31\mu s+0.75\mu s+0.2\mu s)}\times\frac{1}{3}=\frac{1}{3.09} \quad (2)$$

PWM CONTROL

After setting the I_{OUT}, GCCx and SL, the brightness of each LEDs (LED average current (I_{LED})) can be modulated with 256 steps by PWM Register, as described in Formula below.

Where D[n] stands for the individual bit value, 1 or 0, in location n.

I_{OUT} is computed by the Formula (1):

$$I_{OUT(PEAK)}=\frac{40}{R_{ISET}}\times\frac{GCC}{256}\times\frac{SL}{256} \quad (1)$$

$$GCC=\sum_{n=0}^{7}D[n]\cdot 2^n$$

$$SL=\sum_{n=0}^{7}D[n]\cdot 2^n$$

Where D[n] stands for the individual bit value, 1 or 0, in location n.

The final average current of LED, I_{LED} is computed as Formula (3).

$$I_{LED}=\frac{PWM}{256}\times I_{OUT(PEAK)}\times Duty \quad (3)$$

$$PWM=\sum_{n=0}^{7}D[n]\cdot 2^n$$

Where PWM is PWM Registers (PG1~PG4, 02h~30h) data showing in Table 10.

For example, if R_{ISET}= 1kΩ, PWM= 255, and GCC= 255, SL= 255, then

$$I_{OUT(PEAK)}=\frac{40}{1k\Omega}\times\frac{255}{256}\times\frac{255}{256}=39.68mA$$

$$I_{LED}=I_{OUT(PEAK)}\times\frac{1}{4.12}\times\frac{PWM}{256}$$

Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve a breathing effect.

OPERATING MODE

IS32FL3748A can only operate in PWM Mode. The brightness of each LED can be modulated with 256 steps by PWM registers. For example, if the data in PWM Register is “0000 0100”, then the PWM is the fourth step.

Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve a breathing effect.

OPEN/SHORT DETECT FUNCTION

IS32FL3748A has open and short detect bit for each LED.

The open status register stores the open information of LED string. PSW0 is 12h, 14h, 16h; PSW1 is 18h 1Ah 1Ch; PSW2 is 1Eh 20h 22h; PSW3 is 24h 26h 28h.

To get the correct open and short information, several configurations are recommended to set before setting the ODEN bit (D3 of 10h):

1. SL=0xFF. LSB of SL register should be set to “1”. For example, if set SL= “0xFE”, can’t read correct open and short information. If set SL= “0xFF”, can read correct open and short information. Recommend to set SL registers to 0xFF. Notice the default value of SL is 0xFE.
2. GCCx=0x10, too low or too high GCCx, like GCCx=0x01, may read out incorrect open or short information.
3. PWM=0xFE, too low PWM, like PWM=0x01, may read out incorrect open or short information.
4. Disable PSWx Pull Down Voltage and CSy Pull Up Voltage. 30h=0x00, 32h=0x00, 34h=0x00, 36h=0x00.

DE-GHOST FUNCTION

The “ghost” term is used to describe the behavior of an LED that should be OFF but instead glows dimly when another LED is turned ON. A ghosting effect typically can occur when multiplexing LEDs. In matrix architecture any parasitic capacitance found in the constant-current outputs or the PCB traces to the LEDs may provide sufficient current to dimly light an LED to create a ghosting effect.

To prevent this LED ghost effect, the IS32FL3748A has integrated Pull down voltage setting for each PSWx (x=0~3) and Pull up voltage setting for each CSy (y=1~24). Select the right PSWx Pull down voltage (PG9, 30h and 32h) and CSy Pull up voltage (PG9, 34 and 36h) which eliminates the ghost LED for a particular matrix layout configuration.

Typically, need to depending on how many LED is connect in series in one LED dot position, selecting the voltage setting will be sufficient to eliminate the LED ghost phenomenon.

One LED: PSWxPD=2.8V, CSxPU=PVCC-2.8V

Two LEDs: PSWxPD=4.2V, CSxPU=PVCC-4.2V

Three LEDs: PSWxPD=7.0V, CSxPU=PVCC-7.0V

Four LEDs: PSWxPD=8.4V, CSxPU=PVCC-7.0V

Five LEDs: PSWxPD=10.5V, CSxPU=PVCC-7.0V

Six LEDs: PSWxPD=12.6V, CSxPU=PVCC-7.0V

More than six LEDs: PSWxPD=12.6V, CSxPU=PVCC-7.0V

When IS32FL3748A works in hardware shutdown mode, the de-ghost function should be disabled.

INTERFACE RESET

The I2C will be reset if the SDB pin is pull-high from 0V to logic high, at the operating SDB rising edge, the interface operation is not allowed.

SHUTDOWN MODE

Shutdown mode can be used as a means of reducing power consumption. During shutdown mode all registers retain their data.

Software Shutdown

By setting SSD bit of the Configuration Register (PG9, 02h) to “0”, the IS32FL3748A will operate in software shutdown mode. When the IS32FL3748A is in software shutdown, all current sources are switched off, so that the matrix is blanked.

Hardware Shutdown

The chip enters hardware shutdown when the SDB pin is pulled low. All analog circuits are disabled during hardware shutdown.

The chip releases hardware shutdown when the SDB pin is pulled high. During hardware shutdown state Function Register can be operated.

If V_{CC} has risk drop below 1.75V but above 0.1V during SDB pulled low, please re-initialize all Function Registers before SDB pulled high.

LAYOUT

The IS32FL3748A consumes lots of power so good PCB layout will help improve the reliability of the chip. Please consider below factors when layout the PCB.

Power Supply Lines

When designing the PCB layout pattern, the first step should consider about the supply line and GND connection, especially those traces with high current, also the digital and analog blocks’ supply line and GND should be separated to avoid the noise from digital block affect the analog block.

At least one 0.1μF capacitor, if possible with a 0.47μF or 1μF capacitor is recommended to connected to the ground at each power supply pins of the chip, and it

needs to close to the chip and the ground net of the capacitor should be well connected to the GND plane.

RISET

RISET should be close to the chip and the ground side should well connect to the GND plane.

Thermal Consideration

The over temperature of the chip may result in deterioration of the properties of the chip. IS32FL3748A has thermal pad but the chip could be very hot if power is very large. So do consider the ground area connects to the GND pins and thermal pad. Other traces should keep away and ensure the ground area below the package is integrated, and the back layer should be connected to the thermal pad thru 9 or 16 vias to be maximized the area size of ground plane.

The package thermal resistance, θ_{JA}, determines the amount of heat that can pass from the silicon die to the surrounding ambient environment. The θ_{JA} is a measure of the temperature rise created by power dissipation and is usually measured in degree Celsius per watt (°C/W).

When operating the chip at high ambient temperatures, or when driving maximum load current, care must be taken to avoid exceeding the package power dissipation limits. The maximum power dissipation can be calculated using the following Formula (6):

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}} \qquad (6)$$

So, $P_{D(MAX)} = \frac{125°C - 25°C}{37.3°C/W} \approx 2.68W$

Figure 16, shows the power derating of the IS31FL3748A on a JEDEC boards (in accordance with JESD 51-5 and JESD 51-7) standing in still air.

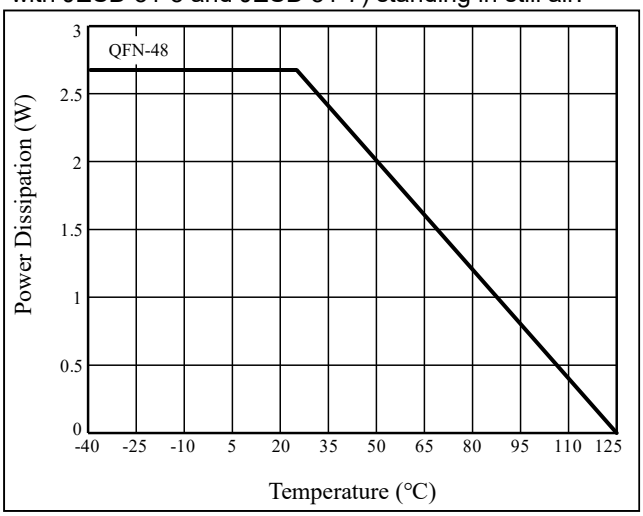


Figure 16 Dissipation Curve

Current Rating Example

For a RISET= 1kΩ application, the current rating for each net is as follows:

• VCC and SWx pins= 39.6mA×24=950.4mA, recommend trace width: 0.3mm~0.5mm.

• CSy pins= 39.4mA, recommend trace width: 0.1016mm~0.254mm.

• All other pins < 15mA, recommend trace width: 0.1016mm~0.254mm.

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	 150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

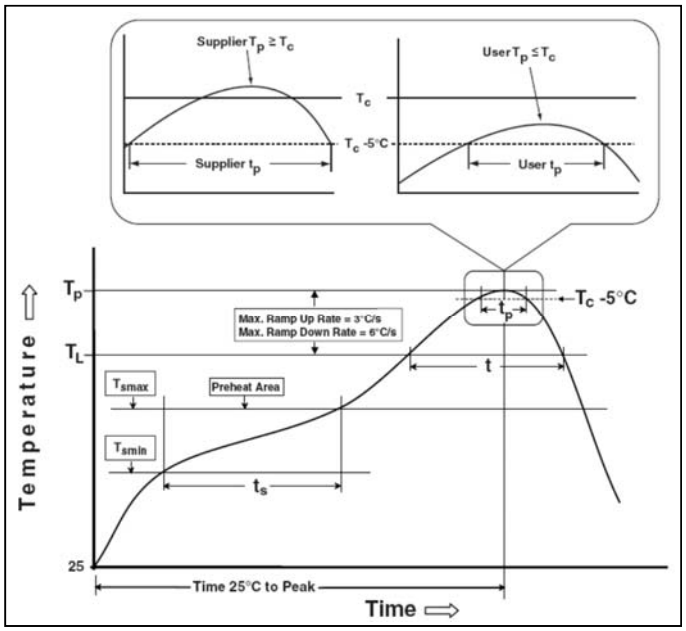
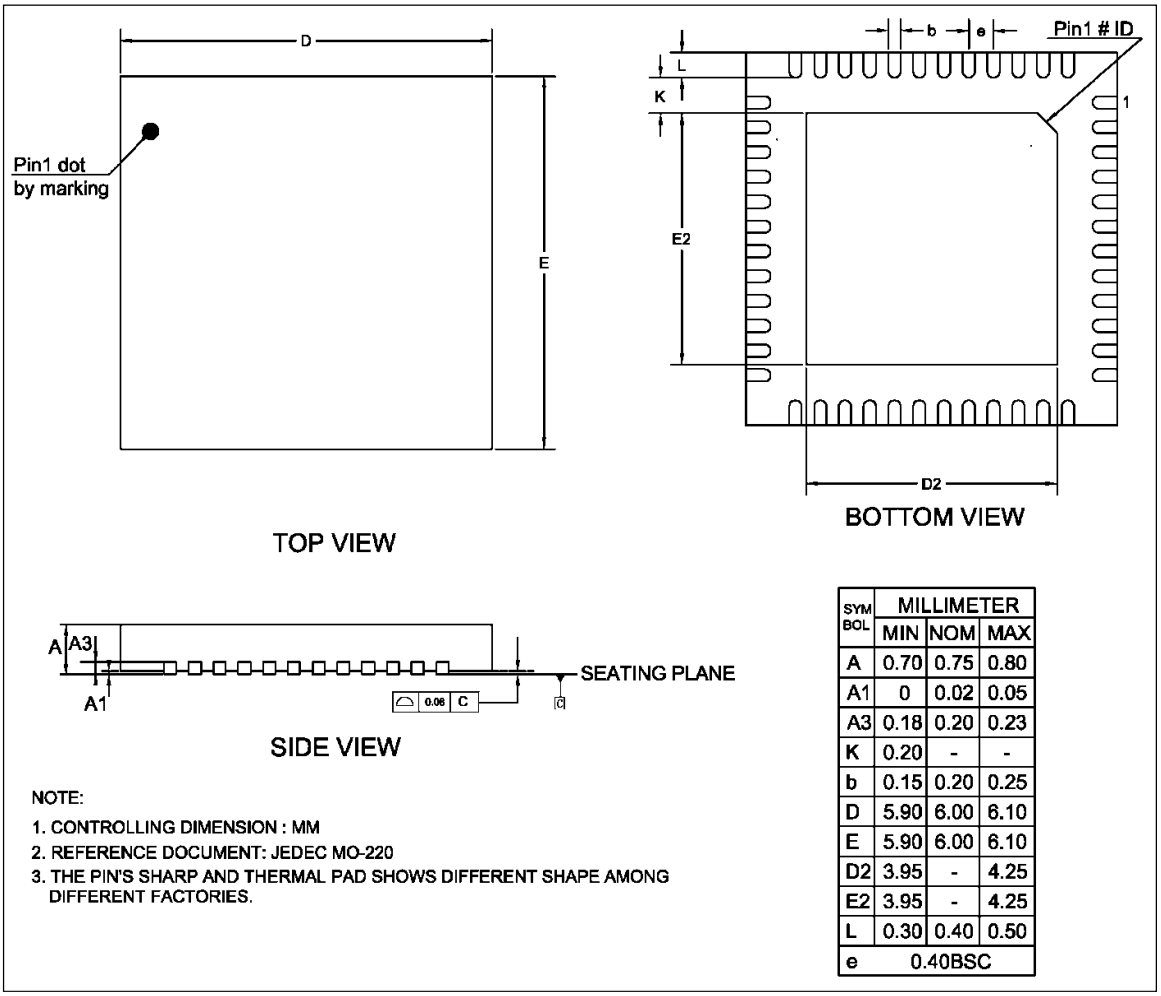


Figure 17 Classification profile

PACKAGE INFORMATION

QFN-48



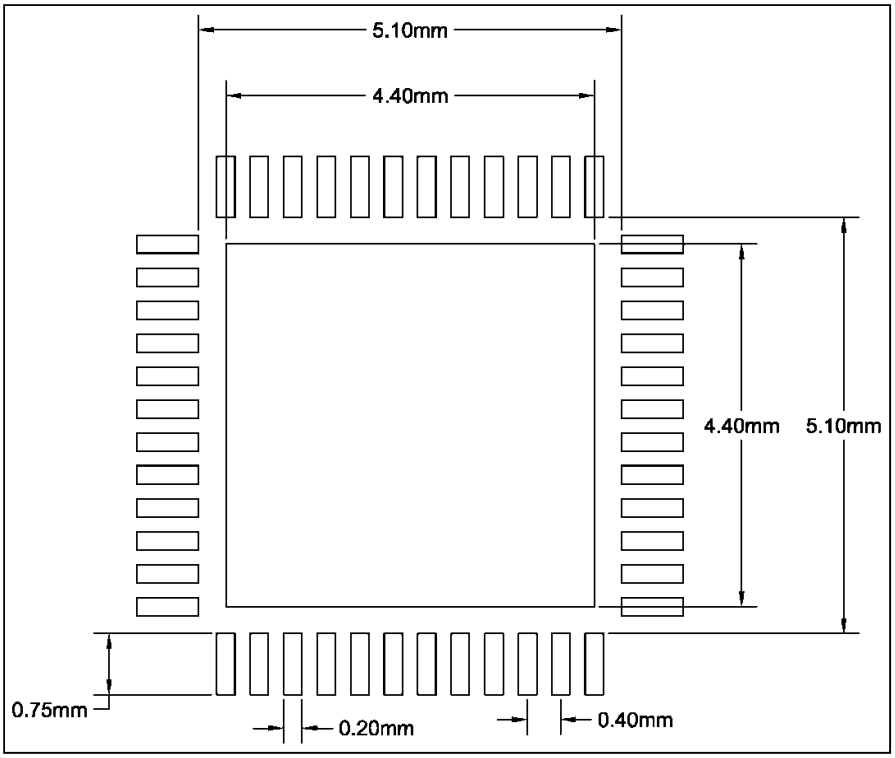
NOTE:

1. CONTROLLING DIMENSION : MM
2. REFERENCE DOCUMENT: JEDEC MO-220
3. THE PIN'S SHARP AND THERMAL PAD SHOWS DIFFERENT SHAPE AMONG DIFFERENT FACTORIES.

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3	0.18	0.20	0.23
K	0.20	-	-
b	0.15	0.20	0.25
D	5.90	6.00	6.10
E	5.90	6.00	6.10
D2	3.95	-	4.25
E2	3.95	-	4.25
L	0.30	0.40	0.50
e	0.40BSC		

RECOMMENDED LAND PATTERN

QFN-48



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. user's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
A	Initial release	2021.05.11
B	1. Update TONL2 value 2. Add I2C address setting	2021.07.06