IS31FL3742A

30×6 DOTS MATRIX LED DRIVER

November 2024

GENERAL DESCRIPTION

The IS31FL3742A is a general purpose 30×n (n=1~6) LED Matrix programmed via an I2C compatible interface. Each LED can be dimmed individually with 8-bit PWM data and 8-bit scaling data which allowing 256 steps of linear PWM dimming and 256 steps of DC current adjustable level.

Additionally each LED open and short state can be detected, IS31FL3742A store the open or short information in Open-Short Registers. The Open-Short Registers allowing MCU to read out via I2C compatible interface. Inform MCU whether there are LEDs open or short and the locations of open or short LEDs.

The IS31FL3742A operates from 2.7V to 5.5V and features a very low shutdown and operational current.

IS31FL3742A is available in QFN-48 (6mm×6mm) package. It operates from 2.7V to 5.5V over the temperature range of -40°C to +125°C.

FEATURES

- Supply voltage range: 2.7V to 5.5V
- 30 Current Sink × 6 SW matrix size: drive up to 180 LEDs or 60 RGBs
- Support 30×n (n=1~6) LED matrix configurations
- Individual 256 PWM control steps
- Individual 256 DC current steps
- Global 256 current setting
- SDB rising edge reset I2C module
- Programmable H/L logic: 1.4V/0.4V, 2.4V/0.6V
- 29kHz/3.6kHz/1.8kHz/900Hz PWM frequency
- 1MHz I2C-compatible interface
- interrupt and state lookup registers
- Individual open and short error detect function
- De-ghost
- Spread spectrum
- QFN-48 (6mm×6mm) package
- RoHS & Halogen-Free Compliance
- TSCA Compliance

APPLICATIONS

- Hand-held devices for LED display
- Gaming device (Keyboard, mouse etc.)
- LED in white goods application
- Music box

TYPICAL APPLICATION CIRCUIT

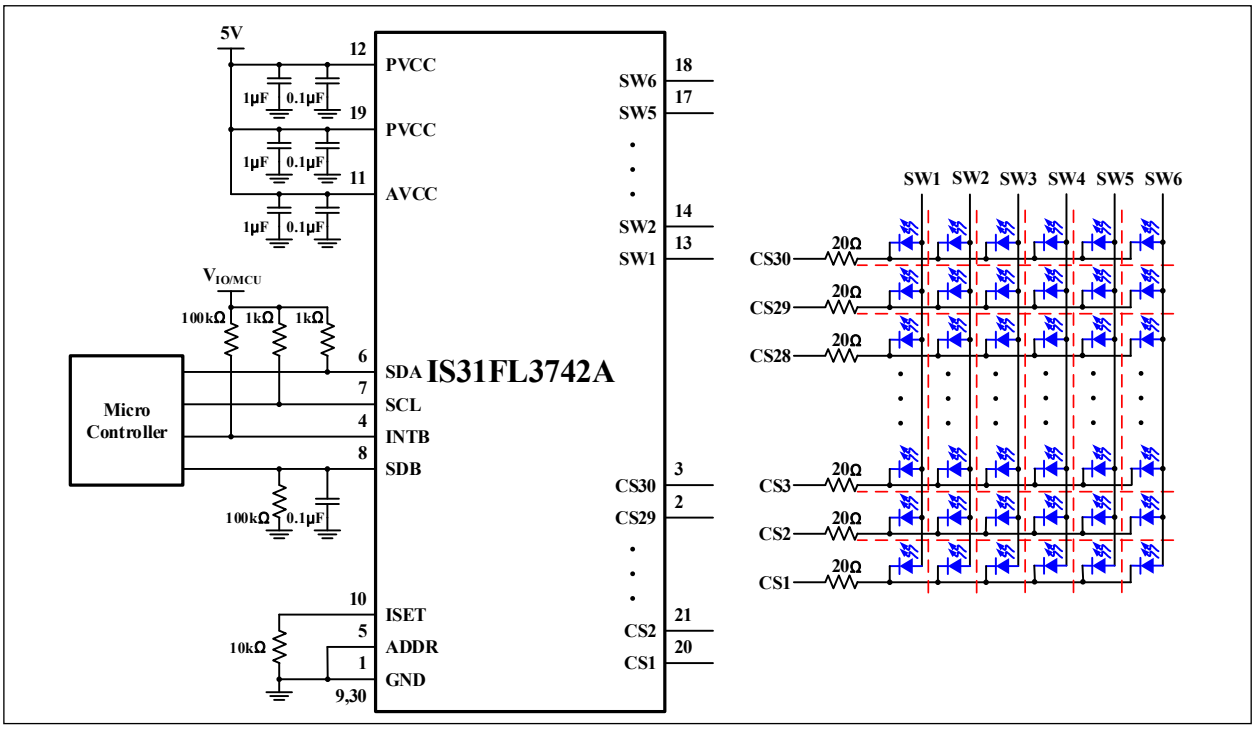


Figure 1 Typical Application Circuit (Single Color: 30x6)

TYPICAL APPLICATION CIRCUIT (CONTINUED)

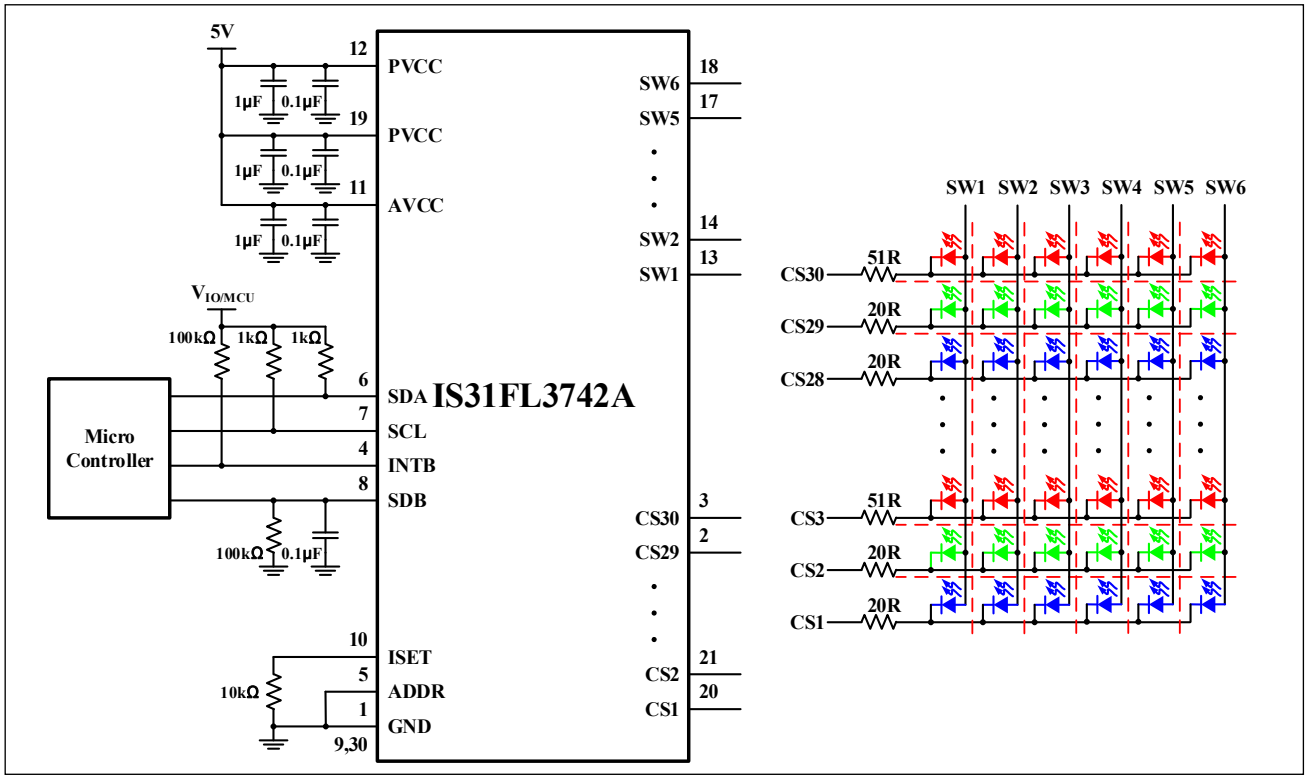
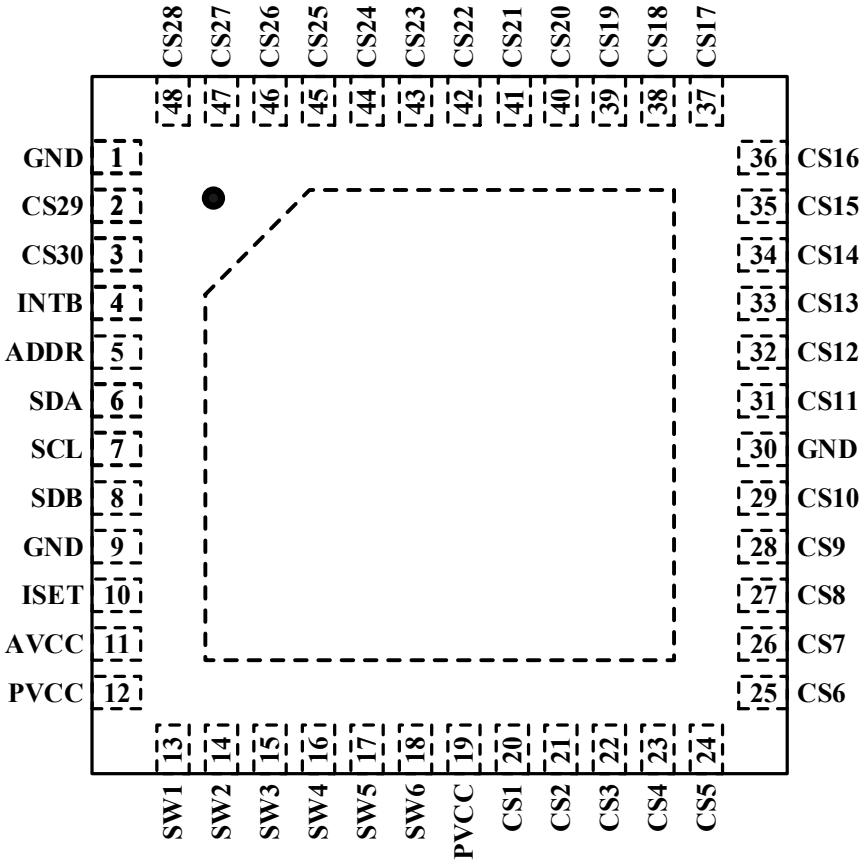


Figure 2 Typical Application Circuit (RGB Color: 10x6)

Note 1: The IC and LED should be placed far away from any local antenna in order to prevent EMI contamination.

PIN CONFIGURATION

Package	Pin Configuration (Top View)
QFN-48	

PIN DESCRIPTION

No.	Pin	Description
1, 9, 30	GND	Power GND (1, 30) and analog GND (9).
20~29, 31~48, 2, 3	CS1~CS30	Current sink pin for LED matrix.
4	INTB	Open drain, interrupt output pin. Register F0h sets the function of the INTB pin and active low when the interrupt event happens. Can be NC (float) if interrupt function no used.
5	ADDR	I2C address select pin.
6	SDA	I2C compatible serial data.
7	SCL	I2C compatible serial clock.
8	SDB	Shutdown pin.
10	ISET	I_{OUT} setting register.
11	AVCC	Power for analog and digital circuits.
12,19	PVCC	Power for current source.
13~18	SW1~SW6	Source/switch pin for LED matrix.
	Thermal Pad	Need to connect to GND pins in PCB.

ORDERING INFORMATION

Industrial Range: -40°C to +125°C

Order Part No.	Package	QTY/Reel
IS31FL3742A-QFLS4-TR	QFN-48, Lead-free	2500

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	-0.3V ~+6.0V
Voltage at any input pin	-0.3V ~ V_{CC}+0.3V
Maximum junction temperature, T_{JMAX}	+150°C
Storage temperature range, T_{STG}	-65°C ~+150°C
Operating temperature range, T_A=T_J	-40°C ~ +125°C
Package thermal resistance, junction to ambient (4-layer standard test PCB based on JESD 51-2A), θ_{JA}	37.8°C/W
ESD (HBM) ESD (CDM)	±2kV ±750V

Note 2: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

The following specifications apply for V_{CC}= 5V, T_A= 25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage		2.7		5.5	V
I_{CC}	Quiescent power supply current	R_{ISET}= 10kΩ, GCC= 0xFF, Scaling= 0xFF, PWM= 0x00, V_{CC}= 3.6V		3.6	4.5	mA
		R_{ISET}= 10kΩ, GCC= 0xFF, Scaling= 0xFF, PWM= 0x00, V_{CC}= 5V		4	5.5	
I_{SD}	Shutdown current	R_{ISET}= 10kΩ, V_{SDB}= 0V or software shutdown, V_{CC}= 3.6V		0.5	1	μA
		R_{ISET}= 10kΩ, V_{SDB}= 0V or software shutdown, V_{CC}= 5V		1	3	
$I_{OUT(PEAK)}$	Maximum constant current of CS1~CS30	R_{ISET}= 10kΩ, GCC= 0xFF, SL= 0xFF	34.96	38	41.04	mA
		R_{ISET}=16.8kΩ, GCC=0xFF, SL= 0xFF	21.16	23	24.84	mA
ΔI_{MATCH}	Output peak current mismatch between channels	R_{ISET}=10kΩ, GCC= 0xFF, SL= 0xFF (Note 3)	-6		6	%
I_{LED}	Average current on each LED I_{LED} = $I_{OUT(PEAK)}$/6.61	R_{ISET}= 10kΩ, GCC= 0xFF, SL= 0xFF	5.29	5.75	6.21	mA
V_{HR}	Current switch headroom voltage SW1~SW6	I_{SWITCH}= 800mA (Note 4,5)		550	750	mV
	Current sink headroom voltage CS1~CS30	I_{SINK}=38mA (Note 4)		350	600	
t_{SCAN}	Period of scanning	PFS= "0000" (29kHz)	28	32	37	μs
		PFS= "0011" (3.6kHz)	224	256	296	
		PFS= "0111" (1.8kHz)	448	512	592	
t_{NOL1}	Non-overlap blanking time during scan, the SWx and CSy are all off during this time	PFS= "0000" (29kHz)	1.75	2	2.32	μs
		PFS= "0011" (3.6kHz)	14	16	18.5	
		PFS= "0111" (1.8kHz)	28	32	37	
t_{NOL2}	Delay total time for CS1 to CS30, during this time, the SWx is on but CSx is not all turned on	PFS= "0000" (29kHz)	1.09	1.25	1.45	μs
		PFS= "0011" (3.6kHz)	8.75	10	11.6	
		PFS= "0111" (1.8kHz)	17.5	20	23.2	

ELECTRICAL CHARACTERISTICS (CONTINUED)

The following specifications apply for V_{CC} = 5V, T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Logic Electrical Characteristics (SDA, SCL, ADDR, SDB)						
V_{IL}	Logic “0” input voltage	V_{CC}=2.7V~5.5V, LGC=0			0.4	V
		V_{CC}=2.7V~5.5V, LGC=1			0.6	
V_{IH}	Logic “1” input voltage	V_{CC}=2.7V~5.5V, LGC=0	1.4			V
		V_{CC}=2.7V~5.5V, LGC=1	2.4			
V_{HYS}	Input schmitt trigger hysteresis	V_{CC}=3.6V, LGC=0		0.2		V
		V_{CC}=3.6V, LGC=1		0.2		
I_{IL}	Logic “0” input current	V_{INPUT}= L (Note 6)		5		nA
I_{IH}	Logic “1” input current	V_{INPUT}= H (Note 6)		5		nA

DIGITAL INPUT SWITCHING CHARACTERISTICS (NOTE 6)

Symbol	Parameter	Fast Mode			Fast Mode Plus			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{SCL}	Serial-clock frequency	-		400	-		1000	kHz
t_{BUF}	Bus free time between a STOP and a START condition	1.3		-	0.5		-	µs
$t_{HD, STA}$	Hold time (repeated) START condition	0.6		-	0.26		-	µs
$t_{SU, STA}$	Repeated START condition setup time	0.6		-	0.26		-	µs
$t_{SU, STO}$	STOP condition setup time	0.6		-	0.26		-	µs
$t_{HD, DAT}$	Data hold time	-		-	-		-	µs
$t_{SU, DAT}$	Data setup time	100		-	50		-	ns
t_{LOW}	SCL clock low period	1.3		-	0.5		-	µs
t_{HIGH}	SCL clock high period	0.7		-	0.26		-	µs
t_R	Rise time of both SDA and SCL signals, receiving	-		300	-		120	ns
t_F	Fall time of both SDA and SCL signals, receiving	-		300	-		120	ns

Note 3: $\Delta I_{MATCH}= (I_{OUT(PEAK)}- I_{AVG(PEAK)})/I_{AVG(PEAK)}\times 100\%$. $I_{AVG(PEAK)}= (I_{OUT(PEAK)1}+I_{OUT(PEAK)2}+\ldots I_{OUT(PEAK)30})/30$

Note 4: Global Current Control Register (GCC, PG4, 01h) written “1111 1111”, SL written “1111 1111”, R_{ISET}=10kΩ.

Note 5: All LEDs are on and PWM=“1111 1111”, GCC = “0xFF”.

Note 6: Guaranteed by design.

DETAILED DESCRIPTION

I2C INTERFACE

The IS31FL3742A uses a serial bus, which conforms to the I2C protocol, to control the chip's functions with two wires: SCL and SDA. The IS31FL3742A has a 7-bit slave address (A7:A1), followed by the R/W bit, A0. Set A0 to "0" for a write command and set A0 to "1" for a read command. The value of bits A1 and A2 are decided by the connection of the ADDR pin.

Table 1 Slave Address:

Bit	A7:A3	A2:A1	A0
Value	01100	ADDR	0/1

ADDR connects to GND, ADDR= 00;
ADDR connects to VCC, ADDR= 11;
ADDR connects to SCL, ADDR= 01;
ADDR connects to SDA, ADDR= 10;

The SCL line is uni-directional. The SDA line is bi-directional (open-drain) with a pull -up resistor (typically 400kHz I2C with 4.7kΩ, 1MHz I2C with 2kΩ). The maximum clock frequency specified by the I2C standard is 1MHz. In this discussion, the master is the microcontroller and the slave is the IS31FL3742A.

The timing diagram for the I2C is shown in Figure 3. The SDA is latched in on the stable high level of the SCL. When there is no interface activity, the SDA line should be held high.

The "START" signal is generated by lowering the SDA signal while the SCL signal is high. The start signal will alert all devices attached to the I2C bus to check the incoming address against their own chip address.

The 8-bit chip address is sent next, most significant bit first. Each address bit must be stable while the SCL level is high.

After the last bit of the chip address is sent, the master checks for the IS31FL3742A's acknowledge. The master releases the SDA line high (through a pull-up resistor). Then the master sends an SCL pulse. If the IS31FL3742A has received the address correctly, then it holds the SDA line low during the SCL pulse. If the SDA line is not low, then the master should send a "STOP" signal (discussed later) and abort the transfer.

Following acknowledge of IS31FL3742A, the register address byte is sent, most significant bit first. IS31FL3742A must generate another acknowledge indicating that the register address has been received.

Then 8-bit of data byte are sent next, most significant bit first. Each data bit should be valid while the SCL level is stable high. After the data byte is sent, the IS31FL3742A must generate another acknowledge to indicate that the data was received.

The "STOP" signal ends the transfer. To signal "STOP", the SDA signal goes high while the SCL signal is high.

ADDRESS AUTO INCREMENT

To write multiple bytes of data into IS31FL3742A, load the address of the data register that the first data byte is intended for. During the IS31FL3742A acknowledge of receiving the data byte, the internal address pointer will increment by one. The next data byte sent to IS31FL3742A will be placed in the new address, and so on. The auto increment of the address will continue as long as data continues to be written to IS31FL3742A (Figure 6).

READING OPERATION

Most of the registers can be read.

To read the FCh, FEh F0h and F1h, after I2C start condition, the bus master must send the IS31FL3742A device address with the R/$\overline{W}$ bit set to "0", followed by the register address (FEh or F1h) which determines which register is accessed. Then restart I2C, the bus master should send the IS31FL3742A device address with the R/$\overline{W}$ bit set to "1". Data from the register defined by the command byte is then sent from the IS31FL3742A to the master (Figure 7).

To read the registers of Page 0 thru Page 5, the FDh should write with 00h before follow the Figure 7 sequence to read the data. That means, when you want to read register of Page 0, the FDh should point to Page 0 first and you can read the Page 0 data.

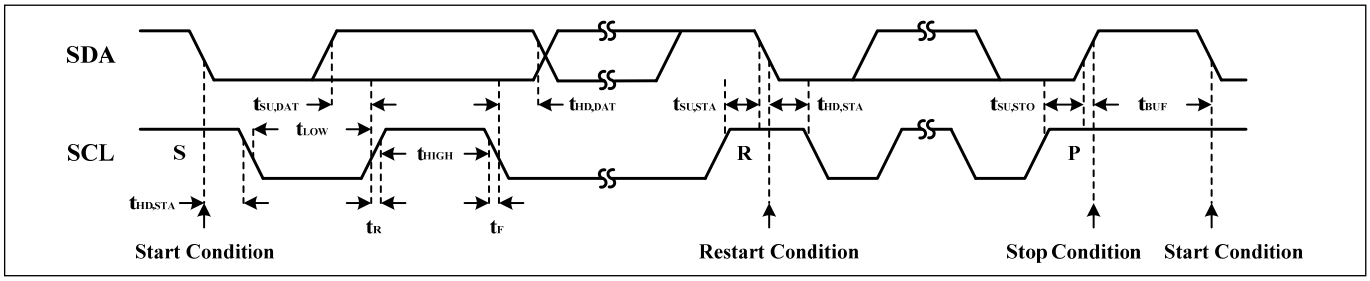


Figure 3 Interface Timing

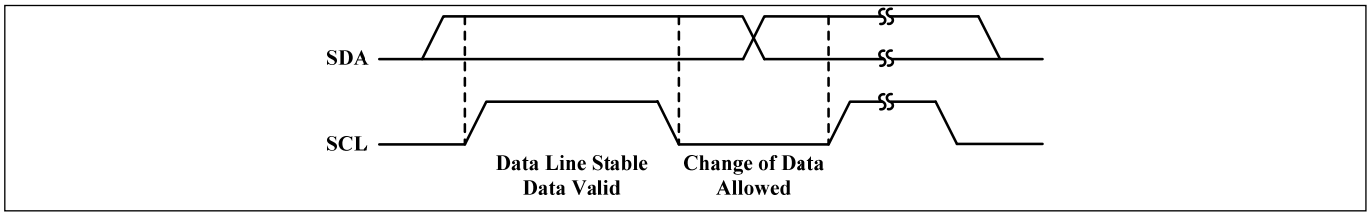


Figure 4 Bit Transfer

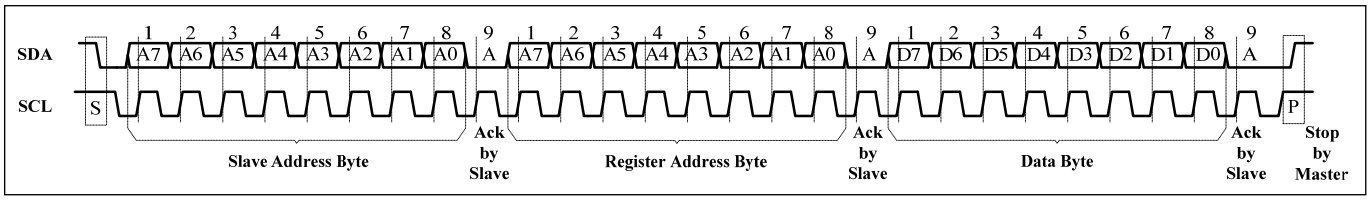


Figure 5 Writing to IS31FL3742A (Typical)

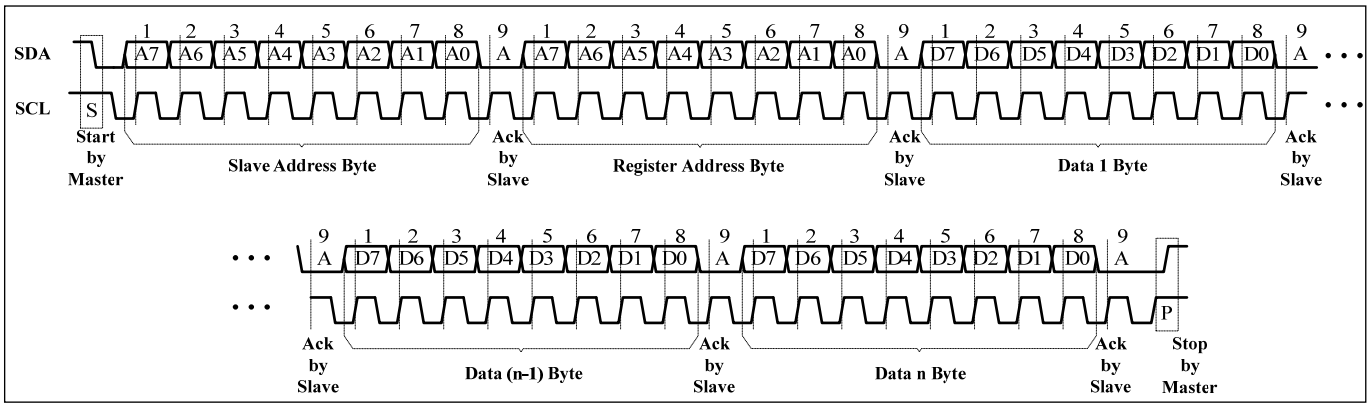


Figure 6 Writing to IS31FL3742A (Automatic Address Increment)

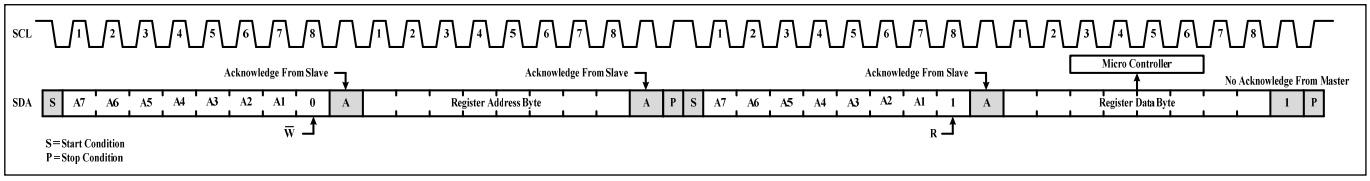


Figure 7 Reading from IS31FL3742A

Table 2 Register Definition-1

Address	Name	Function	Table	R/W	Default
FDh	Command Register	Available Page 0, Page 2 and Page 4 Registers	3	W	0000 0000
FEh	Command Register Write Lock	To lock/unlock Command Register	4	R/W	0000 0000
F0h	Interrupt Mask Register	Configure the interrupt function	5	W	
F1h	Interrupt Status Register	Show the interrupt status	6	R	
FCh	ID Register	For read the product ID only	-	R	Slave address

REGISTER CONTROL

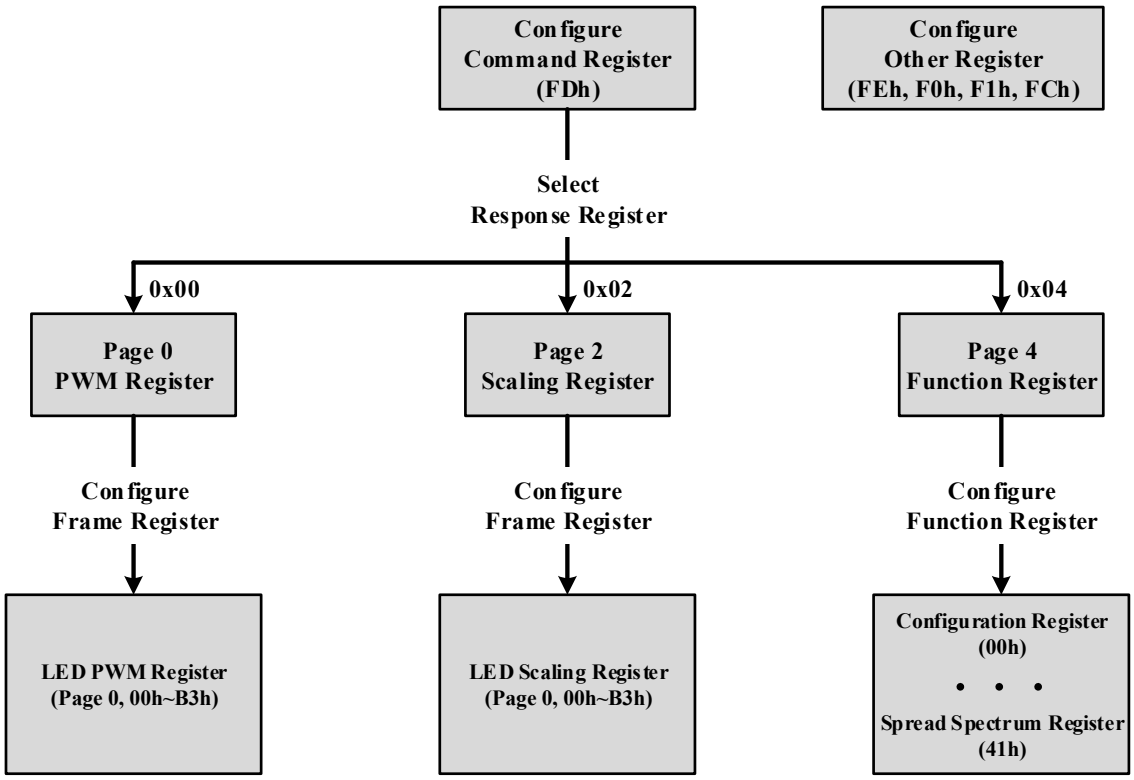


Table 3 FDh Command Register (Write Only)

Data	Function
0000 0000	Point to Page 0 (PG0, PWM Register is available)
0000 0010	Point to Page 2 (PG2, Scaling (SL) Register is available)
0000 0100	Point to Page 4 (PG4, Function Register is available)
Others	Not allowed

Note: FDh is locked when power up, need to unlock this register before write command to it. See Table 4 for detail.

The Command Register should be configured first after writing in the slave address to choose the available register. Then write data in the choosing register. Power up default state is “0000 0000”.

For example, when write “0000 0010” in the Command Register (FDh), the data which writing after will be stored in the page 2 Registers. Write new data can configure other frame position.

Table 4 FEh Command Register Write Lock (Read/Write)

Bit	D7:D0
Name	CRWL
Default	0000 0000

To select the PG0, PG2 and PG4, need to unlock this register first, with the purpose to avoid mis-operation of this register. When FEh is written with 0xC5, FDh is allowed to modify once, after the FDh is modified the FEh will reset to be 0x00 at once.

CRWL Command Register Write Lock
0000 0000 FDh write disable
1100 0101 FDh write enable once

Table 5 F0h Interrupt Mask Register

Bit	D7:D5	D4	D3:D2	D1	D0
Name	-	IAC	-	IS	IO
Default	000	0	00	0	0

Configure the interrupt function for IC.

IAC Auto Clear Interrupt Bit
0 Interrupt could not auto clear
1 Interrupt auto clear when INTB stay low exceeds 8ms

IS Dot Short Interrupt Bit
0 Disable dot short interrupt
1 Enable dot short interrupt

IO Dot Open Interrupt Bit
0 Disable dot open interrupt
1 Enable dot open interrupt

Table 6 F1h Interrupt Status Register (Read Only)

Bit	D7:D2	D1	D0
Name	-	SB	OB
Default	0000 00	0	0

Show the interrupt status for IC.

SB Short Bit
0 No short
1 Short happens

OB Open Bit
0 No open
1 Open happens

FCh ID Register
ID register is read only and read result is the device slave address. For example, if ADDR pin connects to GND, read result is 0x60.

Table 7 Register Definition-2

Address	Name	Function	Table	R/W	Default
PG0 (0x00): PWM Register					
00h~B3h	PWM Register	Set PWM for each LED	8	R/W	0000 0000
PG2 (0x02): LED Scaling ($I_{OUT(PEAK)}$ DC current adjust)					
00h~B3h	Scaling Register	Set Scaling for each LED	9	R/W	0000 0000
PG4 (0x04): Function Register					
00h	Configuration Register	Configure the operation mode	11	R/W	0000 0000
01h	Global Current Control Register	Set the global current	12	R/W	0000 0000
02h	Pull Down/Up Resistor Selection Register	Set the pull down resistor for SWx and the pull up resistor for CSy	13	R/W	0101 0101
03h~1Fh	Open/Short storage	Store the open or short information	14	R	0000 0000
36h	PWM frequency setting register	PWM frequency setting register	15	W	0000 0000
3Fh	Reset Register	Reset all register to POR state	-	W	0000 0000
41h	Spread Spectrum Register	Spread spectrum control register	16	W	0000 0000

Page 0 (PG0, FDh=0x00): PWM Register

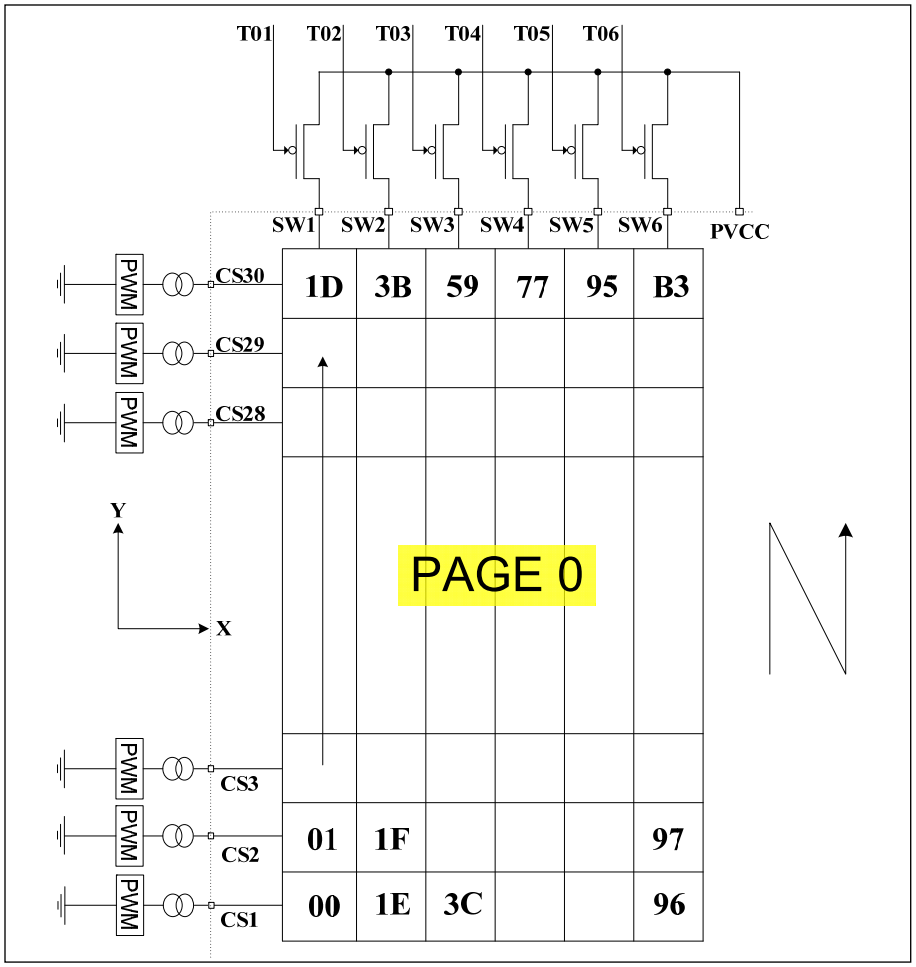


Figure 8 PWM Register

Table 8 00h ~ B3h PWM Register

Bit	D7:D0
Name	PWM
Default	0000 0000

Each dot has a byte to modulate the PWM duty in 256 steps.

The value of the PWM Registers decides the average current of each LED noted I_{LED}.

I_{LED} computed by Formula (1):

$$I_{LED} = \frac{PWM}{256} \times I_{OUT\ (PEAK\ )} \times Duty \quad (1)$$

$$PWM = \sum_{n=0}^{7} D[n] \cdot 2^n$$

Where Duty is the duty cycle of SWx,

$$Duty = \frac{32\mu s}{(32\mu s + 2\mu s + 1.25\mu s)} \times \frac{1}{6} = \frac{1}{6.61} \quad (2)$$

I_{OUT} is the output current of CSy (y=1~30),

$$I_{OUT(PEAK)} = \frac{383}{R_{ISET}} \times \frac{GCC}{256} \times \frac{SL}{256} \quad (3)$$

GCC is the Global Current Control Register (PG4, 01h) value, SL is the Scaling Register value and R_{ISET} is the external resistor of ISET pin. D[n] stands for the individual bit value, 1 or 0, in location n.

For example: if D7:D0=1011 0101 (0xB5, 181), GCC=0xFF, R_{ISET}=10kΩ, SL=0xFF

$$I_{LED} = \frac{383}{10k\Omega} \times \frac{255}{256} \times \frac{255}{256} \times \frac{1}{6.61} \times \frac{181}{256} = 4.06mA$$

Page 2 (PG2, FDh= 0x02): Scaling Register

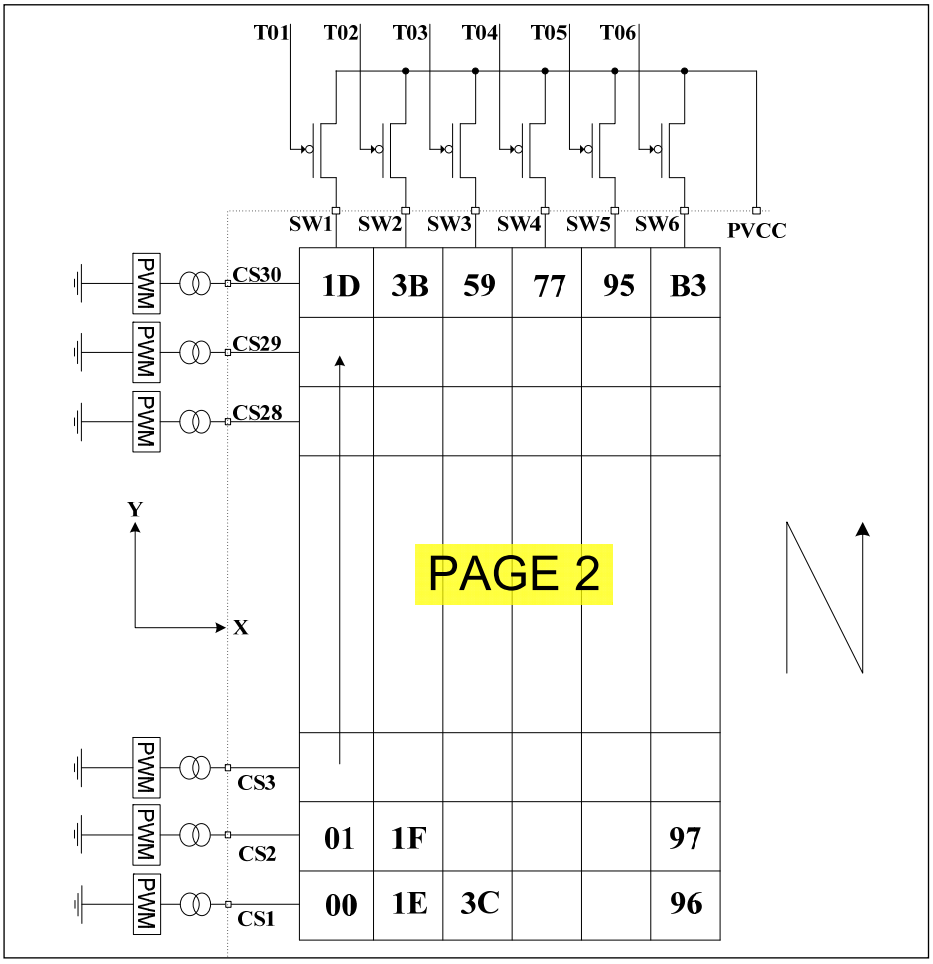


Figure 9 Scaling Register

Table 9 00h ~ B3h Scaling Register

Bit	D7:D0
Name	SL
Default	0000 0000

Scaling register control the DC output current of each dot. Each dot has a byte to modulate the scaling in 256 steps.

The value of the Scaling Registers decides the peak current of each LED noted I_{OUT}.

I_{OUT} computed by Formula (3):

$$I_{OUT(PEAK)} = \frac{383}{R_{ISET}} \times \frac{GCC}{256} \times \frac{SL}{256} \qquad (3)$$

$$SL = \sum_{n=0}^{7} D[n] \cdot 2^n$$

I_{OUT} is the output current of CSy (y=1~30),

GCC is the Global Current Control Register (PG4, 01h) value and R_{ISET} is the external resistor of ISET pin. D[n] stands for the individual bit value, 1 or 0, in location n.

For example: if R_{ISET}=10kΩ, GCC=0xFF, SL=0x7F,

$$SL = \sum_{n=0}^{7} D[n] \cdot 2^n = 127$$

$$I_{OUT(PEAK)} = \frac{383}{10k\Omega} \times \frac{255}{256} \times \frac{127}{256} = 18.93mA$$

$$I_{LED} = 18.93mA \times \frac{1}{6.61} \times \frac{PWM}{256} = 2.86mA \times \frac{PWM}{256}$$

Table 10 Page 4 (PG4, 0x04): Function Register

Register	Name	Function	Table	R/W	Default
00h	Configuration Register	Configure the operation mode	11	R/W	0000 0000
01h	Global Current Control Register	Set the global current	12	R/W	0000 0000
02h	Pull Down/Up Resistor Selection Register	Set the pull down resistor for SWx and pull up resistor for CSy	13	R/W	0101 0101
03h~2Fh	Open/Short Register	Store the open or short information	14	R	0000 0000
36h	PWM frequency setting register	PWM frequency setting register	15	W	0000 0000
3Fh	Reset Register	Reset all register to POR state	-	W	0000 0000
41h	Spread Spectrum Register	Spread spectrum control register	16	W	0000 0000

Table 11 00h Configuration Register

Bit	D7:D4	D3	D2:D1	D0
Name	SWS	LGC	OSDE	SSD
Default	0000	0	00	0

The Configuration Register sets operating mode of IS31FL3742A.

SSD Software Shutdown Control
0 Software shutdown
1 Normal operation

OSDE Open Short Detection Enable
00/11 Disable open/short detection
01 Enable open detection
10 Enable short detection

LGC H/L logic
0 1.4V/0.4V
1 2.4V/0.6V

SWS SWx Setting
0011 n=6, SW1~SW6, 1/6
0100 n=5, SW1~SW5, 1/5, SW6 no-active
0101 n=4, SW1~SW4, 1/4, SW5~SW6 no-active
0110 n=3, SW1~SW3, 1/3, SW4~SW6 no-active
0111 n=2, SW1~SW2, 1/2, SW3~SW6 no-active
1000 All CSx work as current sinks only, no scan
Others 1/6

When OSDE set to “01”, open detection will be trigger once, the user could trigger open detection again by set OSDE from “00” to “01”.

When OSDE set “10”, short detection will be trigger once, the user could trigger short detection again by set OSDE from “00” to “10”.

When SSD is “0”, IS31FL3742A works in software shutdown mode and to normal operate the SSD bit should set to “1”.

SWS control the duty cycle of the SW, for 1/6 duty cycle, the SWS must set to “0011”.

Table 12 01h Global Current Control Register

Bit	D7:D0
Name	GCCx
Default	0000 0000

The Global Current Control Register modulates all CSy (x=1~30) DC current which is noted as I_{OUT} in 256 steps.

I_{OUT} is computed by the Formula (3):

$$I_{OUT(PEAK)} = \frac{383}{R_{ISET}} \times \frac{GCC}{256} \times \frac{SL}{256} \qquad (3)$$

$$GCC = \sum_{n=0}^{7} D[n] \cdot 2^n$$

Where D[n] stands for the individual bit value, 1 or 0, in location n.

Table 13 02h Pull Down/Up Resistor Selection Register

Bit	D7	D6:D4	D3	D2:D0
Name	-	PDR	-	PUR
Default	0	101	0	101

Set pull down resistor for SWx and pull up resistor for CSy.

PUR CSy Pull Up Resistor Selection Bit
000 No pull up resistor
001 0.5kΩ pull-up in t_{NOL1}
010 1.0kΩ pull-up in t_{NOL1}
011 2.0kΩ pull-up in t_{NOL1}
100 4.0kΩ pull-up in t_{NOL1}
101 8.0kΩ pull-up in t_{NOL1}
110 16kΩ pull-up in t_{NOL1}
111 32kΩ pull-up in t_{NOL1}

PDR SWx Pull Down Resistor Selection Bit
000 No pull up resistor
001 0.5kΩ pull-down in t_{NOL1}
010 1.0kΩ pull-down in t_{NOL1}
011 2.0kΩ pull-down in t_{NOL1}
100 4.0kΩ pull-down in t_{NOL1}
101 8.0kΩ pull-down in t_{NOL1}
110 16kΩ pull-down in t_{NOL1}
111 32kΩ pull-down in t_{NOL1}

Table 14-1 Open/Short Register

03h~05h Open/Short Information
08h~0Ah Open/Short Information
0Dh~0Fh Open/Short Information
12h~14h Open/Short Information
17h~19h Open/Short Information
1Ch~1Eh Open/Short Information

Bit	D7:D0
Name	CS8:CS1; CS16:CS09;CS24:CS17(MSB:LSB)
Default	0000 0000

Table 14-2 Open/Short Register

06h Open/Short Information
0Bh Open/Short Information
10h Open/Short Information
15h Open/Short Information
1Ah Open/Short Information
1Fh Open/Short Information

Bit	D7:D6	D5:D0
Name	-	CS30:CS25
Default	00	00 0000

When OSDE (PG4, 00h) set to"01", open detection will be trigger once, and the open information will be store at 03h~1Fh

When OSDE (PG4, 00h) set to "10", short detection will be trigger once, and the short information will be store at 03h~1Fh

Before set OSDE, the GCC should set to 0x01.

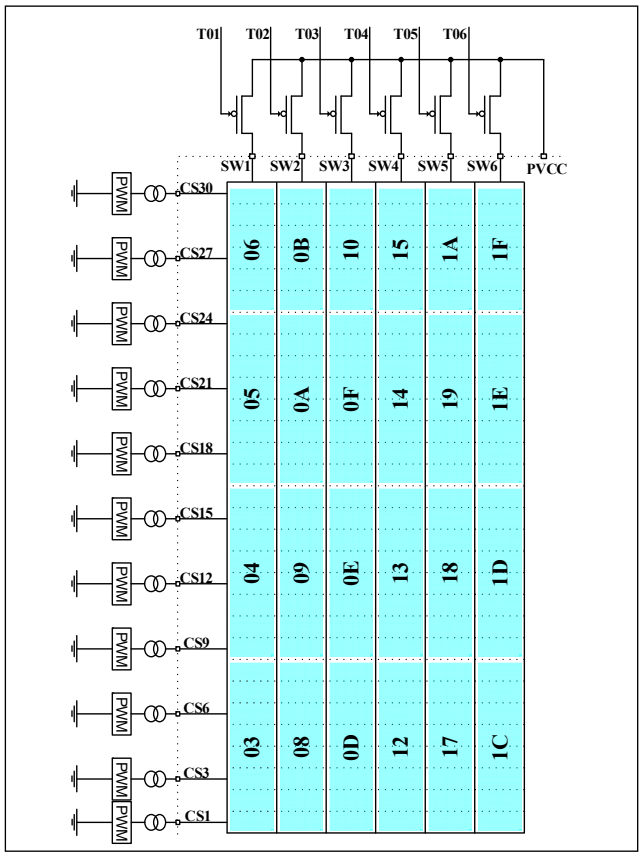


Figure 10 Open/Short Register

Table 15 36h PWM Frequency Setting Register

Bit	D7:D4	D3:D0
Name	-	PFS
Default	0000	0000

The PFS bits selects a fixed PWM operating frequency for all CSx, when PFS set “0000”, the PWM frequency is 29kHz, when PFS set to “1011”, the PWM frequency is 900Hz.

PFS	PWM Frequency Setting
0000	29kHz(default)
0011	3.6kHz
0111	1.8kHz
1011	900Hz

3Fh Reset Register

Once user writes the Reset Register with 0xAE, IS31FL3742A will reset all the IS31FL3742A registers to their default value. On initial power-up, the IS31FL3742A registers are reset to their default values for a blank display.

Table 16 41h Spread Spectrum Register

Bit	D7	D6:D5	D4:D3	D2:D0
Name	SSP	RNG	CLT	-
Default	0	00	00	00

When SSP enable, the spread spectrum function will be enabled and the RNG & CLT bits will adjust the range and cycle time of spread spectrum function.

SSP	Spread spectrum function enable
0	Disable
1	Enable

RNG	Spread spectrum range
00	±5%
01	±15%
10	±24%
11	±34%

CLT	Spread spectrum cycle time
00	1980μs
01	1200μs
10	820μs
11	660μs

APPLICATION INFORMATION

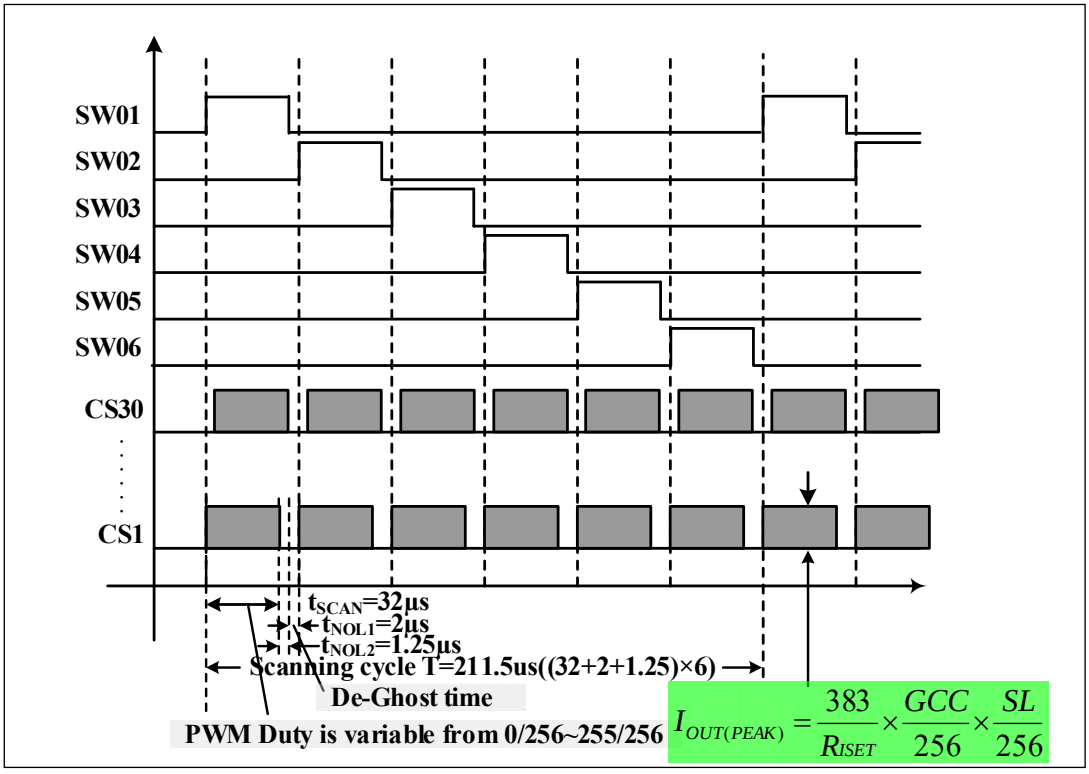


Figure 11 Scanning Timing

SCANING TIMING

As shown in Figure 12, the SW1~SW6 is turned on by serial, LED is driven 6 by 6 within the SWx (x=1~6) on time (SWx, x=1~6) is sink and pull low when LED on), including the non-overlap blanking time during scan, the duty cycle of SWx (active low, x=1~6) is:

$$Duty = \frac{32\mu s}{(32\mu s + 2\mu s + 1.25\mu s)} \times \frac{1}{6} = \frac{1}{6.61} \qquad (2)$$

Where 32μs is t_{SCAN}, the period of scanning and 2μs is t_{NOL1} and t_{NOL2}, the non-overlap time and CSx delay time.

When PFS= "0011" or others, the duty result is same.

PWM CONTROL

After setting the I_{OUT} and GCC, the brightness of each LEDs (LED average current (I_{LED})) can be modulated with 256 steps by PWM Register, as described in Formula (1).

$$I_{LED} = \frac{PWM}{256} \times I_{OUT\ (PEAK\ )} \times Duty \quad (1)$$

Where PWM is PWM Registers (PG0, 00h~B3h) data showing in Table 8.

For example, in Figure 1, if R_{ISET}= 10kΩ, PWM= 255, and GCC= 0xFF, Scaling= 0xFF, then

$$I_{OUT\,(PEAK\,)} = \frac{383}{10k\Omega} \times \frac{255}{256} \times \frac{255}{256} = 38mA$$

$$I_{LED} = 38mA \times \frac{1}{6.61} \times \frac{PWM}{256}$$

Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve a breathing effect.

GAMMA CORRECTION

In order to perform a better visual LED breathing effect we recommend using a gamma corrected PWM value to set the LED intensity. This results in a reduced number of steps for the LED intensity setting, but causes the change in intensity to appear more linear to the human eye.

Gamma correction, also known as gamma compression or encoding, is used to encode linear luminance to match the non-linear characteristics of display. Since the IS31FL3742A can modulate the brightness of the LEDs with 256 steps, a gamma correction function can be applied when computing each subsequent LED intensity setting such that the changes in brightness matches the human eye's brightness curve.

Table 17 32 Gamma Steps with 256 PWM Steps

C(0)	C(1)	C(2)	C(3)	C(4)	C(5)	C(6)	C(7)
0	1	2	4	6	10	13	18
C(8)	C(9)	C(10)	C(11)	C(12)	C(13)	C(14)	C(15)
22	28	33	39	46	53	61	69
C(16)	C(17)	C(18)	C(19)	C(20)	C(21)	C(22)	C(23)
78	86	96	106	116	126	138	149
C(24)	C(25)	C(26)	C(27)	C(28)	C(29)	C(30)	C(31)
161	173	186	199	212	226	240	255

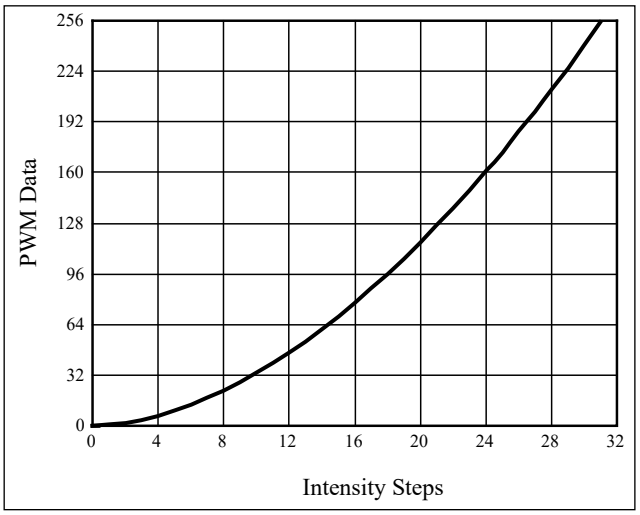


Figure 12 Gamma Correction (32 Steps)

Choosing more gamma steps provides for a more continuous looking breathing effect. This is useful for very long breathing cycles. The recommended configuration is defined by the breath cycle T. When T=1s, choose 32 gamma steps, when T=2s, choose 64 gamma steps. The user must decide the final number of gamma steps not only by the LED itself, but also based on the visual performance of the finished product.

Table 18 64 Gamma Steps with 256 PWM Steps

C(0)	C(1)	C(2)	C(3)	C(4)	C(5)	C(6)	C(7)
0	1	2	3	4	5	6	7
C(8)	C(9)	C(10)	C(11)	C(12)	C(13)	C(14)	C(15)
8	10	12	14	16	18	20	22
C(16)	C(17)	C(18)	C(19)	C(20)	C(21)	C(22)	C(23)
24	26	29	32	35	38	41	44
C(24)	C(25)	C(26)	C(27)	C(28)	C(29)	C(30)	C(31)
47	50	53	57	61	65	69	73
C(32)	C(33)	C(34)	C(35)	C(36)	C(37)	C(38)	C(39)
77	81	85	89	94	99	104	109
C(40)	C(41)	C(42)	C(43)	C(44)	C(45)	C(46)	C(47)
114	119	124	129	134	140	146	152
C(48)	C(49)	C(50)	C(51)	C(52)	C(53)	C(54)	C(55)
158	164	170	176	182	188	195	202
C(56)	C(57)	C(58)	C(59)	C(60)	C(61)	C(62)	C(63)
209	216	223	230	237	244	251	255

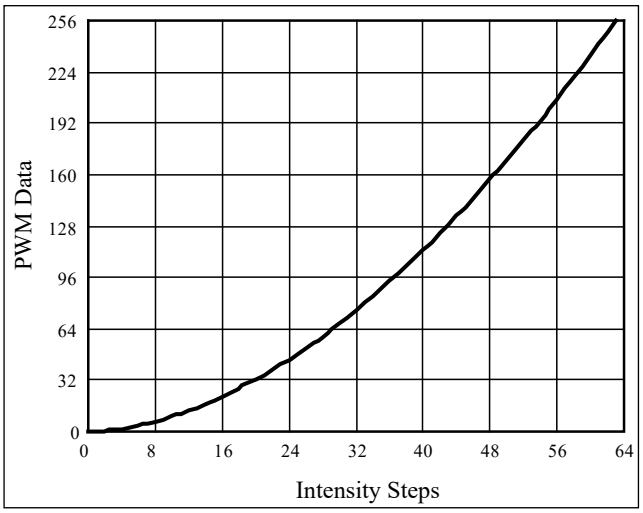


Figure 13 Gamma Correction (64 Steps)

Note: The data of 32 gamma steps is the standard value and the data of 64 gamma steps is the recommended value.

OPERATING MODE

PWM Mode

IS31FL3742A can only operate in PWM Mode. The brightness of each LED can be modulated with 256 steps by PWM registers. For example, if the data in PWM Register is “0000 0100”, then the PWM is the fourth step.

Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve a breathing effect.

DE-GHOST FUNCTION

The “ghost” term is used to describe the behavior of an LED that should be OFF but instead glows dimly when another LED is turned ON. A ghosting effect typically can occur when multiplexing LEDs. In matrix architecture any parasitic capacitance found in the constant-current outputs or the PCB traces to the LEDs may provide sufficient current to dimly light an LED to create a ghosting effect.

To prevent this LED ghost effect, the IS31FL3742A has integrated pull down resistors for each SWx (x=1~6) and pull up resistors for each CSy (y=1~30). Select the right SWx pull down resistor (PG4, 02h) and CSy pull up resistor (PG4, 02h) which eliminates the ghost LED for a particular matrix layout configuration.

Typically, selecting the 32kΩ will be sufficient to eliminate the LED ghost phenomenon.

The SWx pull down resistors and CSy pull up resistors are active only when the CSy/SWx output working the OFF state and therefore no power is lost through these resistors

SHUTDOWN MODE

Shutdown mode can be used as a means of reducing power consumption. During shutdown mode all registers retain their data.

Software Shutdown

By setting SSD bit of the Configuration Register (PG4, 00h) to “0”, the IS31FL3742A will operate in software shutdown mode. When the IS31FL3742A is in software shutdown, all current sources are switched off, so that the matrix is blanked. All registers can be operated. Typical current consume is 3μA (VCC=5V).

Hardware Shutdown

The chip enters hardware shutdown when the SDB pin is pulled low. All analog circuits are disabled during hardware shutdown, typical the current consume is 2μA.

The chip releases hardware shutdown when the SDB pin is pulled high. When set SDB high, the rising edge will reset the I2C module, but the register information retains. During hardware shutdown state Function Register can be operated.

If VCC has risk drop below 1.75V but above 0.1V during SDB pulled low, please re-initialize all Function Registers before SDB pulled high.

LAYOUT

As described in external resistor (R_{ISET}), the chip consumes lots of power. Please consider below factors when layout the PCB.

1. The VCC (PVCC, AVCC) capacitors need to close to the chip and the ground side should well connect to the GND of the chip.

2. R_{ISET} should be close to the chip and the ground side should well connect to the GND of the chip.

3. The thermal pad should connect to ground pins and the PCB should have the thermal pad too, usually this pad should have 16 or 25 via thru the PCB to other side’s ground area to help radiate the heat. About the thermal pad size, please refer to the land pattern of each package.

4. The CSy pins maximum current is 38mA (R_{ISET}=10kΩ), and the SWx pins maximum current is larger, the width of the trace, SWx should have wider trace then CSy.

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

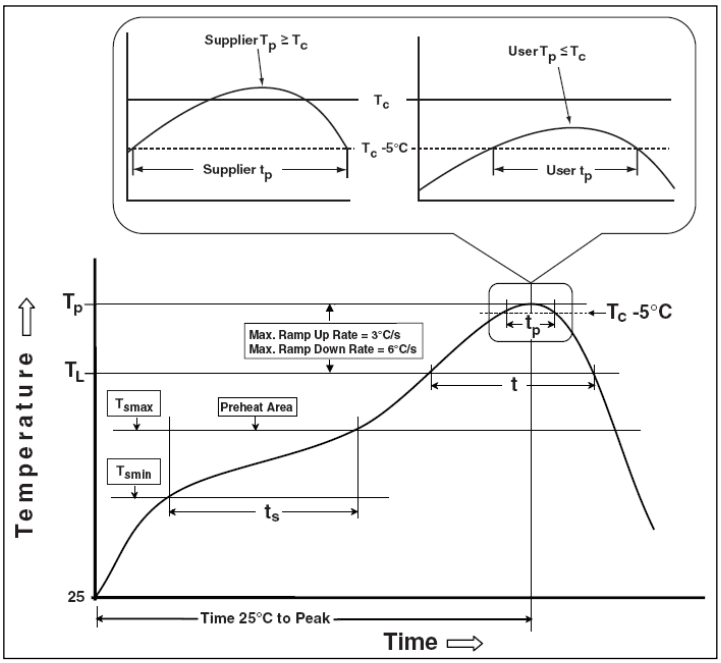
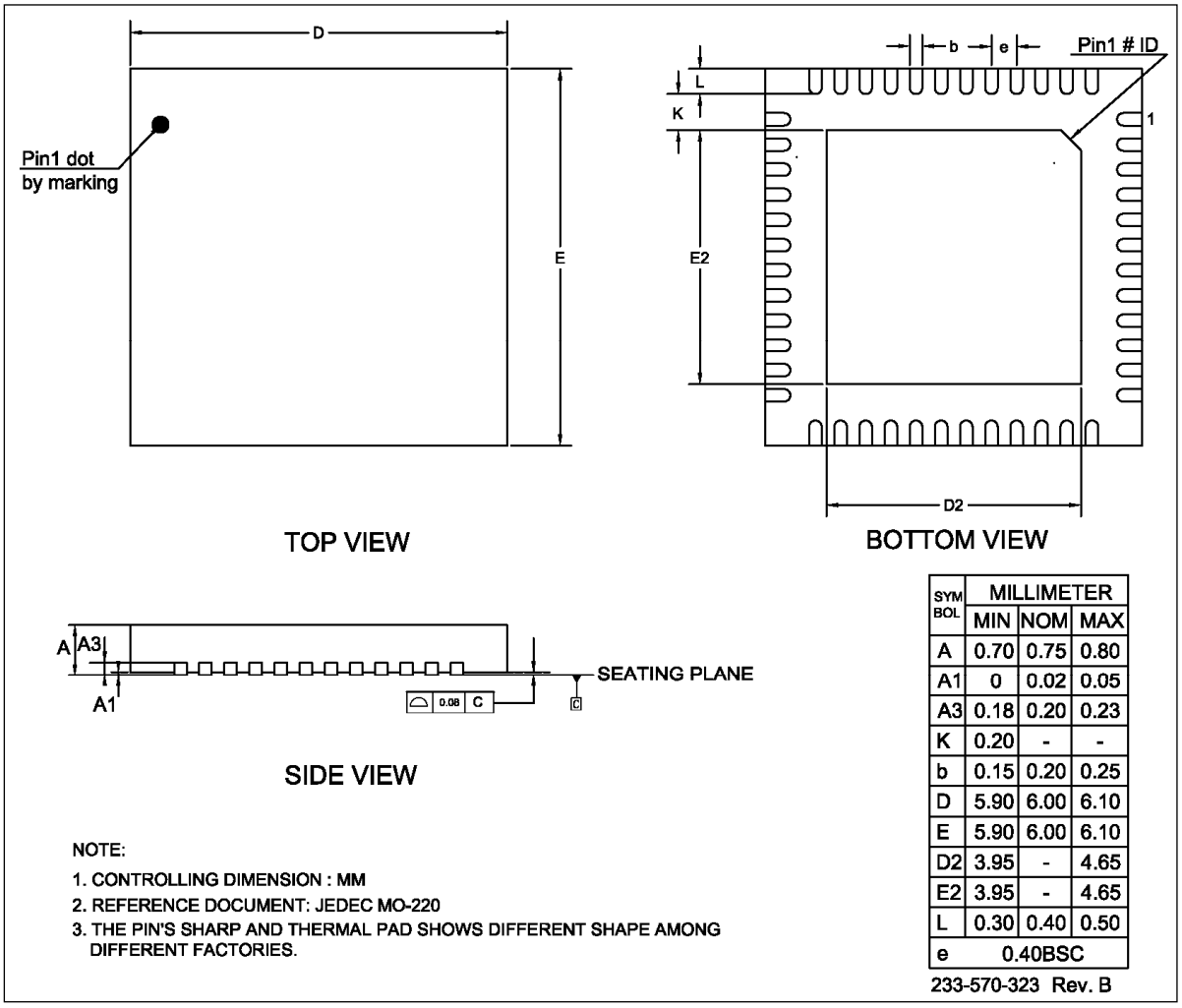


Figure 14 Classification Profile

PACKAGE INFORMATION

QFN-48



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3	0.18	0.20	0.23
K	0.20	-	-
b	0.15	0.20	0.25
D	5.90	6.00	6.10
E	5.90	6.00	6.10
D2	3.95	-	4.65
E2	3.95	-	4.65
L	0.30	0.40	0.50
e	0.40BSC		

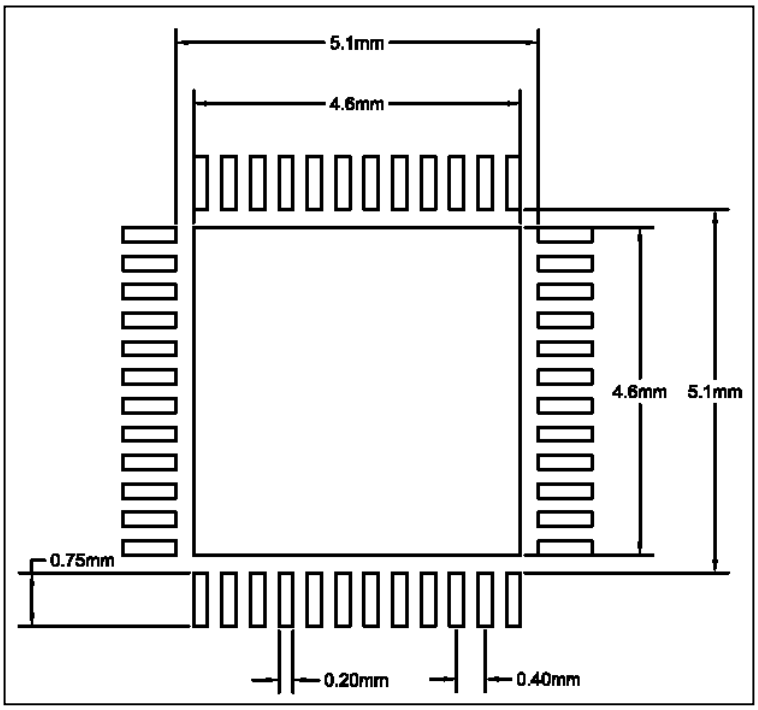
233-570-323 Rev. B

NOTE:

1. CONTROLLING DIMENSION : MM
2. REFERENCE DOCUMENT: JEDEC MO-220
3. THE PIN'S SHARP AND THERMAL PAD SHOWS DIFFERENT SHAPE AMONG DIFFERENT FACTORIES.

RECOMMENDED LAND PATTERN

QFN-48



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. user's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
A	Initial release	2019.12.16
B	1. Revise SWS bit in Table 11 2. Add scanning time in feature	2020.12.01
C	1. Correct PDR and PUR definition 2. Update t_{NOL2} describe ,Figure 10 and add “open drain” for INTB pin 3. Update to new Lumissil logo, LP, add RoHS	2024.11.06