IS31FL3716

8×7/9×6/10×5 MATRIX LED DRIVER

October 2024

GENERAL DESCRIPTION

IS31FL3716 is a general purpose 8×7 LED matrix driver. The general LED matrix display defaults to an 8×7 configuration, however, it can be configured for a 9×6, 10×n (n=5~1) dot matrix display. In matrix display, the array is internally scanned, and requires only one-time programming, thus eliminating the need for real time system resource utilization. All LED can be dimmed globally with 7-bit DC data which allowing 128 steps of linear current setting.

It programs the LED array through I2C interface, each dot of the LED array is independently programmed on or off over time.

Additionally, each LED open and short state can be detected, IS31FL3716 store the open or short information in Open-Short Registers. The Open-Short Registers allowing MCU to read out via I2C compatible interface. Inform MCU whether there are LEDs open or short and the locations of open or short LEDs.

IS31FL3716 is available in QFN-20 (3mm×3mm) and SOP-20 package. It operates from 2.7V to 5.5V over the temperature range of -40°C to +125°C.

FEATURES

- Supply voltage range: 2.7V to 5.5V
- 10 current sinks
- 1~7 power source outputs for row scan control
- 8~10 current sink outputs for column control
- Support 8×7, 9×6, 10×n (n=1~5) matrix configurations
- Individual on/off control
- 128 global current steps
- 25kHz scan frequency to minimize the MLCC capacitor audible noise
- SDB rising edge reset I2C module
- 1MHz I2C-compatible interface
- Individual open and short error detect function
- De-ghost
- QFN-20 (3mm×3mm) and SOP-20 packages
- RoHS & Halogen-Free Compliance
- TSCA Compliance

APPLICATIONS

- White goods LED display panel.
- IOT device

TYPICAL APPLICATION CIRCUIT

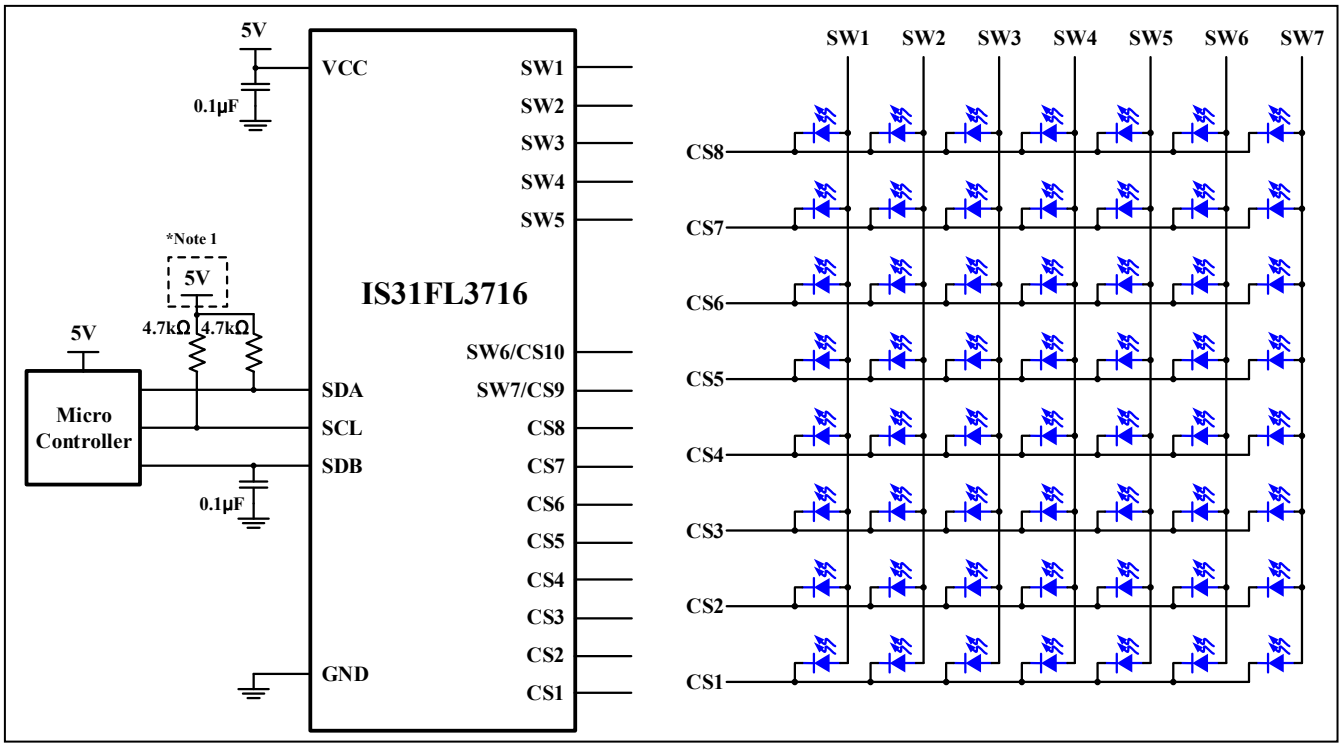


Figure 1 Typical Application Circuit (8×7)

Note 1: The V_{IH} of I2C bus should be same as V_{CC} of MCU. If V_{CC} of MCU is 3.3V, V_{IH}= 3.3V, if V_{CC} of MCU is 5V, V_{IH}= 5V.

TYPICAL APPLICATION CIRCUIT (CONTINUED)

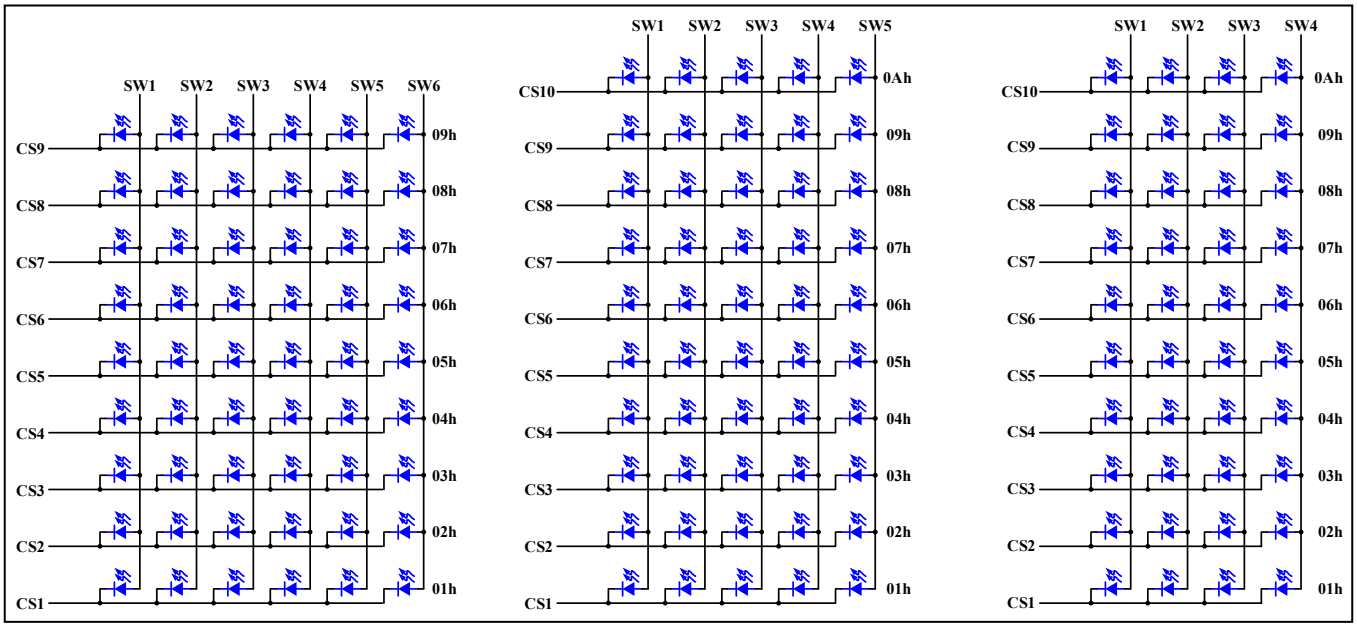


Figure 2 LED connection (9×6, 10×5, 10×4)

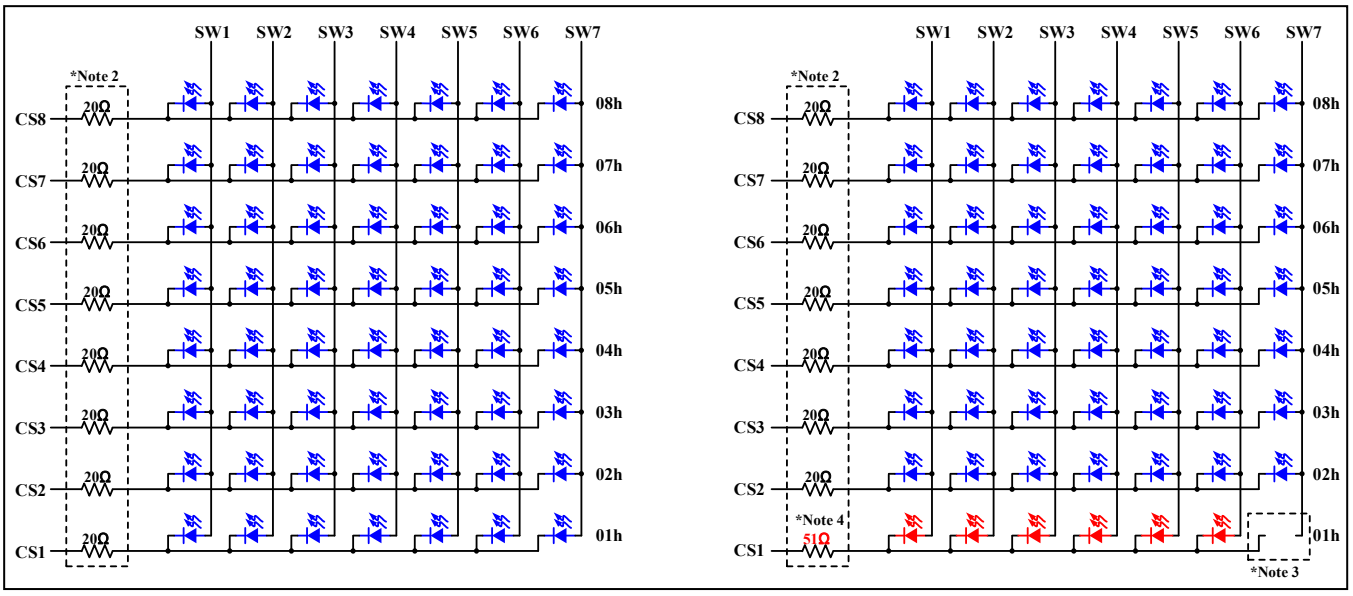


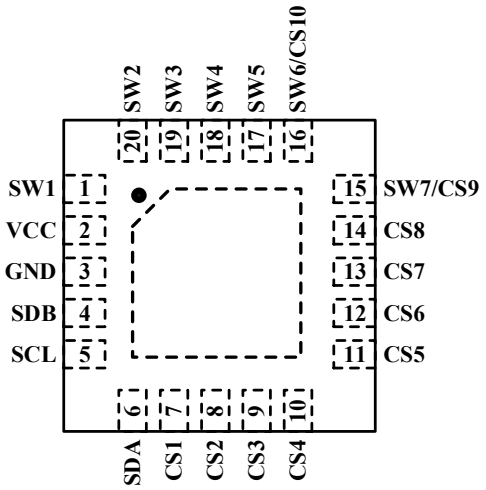
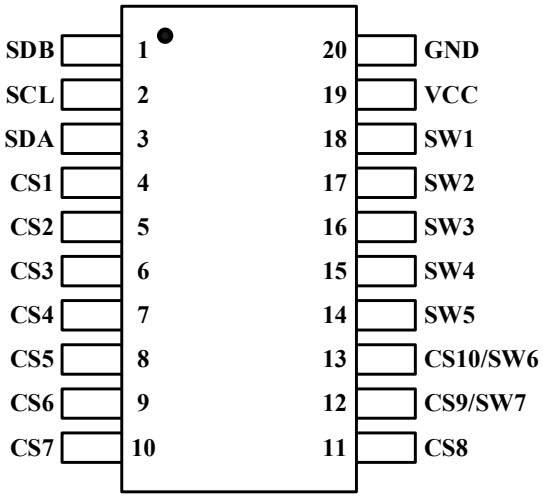
Figure 3 LED Connection With Or Without Series Resistors

Note 2: These optional resistors are for offloading the thermal dissipation (P= I^2R) away from the IS31FL3716, it is optional or 20Ω for white/blue/green LEDs, 51Ω recommended for red/yellow/orange LEDs.

Note 3: The unused LED position can be NC.

Note 4: When all LEDs in CSx are lower V_F LED, like red/yellow/orange LEDs, the series resistor can be lager to offload more thermal dissipation.

PIN CONFIGURATION

Package	Pin Configuration (Top View)
QFN-20	
SOP-20	

PIN DESCRIPTION

No.		Pin	Description
QFN-20	SOP-20		
1,20,19,18, 17,16,15	18,17,16,15, 14,13,12	SW1~SW7	Switch power source.
2	19	VCC	Power supply.
3	20	GND	Ground.
4	1	SDB	Shutdown the chip when pull to low.
5	2	SCL	Serial data.
6	3	SDA	Serial clock.
7~16	4~13	CS1~CS10	Current sinks output.
	-	Thermal Pad	Need to connect to GND pins.

ORDERING INFORMATION

Industrial Range: -40°C to +125°C

Order Part No.	Package	QTY/Reel
IS31FL3716-QFLS4-TR	QFN-20, Lead-free	2500
IS31FL3716-GRLS4-TR	SOP-20, Lead-free	1000

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	-0.3V ~+6.0V
Voltage at any input pin	-0.3V ~ V_{CC}+0.3V
Maximum junction temperature, T_{JMAX}	+150°C
Storage temperature range, T_{STG}	-65°C ~+150°C
Operating temperature range, T_A=T_J	-40°C ~ +125°C
Package thermal resistance, junction to ambient (4-layer standard test PCB based on JESD 51-2A), θ_{JA}	57.6°C/W (QFN) 64.2°C/W (SOP)
ESD (HBM) ESD (CDM)	±8kV ±750V

Note 5: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

The following specifications apply for V_{CC}= 5V, T_A= 25°C, unless otherwise noted.

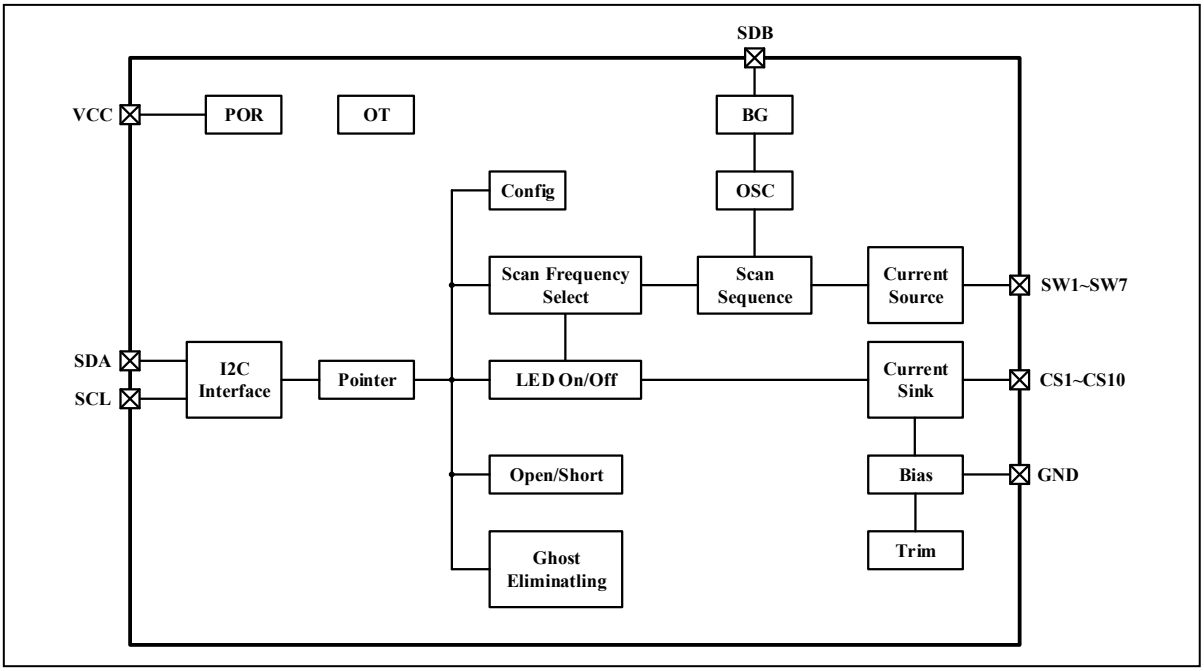
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage		2.7		5.5	V
I_{CC}	Quiescent power supply current	V_{SDB}= V_{CC}, all LEDs off		1.1	1.5	mA
I_{SD}	Shutdown current	V_{SDB}= 0V		1	2	μA
I_{OUT}	Constant current of CSx	I_{SINK}= 40mA	37.6	40	42.4	mA
V_{HR}	Current switch headroom voltage SWx	I_{SWITCH}= 400mA		300	400	mV
	Current sink headroom voltage CSx	I_{SINK}= 40mA		490	600	
ΔI_{MAT}	Between channels		-4		4	%
t_{SCAN_SW}	Period of scanning (single SWx only)	SFS= "001" (25kHz)	4	5	6	μs
t_{NOL1}	Non-overlap blanking time during scan, the SWx and CSy are all off during this time	SFS= "001" (25kHz), DT= "00"	0.12	0.18	0.3	μs
t_{NOL2}	Delay total time for CS1 to CS10, during this time, the SWx is on but CSy is not all turned on	SFS= "001" (25kHz) (Note 6)		0.01		μs
Logic Electrical Characteristics (SDA, SCL, SDB)						
V_{IL}	Logic "0" input voltage	V_{CC}= 2.7V~5.5V	GND		0.3V_{CC}	V
V_{IH}	Logic "1" input voltage	V_{CC}= 2.7V~5.5V	0.5V_{CC}		V_{CC}	V
V_{HYS}	Input Schmitt trigger hysteresis	V_{CC}= 3.6V		0.2		V
I_{IL}	Logic "0" input current	SDB= L, V_{INPUT}= L (Note 6)		5		nA
I_{IH}	Logic "1" input current	SDB= L, V_{INPUT}= H (Note 6)		5		nA

DIGITAL INPUT I2C SWITCHING CHARACTERISTICS (NOTE 6)

Symbol	Parameter	Fast Mode			Fast Mode Plus			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{SCL}	Serial-clock frequency	-		400	-		1000	kHz
t_{BUF}	Bus free time between a STOP and a START condition	1.3		-	0.5		-	μs
$t_{HD, STA}$	Hold time (repeated) START condition	0.6		-	0.26		-	μs
$t_{SU, STA}$	Repeated START condition setup time	0.6		-	0.26		-	μs
$t_{SU, STO}$	STOP condition setup time	0.6		-	0.26		-	μs
$t_{HD, DAT}$	Data hold time	-		-	-		-	μs
$t_{SU, DAT}$	Data setup time	100		-	50		-	ns
t_{LOW}	SCL clock low period	1.3		-	0.5		-	μs
t_{HIGH}	SCL clock high period	0.7		-	0.26		-	μs
t_R	Rise time of both SDA and SCL signals, receiving	-		300	-		120	ns
t_F	Fall time of both SDA and SCL signals, receiving	-		300	-		120	ns

Note 6: Guaranteed by design.

FUNCTIONAL BLOCK DIAGRAM



DETAILED DESCRIPTION

I2C INTERFACE

The IS31FL3716 uses a serial bus, which conforms to the I2C protocol, to control the chip's functions with two wires: SCL and SDA. The IS31FL3716 has a 7-bit slave address (A7:A1), followed by the R/W bit, A0. Set A0 to "0" for a write command and set A0 to "1" for a read command. The complete slave address is:

Table 1 Slave Address (Write only):

Bit	A7:A1	A0
Value	1011010	0

The SCL line is uni-directional. The SDA line is bi-directional (open-drain) with a pull-up resistor (typically 400kHz I2C with 4.7kΩ, 1MHz I2C with 2kΩ). The maximum clock frequency specified by the I2C standard is 1MHz. In this discussion, the master is the microcontroller and the slave is the IS31FL3716.

The timing diagram for the I2C is shown in Figure 4. The SDA is latched in on the stable high level of the SCL. When there is no interface activity, the SDA line should be held high.

The "START" signal is generated by lowering the SDA signal while the SCL signal is high. The start signal will alert all devices attached to the I2C bus to check the incoming address against their own chip address.

The 8-bit chip address is sent next, most significant bit first. Each address bit must be stable while the SCL level is high.

After the last bit of the chip address is sent, the master checks for the IS31FL3716's acknowledge. The master releases the SDA line high (through a pull-up resistor). Then the master sends an SCL pulse. If the IS31FL3716 has received the address correctly, then it holds the SDA line low during the SCL pulse. If the SDA line is not low, then the master should send a "STOP" signal (discussed later) and abort the transfer.

Following acknowledge of IS31FL3716, the register address byte is sent, most significant bit first. IS31FL3716 must generate another acknowledge indicating that the register address has been received.

Then 8-bit of data byte are sent next, most significant bit first. Each data bit should be valid while the SCL level is stable high. After the data byte is sent, the IS31FL3716 must generate another acknowledge to indicate that the data was received.

The "STOP" signal ends the transfer. To signal "STOP", the SDA signal goes high while the SCL signal is high.

ADDRESS AUTO INCREMENT

To write multiple bytes of data into IS31FL3716, load the address of the data register that the first data byte is intended for. During the IS31FL3716 acknowledge of receiving the data byte, the internal address pointer will increment by one. The next data byte sent to IS31FL3716 will be placed in the new address, and so on. The auto increment of the address will continue as long as data continues to be written to IS31FL3716 (Figure 7).

READING OPERATION

Most of the registers can be read.

To read the register, after I2C start condition, the bus master must send the IS31FL3716 device address with the R/$\overline{W}$ bit set to "0", followed by the register address which determines which register is accessed. Then restart I2C, the bus master should send the IS31FL3716 device address with the R/$\overline{W}$ bit set to "1". Data from the register defined by the command byte is then sent from the IS31FL3716 to the master (Figure 8).

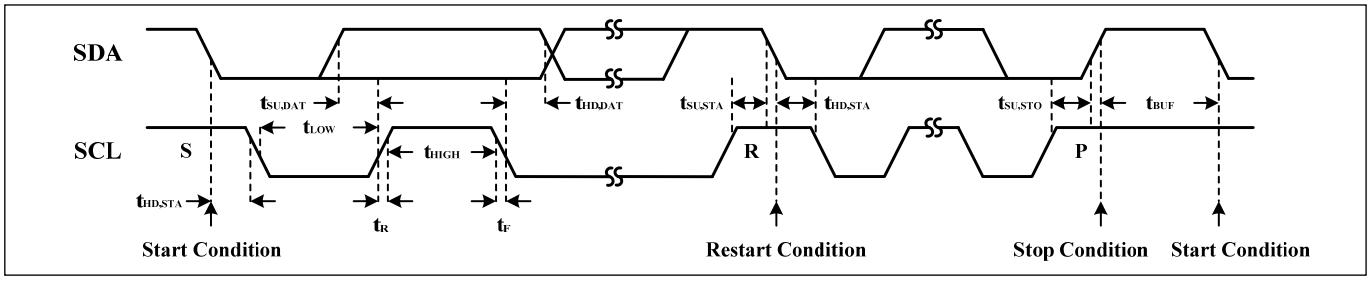


Figure 4 I2C Interface Timing

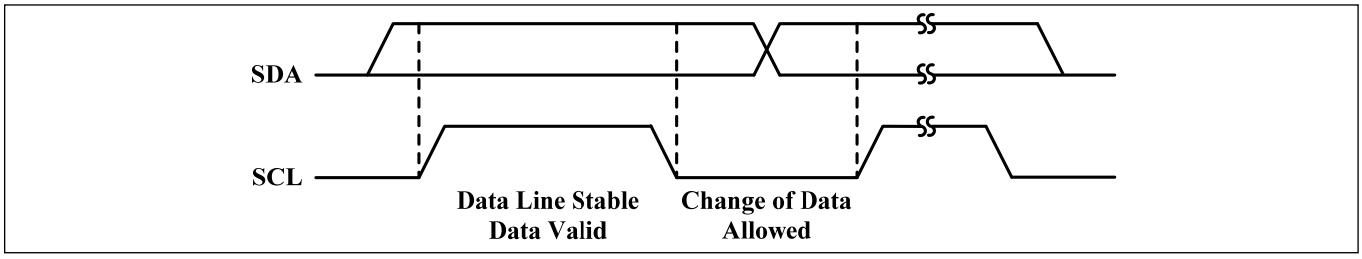


Figure 5 I2C Bit Transfer

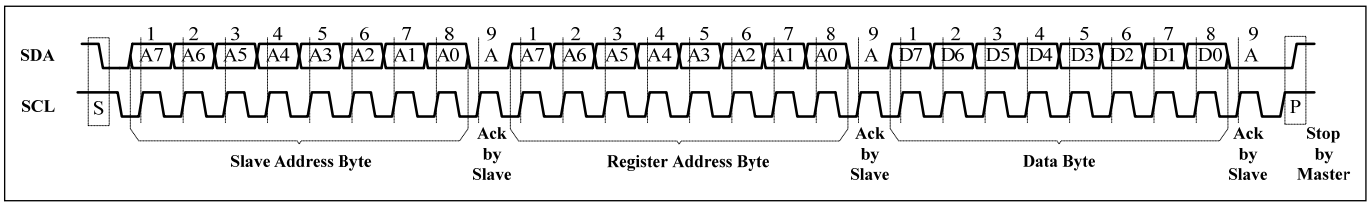


Figure 6 I2C Writing to IS31FL3716 (Typical)

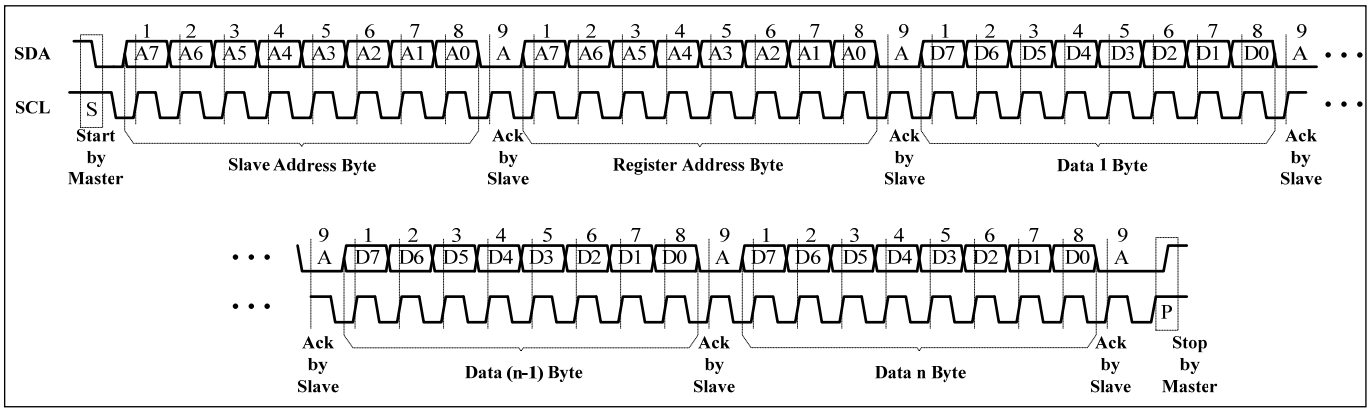


Figure 7 I2C Writing to IS31FL3716 (Automatic Address Increment)

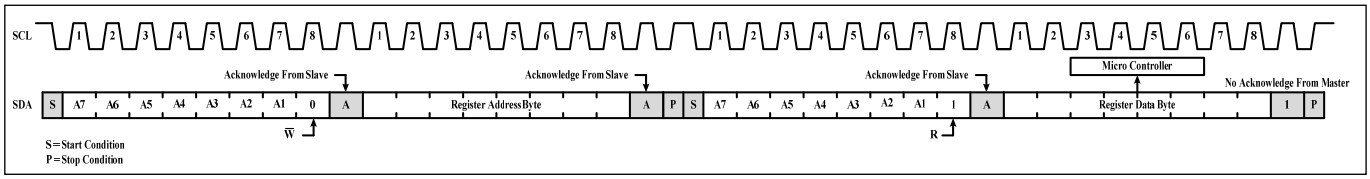


Figure 8 I2C Reading from IS31FL3716

Table 2 Register Definition

Address	Name	Function	Table	R/W	Default
00h	Configuration Register	Configure the operation mode	3	R/W	0000 0001
01h~0Ah	On Off Control Register	Set On off value for LED	4	R/W	0000 0000
0Bh	GCC, Global Current Control	Maximum current of all CSx pins	5	R/W	0111 1111
0Ch	Deghost Options/ Scan Frequency Register	Set deghost pull voltage option Set the scan frequency	6	R/W	0000 0001
0Dh	Open/Short EN Register	Enable open/short detect	-	W	0000 0000
0Eh	Open/Short Register	Store the short information (CS1~CS10)	7	R	0000 0000

Table 3 00h Configuration Register

Bit	D7	D6:D4	D3:D2	D1	D0
Name	PSMD	SWS	DT	-	SSD
Default	0	000	00	0	1

The Configuration Register sets operation mode of IS31FL3716.

SSD Software Shutdown Enable

0 shutdown mode
1 normal operation mode

PSMD Power Save Mode Disable

0 power save mode enable
1 power save mode disable

DT Deghost Time

00/11 1.5 clock time
01 3.5 clock time
10 5.5 clock time

SWS SWx Setting

000 8×7 display mode, SWS=1/7
001 9×6 display mode, SWS=1/6
010 10×5 display mode, SWS=1/5
011 10×4 display mode, SWS=1/4
100 10×3 display mode, SWS=1/3
101 10×2 display mode, SWS=1/2
110 10×1 display mode, SWS=1
111 8×7 display mode, SWS=1/7

Table 4 01h~0Ah On Off Control Register (CS1~CS10)

Bit	D7	D6:D0
Name	-	SW7:SW1
Default	-	000 0000

The on off control registers store the on or off state of each LED in the array.

SWx LED State

0 LED off
1 LED on

10 registers are assigned to CS1~CS10 rows respectively; the LED at a particular (CSy, SWx) location will be turned on when the respective data is set to 1. When configured to other than 8×7 dot matrix display mode operation, only the required number of LSBs is used in each row register. For example, in 10×5 dot matrix display mode, only bits SW5 through SW1 are used, and bits SW8 through SW6 are ignored.

Table 5 0Bh GCC Register

Bit	D7	D6:D0
Name	MAX	GCC
Default	0	111 1111

The Global Current Control Register modulates all LEDs DC current which is noted as $I_{OUT(PEAK)}$ in more than 128 steps.

Note that the $I_{OUT(PEAK)}$ should be limited in 70mA.

MAX I_{OUT} Maximum Setting

0 $I_{OUT(MAX)}$= 40mA (V_{CC}= 2.7V~5.5V)
1 $I_{OUT(MAX)}$= 120mA (V_{CC}= 4.0V~5.5V)

$I_{OUT(PEAK)}$ computed by Formula (1):

$$I_{OUT(PEAK)} = I_{OUT(MAX)} \times \frac{GCC}{128} \qquad (1)$$

$$GCC = \sum_{n=0}^{6} D[n] \cdot 2^n$$

Where $I_{OUT(MAX)}$ is 40mA when D7 of 0Bh is set to "0", (default, 40mA), and it is 120mA when D7 is set to "1".

According to formula (1), when 0Bh is 0x00~0x7F, the $I_{OUT(PEAK)}$ is 0mA to 40mA, when MAX bit is set to "1", if 0Bh is 0x80~0xCA, the $I_{OUT(PEAK)}$ is 0mA to 70mA, recommend value for 0Bh is 0x00~0x7F, 0xAB~0xCA, other values are not recommended.

0x00	$I_{OUT(PEAK)}$ =0mA
0x01	$I_{OUT(PEAK)}$ =40mA/127 (not recommend when scan frequency is 25kHz and 12.5kHz)
0x02	$I_{OUT(PEAK)}$ =40mA×2/127
…	
0x7F(127)	$I_{OUT(PEAK)}$ =40mA
0xAB(171)	$I_{OUT(PEAK)}$ =40.63mA
0xAC(172)	$I_{OUT(PEAK)}$ =41.57mA
…	
0xBF(191)	$I_{OUT(PEAK)}$ =59.53mA
…	
0xCA(202)	$I_{OUT(PEAK)}$ =70mA
>0xCA	Not allowed

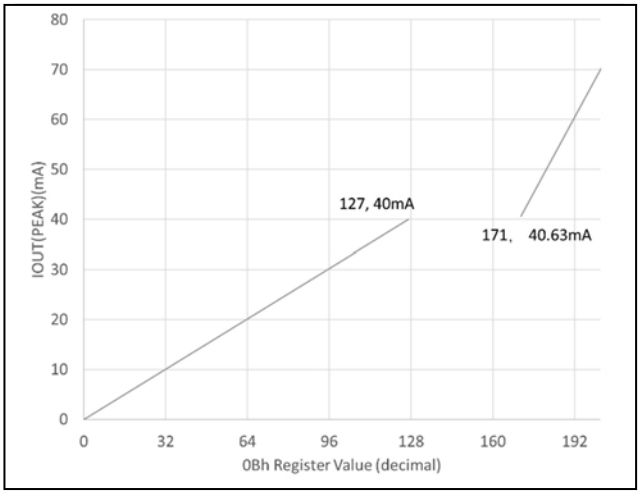


Figure 9 $I_{OUT(PEAK)}$ vs. 0Bh Register Value

The average current of each LED noted I_{LED}. I_{LED} computed by Formula (2):

$$I_{LED} = I_{OUT(PEAK)} \times Duty \qquad (2)$$

SWS=1/7: $$Duty = \frac{(5.3-0.01)\mu s}{(5.3+0.4)\mu s} \times \frac{1}{7} = \frac{1}{7.54} \qquad (3\text{-}1)$$

SWS=1/6: $$Duty = \frac{(5.3-0.01)\mu s}{(5.3+0.4)\mu s} \times \frac{1}{6} = \frac{1}{6.47} \qquad (3\text{-}2)$$

…

Duty is the duty cycle of SWx, see SCANING TIMING section for more information.

For example: if $I_{OUT(PEAK)}$= 40mA, SWS= 1/7:

$$I_{LED} = 40mA \times \frac{1}{7.54} = 5.31mA$$

Table 6 0CH Scan Frequency Register

Bit	D7:D6	D5:D4	D3	D2:D0
Name	PUS	PDS	DGENB	SFS
Default	00	00	0	001

The Scan Frequency Register configure the scan frequency of SWx and deghost function if IS31FL3716.

The "ghost" term is used to describe the behavior of an LED that should be OFF but instead glows dimly when another LED is turned ON. A ghosting effect typically can occur when multiplexing LEDs. In matrix architecture any parasitic capacitance found in the constant-current outputs or the PCB traces to the LEDs may provide sufficient current to dimly light an LED to create a ghosting effect.

To prevent this LED ghost effect, the IS31FL3716 has integrated Pull down voltage setting for each SWx (x=1~7) and Pull up voltage setting for each CSy (y=1~10). Select the right SWx Pull down voltage (0Ch) and CSy Pull up voltage (0Ch) which eliminates the ghost LED for a particular matrix layout configuration, selecting the voltage setting will be sufficient to eliminate the LED ghost phenomenon. Recommend setting is

SWPD= 2.2V, CSPU= V_{CC}-2.2V

(Reverse voltage of LED is around -2.6V)

Higher value of SWPD and CSPU will have stronger pull ability to LED and may let LED have higher reverse voltage.

When IS31FL3716 works in hardware shutdown mode, the de-ghost function should be disabled.

SFS	Scan Frequency of SWx, SW1~SWn
000	25kHz
001	25kHz (default)
010	12.5kHz
011	4kHz
100	2kHz
101	1kHz
110	500Hz
111	250Hz

DGENB	De-Ghost Disable Bit
0	Enable
1	Disable

PDS	Swx Pull Down Select
00	2.2V(default)
01	1.4V
10	0.6V
11	GND

PUS	Csy Pull Up Select
00	V_{CC}-2.2V (default)
01	V_{CC}-1.4V
10	V_{CC}-0.6V
11	V_{CC}

Table 7 0EH Open Short Register

Bit	D7	D6:D0
Name	-	OP/ST: SW7:SW1
Default	0	000000

The open short register stores the on or off state of each LED in the array.

When 0Dh is set to:

0001 0101	Select CS1 LED open detect enable
0010 0101	Select CS2 LED open detect enable
0011 0101	Select CS3 LED open detect enable
0100 0101	Select CS4 LED open detect enable
0101 0101	Select CS5 LED open detect enable
0110 0101	Select CS6 LED open detect enable
0111 0101	Select CS7 LED open detect enable
1000 0101	Select CS8 LED open detect enable
1001 0101	Select CS9 LED open detect enable
1010 0101	Select CS10 LED open detect enable

When 0Dh is set to:

0001 0110	select CS1 LED SHORT EN
0010 0110	select CS2 LED SHORT EN
0011 0110	select CS3 LED SHORT EN
0100 0110	select CS4 LED SHORT EN
0101 0110	select CS5 LED SHORT EN
0110 0110	select CS6 LED SHORT EN
0111 0110	select CS7 LED SHORT EN
1000 0110	select CS8 LED SHORT EN
1001 0110	select CS9 LED SHORT EN
1010 0110	select CS10 LED SHORT EN

After setting 0Dh, 0Eh can be read for the open or short information of each LED dot. 0Dh need to set to 0x00 before another set to enable open or short test.

APPLICATION INFORMATION

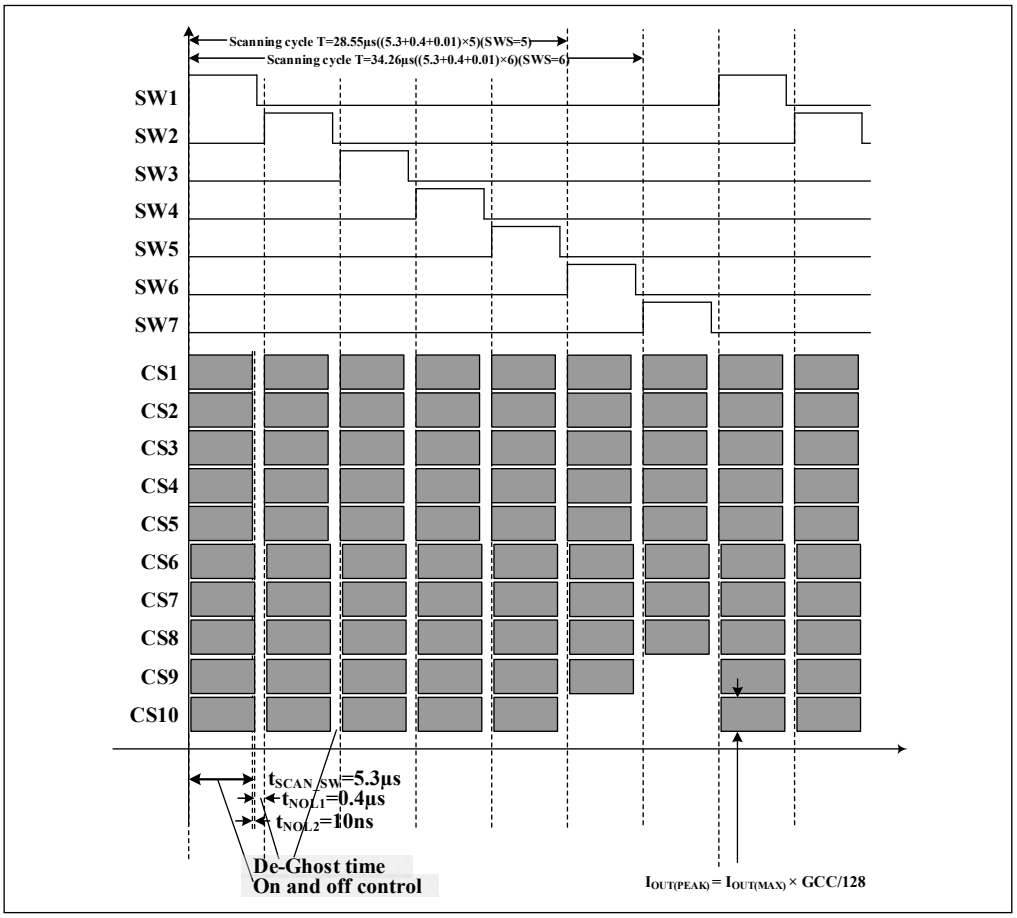


Figure 10 8×7 Scanning Timing

SCANING TIMING

As shown in Figure 10 above, the SWy (y=1~7) work as power source and turned on by serial, LED is driven within the CSx (x=1~10) on time (SWy is source and it is high when LED on), including the non-overlap blanking time during scan, the duty cycle of SWy (active high, y=1~7) is:

SWS=1/7: $$Duty = \frac{(5.3-0.01)\mu s}{(5.3+0.4)\mu s} \times \frac{1}{7} = \frac{1}{7.54} \quad (3\text{-}1)$$

SWS=1/6: $$Duty = \frac{(5.3-0.01)\mu s}{(5.3+0.4)\mu s} \times \frac{1}{6} = \frac{1}{6.47} \quad (3\text{-}2)$$

…

Where 5.3μs is t_{SCAN_SW}, the period of scanning and 0.4μs is t_{NOL1}, the non-overlap time and 0.01μs is the CSx delay time.

LED AVERAGE CURRENT (I_{LED})

The output current for each CSx can be can be set by GCC register.

$I_{OUT(PEAK)}$ computed by Formula (1):

$$I_{OUT(PEAK)} = I_{OUT(MAX)} \times \frac{GCC}{128} \quad (1)$$

$$GCC = \sum_{n=0}^{6} D[n] \cdot 2^n$$

Where $I_{OUT(MAX)}$ is 40mA when D7 of 0Bh is set to “0”, (default, 40mA), and it is 120mA when D7 is set to “1”.

According to formula (1), when 0Bh is 0x00~0x7F, the $I_{OUT(PEAK)}$ is 0mA to 40mA, when MAX bit is set to “1”, if 0Bh is 0x80~0xCA, the $I_{OUT(PEAK)}$ is 0mA to 70mA, recommend value for 0Bh is 0x00~0x7F, 0xAB~0xCA, other values are not recommended.

Note that the $I_{OUT(PEAK)}$ should be limited in 70mA.

For example, if GCC= 120, SWS=1/7, then

$$I_{OUT(PEAK)} = \frac{120}{128} \times 40 \times \frac{1}{7.54} = 4.97mA$$

Another example, if GCC=127, SWS=1/6, then

$$I_{OUT(PEAK)} = \frac{127}{128} \times 40 \times \frac{1}{6.47} = 6.13mA$$

OPEN/SHORT DETECT FUNCTION

IS31FL3716 has open and short detect bit for each LED.

After setting 0Dh, 0Eh can be read for the open or short information of each LED dot. 0Dh need to set to 0x00 before another set to enable open or short test.

In order to have accurate open and short result, before open or short enable, the GCC should set to 0x0F.

DE-GHOST FUNCTION

The “ghost” term is used to describe the behavior of an LED that should be OFF but instead glows dimly when another LED is turned ON. A ghosting effect typically can occur when multiplexing LEDs. In matrix architecture any parasitic capacitance found in the constant-current outputs or the PCB traces to the LEDs may provide sufficient current to dimly light an LED to create a ghosting effect.

To prevent this LED ghost effect, the IS31FL3716 has integrated Pull down voltage setting for each SWx (x=1~7) and Pull up voltage setting for each CSy (y=1~10). Select the right SWx Pull down voltage (0Ch) and CSy Pull up voltage (0Ch) which eliminates the ghost LED for a particular matrix layout configuration, selecting the voltage setting will be sufficient to eliminate the LED ghost phenomenon. Recommend setting is

SWPD= 2.2V, CSPU= V_{CC}-2.2V

(Reverse voltage of LED is around -2.6V)

Higher value of SWPD and CSPU will have stronger pull ability to LED and may let LED have higher reverse voltage.

When IS31FL3716 works in hardware shutdown mode, the de-ghost function should be disabled.

I2C RESET

The I2C will be reset if the SDB pin is pull-high from 0V to logic high, at the operating SDB rising edge, the interface operation is not allowed.

SHUTDOWN MODE

Shutdown mode can be used as a means of reducing power consumption. During shutdown mode all registers retain their data.

Software Shutdown

By setting the SSD bit of the Control Register (00h) to “0”, the IS31FL3716 will operate in software shutdown mode. When the IS31FL3716 is in software shutdown, all current sources are switched off, so the LEDs are OFF but all registers accessible. Typical current consume is 2μA (V_{CC}=5V).

Hardware Shutdown

The chip enters hardware shutdown when the SDB pin is pulled low. All analog circuits are disabled during hardware shutdown typical the current consumption is 2μA (V_{CC}=5V).

The chip releases hardware shutdown when the SDB pin is pulled high. The rising edge of SDB pin will reset the I2C module, but the register information retains. During hardware shutdown the registers are accessible.

If the VCC supply drops below 1.75V but remains above 0.1V during SDB pulled low, please re-initialize all Registers before SDB pulled high.

LAYOUT GUIDE

The IS31FL3716 consumes lots of power so good PCB layout will help improve the reliability of the chip. Please consider below factors when layout the PCB.

Power Supply Lines

When designing the PCB layout pattern, the first step should consider about the supply line and GND connection, especially those traces with high current, also the digital and analog blocks’ supply line and GND should be separated to avoid the noise from digital block affect the analog block.

At least one 0.1μF capacitor, if possible with a more 1μF capacitor is recommended to connected to the ground at power supply pin of the chip, and it needs to close to the chip and the ground net of the capacitor should be well connected to the GND plane.

Thermal Consideration

The over temperature of the chip may result in deterioration of the properties of the chip. The thermal pad of IS31FL3716 QFN package should connect to GND net and need to use 4 or 9 vias connect to GND copper area, the GND area should be as large area as possible to help radiate the heat from the IS31FL3716.

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

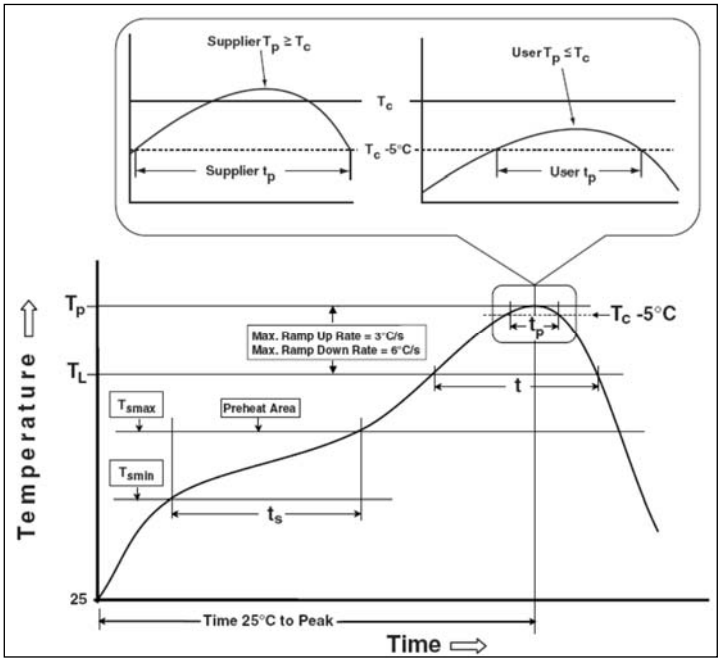
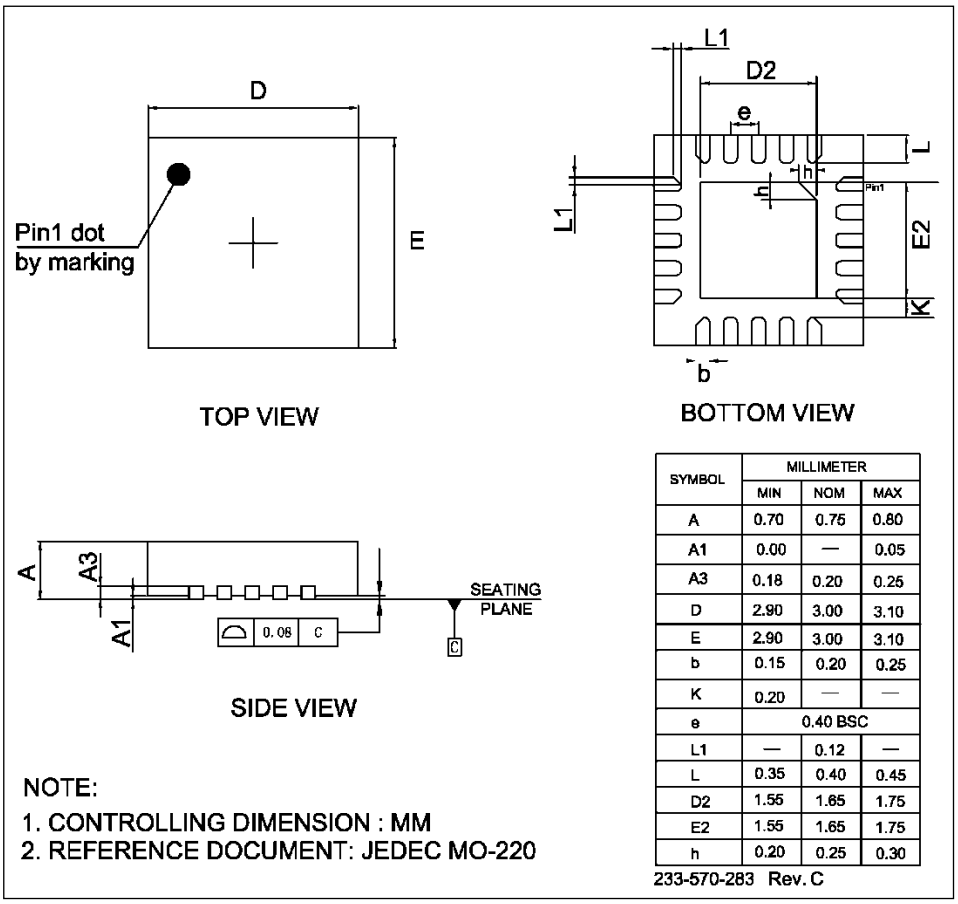


Figure 11 Classification Profile

PACKAGE INFORMATION

QFN-20



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	—	0.05
A3	0.18	0.20	0.25
D	2.90	3.00	3.10
E	2.90	3.00	3.10
b	0.15	0.20	0.25
K	0.20	—	—
e	0.40 BSC		
L1	—	0.12	—
L	0.35	0.40	0.45
D2	1.55	1.65	1.75
E2	1.55	1.65	1.75
h	0.20	0.25	0.30

NOTE:
1. CONTROLLING DIMENSION : MM
2. REFERENCE DOCUMENT: JEDEC MO-220

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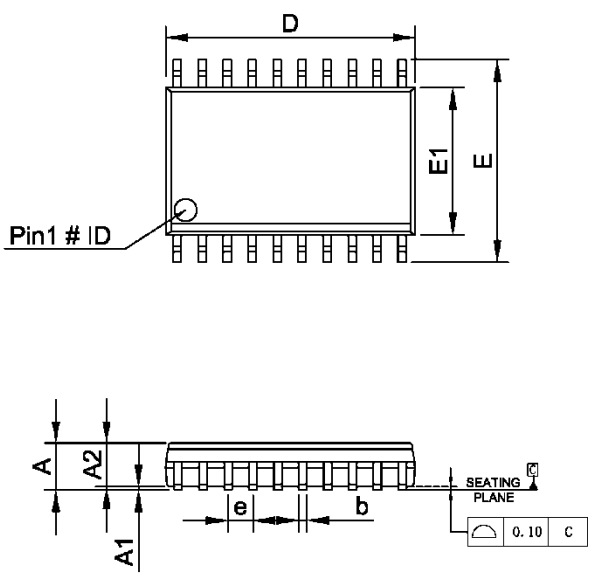
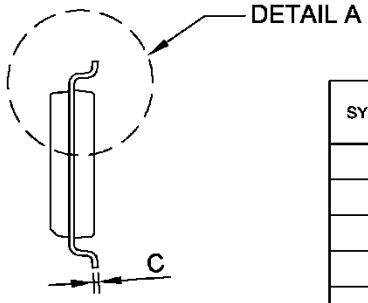
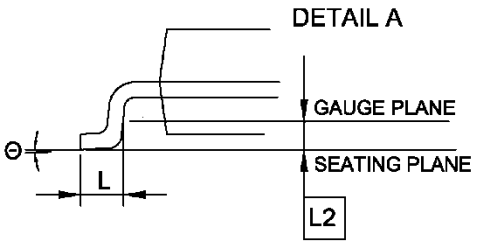






SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	–	–	2.65
A1	0.10	–	0.30
A2	2.05	–	–
E1	7.40	7.50	7.60
E	10.10	10.30	10.61
D	12.5	12.8	13.0
b	0.31	–	0.51
e	1.27BSC		
L	0.40	–	1.27
L2	0.25BSC		
θ	0°	–	8°
C	0.20	–	0.33

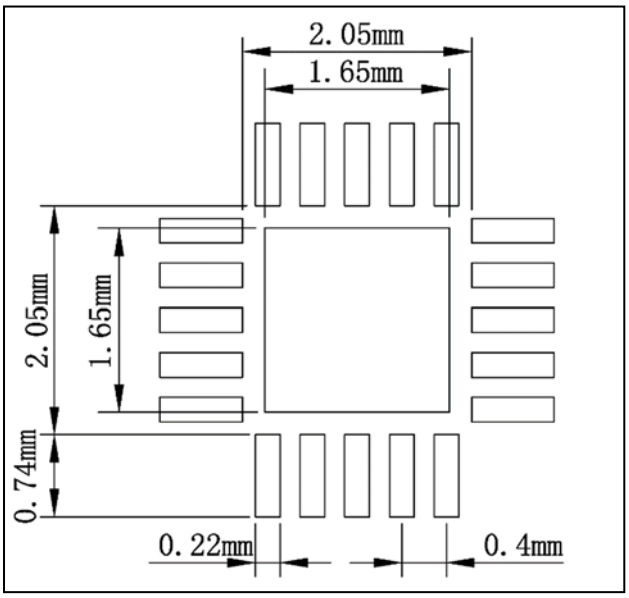
233-570-397 Rev. A

NOTE :

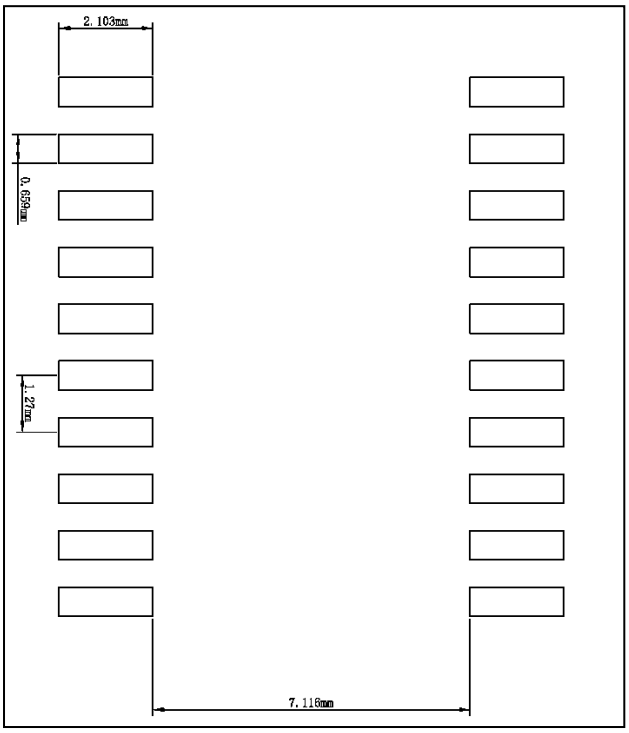
1. CONTROLLING DIMENSION : MM
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3. REFERENCE DOCUMENT: JEDEC MS-013
4. THE SHAPE OF BODY SHOW DIFFERENT SHAPE AMONG DIFFERENT FACTORIES.

RECOMMENDED LAND PATTERN

QFN-20



SOP-20



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. User's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
A	Initial release	2021.11.10
B	Update to new Lumissil logo and add RoHS	2024.10.10