IS31FL3293

1-RGB/3-LED DRIVER

May 2024

GENERAL DESCRIPTION

The IS31FL3293 is a 3 LED current sink LED driver programmed via 1MHz I2C compatible interface. Each LED can be dimmed individually with 4096 steps PWM data and each current sink has 8-bit DC current level scaling (Color Calibration) data which allowing 4096 steps of linear PWM dimming and 256 steps of DC current adjustable level.

The IS31FL3293 operates from 2.7V to 5.5V and features a very low shutdown and operational current.

The IS31FL3293 can operate in either "Current Level & PWM mode" or "Pattern" mode. In Current Level & PWM mode, the output current of each output is independently programmed and controlled in 256 steps to achieve color mixing and the PWM duty cycle of each output is also independently programmed and controlled in 4096 steps to simplify color mixing or for smoothly diming control. In Pattern mode, the timing characteristics for RGB channels output can be individually adjusted to maintain a pre-established pattern sequence without requiring any additional MCU interaction, thus saving valuable system resources.

IS31FL3293 is available in UTQFN-9 (1.5mm × 1.5mm) package. It operates from 2.7V to 5.5V over the temperature range of -40°C to +125°C.

FEATURES

- Supply voltage range: 2.7V to 5.5V
- 3 current sinks, I_{OUT}= 20mA (Max.)
- Ultra-low operational current (90μA Typ. at V_{CC}= 3.6V, all LED off)
- Accurate color rendition
  - 12-bit PWM/channel
  - 8-bit Current Level/channel
  - 6-bit global DC current adjust
- SDB rising edge reset I2C module
- 1MHz I2C-compatible interface
- ±5% accuracy and mismatch @I_{OUT}= 20mA and I_{OUT}= 3mA
- Auto breath function:
  - Auto breath pattern for 3 channels and each channel can quit the pattern and control by CL&PWM
  - Fade in/ fade out time length max value up to 9.96s.
  - Single Pulse/Multi pulse/manual control modes for auto breath
  - 3 color pre-configure pattern registers for color breath
- UTQFN-9 (1.5mm × 1.5mm) package
- RoHS & Halogen-Free Compliance
- TSCA Compliance

APPLICATIONS

- Hand-held devices for LED display
- Logo LED (Mouse, TWS etc.)
- IOT device (AI speaker etc.)

TYPICAL APPLICATION CIRCUIT

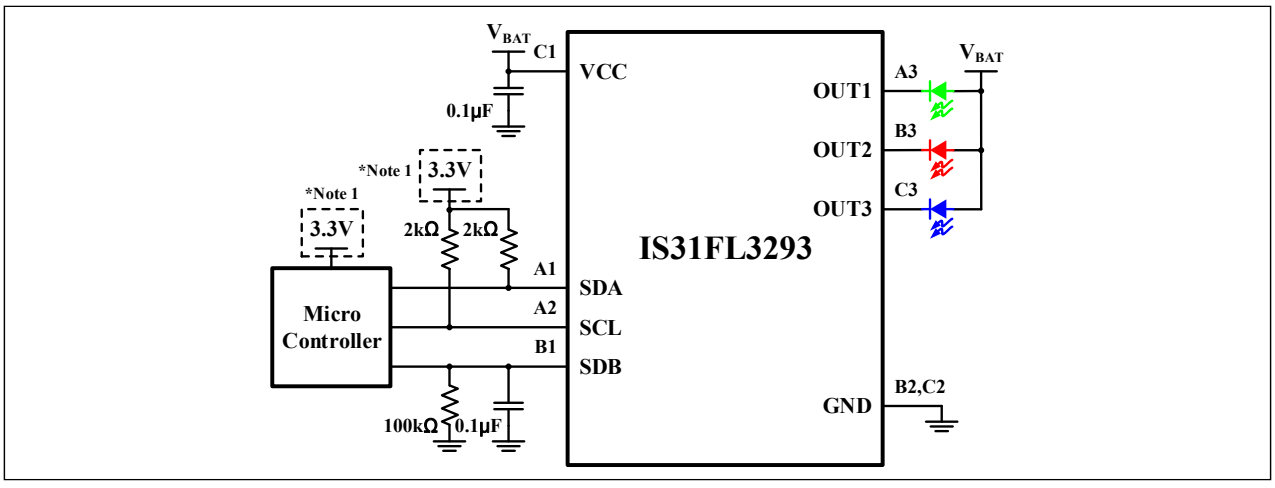
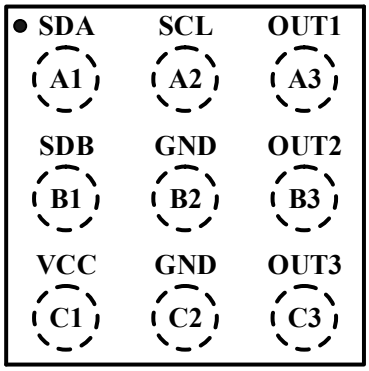


Figure 1 Typical Application Circuit: 1 RGB

Note 1: This 3.3V is the high level voltage (V_{IH}) for IS31FL3293, which is usually same as VCC of Micro Controller, e.g. if V_{IH} is <3.3V, recommend to have a level shift circuit.

PIN CONFIGURATION

Package	Pin Configuration (Top View)
UTQFN-9	

PIN DESCRIPTION

No.	Pin	Description
A1	SDA	I2C compatible serial data.
B1	SDB	Shutdown pin.
C1	VCC	Power for IC.
A2	SCL	I2C compatible serial clock.
B2, C2	GND	Ground.
A3、B3、C3	OUT1~OUT3	Current sink pin for LED.

ORDERING INFORMATION

Industrial Range: -40°C to +125°C

Order Part No.	Package	QTY/Reel
IS31FL3293-UTLS4-TR	UTQFN-9, Lead-free	3000

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	-0.3V ~+6.0V
Voltage at any input pin, OUTx	-0.3V ~ V_{CC}+0.3V
Maximum junction temperature, T_{JMAX}	+150°C
Storage temperature range, T_{STG}	-65°C ~+150°C
Operating temperature range, T_A=T_J	-40°C ~ +125°C
Package thermal resistance, junction to ambient (4-layer standard test PCB based on JESD 51-2A), θ_{JA}	124.48°C/W
ESD (HBM) ESD (CDM)	±2kV ±750V

Note 2: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

The following specifications apply for V_{CC}= 3.6V, T_A= 25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage		2.7		5.5	V
I_{CC}	Quiescent power supply current	V_{CC}= 3.6V, all channels PWM= 0x000, PWM Frequency= 200Hz		90	120	μA
		V_{CC}= 3.6V, one channels I_{OUT}= 20mA, PWM Frequency= 200Hz		195	220	
		V_{CC}= 3.6V, all channels I_{OUT}= 20mA, PWM Frequency= 200Hz		400	440	
I_{SD}	Shutdown current	V_{SDB}= 0V		0.3	1	μA
		V_{SDB}= V_{CC} = 3.6V, Configuration Register written "0000 0000		0.3	1	
I_{OUT}	Maximum constant current of OUTx	I_{OUT}=20mA, GCC=0x3F, CL=0xFF	18.6	20	21.4	mA
I_{OUT}	Minimum constant current of OUTx	LCAI= "1", GCC=0x1D, CL=0xFF	2.8	3	3.2	mA
ΔI_{MAT}	Between channels	I_{OUT}=20mA, GCC=0x3F, CL=0xFF	-5		5	%
ΔI_{ACC}	Between device to device	I_{OUT}=20mA, GCC=0x3F, CL=0xFF	-5		5	%
ΔI_{MAT}	Between channels (Note 3)	LCAI= "1", I_{OUT}=3mA, GCC=0x1D, CL=0xFF	-5		5	%
ΔI_{ACC}	Between device to device (Note 4)	LCAI= "1", I_{OUT}=3mA, GCC=0x1D, CL=0xFF	-5		5	%
f_{OUT}	PWM frequency of output	PFS=0	180	200	220	Hz
		PFS=1	360	400	440	Hz
V_{HR}	Current sink headroom voltage	I_{OUT}=20mA		250	330	mV
T_{SD}	Thermal shutdown	(Note 5)		160		°C
T_{SD_HY}	Thermal shutdown hysteresis	(Note 5)		18		°C
Logic Electrical Characteristics (SDA, SCL, SDB)						
V_{IL}	Logic "0" input voltage	V_{CC}=2.7V~5.5V	GND		0.4	V
V_{IH}	Logic "1" input voltage	V_{CC}=2.7V~5.5V	1.4		V_{CC}	V
I_{IL}	Logic "0" input current	V_{INPUT} = 0V (Note 5)		5		nA
I_{IH}	Logic "1" input current	V_{INPUT} = V_{CC} (Note 5)		5		nA

DIGITAL INPUT I2C SWITCHING CHARACTERISTICS (NOTE 5)

Symbol	Parameter	Fast Mode			Fast Mode Plus			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{SCL}	Serial-clock frequency	-		400	-		1000	kHz
t_{BUF}	Bus free time between a STOP and a START condition	1.3		-	0.5		-	μs
$t_{HD, STA}$	Hold time (repeated) START condition	0.6		-	0.26		-	μs
$t_{SU, STA}$	Repeated START condition setup time	0.6		-	0.26		-	μs
$t_{SU, STO}$	STOP condition setup time	0.6		-	0.26		-	μs
$t_{HD, DAT}$	Data hold time	-		-	-		-	μs
$t_{SU, DAT}$	Data setup time	100		-	50		-	ns
t_{LOW}	SCL clock low period	1.3		-	0.5		-	μs
t_{HIGH}	SCL clock high period	0.7		-	0.26		-	μs
t_R	Rise time of both SDA and SCL signals, receiving	-		300	-		120	ns
t_F	Fall time of both SDA and SCL signals, receiving	-		300	-		120	ns

Note 3: I_{OUT} mismatch (bit to bit) $\triangle I_{MAT}$ is calculated:

$$\Delta I_{MAT} = \left(\frac{I_{OUTn}(n=1\sim 3)}{\left(\frac{I_{OUT1}+I_{OUT2}+I_{OUT3}}{3} \right)} - 1 \right) \times 100\%$$

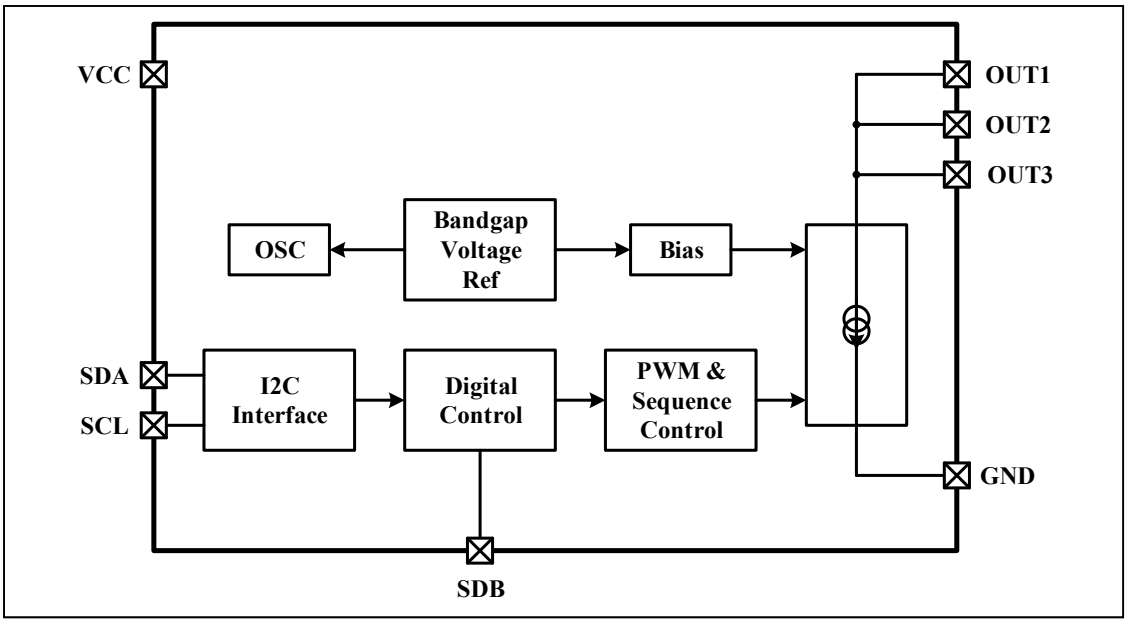
Note 4: I_{OUT} accuracy (device to device) $\triangle I_{ACC}$ is calculated:

$$\Delta I_{ACC} = \left(\frac{\left(\frac{I_{OUT1}+I_{OUT3}+I_{OUT3}}{3} - I_{OUT(IDEAL)} \right)}{I_{OUT(IDEAL)}} \right) \times 100\%$$

Where $I_{OUT(IDEAL)}$= 20mA.

Note 5: Guaranteed by design.

FUNCTION BLOCK DIAGRAM



DETAILED DESCRIPTION

I2C INTERFACE

IS31FL3293 uses a serial bus, which conforms to the I2C protocol, to control the chip's functions with two wires: SCL and SDA. The IS31FL3293 has a 7-bit slave address (A7:A1), followed by the R/W bit, A0. Set A0 to "0" for a write command and set A0 to "1" for a read command. The complete slave address is:

Table 1 Slave Address

Bit	A7:A1	A0
Value	1101100	0/1

The SCL line is uni-directional. The SDA line is bi-directional (open-drain) with a pull-up resistor (typically 2kΩ). The maximum clock frequency specified by the I2C standard is 1MHz. In this discussion, the master is the microcontroller and the slave is the IS31FL3293.

The timing diagram for the I2C is shown in Figure 2. The SDA is latched in on the stable high level of the SCL. When there is no interface activity, the SDA line should be held high.

The "START" signal is generated by lowering the SDA signal while the SCL signal is high. The start signal will alert all devices attached to the I2C bus to check the incoming address against their own chip address.

The 8-bit chip address is sent next, most significant bit first. Each address bit must be stable while the SCL level is high.

After the last bit of the chip address is sent, the master checks for the IS31FL3293's acknowledge. The master releases the SDA line high (through a pull-up resistor). Then the master sends an SCL pulse. If the IS31FL3293 has received the address correctly, then it holds the SDA line low during the SCL pulse. If the SDA line is not low, then the master should send a "STOP" signal (discussed later) and abort the transfer.

Following acknowledge of IS31FL3293, the register address byte is sent, most significant bit first. IS31FL3293 must generate another acknowledge indicating that the register address has been received.

Then 8-bit of data byte are sent next, most significant bit first. Each data bit should be valid while the SCL level is stable high. After the data byte is sent, the IS31FL3293 must generate another acknowledge to indicate that the data was received.

The "STOP" signal ends the transfer. To signal "STOP", the SDA signal goes high while the SCL signal is high.

ADDRESS AUTO INCREMENT

To write multiple bytes of data into IS31FL3293, load the address of the data register that the first data byte is intended for. During the IS31FL3293 acknowledge of receiving the data byte, the internal address pointer will increment by one. The next data byte sent to IS31FL3293 will be placed in the new address, and so on. The auto increment of the address will continue as long as data continues to be written to IS31FL3293 (Figure 5).

READING OPERATION

Most of the registers can be read.

To read the register, after I2C start condition, the bus master must send the IS31FL3293 device address with the R/$\overline{W}$ bit set to "0", followed by the register address which determines which register is accessed. Then restart I2C, the bus master should send the IS31FL3293 device address with the R/$\overline{W}$ bit set to "1". Data from the register defined by the command byte is then sent from the IS31FL3293 to the master (Figure 6).

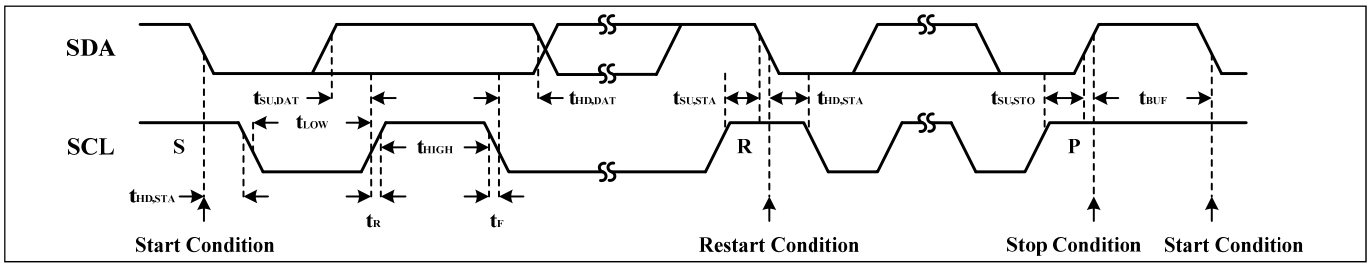


Figure 2 I2C Interface Timing

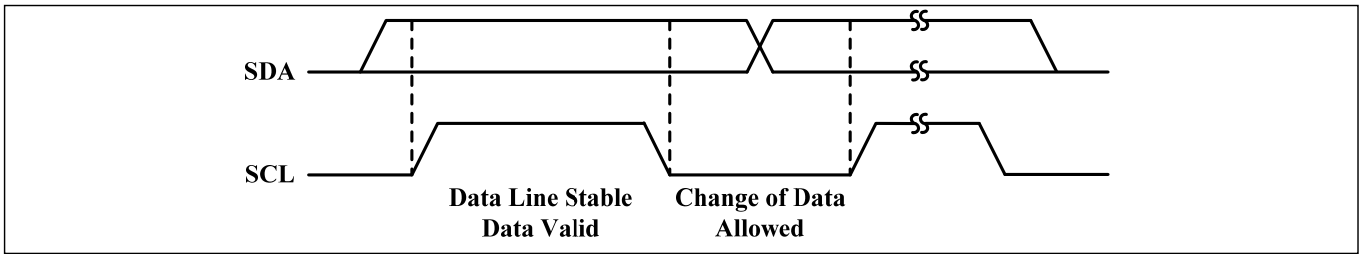


Figure 3 I2C Bit Transfer

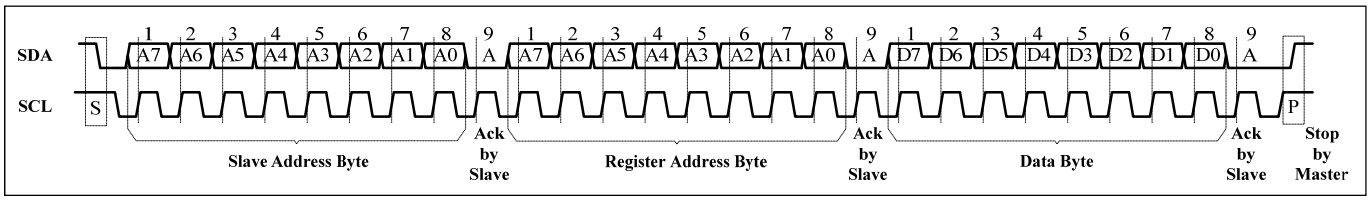


Figure 4 I2C Writing to IS31FL3293 (Typical)

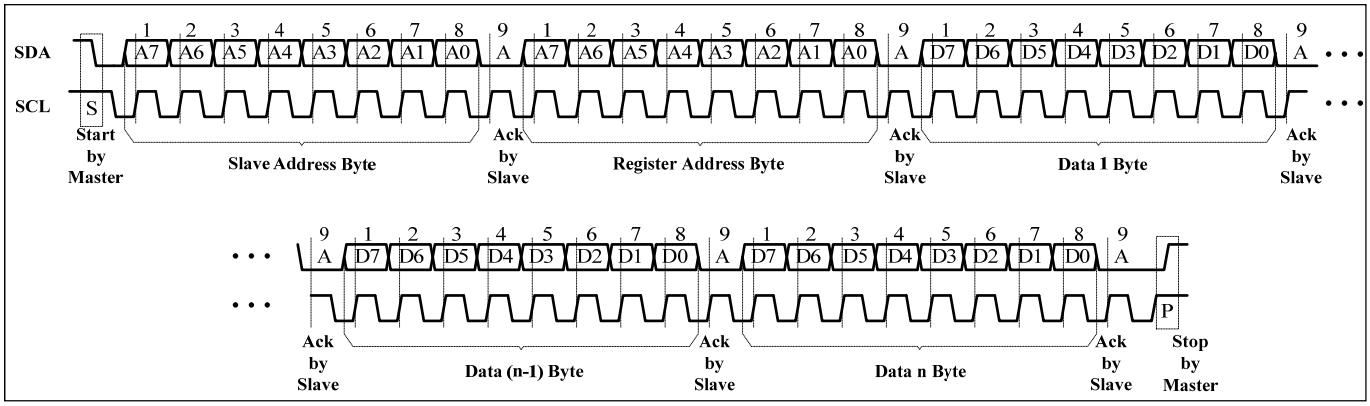


Figure 5 I2C Writing to IS31FL3293 (Automatic Address Increment)

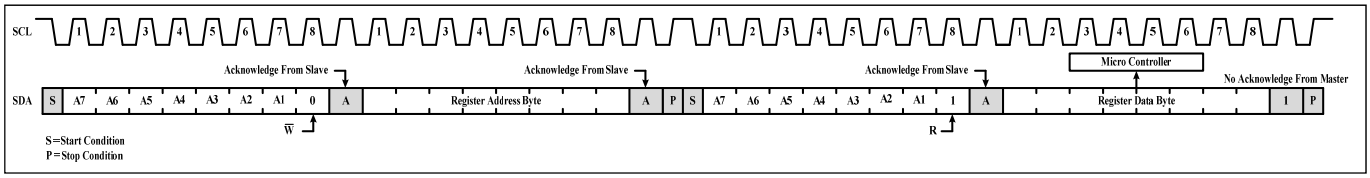


Figure 6 I2C Reading from IS31FL3293

Table 2 REGISTER DEFINITIONS

Address	Name	Function	R/W	Table	Default
00h	Product ID	For read only, read result is Slave address	R	-	-
01h	Shutdown Control Register	Set power down mode and outputs shutdown control	R/W	3	1111 0000
02h	Operation Configure Register	Set output operation mode	R/W	4	0000 0000
03h	Global Current Control Register	Set global current	R/W	5	0000 0000
04h	Color Hold Function Register	Set the hold function of each Output	R/W	6	0011 0000
0Ch	PWM Frequency Adjust Unlock Register	Unlock the 0Dh	W		0011 0000
0Dh	PWM Frequency Adjust Register	Adjust the PWM Frequency	R/W	7	0000 0000
0Fh	Pattern State Register	For reading the pattern running state	R	8	0000 0000
10h~12h	OUT1/OUT2/OUT3 Current Level Register	Output current level data register	R/W	9	0000 0000
10h~12h	Color 1 Setting Register of Pattern	Output current level data register-Color 1	R/W	10	0000 0000
13h~14h	Color 2 Setting Register of Pattern	Output current level data register-Color 2	R/W		0000 0000
16h~18h	Color 3 Setting Register of Pattern	Output current level data register-Color 3	R/W		0000 0000
19h~1Eh	PWM Register	Set PWM data	R/W	11	0000 0000
20h	Pattern TS &T1 Setting Register	Set the TS~T1 time	R/W	12	0000 0000
21h	Pattern T2 &T3 Setting Register	Set the T2~T3 time	R/W	13	0000 0000
22h	Pattern TP &T4 Setting Register	Set the TP~T4 time	R/W	14	0000 0000
23h	Pattern Color Enable Register	Set the color enable/disable	R/W	15	0000 0001
24h	Pattern Color Cycle Times Register	Set color repeat time	R/W	16	0000 0000
25h	Pattern Register	Set next step and Gamma of each pattern	R/W	17	0000 0000
26h	Pattern Loop Times Register	Set the loop time of Pattern	R/W	18	0000 0000
27h	Color Update Register	Update color data	R/W	-	0000 0000
28h	PWM Update Register	Update PWM data	R/W	-	0000 0000
29h	Pattern Update Register	Update the time data and start to run pattern	R/W	-	0000 0000
3Fh	Reset Register	Reset the registers value to default	W	-	0000 0000

Table 3 01h Shutdown Control Register

Bit	D7	D6:D4	D3	D2	D1	D0
Name	LCAI	EN3:EN1	-	PFS	SLE	SSD
Default	0	111	0	0	0	0

The Shutdown Control Register sets software shutdown and sleep modes of IS31FL3293.

The Output Enable Register enables/disables the outputs independently. The ENx is only effective when SSD= "1".

When SLE bit is set to "1" IS31FL3293 enters in to Sleep Mode, if all OUTx outputs are off for >40s.All OUTx are off without any bias. I_SLEEP= 1μA (Typ.). When the IS31FL3293 is in sleep mode, the SLE bit needs to set as "0", that the IS31FL3293 will wake up and disable the sleep mode.

SSD Software Shutdown Enable

0 Software shutdown mode

1 Normal operation

SLE Sleep Mode Enable

0 Sleep mode disable

1 Sleep mode enable (30s after no current)

PFS PWM Frequency Select

0 200Hz (Force 200Hz if any output in Pattern Mode)

1 400Hz

ENx Output Enable Control

0 Output disable

1 Output enable

LCAI Low Current Accuracy Improve

0 Default 20mA

1 Enable half current, improve low current accuracy

Table 4 02h Operating Configure Register

Bit	D7:D6	D5:D4	D3:D2	D1:D0
Name	-	MOD3	MOD2	MOD1
Default	00	00	00	00

The MODx (x=1~3) bits set output operation modes of IS31FL3293. The PMS bit sets the PWM resolution.

MODx OUT1~OUT3 LED Mode

00 PWM & Current Level Mode

01 Pattern Mode

1x Current Level Mode

When the OUTx works in PWM Mode, means the output current is controlled by PWM Registers (19h~1Eh).

When the OUTx works in Pattern Mode, means the output current is controlled by Color Setting Registers.

When the OUTx works in Current Level Mode, means the output current is controlled by Current Level Register.

Table 5 03h Global Current Control Register

Bit	D7:D6	D5:D0
Name	-	GCC
Default	00	11 1111

GCC registers control I_{OUT} as shown in Formula (1).

$$I_{OUT} = 20mA \times \frac{GCC}{64} \times \frac{CL}{256} \quad (1)$$

$$GCC = \sum_{n=0}^{5} D[n] \cdot 2^n \quad (2)$$

Table 6 04h Color Hold Function Register

Bit	D7:D2	D1	D0
Name	-	CHF	HT
Default	0000 00	0	0

The Color Hold Function Register configures hold time for each output in Pattern Mode.

HT Hold Time Selection

0 Hold at end of T4 when color loop done (always off)

1 Hold at end of T2 when color loop done (always on)

CHF Hold Function Enable

0 hold function disable

1 hold function enable

0Ch PWM Frequency Adjust Unlock Register

Write "0xA5" to 0Ch to unlock the PWM Frequency Adjust Register (0Dh).

Table 7 0Dh PWM Frequency Adjust Register

Bit	D7:D3	D2:D0
Name	-	PFA
Default	0000 0	000

The PFA bits adjust the PWM Frequency. Before access to 0Dh, the 0Ch need to write 0xA5 first to unlock it.

PFA	PWM Frequency Adjust
000	0%
001	+22.07%
010	+36.29%
011	+57.04%
100	-51.58%
101	-44.48%
010	-30.89%
111	-15.22%

Table 8 0Fh Pattern State Register (Read Only)

Bit	D7	D6	D5	D4	D3	D2:D0
Name	PS	CS3	CS2	CS1	-	TS
Default	0	0	0	0	0	000

The Pattern State Register stores the pattern status. PS is the pattern enabled or not, OUTx is the color enable or not, TS will show the running position of Pattern.

TS	**Time State**
000	Running at TS
001	Running at T1
010	Running at T2
011	Running at T3
100	Running at TP
101	Running at T4

CSx	**Color State**
0	Not running at Color x
1	Running at Color x

PS	**Pattern State**
0	Not running at Pattern
1	Running at Pattern

Table 9 10h/11h/12h OUT1/OUT2/OUT3 Current Level Register

Bit	D7:D0
Name	CL
Default	0000 0000

The output current may be computed using the Formula (1):

$$I_{OUT} = 20mA \times \frac{GCC}{64} \times \frac{CL}{256} \quad (1)$$

$$CL = \sum_{n=0}^{7} D[n] \cdot 2^n \quad (3)$$

$$I_{LED} = 20mA \times \frac{GCC}{64} \times \frac{CL}{256} \times \frac{PWM}{4096} \quad (4)$$

Where D[n] stands for the individual bit value, 1 or 0, in location n, PWM is the value of 19h~1Eh, I_{OUT} is the peak current of the outputs. I_{LED} is the average current of the outputs.

When IS31FL3293 operates in Current Level Mode, PWM = 4096.

When IS31FL3293 operates in PWM & Current Level Mode, the value of CL and PWM will decide the output current together.

When IS31FL3293 operates in Pattern Mode, PWM changes to make the auto breathing effect.

For example: in Current Level node only, if D7:D0 = 10110101,

I_{OUT} = 20mA × (2^7 +2^5 +2^4 +2^2 +2^0)/256

Table 10-1 10h~12h Color 1 Setting Register of Pattern (OUT1~OUT3)

Bit	D7:D0
Name	COL1_Oy
Default	0000 0000

Table 10-2 13h~15h Color 2 Setting Register of Pattern (OUT1~OUT3)

Bit	D7:D0
Name	COL2_Oy
Default	0000 0000

Table 10-3 16h~18h Color 3 Setting Register of Pattern (OUT1~OUT3)

Bit	D7:D0
Name	COL3_Oy
Default	0000 0000

Color Setting Registers store the color setting for each output in Pattern Mode. Check Pattern Color Setting section for more information about the color setting registers.

When IS31FL3293 operates in Pattern Mode, the value of Color Registers will decide the output current of each output in 256 levels.

The output current may be computed using the Formula (5):

$$I_{OUT} = 20\,mA \times \frac{COLx\_Oy}{256} \qquad (5)$$

$$COLx\_Oy = \sum_{n=0}^{7} D[n] \cdot 2^n \qquad (6)$$

Where D[n] stands for the individual bit value, 1 or 0, in location n.

For example: if D7:D0 = 10110101,

I_{OUT} = 20mA× (2^7 +2^5 +2^4 +2^2 +2^0)/256

I_{OUT} is the peak current of the outputs.

Need to write Color Update Register (27h) to update the data.

Table 11 19h~1Eh PWM Register

Reg	1Ah (1Ch, 1Eh)		19h (1Bh, 1Dh)
Bit	D7:D4	D3:D0	D7:D0
Name	-	PWM_H	PWM_L
Default	0000	0000	0000 0000

When IS31FL3293 operates only in PWM & Current Level Mode, each output has 2 bytes to modulate the PWM duty in 4096 steps, in Pattern Mode, the PWM is not allowed be accessed.

Each dot has a byte to modulate the PWM duty in 4096 steps.

The value of the PWM Registers decides the average current of each LED noted I_{LED}.

I_{LED} computed by Formula (4):

$$I_{LED} = 20mA \times \frac{GCC}{64} \times \frac{CL}{256} \times \frac{PWM}{4096} \qquad (4)$$

Where I_{OUT} is the peak current of the outputs. I_{LED} is the average current of the outputs.

$$PWM = \sum_{n=0}^{11} D[n] \cdot 2^n \qquad (7)$$

Where D[n] stands for the individual bit value, 1 or 0, in location n.

For example: if PWM_H = 00001001, PWM_L = 10110101, GCC=63, CL=255,

I_{LED} = 20mA*(2^{11} +2^8 +2^7 +2^5 +2^4 +2^2 +2^0)/4096

Table 12 20h Pattern TS &T1 Setting Register

Bit	D7:D3	D4:D0
Name	T1	TS
Default	0000	0000

The TS & T1 Setting Registers set the TS and T1 time in Pattern Mode.

TS	Pattern Start Time Selection
0000	0.04s
0001	0.16s
0010	0.31s
0011	0.46s
0100	0.61s
0101	0.92s
0110	1.25s
0111	1.92s
1000	2.52s
1001	3.12s
1010	3.72s
1011	5.04s
1100	6.24s
1101	7.44s
1110	8.76s
1111	9.96s

T1	Rise Time Selection
0000	0.04s
0001	0.16s
0010	0.31s
0011	0.46s
0100	0.61s
0101	0.92s
0110	1.25s
0111	1.92s
1000	2.52s
1001	3.12s
1010	3.72s
1011	5.04s
1100	6.24s
1101	7.44s
1110	8.76s
1111	9.96s

Table 13 21h Pattern T2 &T3 Setting Register

Bit	D7:D3	D4:D0
Name	T3	T2
Default	0000	0000

The T2 & T3 Setting Registers set the T2 and T3 time in Pattern Mode.

T2	Hold Time Selection
0000	0.04s
0001	0.16s
0010	0.31s
0011	0.46s
0100	0.61s
0101	0.92s
0110	1.25s
0111	1.92s
1000	2.52s
1001	3.12s
1010	3.72s
1011	5.04s
1100	6.24s
1101	7.44s
1110	8.76s
1111	9.96s

T3	Fall Time Selection
0000	0.04s
0001	0.16s
0010	0.31s
0011	0.46s
0100	0.61s
0101	0.92s
0110	1.25s
0111	1.92s
1000	2.52s
1001	3.12s
1010	3.72s
1011	5.04s
1100	6.24s
1101	7.44s
1110	8.76s
1111	9.96s

Table 14 22h Pattern TP &T4 Setting Register

Bit	D7:D4	D3:D0
Name	T4	TP
Default	0000	0000

The TP & T4 Setting Registers set the TP and T4 time in Pattern Mode.

TP	Time between Pulses
0000	0.04s
0001	0.16s
0010	0.31s
0011	0.46s
0100	0.61s
0101	0.92s
0110	1.25s
0111	1.92s
1000	2.52s
1001	3.12s
1010	3.72s
1011	5.04s
1100	6.24s
1101	7.44s
1110	8.76s
1111	9.96s

T4	Off Time Selection
0000	0.04s
0001	0.16s
0010	0.31s
0011	0.46s
0100	0.61s
0101	0.92s
0110	1.25s
0111	1.92s
1000	2.52s
1001	3.12s
1010	3.72s
1011	5.04s
1100	6.24s
1101	7.44s
1110	8.76s
1111	9.96s

Table 15 23h Pattern Color Enable Register

Bit	D7:D3	D2	D1	D0
Name	-	CE3	CE2	CE1
Default	00000	0	0	1

Color Enable Register enables the color function for each color in Pattern Mode.

CEx	Color Enable Selection
0	Color x disable
1	Color x enable

Table 16 24h Pattern Color Cycle Times Register

Bit	D7:D6	D5:D4	D3:D2	D1:D0
Name	-	CCT3	CCT2	CCT1
Default	00	00	00	00

Pattern Color Cycle Times Register sets Color loop times for each color.

CCTx	Color Cycle Times Selection
00	Endless
01	1 time
10	2 times
11	3 times

Table 17 25h Pattern Register

Bit	D7:D4	D3	D2:D0
Name	MTPLT	GAM	-
Default	0000	0	000

GAM controls the gamma of pattern. MTPLT controls the loop of Pattern.

GAM	Gamma Selection
0	Gamma=2.4
1	Linearity

MTPLT Multy-Pulse Loop Time

0000	endless
0001	1 time
…	
1111	15 times

Table 18 26h Pattern Loop Times Register

Bit	D7	D6:D0
Name	PLT_H	PLT_L
Default	0	000 0000

If PLT_H(D7)=0, PLT_L!=0

Pattern loop times:

$$Looptime = \sum_{n=0}^{6} D[n] \times 2^n \quad (9)$$

If PLT_H(D7)=0, PLT_L=0, endless

If PLT_H(D7)=1, PLT_L!=0

Pattern loop times:

$$Looptime = 16 \times \sum_{n=0}^{6} D[n] \times 2^n \quad (10)$$

If PLT_H(D7)=1, PLT_L=0, endless

27h Color Update Register

Write “0xC5” to 27h will update the data of 10h~18h.

28h PWM Update Register

Write “0xC5” to 28h will update the data of 19h~1Eh.

29h Pattern time Update Register

Write “0xC5” to 29h will update the data of 20h~22h.

3Fh Reset Register

Once user writes “0xC5” to the Reset Register, IS31FL3293 will reset all registers to their default value. On initial power-up, the IS31FL3293 registers are reset to their default values for a blank display.

TYPICAL APPLICATION INFORMATION

GENERAL DESCRIPTION

IS31FL3293 is a 3-channel fun LED driver which auto breathing mode. It has Pattern Mode and Current Lever Mode for RGB lighting effects.

CURRENT SETTING

The maximum output current is 20mA. The Global Current Control register GCC can be used to set a lower current. The 8-bit CL registers (10h~12h) control the individual currents for each of the outputs.

For example, OUT1, OUT2 and OUT3 drive an RGB LED, OUT1 is Red LED, OUT2 is Green LED and OUT 3 is Blue LED. If GCC and CL bits are the same, then the RGB LED may appear slightly pink, or not so white. The CL bits can be used to adjust the IOUTx current, so the RGB LED appears closer to a pure white color. We call this CL bit adjustment by another name: white balance registers.

PWM CONTROL

The PWM Registers (19h~1Eh) can modulate LED brightness of each channel with 4096 steps. For example, if the data in PWM_H Register is “0000 0000” and in PWM_L Register is “0000 0100”, then the PWM is 4/4096.

Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve a breathing effect.

CURRENT LEVEL MODE

The Current Level Registers (10h~12h) are active and can modulate LED peak current IOUT of each output with 256 steps independently. For example, if the data in Current Lever Register is “0000 0100”, then the current level is the fourth step, with a current level of 4/256.

In Current Level Mode, user doesn’t need to turn on the CEx of 23h, a new value must be written to the Current Level registers to change the output current. Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve breathing, blinking, or any other effects that the user defines.

PWM & CURRENT LEVEL MODE

PWM & Current Level Mode is the combination of PWM and Current Level Mode. In this mode, the Current Level Registers (10h~12h) adjust the peak current (I_{OUT}) of the outputs, the PWM Registers (19h~1Eh) adjust the duty cycle of the output current, the finial result is the output average current ILED.

PATTERN MODE

By setting the MOD1~MOD3 bits of the Operating Configure Register (02h) to “01”, the corresponding output will operate in Pattern Mode. In Pattern Mode, the timing characteristics for output current - current rising (T1), holding (T2), falling (T3) and off time (TS, TP, T4), can be adjusted individually so that each output can independently maintain a pre-established pattern achieving mixing color breathing or a single color breathing without requiring any additional interface activity, thus saving valuable system resources.

PATTERN COLOR SETTING

In Pattern Mode, the LED color is defined by COLx_Oy (x, y= 1, 2, 3) bits in Color Setting Registers (10h~18h). There are 3 RGB current combinations to generate 3 pre-defined colors for display. More than one of the 3 pre-defined colors can be chosen by setting CEx bits in Color Enable Register (23h). When CEx is set, the color x is allowed to be displayed in current pattern.

In Current Level Mode, the output current (OUT1~OUT3) is configured by the Current Level Register (10h~12h) as Table 19.

Table 19 Current Level Mode

Mode	OUT1	OUT2	OUT3
Current Level	10h	11h	12h

In PWM Mode, the output current (OUT1~OUT3) is configured by the PWM Register (19h~1Eh) as Table 20.

Table 20 PWM Register of PWM & Current Level Mode

Mode	OUT1	OUT2	OUT3
PWM_H	1Ah	1Ch	1Eh
PWM_L	19h	1Bh	1Dh

In Pattern Mode, the output current (OUT1~OUT3) is configured by the Color Setting Register of Pattern as Table 21.

Table 21 Color Register of Pattern Mode

Pattern Mode	Color Enable	OUT1	OUT2	OUT3
Pattern	CE(23h)	01h	02h	04h

PATTERN TIME SETTING

User should configure the related pattern time setting registers according to actual timing requirements via I2C interface before starting pattern. The pattern time is including TS, T1~T4 and TP. And the pattern has three continue lighting cycle as Color 1~Color 3. Please check the LED OPERATING MODE section for more about the time setting.

GAMMA CORRECTION

In order to perform a better visual LED breathing effect, the device integrates gamma correction to the Pattern Mode. The gamma correction causes the change in intensity to appear more linear to the human eye.

Gamma correction, also known as gamma compression or encoding, is used to encode linear luminance to match the non-linear characteristics of display. Since the IS31FL3293 can modulate the brightness of the LEDs with 256 steps, a gamma correction function can be applied when computing each subsequent LED intensity setting such that the changes in brightness matches the human eye's brightness curve.

The IS31FL3293 provides two gamma corrections which can be set by GAM bits of Pattern Registers (25h) for each pattern. The gamma correction is shown as below.

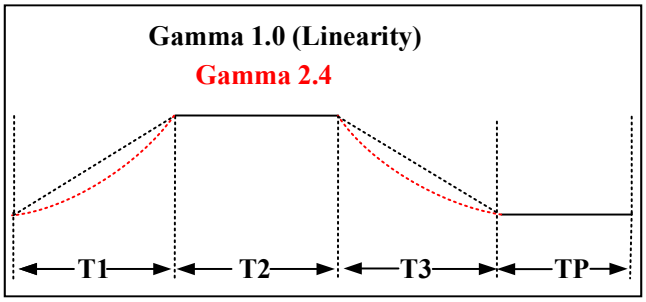


Figure 7 Gamma Correction

SHUTDOWN MODE

Shutdown mode can either be used as a means of reducing power consumption or generating a flashing display (repeatedly entering and leaving shutdown mode). During shutdown mode all registers retain their data.

Software Shutdown

By setting SSD bit of the Shutdown Register (01h) to "0", the IS31FL3293 will operate in software shutdown mode, wherein it will consume only 0.3μA (typ.) current. When the IS31FL3293 is in software shutdown mode, all current sources are switched off.

Hardware Shutdown

The chip enters hardware shutdown mode when the SDB pin is pulled low, wherein they consume only 0.3μA (Typ.) current. When set SDB high, the rising edge will reset the I2C module, but the register information retains.

LED OPERATING MODE

The IS31FL3293 has three operating modes which can be chosen by the MODx bits of Operating Configure Register (02h).

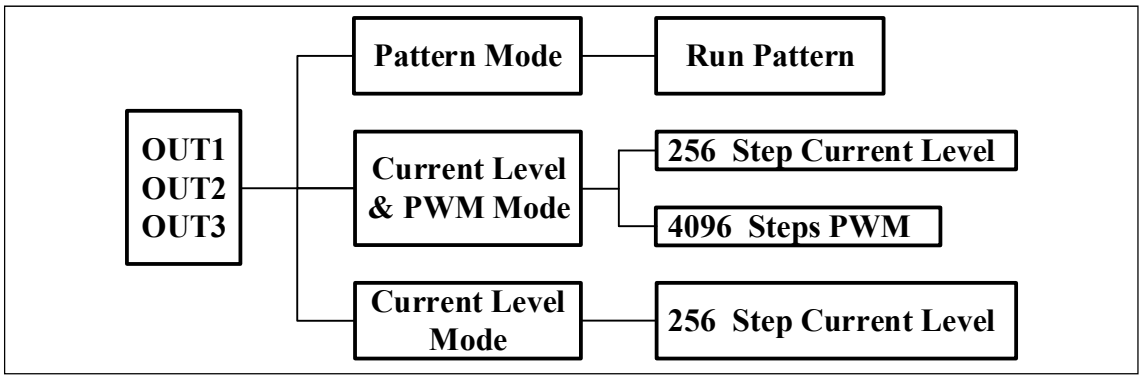


Figure 8 Operating Mode Map

Pattern Mode

If MODx=01 (Pattern Mode), OUT1~OUT3 can operate in Pattern Mode only and run the pattern.

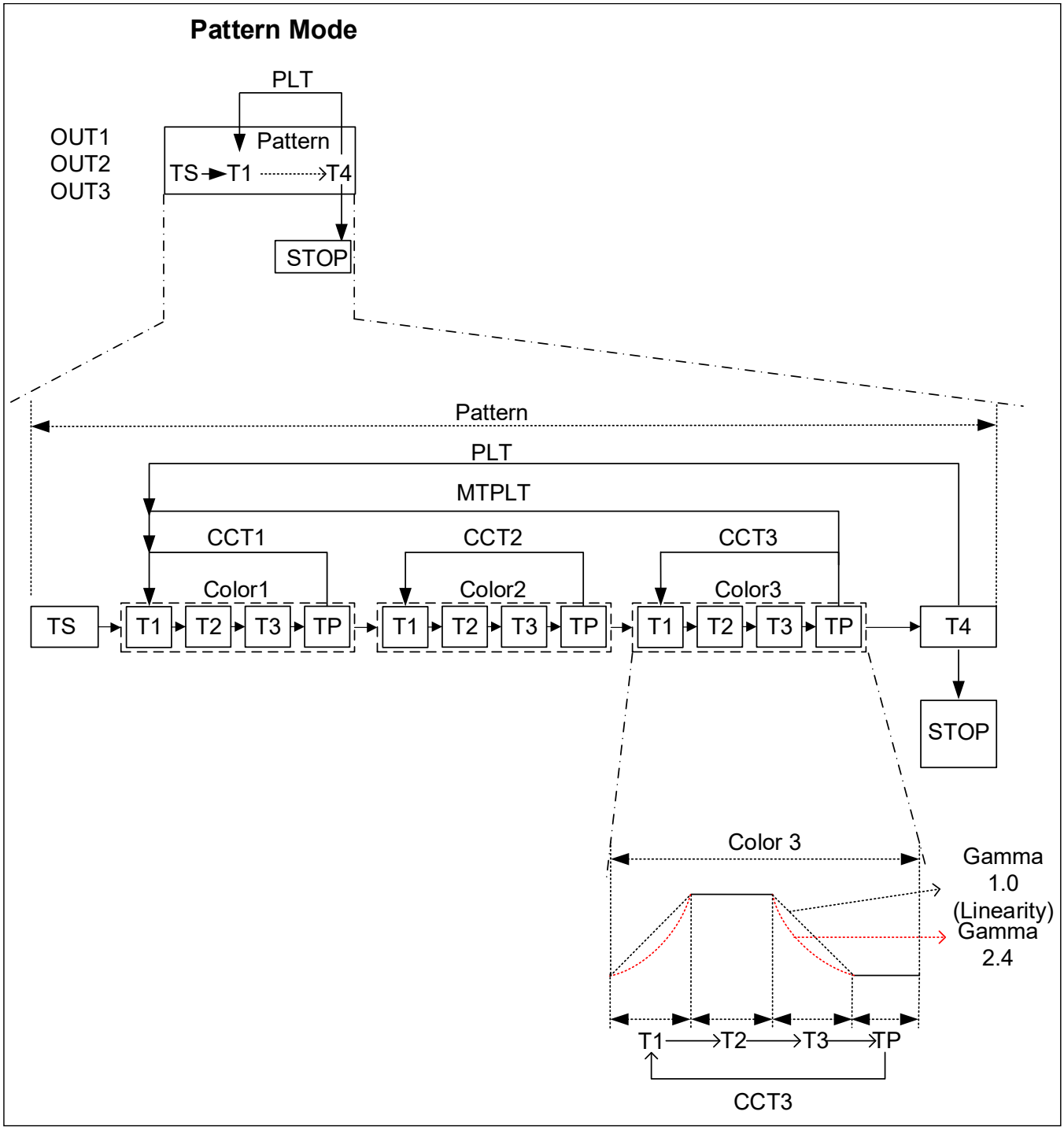


Figure 9 Pattern Mode

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

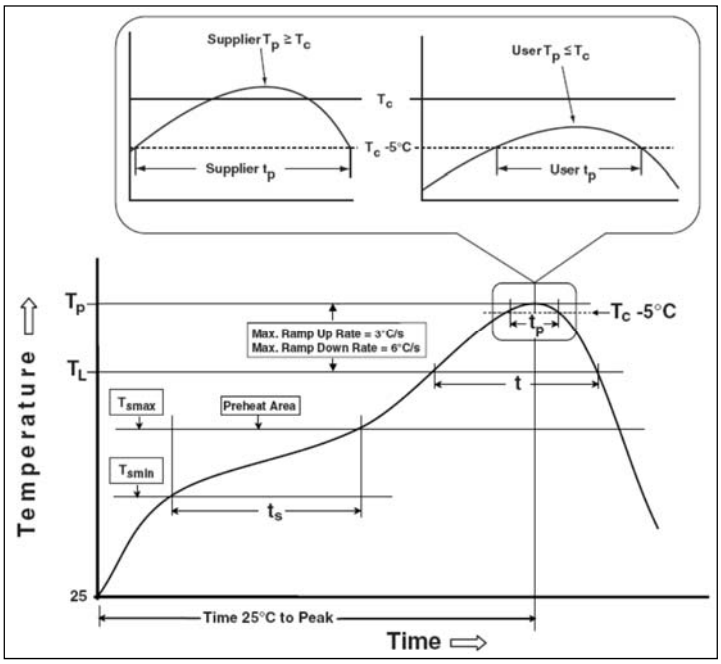


Figure 10 Classification Profile

PACKAGE INFORMATION

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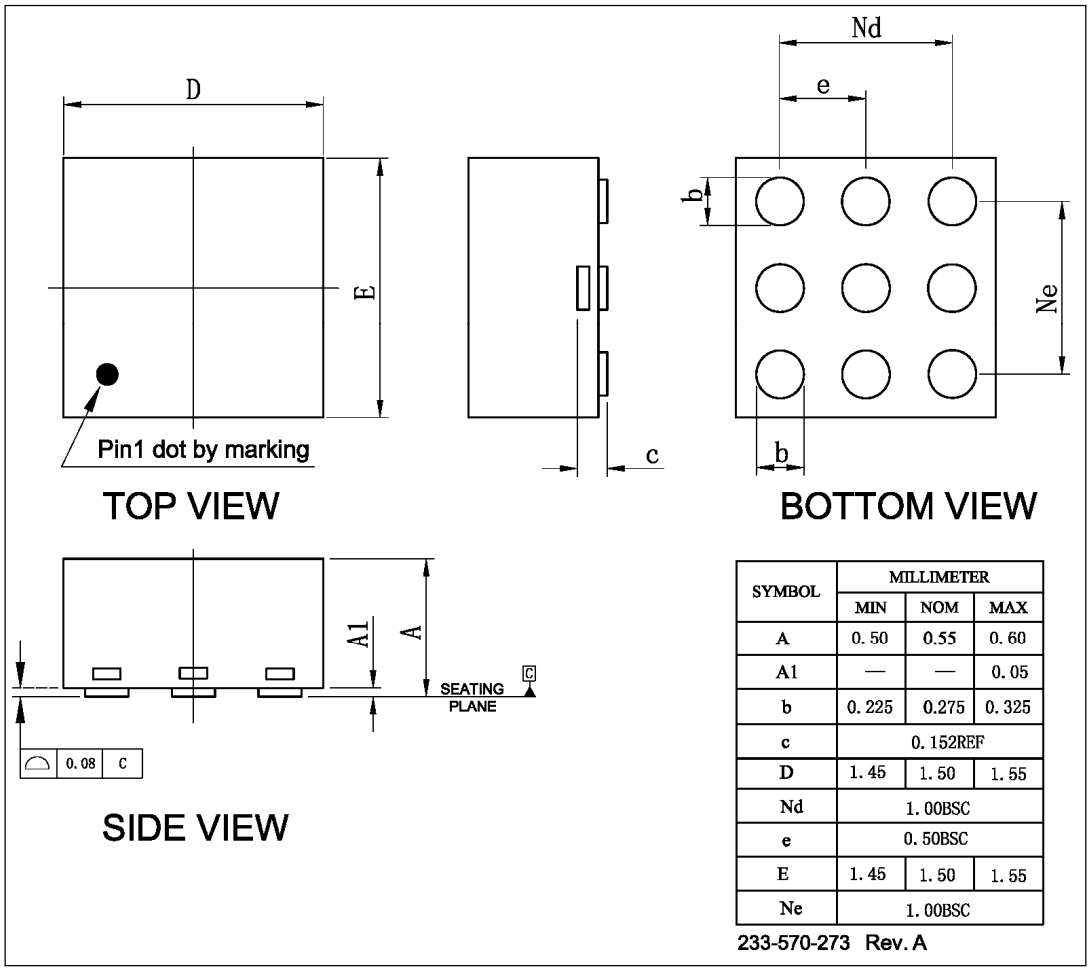

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	—	—	0.05
b	0.225	0.275	0.325
c	0.152REF		
D	1.45	1.50	1.55
Nd	1.00BSC		
e	0.50BSC		
E	1.45	1.50	1.55
Ne	1.00BSC		

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RECOMMENDED LAND PATTERN

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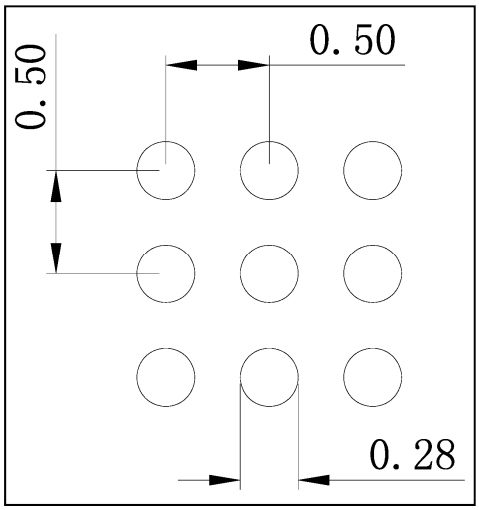

Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. User's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
0A	Initial release	2022.05.30
A	Update EC table value and release to mass production.	2022.09.22
B	1. Updated Lumissil Logo. 2. Updated description of 01h register (Sleep mode).	2024.05.07