# IS31FL3268

## 24-CHANNEL, 16-BIT PWM LED DRIVER

**March 2024**

### GENERAL DESCRIPTIONS

The IS31FL3268 is a 24-channel constant current LED driver. Each channel has 16-bit PWM brightness control, and 64 steps of constant-current scaling (SL). SL can adjust brightness deviation between channels. GCC can adjusts brightness deviation between the R, G, and B color groups. The 8 steps maximum current band control (CB) selects the maximum output current range for all channels.

Proprietary programmable algorithms are used in IS31FL3268 to minimize audible noise that can result from MLCC decoupling capacitor. SL, GCC, CB and all other registers can be programmed via a high-speed VSB (video series bus, up to 20MHz) or SPI (up to 20MHz) serial interface port.

IS31FL3268 software shutdown mode can put the device to sleep (for minimum power consumption) while retaining all register values.

IS31FL3268 is available in QFN-40 (5mm×5mm). It operates from 3.0V to 5.5V over the temperature range of -40°C to +125°C.

### APPLICATIONS

- Mini LED Back Light
- LED Back Light
- Center Information Display
- Signage
- LED Video Displays

### FEATURES

- $V_{CC}$= 3.0V to 5.5V
- 24 current sink output channels tolerate up to 16V, multiple LEDs can be connected in series
- Support 24 current sink output channels and sink current capability with CB and GCC
  - 51mA ($V_{CC}$≥ 3.2V, CB= “111”)
  - 37.5mA ($V_{CC}$< 3.2V, CB= “101”)
- Maximum Current Band (CB)
  - 3 bits (8 steps) with a 9.1% to 100% range
- DC Current Scaling (SL)
  - 6 bits (64 steps) with a 25.9% to 100% range
- Individual 16-bit, 8+8-bit dithering, 8+4-bit dithering, 8-bit PWM mode
- Global Current Control (GCC)
  - 8 bits (256 steps) with a 9.6% to 100% range
  - 3 GCC sets for each color group
- Constant Current Accuracy
  - Channel to Channel= ±3% (Max.@25°C)
  - Device to Device= ±6% (Max.@25°C)
- Chain topology via VSB interface, PWM data I/O is daisy chained with bi-directional data transmission (write and read)
- Support bi-directional data output via DI
- Auto display repeat
- Display timing reset
- Real-time LED open detection (LOD)
- Real-time LED short detection (LSD)
- Over temperature protection
- Spread Spectrums
- Software shutdown mode
- 180-degree phase delay operation to reduce power noise
- Operation temperature range: -40°C to +125°C
- QFN-40 (5mm×5mm) package
- RoHS & Halogen-Free Compliance
- TSCA Compliance

## TYPICAL APLICATION CIRCUITE

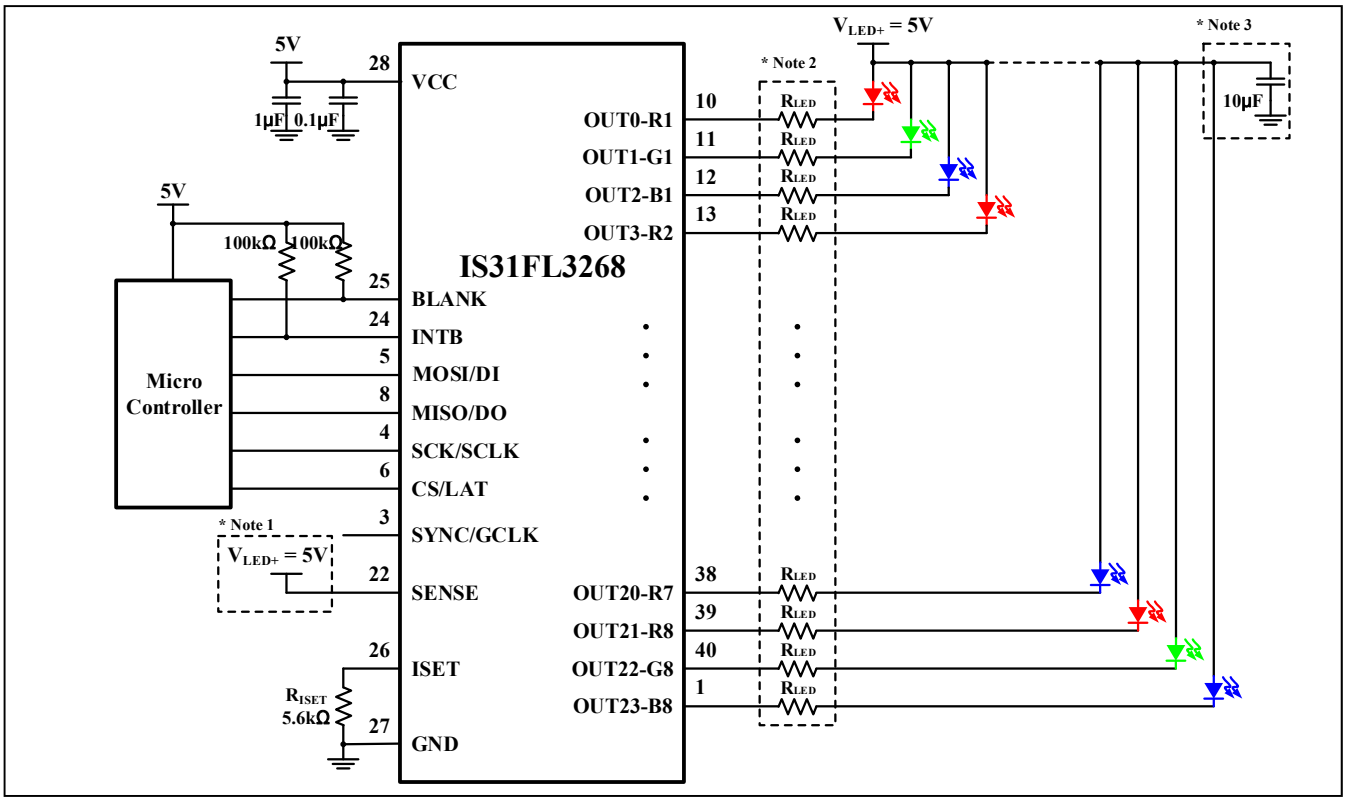



**Figure 1** Typical Application Circuit

## TYPICAL APLICATION CIRCUITE (CONTINUED)

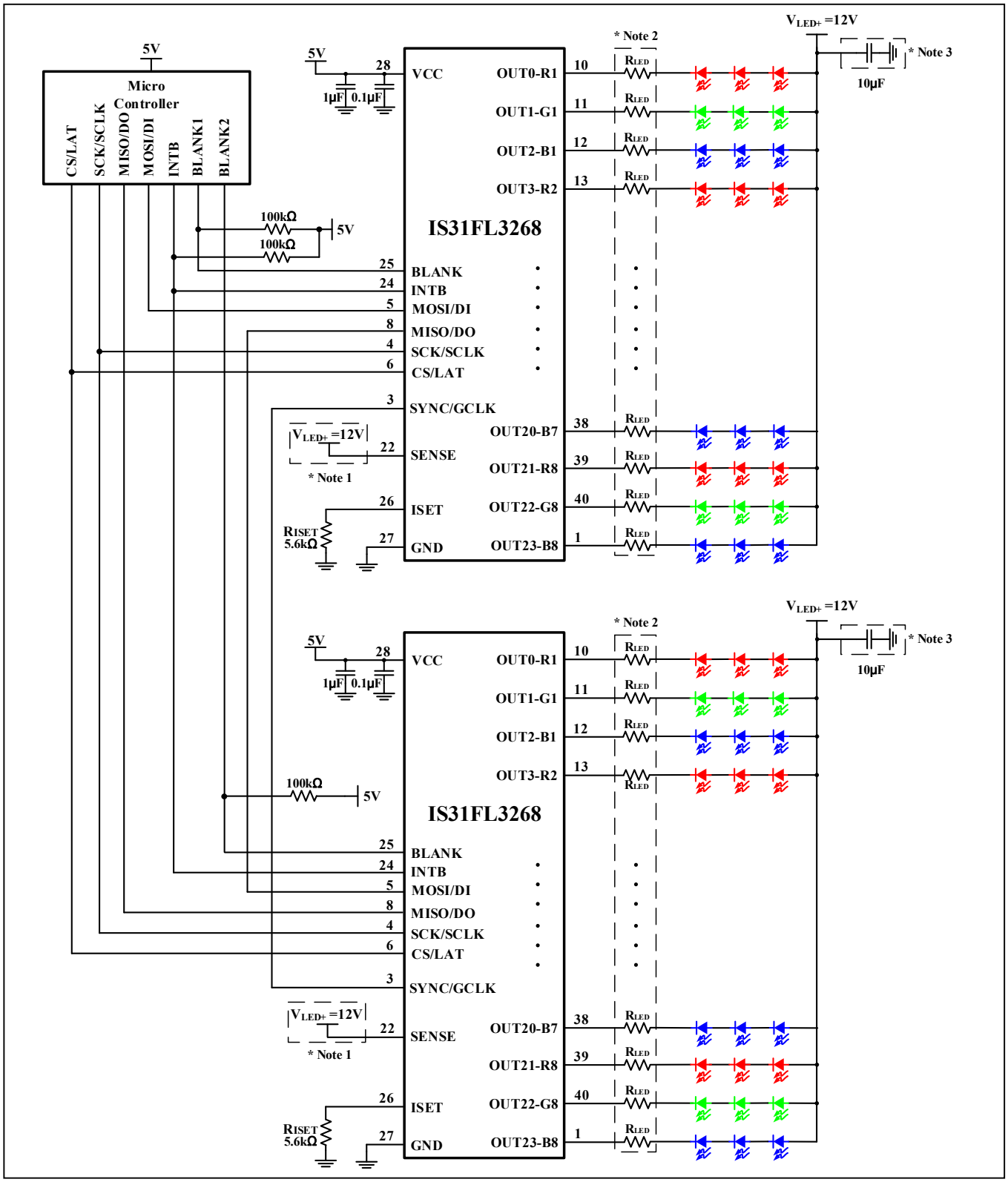


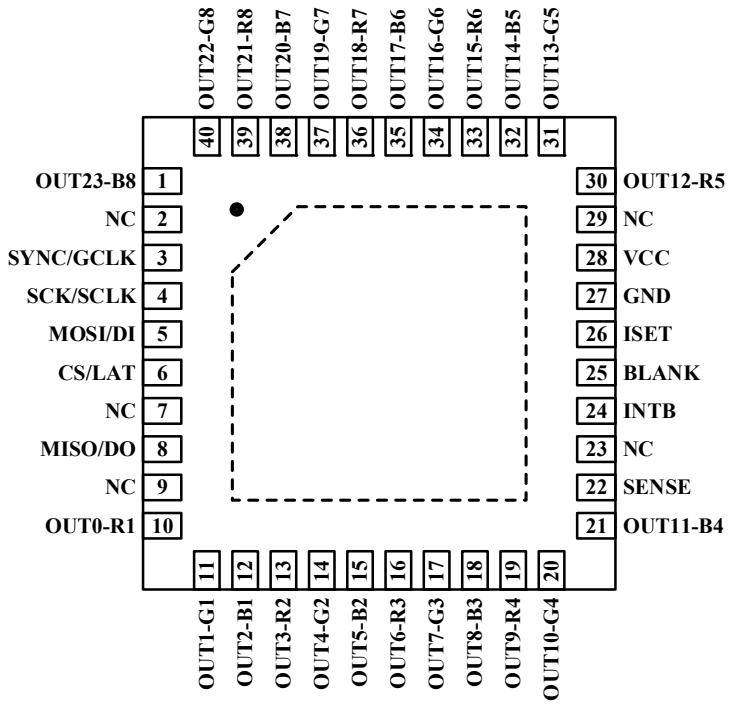

**Figure 2** Typical Application Circuit (Cascade)

**Note 1:** The SENSE pin is short detect reference voltage, should connect to $V_{LED+}$.

**Note 2:** These optional resistors are for offloading the thermal dissipation ($P=I^2R$) away from the IS31FL3268, it is determined by $V_{LED+}$, $I_{OUT}$, $V_F$ of LED, $V_{HR}$ of OUTx. $R_{LED}$= ($V_{LED+}$-$V_F$-$V_{HROUT}$)/$I_{OUT}$. It is optional or 24Ω recommended for white/blue/green LEDs, 39Ω recommended for red/yellow/orange LEDs when $V_{LED+}$=5V and single LED application.

**Note 3:** At least add one 10μF capacitor to $V_{LED+}$, if possible, it is recommended to add a 10μF to each group (R/G/B group), and this capacitor needs to close to the LEDs cathode and the ground net of the capacitor should be well connected to the GND plane.

## PIN CONFIGURATION

| Package | Pin Configuration (Top View) |
|---|---|
| QFN-40 |  |



## PIN DESCRIPTION

| No. | Pin | Description |
|---|---|---|
| 1,10~21,30~40 | OUT [0:23] | Output channel for LEDs. |
| 2,7,9,23,29 | NC | Not connect. |
| 3 | SYNC/GCLK | Synchronization. |
| 4 | SCK / SCLK | SPI clock / VSB clock. |
| 5 | MOSI / DI | SPI input data / VSB input data. |
| 6 | CS / LAT | CS signal of SPI / Latch signal of VSB. |
| 8 | MISO / DO | SPI output data / VSB output data. |
| 22 | SENSE | Short detect reference voltage. The SENSE pin should connect to $V_{LED+}$. |
| 24 | INTB | Interrupt output pin. Send DEh command can read the interrupt event happens and the INTB pin active low when the interrupt event happens. Can be NC (float) if interrupt function is not used. |
| 25 | BLANK | Blank all outputs. BLANK low forces all channels off. PWM timing controller is initialized. BLANK high starts PWM timing controller, channels are controlled by PWM timing controller. |
| 26 | ISET | Set the maximum $I_{OUT}$ current. |
| 27 | GND | Ground |
| 28 | VCC | Power |
| | Thermal Pad | Connect to GND. |

## ORDERING INFORMATION

**Industrial Range: -40°C to +125°C**

| Order Part No. | Package | QTY/Reel |
|---|---|---|
| IS31FL3268-QFLS4-TR | QFN-40, Lead-free | 2500 |

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply voltage, $V_{CC}$ | -0.3V ~+6.0V |
| Voltage at any input pin | -0.3V ~ $V_{CC}$+0.3V |
| Voltage at $OUT_X$ and SENSE pin | -0.3V ~ +18V |
| Maximum junction temperature, $T_{JMAX}$ | +150°C |
| Storage temperature range, $T_{STG}$ | -65°C ~+150°C |
| Operating temperature range, $T_A$=$T_J$ | -40°C ~ +125°C |
| Package thermal resistance, junction to ambient (4-layer standard test PCB based on JESD 51-2A), $\theta_{JA}$ | 31.2°C/W |
| ESD (HBM)<br>ESD (CDM) | ±2kV<br>±750V |

**Note 4:** Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

The following specifications apply for $V_{CC}$ = 5V, $T_J$ = 25°C.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 3 | | 5.5 | V |
| $I_{CC}$ | Quiescent power supply current | $R_{ISET}$=5.6kΩ, OSC=16MHz, SL=0xFC, $GCC_X$=0xFF, CB= "111", PWM= 0x0000, all LEDs off | | 10 | 11 | mA |
| $I_{SD}$ | Software shutdown mode current | $R_{ISET}$=5.6kΩ, OSC=16MHz, SSD = "1" | | 150 | 240 | μA |
| $I_{OUT}$ | Maximum constant current of $OUT_X$ | $R_{ISET}$=5.6kΩ, $V_{OUT}$=0.8V, SL=0xFC, $GCC_X$=0xFF, CB= "101", PWM=0xFFFF | 34.5 | 37.5 | 40.5 | mA |
| | | $R_{ISET}$=5.6kΩ, $V_{OUT}$=0.8V, SL=0xFC, $GCC_X$=0xFF, CB= "111", PWM=0xFFFF | | 51 | | |
| $\Delta I_{MAT}$ | Output current error between outputs (Note 5) | $R_{ISET}$=5.6kΩ, $V_{OUT}$= 0.8V, SL=0xFC, $GCC_X$=0xFF, CB= "101", PWM=0xFFFF | -3 | | 3 | % |
| $\Delta I_{ACC}$ | Output current error between devices (Note 6) | $R_{ISET}$=5.6kΩ, $V_{OUT}$= 0.8V, SL=0xFC, $GCC_X$=0xFF, CB= "101", PWM=0xFFFF | -6 | | 6 | % |
| $I_{OZ}$ | Output leakage current | PWM= 0x0000, $V_{OUT}$= 16V | | | 0.1 | μA |
| $V_{HR}$ | Current sink headroom voltage OUTx | $R_{ISET}$=5.6kΩ, SL=0xFC, GCCx=0xFF, PWM=0xFFFF, CB= "111", $I_{SINK}$=51mA | | 350 | 500 | mV |
| $V_{OD}$ | LED open detect threshold | $I_{OUT}$≥0.1mA, PWM> 25%, measured at OUTx, LODVTH= "00", Minimum level 1 | 0.05 | 0.09 | | V |
| | | $I_{OUT}$≥0.1mA, PWM> 25%, measured at OUTx, LODVTH= "01", Minimum level 2 | 0.15 | 0.19 | | |
| | | $I_{OUT}$≥0.1mA, PWM> 25%, measured at OUTx, LODVTH= "10", Minimum level 3 | 0.3 | 0.35 | | |
| | | $I_{OUT}$≥0.1mA, PWM> 25%, measured at OUTx, LODVTH= "11", Minimum level 4 | 0.44 | 0.49 | | |

**ELECTRICAL CHARACTERISTICS (CONTINUE)**

The following specifications apply for $V_{CC}$ = 5V, $T_J$ = 25°C.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{SD}$ | LED short detect threshold | $I_{OUT}$≥0.1mA, PWM> 25%, $V_{CC}$=$V_{SENSE}$=5V, measured at ($V_{SENSE}$-$V_{OUT}$) | 0.6 | 1.1 | | V |
| | | $I_{OUT}$≥0.1mA, PWM> 25%, $V_{CC}$=$V_{SENSE}$=16V, measured at ($V_{SENSE}$-$V_{OUT}$) | 0.6 | 1.2 | | V |
| $V_{ISET}$ | Voltage of ISET pin | $R_{ISET}$=5.6kΩ | | 1.22 | | V |
| $f_{OUT}$ | PWM frequency of output | OSC= 16MHz, PWM mode=16-bit mode | | 244 | | Hz |
| | | OSC= 16MHz, PWM mode=8+8-bit mode PWM> 0x0100 | | 62.5 | | kHz |
| $I_{PT}$ | LED protect current | $V_{OUT}$= 0.8V, SL=0xFC, $GCC_X$=0xFF, CB = “111”, PWM=0xFFFF | | 105 | | mA |
| $T_{SD}$ | Thermal shutdown | (Note 7) | | 165 | | °C |
| $T_{SD\_HYS}$ | Thermal shutdown hysteresis | (Note 7) | | 20 | | °C |
| **Logic Electrical Characteristics (MOSI/DI, MISO/DO, CS/LAT, SCK/SCLK, BLANK, INTB)** | | | | | | |
| $V_{IL}$ | Logic “0” input voltage | $V_{CC}$=3V~5.5V | GND | | 0.3$V_{CC}$ | V |
| $V_{IH}$ | Logic “1” input voltage | $V_{CC}$=3V~5.5V | 0.7$V_{CC}$ | | $V_{CC}$ | V |
| $V_{OH}$ | H level pin output voltage | $I_{OH}$= -2mA | $V_{CC}$-0.4V | | $V_{CC}$ | V |
| $V_{OL}$ | L level pin output voltage | $I_{OL}$= 2mA | 0 | | 0.4 | V |
| $V_{OL}$ | L level pin output voltage (INTB) | $I_{OH}$= 1mA | 0 | | 0.4 | V |
| $I_{IL}$ | Logic “0” input current | $V_{INPUT}$= L (Note 7) | | 5 | | nA |
| $I_{IH}$ | Logic “1” input current | $V_{INPUT}$= H (Note 7) | | 5 | | nA |

**DIGITAL INPUT SPI PSWITCHING CHARACTERISTICS (NOTE 7)**

| Symbol | Parameter | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $f_C$ | Clock frequency | - | | 20 | MHz |
| $t_{CH}$ | Clock high pulse duration | 10 | | | ns |
| $t_{CL}$ | Clock low pulse duration | 10 | | | ns |
| $t_{SICH}$ | MOSI to Clock rising edge setup time | 5 | | | ns |
| $t_{CLCH}$ | CS falling edge to Clock rising edge | 33 | | | ns |
| $t_{CHSI}$ | Clock rising edge to MOSI hold time | 3 | | | ns |
| $t_{CLCH}$ | Clock falling edge to CS rising edge hold time | 10 | | | ns |
| $t_{CSH}$ | CS high pulse duration | 60 | | | ns |
| $t_{SOR}$ | MISO rise time | | 25 | | ns |
| $t_{SOF}$ | MISO fall time | | 25 | | ns |
| $t_{CHSO}$ | Clock rising edge to MISO | | 30 | | ns |

**DIGITAL INPUT VSB PSWITCHING CHARACTERISTICS (NOTE 7)**

| Symbol | Parameter | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $f_C$ | Clock frequency | - | | 20 | MHz |
| $t_{CH}$ | Clock high pulse duration | 10 | | | ns |
| $t_{CL}$ | Clock low pulse duration | 10 | | | ns |
| $t_{DICH}$ | DI to Clock rising edge setup time | 5 | | | ns |
| $t_{LLCH}$ | LAT falling edge to Clock rising edge | 33 | | | ns |
| $t_{CHDI}$ | Clock rising edge to DI hold time | 3 | | | ns |
| $t_{CLLH}$ | Clock falling edge to LAT rising edge hold time | 10 | | | ns |
| $t_{LH}$ | LAT high pulse duration | 60 | | | ns |
| $t_{DOR}$ | DO rise time | | 25 | | ns |
| $t_{DOF}$ | DO fall time | | 25 | | ns |
| $t_{CHDO}$ | Clock rising edge to DO | | 30 | | ns |

**Note 5:** $I_{OUT}$ mismatch (bit to bit) $\triangle I_{MAT}$ is calculated:

$$\Delta I_{MAT} = \pm\left(\frac{I_{OUT(MAX)}-I_{OUT(MIN)}}{\left(\frac{I_{OUT0}+I_{OUT1}+\ldots+I_{OUT23}}{24}\times 2\right)}\right)\times 100\%$$

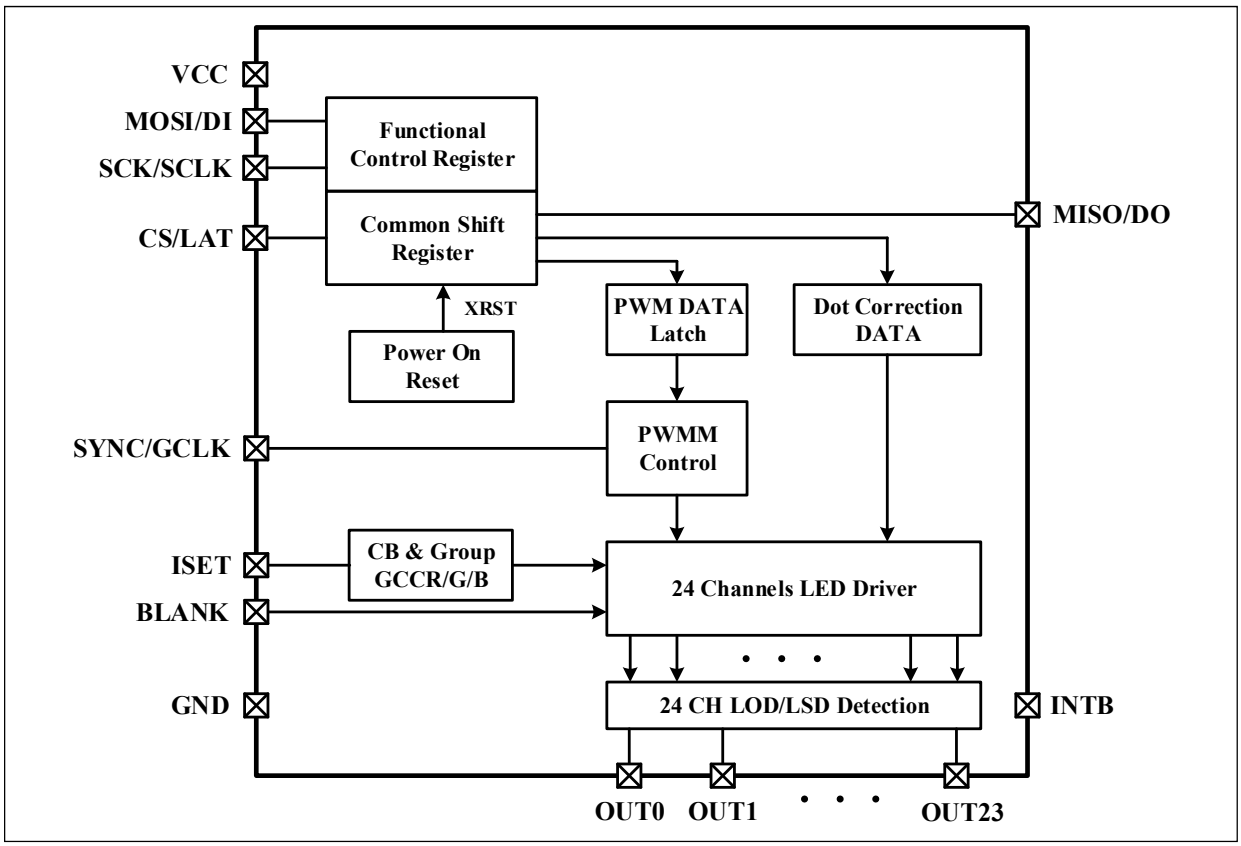
**Note 6:** $I_{OUT}$ accuracy (device to device) $\triangle I_{ACC}$ is calculated:

$$\Delta I_{ACC} = \left(\frac{I_{OUT(MIN)}-I_{OUT(IDEAL)}}{I_{OUT(IDEAL)}}\right)\times 100\% \sim \left(\frac{I_{OUT(MAX)}-I_{OUT(IDEAL)}}{I_{OUT(IDEAL)}}\right)\times 100\%$$

Where $I_{OUT(IDEAL)}$= 37.5mA when $R_{ISET}$= 5.6kΩ and CB= “101”.

**Note 7:** Guaranteed by design.

## FUNCTIONAL BLOCK DIAGRAM



## DETAILED DESCRIPTION

### SPI INTERFACE

IS31FL3268 uses a SPI protocol to control the chip's function with four wires: CS, SCK, MOSI and MISO. SPI transfer starts form CS pin from high to low controlled by Master (Microcontroller), and IS31FL3268 latches data when CS is asserted (low to high).

The maximum SCK frequency supported in IS31FL3268 is 20MHz.

### WRITING OPERATION

SPI write data format is 8-bit (byte) command followed by the register data. The command byte determines the length and function of the register data. When writing Update/Reset/Interrupt Flag Clear Register to IS31FL3268, only the command is sent (without data).

The IS31FL3268 VSB write register timing is as shown in Figure 4~7.

### READING OPERATION

FC0, FC1, Interrupt flag status, open detect result and short detect result registers can be read by SPI.

To read the registers, the first command byte selects the corresponding register, followed by a CS pulse to latch after read command byte is written to IS31FL3268. Read register timing is as shown in figure 9.

All register writes and reads command as shown in Table 1.

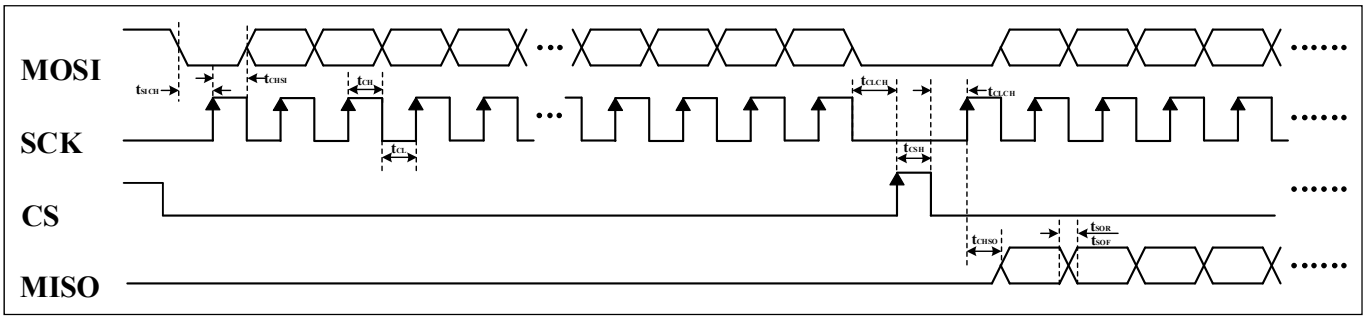



**Figure 3** SPI Input Timing

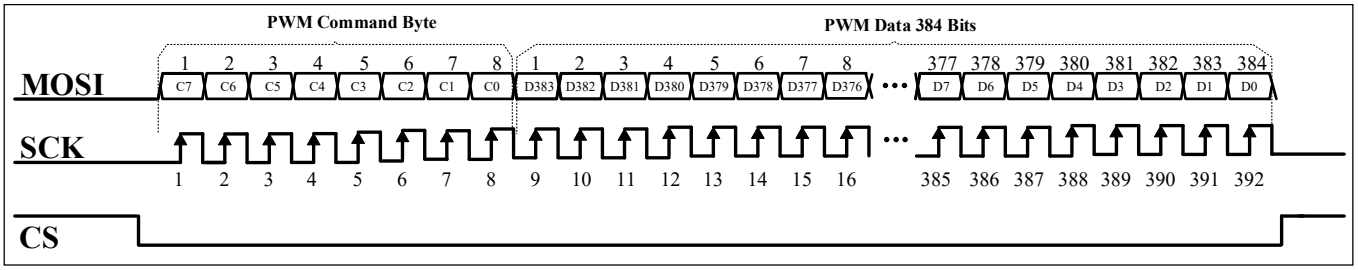



**Figure 4** SPI Writing PWM Register Data to IS31FL3268

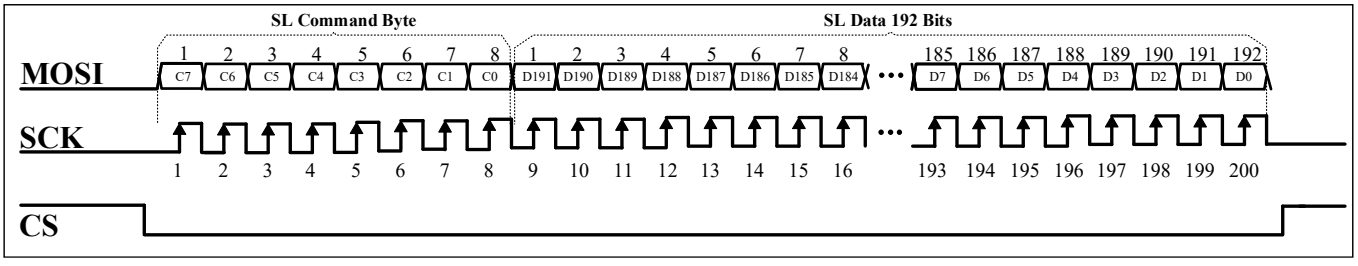



**Figure 5** SPI Writing SL Register Data to IS31FL3268

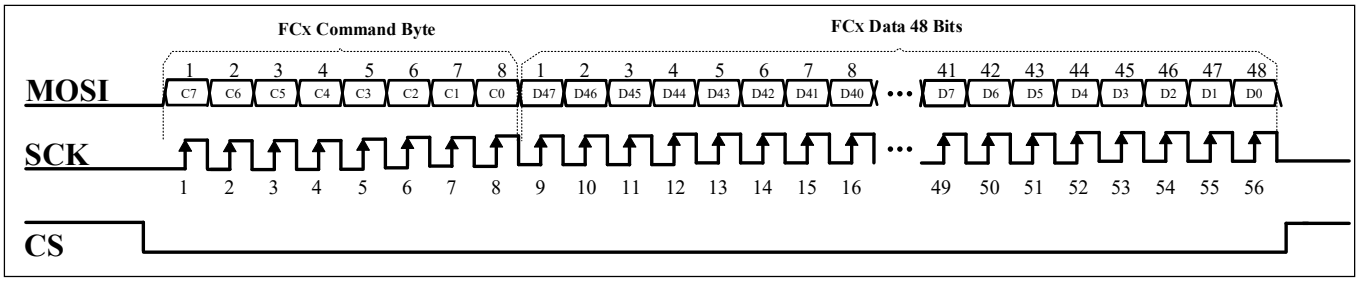



**Figure 6** SPI Writing FCx Register Data to IS31FL3268

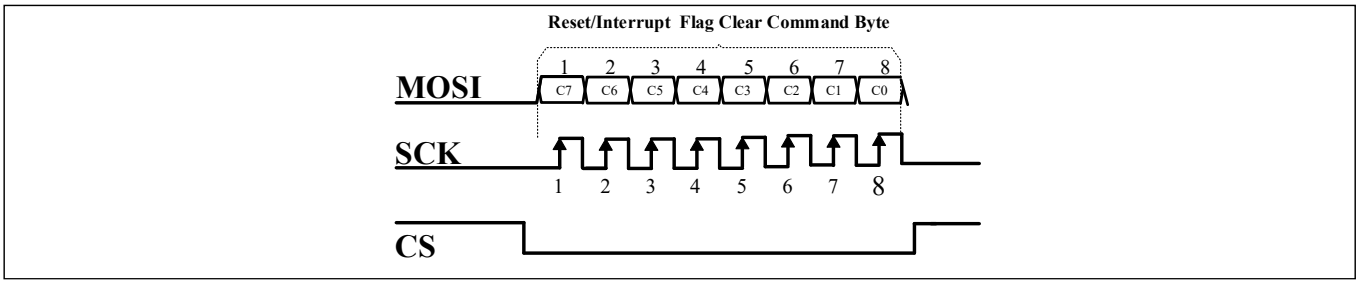



**Figure 7** SPI Writing Update/Reset/Interrupt Flag Clear Register Data to IS31FL3268

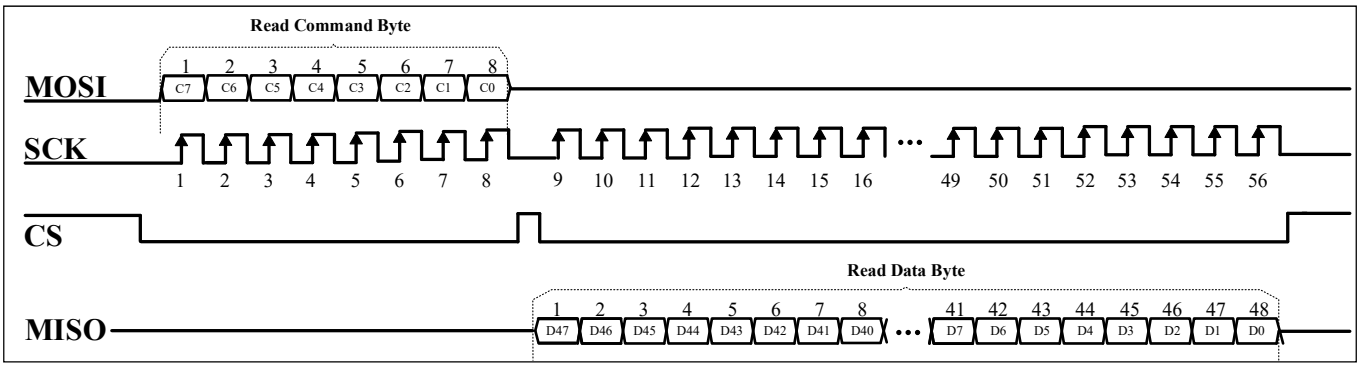



**Figure 8** SPI Reading from IS31FL3268

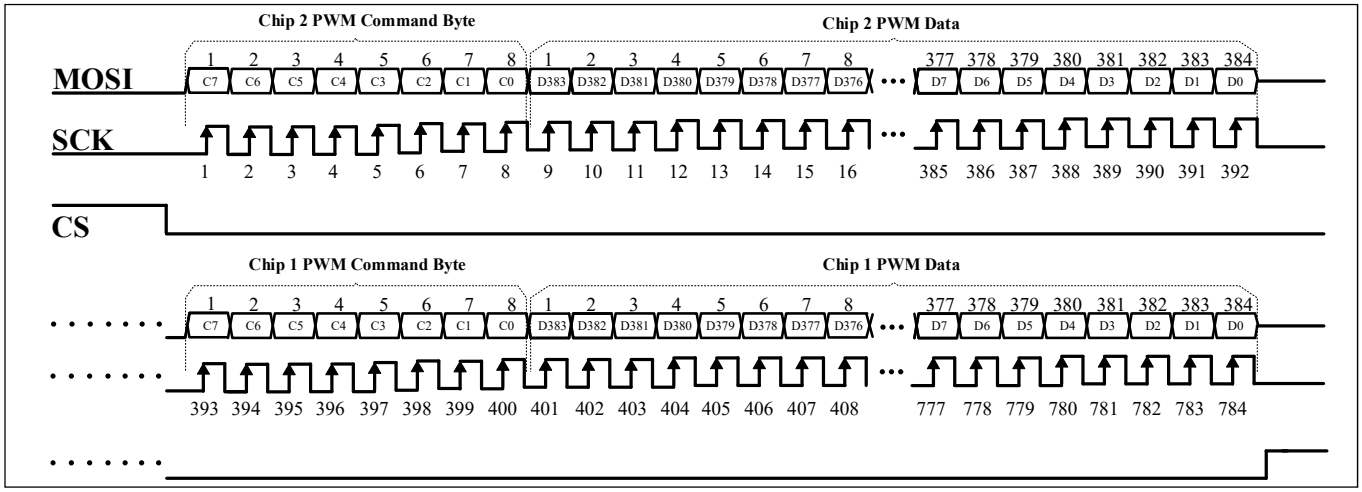



**Figure 9** SPI Writing PWM Register Data to IS31FL3268(Two Chips Cascade)

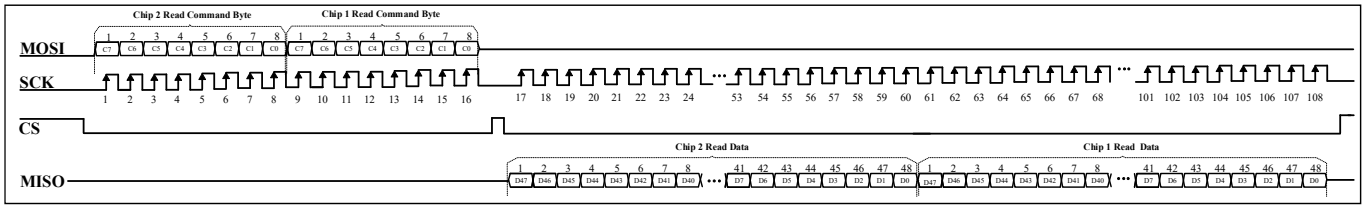



**Figure 10** SPI Reading from IS31FL3268 (Two Chips Cascade)

## VSB INTERFACE

IS31FL3268 uses a VSB protocol to control the chip's function with four wires: DI, SCLK, LAT and DO. VSB transfer starts from DI and SCLK controlled by Master (Microcontroller), and IS31FL3268 latches data when LAT is asserted (low to high).

The maximum SCLK frequency supported in IS31FL3268 is 20MHz.

## WRITING OPERATION

VSB write data format is 8-bit (byte) command followed by the register data. The command byte determines the length and function of the register data. When writing Update/Reset/Interrupt Flag Clear Register to IS31FL3268, only the command is sent (without data). The IS31FL3268 VSB write register timing is as shown in figure 12~15.

## READING OPERATION

FC0, FC1, Interrupt flag status, open detect result and short detect result registers can be read by VSB.

To read the registers, the first command byte selects the corresponding register, followed by a LAT pulse to latch after read command byte is written to IS31FL3268. Read register timing is as shown in figure 16~17.

All register writes and reads command as shown in Table 1.

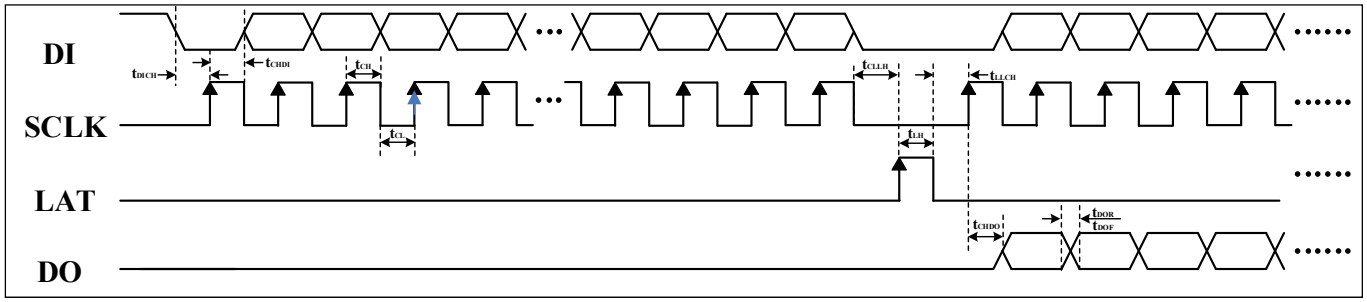



**Figure 11** IS31FL3268 VSB Input Timing

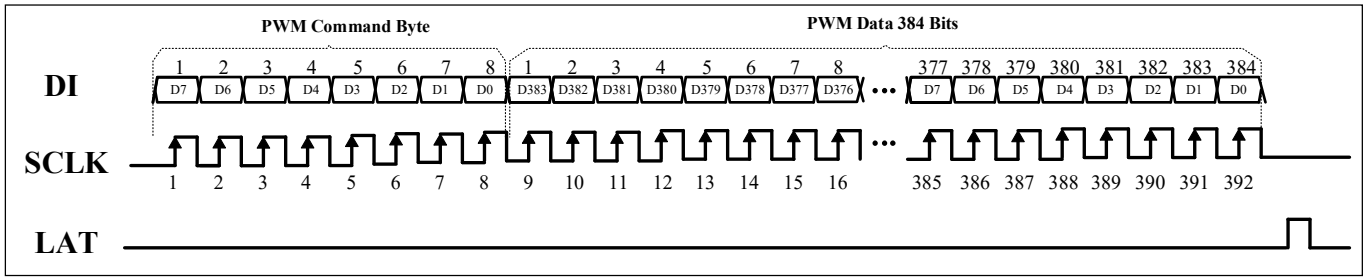



**Figure 12** VSB Writing PWM Register Data to IS31FL3268

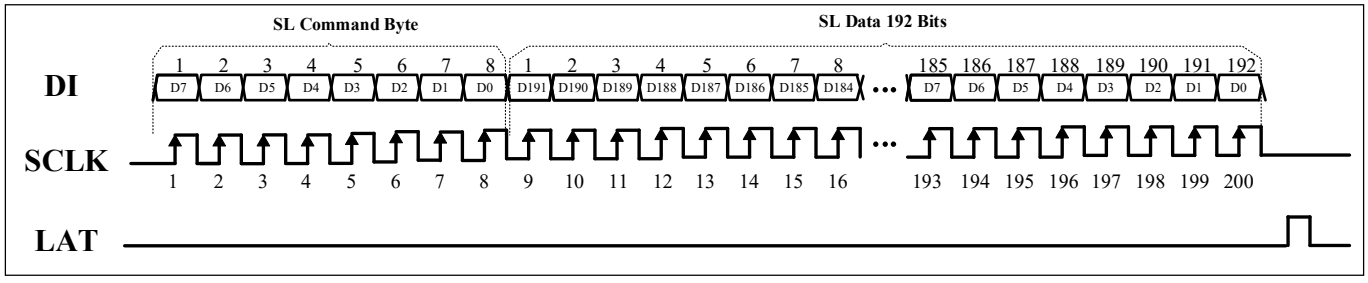



**Figure 13** VSB Writing SL Register Data to IS31FL3268

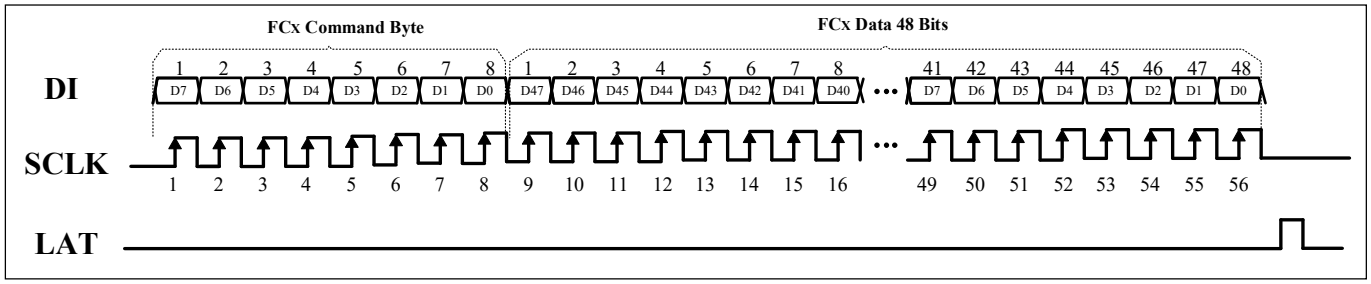



**Figure 14** VSB Writing FC0/FC1 Register Data to IS31FL3268

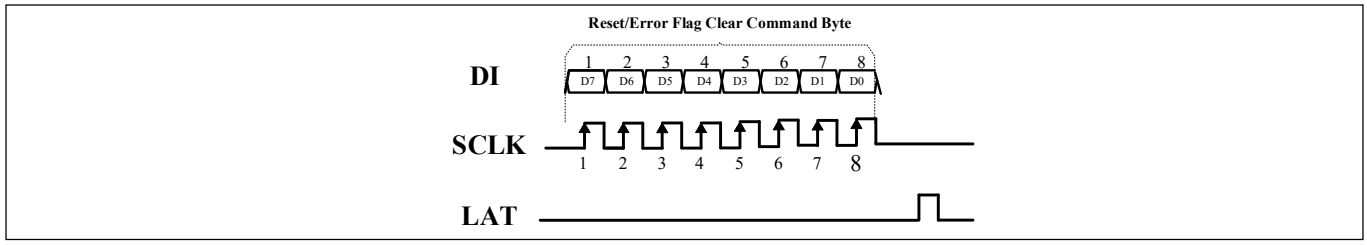



**Figure 15** VSB Writing Update/Reset/Interrupt Flag Clear Register Data to IS31FL3268

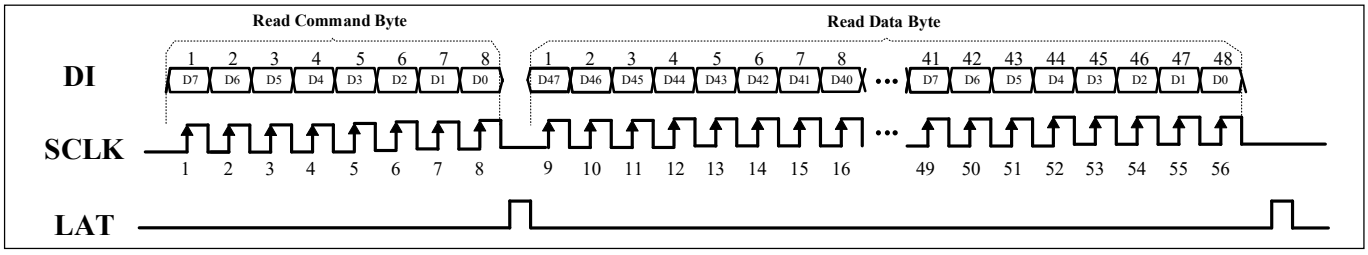



**Figure 16** VSB Reading from IS31FL3268 (Single-direction, read data from DO)

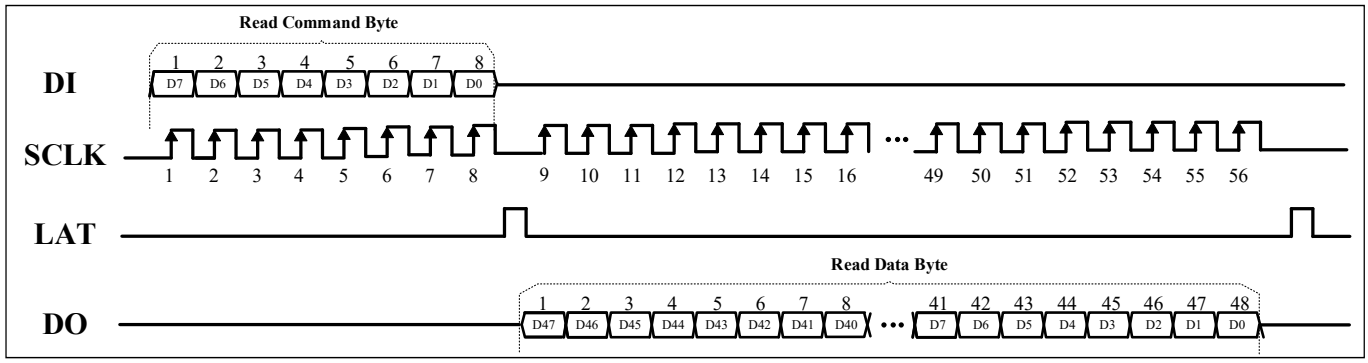



**Figure 17** VSB Reading from IS31FL3268 (Bi-direction, read data from DI)

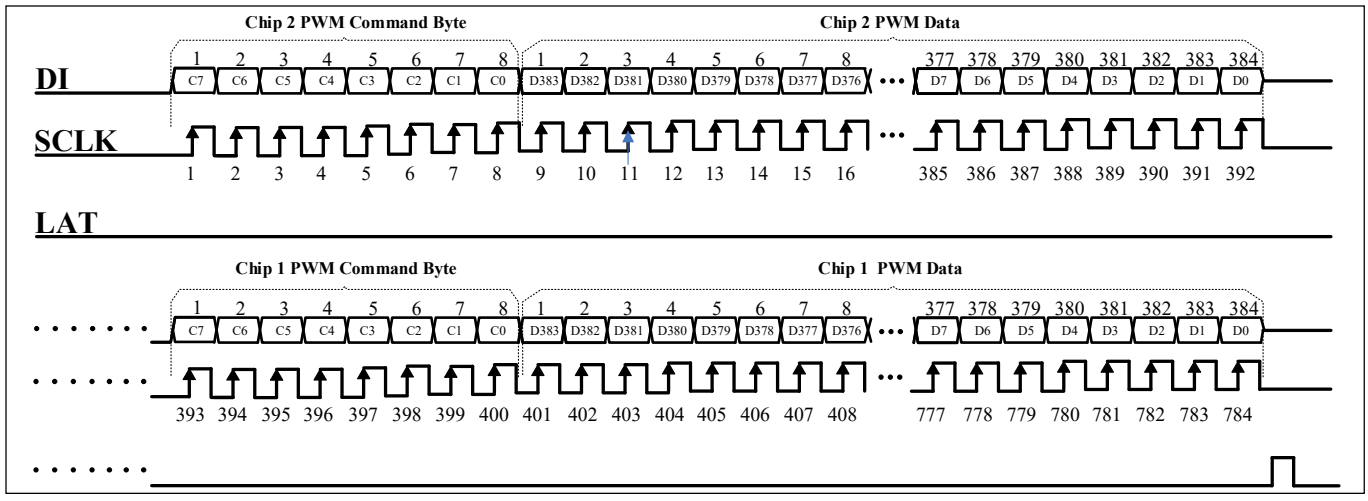



**Figure 18** VSB Writing PWM Register Data to IS31FL3268(two chips cascade)

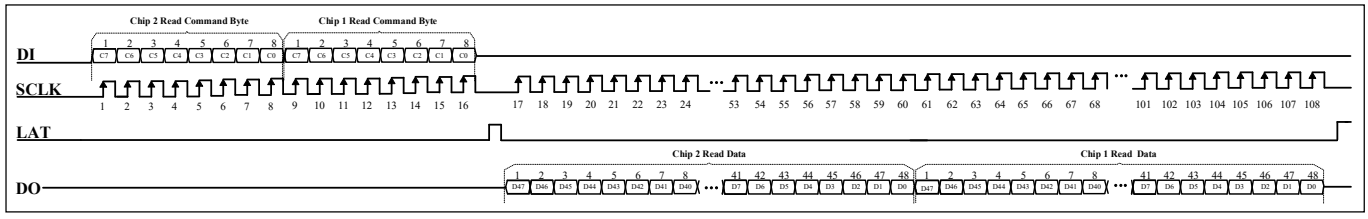



**Figure 19** VSB Reading from IS31FL3268 (two chips cascade)

**Table 1 Register Write and Read Command**

| Command | Data Length | Function |
|---|---|---|
| 0110000x | 8bits+384bits | Write PWM Register data |
| 0100000x | 8bits+192bits | Write SL Register data |
| 0010000x | 8bits+48bits | Write FC0 Register data |
| 1010000x | 8bits+48bits | Read FC0 Register data |
| 0010001x | 8bits+48bits | Write FC1 Register data |
| 1010001x | 8bits+48bits | Read FC1 Register data |
| 1011000x | 8bits+48bits | Read open detect result of 24 channels |
| 1100000x | 8bits+48bits | Read short detect result of 24 channels |
| 1101111x | 8bits+48bits | Read interrupt flag status |
| 0000001x | 8bits | Interrupt flag clear |
| 0000111x | 8bits | Global reset |

## REGISTER DEFINITION

**Table 2 Register Definition**

| Unit | Name | Function | Table | R/W | Default |
|---|---|---|---|---|---|
| PWM0~PWM23 | PWM Register | Set PWM for each channel | 3 | W | 0000 0000<br>0000 0000 |
| SL0~SL23 | SL Register | Set SL for each channel | 4 | W | 1111 11xx |
| FC0 | Global Current Control Register | Set global current for R channels (OUT0, OUT3 … OUT21) | 5 | R/W | 1111 1111 |
| | | Set global current for G channels (OUT1, OUT4 … OUT22) | 6 | R/W | 1111 1111 |
| | | Set global current for B channels (OUT2, OUT5 … OUT23) | 7 | R/W | 1111 1111 |
| | Current Band Register | Maximum current band control | 8 | R/W | 011 |
| | Configuration Register | Configure operating mode | 9 | R/W | 01 1101 |
| FC1 | Open/Short Detect and Threshold Register and Read Direction Select Register & SYNC | Set Open/Short function and read direction & SYNC | 10 | R/W | 1011 1010 |
| | Frequency Selection Register and Spread Spectrum Register | Set OSC frequency and Spread Spectrum | 11 | R/W | 0000 0000 |
| | Phase/OUT Delay and Report Enable Register | Set phase/out delay and flag report enable | 12 | R/W | 11 0000 |
| | Edge Select Register | Set MOSI/DI, MISO/DO edge and MOSI/DO output delay time | 14 | R/W | 1 |
| | Open Action Enable Register | Set the IOUT open protection action | 15 | R/W | 0 |
| OP0~OP23 | Open Detect Result Register | Store the open information of LED | 16 | R | - |
| ST0~ST23 | Short Detect Result Register | Store the short information of LED | 17 | R | - |
| Interrupt Flag Status Read | Interrupt Flag Status Read Register | Store interrupt flag status | 18 | R | - |
| Interrupt Flag Clear | Interrupt Flag Clear Register | Interrupt flag clear | 19 | W | ---- ---- |
| Reset | Reset Register | Reset all registers | 20 | W | ---- ---- |

**able 3 PWM0~PWM23 PWM Register**

| Unit | PWM23 | | … | PWM0 | |
|---|---|---|---|---|---|
| Bit | 383:376 | 375:368 | … | 15:8 | 7:0 |
| Name | PWM_H | PWM_L | … | PWM_H | PWM_L |
| Default | 00000000 | 00000000 | … | 00000000 | 00000000 |

PWM0~PWM23 is PWM register for OUTx. Each $PWM_X$ contains 16 bits data, control the PWM duty of each dot. Each dot has two bytes to modulate the PWM duty in 256/4096/65536 steps. If using 8 bits PWM resolution, only PWM_H 8 bits need to be set.

If using 8+4-bit PWM resolution, only PWM_H 8 bits and high 4 bits of PWM_L need to be set.

The channel output current, $I_{OUT}$ and the value of the PWM registers decide the average current of each LED noted as $I_{LED}$.

$I_{OUT}$ is computed by Formula (1):

$$I_{OUT} = I_{CB} \times I_{SL} \times I_{GCC} \quad (1)$$

Where $I_{CB}$ is current resulting from current band setting (See Table 8 Current Band Register and definitions), $I_{SL}$ is current resulting from SL setting (See Table 4 SL Register and definitions), and $I_{GCC}$ is current resulting from GCCx setting (See Table 5~7 GCCR/GCCB/GCCR Register and definitions).

$I_{LED}$ computed by Formula (2):

$$I_{LED} = \frac{PWM}{N} \times I_{OUT} \quad (2)$$

N=256: $PWM = \sum_{n=0}^{7} D[n] \cdot 2^n$ (8-bit mode)

N=4096: $PWM = \sum_{n=0}^{11} D[n] \cdot 2^n$ (8+4-bit mode)

N=65536: $PWM = \sum_{n=0}^{15} D[n] \cdot 2^n$ (8+8-bit/16-bit mode)

**Table 4 SL0~SL23 SL Register**

| Unit | SL23 | … | SL0 |
|---|---|---|---|
| Bit | 191:184 | … | 7:0 |
| Name | SL | … | SL |
| Default | 111111xx | … | 111111xx |

SL0~SL23 is the SL Register for OUTx. Each SLx contains 6-bit data that controls the DC output current for each dot. Each dot has a byte (only high 6 bits need to be set) to modulate DC current in 64 steps.

The SL Register value determines the output current of each channel, noted $I_{OUT}$.

$I_{OUT}$ computed by Formula (1):

$$I_{OUT} = I_{CB} \times I_{SL} \times I_{GCC} \quad (1)$$

$$I_{SL} = 0.259 + \frac{SL}{64} \times 0.741 \quad (3)$$

$$SL = \sum_{n=2}^{7} D[n] \cdot 2^n \quad (4)$$

Where D[n] stands for the individual bit value, 1 or 0, in location n, $I_{CB}$ is current resulting from current band setting (See Table 8 Current Band Register and definitions), and $I_{GCC}$ is current resulting from GCCx setting (See Table 5~7 GCCR/GCCB/GCCR Register and definitions).

**Table 5 FC0 Unit (7:0) Global Current Control Register**

| Bit | 7:0 |
|---|---|
| Name | GCCR |
| Default | 11111111 |

**Table 6 FC0 Unit (15:8) Global Current Control Register**

| Bit | 15:8 |
|---|---|
| Name | GCCG |
| Default | 11111111 |

**Table 7 FC0 Unit (23:16) Global Current Control Register**

| Bit | 23:16 |
|---|---|
| Name | GCCB |
| Default | 11111111 |

The Global Current Control Register modulates all OUTx (x=0~23) global current which is noted as $I_{OUT}$ in 256 steps.

$I_{OUT}$ is computed by the Formula (1):

$$I_{OUT} = I_{CB} \times I_{SL} \times I_{GCC} \quad (1)$$

$$I_{GCC} = 0.096 + \frac{GCC}{256} \times 0.904 \quad (5)$$

$$GCC = \sum_{n=0}^{7} D[n] \cdot 2^n \quad (6)$$

Where D[n] stands for the individual bit value, 1 or 0, in location n.

**Table 8 FC0 Unit (26:24) Current Band Register**

| Bit | 26:24 |
|---|---|
| Name | CB |
| Default | 011 |

The Current Band Register stores the current band or the maximum output current range of each LED output.

$I_{OUT(MAX)}$ is the maximum current output decided by $R_{ISET}$ (Check $R_{ISET}$ section for more information). Example: when $R_{ISET}$=5.6kΩ, $I_{OUT(MAX)}$ =51mA.

$I_{CB}$ is the maximum current band decided by CB registers.

**CB** Current Band Setting
000 Band 1: $I_{CB}= I_{OUT(MAX)} \times 9.1\%$
001 Band 2: $I_{CB}= I_{OUT(MAX)} \times 20.6\%$
010 Band 3: $I_{CB}= I_{OUT(MAX)} \times 33.1\%$
011 Band 4: $I_{CB}= I_{OUT(MAX)} \times 45.8\%$
100 Band 5: $I_{CB}= I_{OUT(MAX)} \times 59.1\%$
101 Band 6: $I_{CB}= I_{OUT(MAX)} \times 73.5\%$
110 Band 7: $I_{CB}= I_{OUT(MAX)} \times 86.4\%$
111 Band 7: $I_{CB}= I_{OUT(MAX)} \times 100\%$

**Table 9 FC0 Unit (32:27) Configuration Register**

| Bit | 32 | 31:30 | 29 | 28 | 27 |
|---|---|---|---|---|---|
| Name | SSD | ES-PWM | AUTO_UPD | DTMRST | - |
| Default | 0 | 00 | 0 | 0 | 1 |

The Configuration Register sets operating mode of IS31FL3268.

When SSD is “1”, IS31FL3268 enters software shutdown mode. When SSD is “0”, IS31FL3268 is in normal operation.

The ES-PWM bits selects PWM resolution mode, default PWM resolution mode is 16-bits.

The AUTO_UPD set auto data update function of IS31FL3268. When this bit is 0, the outputs PWM duty update immediately at the next LAT rising edge for a new PWM value data write. When this bit is 1, the output PWM duty will update at the 65,536th PWM clock after the LAT rising edge for a new PWM value write. The write control of SL data is the same.

The DTMRST set display timing reset function of IS31FL3268. When this bit is 0, the output PWM duty is not reset, the outputs are not forced off and new PWM duty update immediately at LAT rising edge for a new PWM value data write. When this bit is 1, the PWM duty is reset to 0 and all outputs are forced off at the LAT rising edge for a new PWM value data write, and all output new PWM duty will update after all outputs are forced off.

**SSD** Software Shutdown control
0 Normal operation
1 Software shutdown

**ES-PWM** PWM Mode Select
00 16-bit
01 8+8-bit dithering
10 8+4-bit dithering
11 8-bit

**ATUO_OPD** Auto Data Update Mode
0 Disable
1 Enable

**DTMRST** Display Timing Reset Mode
0 Disable
1 Enable

**Table 10 FC1 Unit (7:0) Open/Short Detect and Threshold Register and Read Direction Select Register & SYNC**

| Bit | 7 | 6 | 5 | 4 | 3 | 2:1 | 0 |
|---|---|---|---|---|---|---|---|
| Name | MS | GCLK_EN | SIOM | LSD_EN | LOD_EN | LOD VTHN | - |
| Default | 1 | 0 | 1 | 1 | 1 | 01 | 0 |

When two or more IS31FL3268 are cascaded, the MS bit is set to “1” for the master IS31FL3268. The master IS31FL3268’s SYNC/GCLK pin will generate a clock signal to all the slave devices. To be configured as a clock slave device and accept an external clock input the slave device’s MS bit must be set to “0”.

Set SIOM to “1” for single direction read data mode. In this mode, read register data will be from DO pin after sending the read command. Set SIOM to “0” for Bi-direction read mode where read register data will be from DI pin after sending the read command.

LOD_EN/LSD_EN enables the open or short LED channel detection with the result stored in open/short detect result registers.

Set LODVTH to select open detect threshold voltage.

**MS** Enable of SYNC Function
0 Slave mode
1 Master mode

**GCLK_EN** GCLK Clock Signal Output
0 Inside (no output)
1 Output

**SIOM** Read Direction Select
0 Read data Bi-direction
1 Read data single direction

**LSD_EN** Short Detection Enable
0 Disable
1 Enable

**LOD_EN** Open Detection Enable
0 Disable
1 Enable

**LODVTH** Open Detect Threshold Select;
00 0.09V
01 0.19V
10 0.35V
11 0.49V

**Table 11 FC1 Unit (15:8) Frequency Selection Register and Spread Spectrum Register**

| Bit | 15:14 | 13:12 | 11 | 10 | 9:8 |
|---|---|---|---|---|---|
| Name | CLT | RNG | SSP | - | OSC |
| Default | 00 | 00 | 0 | 0 | 00 |

Spread Spectrum Register set the spread spectrum (SSP) and synchronization function of IS31FL3268. When SSP is 1, the spread spectrum function will be enabled; the CLT bits will adjust the cycle time of spread spectrum function and the RNG bits will adjust spread spectrum range of the spread spectrum function. The oscillator clock frequency has to be 16MHz or 8MHz when the spread spectrum function is enabled.

The OSC bit selects the oscillator clock frequency, default is 16MHz.

**CLT** Spread Spectrum Cycle Time
00 1980μs
01 1200μs
10 820μs
11 660μs

**RNG** Spread Spectrum Range
00 ±3%
01 ±9%
10 ±16%
11 ±24%

**SSP** Spread Spectrum Function
0 Disable
1 Enable (OSC need select 16MHz or 8MHz)

**OSC** Oscillator Clock Frequency Select
00 16MHz (default)
01 8MHz
10 4MHz
11 2MHz (not recommended for 16-bit PWM mode)

**Table 12 PWM Frequency**

| PWM Frequency | 16MHz | 8MHz | 4MHz | 2MHz |
|---|---|---|---|---|
| 16-bit | 244Hz | 122Hz | - | - |
| 8+8-bit | 244Hz~ 62.5kHz | 122Hz~ 32.2kHz | - | - |
| 8+4-bit | 3.9kHz~6 2.5kHz | 1.95kHz~ 32.2kHz | 0.98kHz~ 15.6kHz | 0.49kHz ~7.8kHz |
| 8-bit | 62.5kHz | 32.2kHz | 15.6kHz | 7.8kHz |

**Table 13 FC1 Unit (21:16) Phase/OUT Delay and Report Enable Register**

| Bit | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|
| Name | SHORT _RE | OPEN _RE | TSD _RE | REST _RE | PHASE | OD _EN |
| Default | 1 | 1 | 0 | 0 | 0 | 1 |

When SHORT_RE is 1, the short detect result reporting is enabled.

When OPEN_RE is 1, the open detect result reporting is enabled.

When TSD_RE is 1, the thermal shutdown result reporting is enabled.

When REST_RE is 1, the ISET pin short to ground result reporting is enabled.

If reporting is enabled, the INTB pin active low when the any interrupt event happens.

**SHORT_RE** Short Detect Result Report
0 Disable
1 Enable

**OPEN_RE** Open Detect Result Report
0 Disable
1 Enable

**TSD_RE** Thermal Shutdown Result Report
0 Disable
1 Enable

**RSET_RE** ISET Pin Short to Ground Result Report
0 Disable
1 Enable

**PHASE** Phase Delay Enable
0 Disable
1 Enable

**OD_EN** OUT Delay Function
0 Disable
1 Enable

**Table 14 FC1 Unit (25:22) Edge Select Register**

| Bit | 25:24 | 23 | 22 |
|---|---|---|---|
| Name | TDO | DOE | DIE |
| Default | 11 | 1 | 0 |

Set TDO to select MISO/DO output delay time.

Set DOE to select MISO/DO transmit edge.

Set DIE to select MOSI/DI sample edge.

**TDO** MISO/DO Output Delay Time
00 0ns
10 1ns
01 2ns
11 3ns

**DOE** MISO/DO Transmit at SCK Edge
0 Falling edge
1 Rising edge

**DIE** MOSI/DI Data Sample at SCK Edge
0 Rising edge
1 Falling edge

**Table 15 FC1 Unit (26) Open Action Enable Register**

| Bit | 26 |
|---|---|
| Name | OPEN_ACTION_EN |
| Default | 0 |

The OPEN_ACTION_EN is set to the $I_{OUT}$ open protection action when open happen.

If OPEN_ACTION_EN bit is set to "0", the $I_{OUT}$ open protection is disabled, and $I_{OUT}=I_{OUT(MAX)}$ when an open happens.

If OPEN_ACTION_EN bit is set to "1", the $I_{OUT}$ open protection is enabled, and $I_{OUT}=I_{OUT(MAX)} \times 1/4$ when an open happens.

**Table 16 OP23~OP0 Unit (23:0) Open Detect Result Register (Read Only)**

| Bit | 47:0 |
|---|---|
| Name | OP23:OP0 |
| Default | - |

When LOD_EN (D3 of FC1) is set to "1", open detection will be enabled, and the LED open status will be detected in real time, the open status information will be stored in this register.

When read open detect result command (0xB0) is sent to IS31FL3268, then all channels open status information is read from this register. The read open detect result register timing is as shown in figure 8/17/19.

**Table 17 ST23~ST0 Unit (47:0) Short Detect Result Register (Read Only)**

| Bit | 47:0 |
|---|---|
| Name | ST23:ST0 |
| Default | - |

When LSD_EN (D4 of FC1) is set to "1", short detection will be enabled and the LED short will be detected in real time. The short status information will be stored in this register.

When the read short detect result command (0xC0) is sent to IS31FL3268, then all channels short status information is read from this register. The read short detect result register timing is as shown in figure 8/17/19.

**Table 18 Interrupt Flag Read (DEh) Unit (7:0) Interrupt Flag Status Read Register (Read Only)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | - | - | - | - | SF | OF | TSDF | RSF |
| Default | - | - | - | - | - | - | - | - |

**SF** Short Flag
0 normal
1 LED short detected

**OF** Open Flag
0 normal
1 LED open detected

**TSDF** Thermal Shutdown Flag
0 normal
1 thermal shutdown detected

**RSF** ISET Pin Short to Ground Flag
0 normal
1 ISET pin short to GND detected

**Table 19 Interrupt Flag Clear Unit (7:0) Register (Write Only)**

| Bit | 7:0 |
|---|---|
| Name | Interrupt Flag Clear |
| Default | - |

When working in normal operation mode, sending Interrupt Flag Clear Command (0x02) to IS31FL3268 will clear Interrupt Flag Register status and Open/Short detect status result Registers.

**Table 20 Reset Unit (7:0) Reset Register (Write Only)**

| Bit | 7:0 |
|---|---|
| Name | Reset |
| Default | - |

When working in normal operation mode, sending Reset Command (0x0E) to IS31FL3268 will reset all registers to default values.

## APPLICATION INFORMATION

### $R_{ISET}$

The maximum output current $I_{OUT(MAX)}$ for OUT0~OUT23 can be adjusted by the external resistor, $R_{ISET}$, as described in Formula (7).

$$I_{OUT(MAX)} = x \cdot \frac{V_{ISET}}{R_{ISET}} \qquad (7)$$

x = 234, $V_{ISET}$ = 1.22V.

The recommended minimum value of $R_{ISET}$ is 5.6kΩ.

When $R_{ISET}$=5.6kΩ, $I_{OUT(MAX)}$=50.98mA

When $R_{ISET}$= 7.5kΩ, $I_{OUT(MAX)}$= 38.06mA

$R_{ISET}$ should be placed close to the chip and connected to the GND plane properly.

## PWM CONTROL

The PWM Registers (PWM0~PWM23) can modulate the LED brightness of each of the 24 channels with 256/4096/65536 steps. For example, if the data in PWM_H Register is “0000 0000” and in PWM_L Register is “0000 0100”, then the PWM is the fourth step.

Writing varying new data continuously to the PWM registers modulates the brightness of the LEDs to achieve lighting patterns. e.g. breathing effect.

## SPREAD SPECTRUM FUNCTION

PWM current switching of LED outputs can be particularly troublesome with regards to EMI. To optimize the EMI performance, the IS31FL3268 includes a spread spectrum function. By setting the RNG bit of Spread Spectrum Register, Spread Spectrum range can be chosen from ±3%, ±9%, ±16%, or ±24%. The spread spectrum function will lower the total emitting electromagnetic energy by spreading the energy into a wider frequency range to significantly degrade the EMI energy peaks. With spread spectrum, the EMI conformance test is easier to pass with a smaller and lower-cost filter circuit.

## SOFTWARE SHUTDOWN MODE

Software shutdown mode can be used as a means of reducing power consumption. During software shutdown mode all registers retain their data.

By setting SSD bit of the Configuration Register (D32 of FC0) to “1”, the IS31FL3268 will operate in software shutdown mode. When the IS31FL3268 is in software shutdown mode, all current sources are switched off.

## LAYOUT RECOMMEDATION

The IS31FL3268 reliability can be improved by good PCB layout. Please consider below factors when designing the PCB.

The first step to consider are the supply lines and GND connections; especially those traces with high current. The digital and analog blocks’ supply lines and GND should be separated to avoid noise from digital block affecting the analog block.

Add at least one 10μF capacitor to $V_{LED+}$, if possible additional 0.47μF or 1μF capacitor is recommended to connected to the ground at each power supply pins of the chip. These needs to be close to the chip and the ground net of the capacitor should be well connected to the GND plane.

1. The VCC/ $V_{LED+}$ capacitors need to be close to the chip and the ground side should be well connected to the GND plane.

2. $R_{ISET}$ should be close to the chip and the ground side should be well connected to the GND plane.

3. The thermal pad should connect to the ground plane. The PCB should have the thermal pad with 16 or 25 vias through the PCB to other side’s ground area to help radiate the heat. About the thermal pad size, please refer to the land pattern of corresponding package.

4. VCC pin maximum current is 30mA when VCC=5V, but the $V_{LED+}$ net is providing total current of all outputs, its current can as much as 51mA×24=1224mA, recommend trace width for VCC pin is 0.20mm~0.3mm, recommend trace width for $V_{LED+}$ net is 1.2mm~1.5mm,

• Output pins=51mA, recommend trace width is 0.2mm~0.254mm

• All other pins<30mA, recommend trace width is 0.15mm~0.254m

## THERMAL CONSIDERATION

The over temperature of the chip may result in deterioration of the properties of the chip. IS31FL3268 has thermal pad but the chip could be very hot if power is very high. So, do consider the ground area connecting to the GND pins and the thermal pad. Other traces should keep clearance and ensure the ground area below the package is integrated. The backside ground layer should be connected to the thermal pad through 9 or 16 vias to maximized the ground plane area.

The package thermal resistance, $\theta_{JA}$, determines the amount of heat that can pass from the silicon die to the surrounding ambient environment. The $\theta_{JA}$ is a measure of the temperature rise caused by power dissipation and is usually measured in degree Celsius per watt (°C/W).

When operating the chip at high ambient temperatures, or when driving maximum load current, care must be taken to avoid exceeding the package

power dissipation limits. The maximum power dissipation can be calculated using the following Formula (6):

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}} \quad (6)$$

So, $P_{D(MAX)} = \frac{125℃-25℃}{31.2℃/W} \approx 3.205W$

Figure 20, shows the power derating of the IS31FL3268 on a JEDEC boards (in accordance with JESD 51-5 and JESD 51-7) standing in still air.

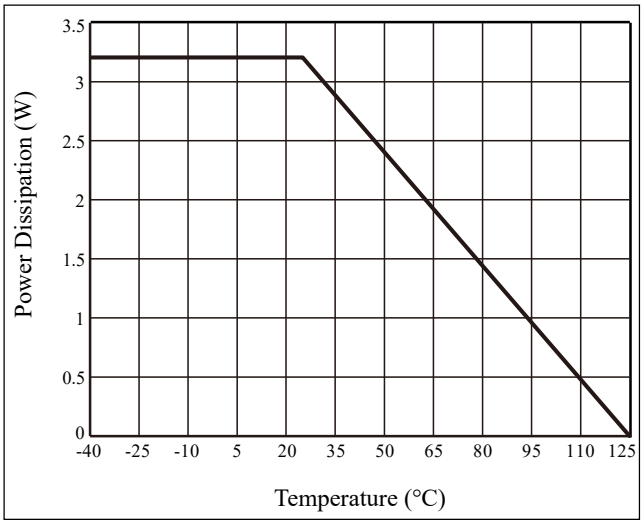



**Figure 20** Dissipation Curve

## CLASSIFICATION REFLOW PROFILES

| Profile Feature | Pb-Free Assembly |
|---|---|
| **Preheat & Soak**<br>Temperature min (Tsmin)<br>Temperature max (Tsmax)<br>Time (Tsmin to Tsmax) (ts) | 150°C<br>200°C<br>60-120 seconds |
| Average ramp-up rate (Tsmax to Tp) | 3°C/second max. |
| Liquidous temperature (TL)<br>Time at liquidous (tL) | 217°C<br>60-150 seconds |
| Peak package body temperature (Tp)* | Max 260°C |
| Time (tp)** within 5°C of the specified classification temperature (Tc) | Max 30 seconds |
| Average ramp-down rate (Tp to Tsmax) | 6°C/second max. |
| Time 25°C to peak temperature | 8 minutes max. |

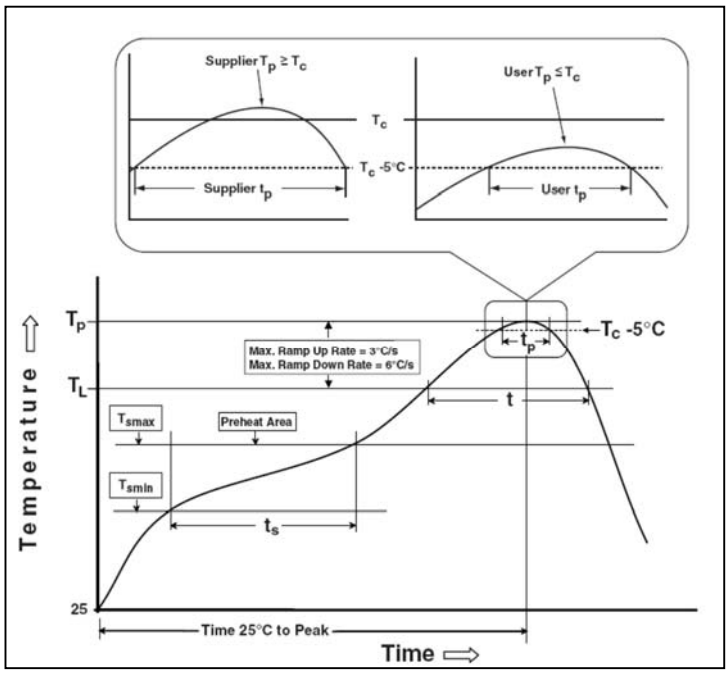
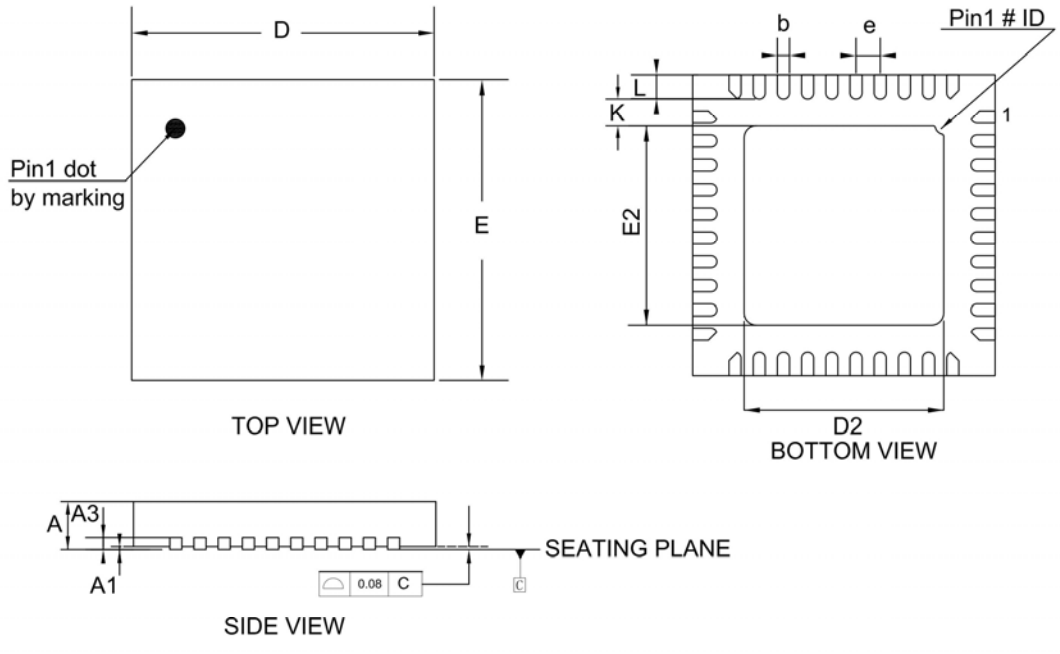



**Figure 21** Classification profile

## PACKAGE INFORMATION

### QFN-40




| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0 | 0.02 | 0.05 |
| A3 | 0.18 | 0.20 | 0.25 |
| K | 0.20 | - | - |
| b | 0.15 | 0.20 | 0.25 |
| D | 4.90 | 5.00 | 5.10 |
| E | 4.90 | 5.00 | 5.10 |
| D2 | 3.15 | - | 3.80 |
| E2 | 3.15 | - | 3.80 |
| L | 0.30 | 0.40 | 0.50 |
| e | 0.40BSC | | |

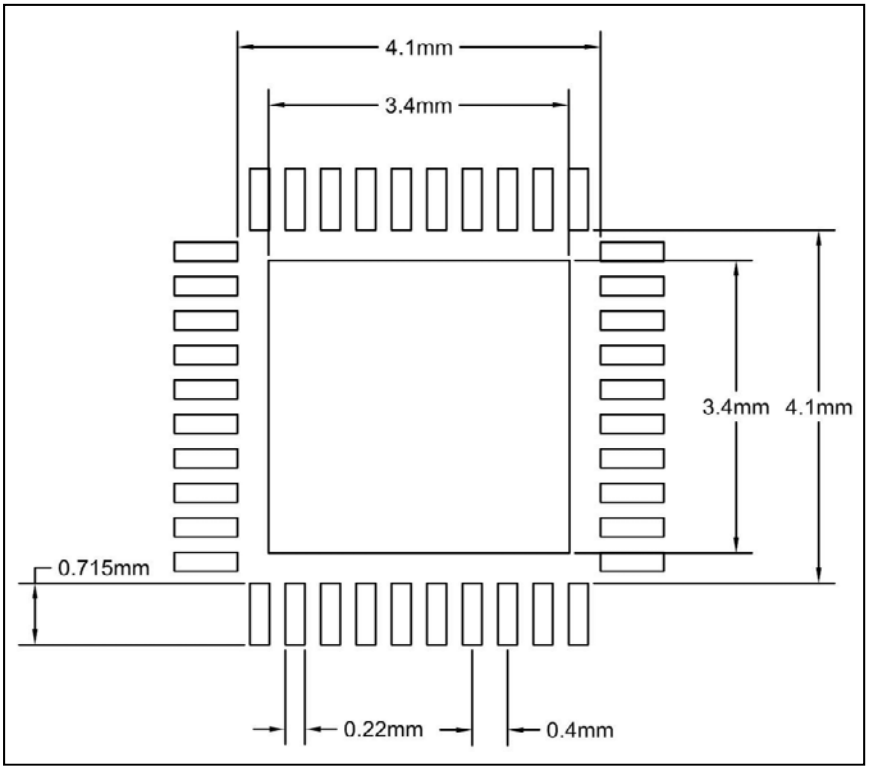
233-570-291 Rev.B

NOTE:

1. CONTROLLING DIMENSION : MM
2. REFERENCE DOCUMENT: JEDEC MO-220
3. THE PIN'S SHARP AND THERMAL PAD SHOWS DIFFERENT SHAPE AMONG DIFFERENT FACTORIES.

## RECOMMENDED LAND PATTERN

### QFN-40




**Note:**

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. User's board manufacturing specs), user must determine suitability for use.

**REVISION HISTORY**

| Revision | Detail Information | Date |
|---|---|---|
| A | Initial release | 2024.03.18 |