IS31FL3252

4-RGB/12-CH LED DRIVER

October 2024

GENERAL DESCRIPTION

The IS31FL3252 is a 12 LED current sinks LED driver programmed via 1MHz I2C compatible interface. Each LED can be dimmed individually with 16-bit PWM data and each color current sinks has 8-bit group DC scaling (Color Calibration) data which allowing 65536 steps of linear PWM dimming for each channel and 256 steps of DC current adjustable level for each color group. The output current of each channel can be set at up to 27.5mA (max.), all channels are grouped as G group (OUT1, OUT4, OUT7...), R group (OUT2, OUT5, OUT8...), B group (OUT3, OUT6, OUT9...) and each group has 8 bits output current control register which allows fine tuning the current for rich global RGB color mixing.)

Additionally each LED open and short state can be detected, IS31FL3252 stores the open or short information in Open Short Registers. The Open Short Registers allowing MCU to read out via I2C compatible interface. Inform MCU whether there are LEDs open or short and the locations of open or short LEDs.

The IS31FL3252 operates from 2.7V to 5.5V and features a very low shutdown and operational current.

IS31FL3252 is available in QFN-20 (3mm×3mm) package. It operates from 2.7V to 5.5V over the temperature range of -40°C to +125°C.

FEATURES

- Supply voltage range: 2.7V to 5.5V
- 12 current sinks
- Accurate color rendition
  - 8/10+4/12/16-bit PWM/channel
  - Three 8-bit global DC current adjust
- SDB rising edge reset I2C module
- 128kHz PWM frequency (8-bit PWM mode)
- 1MHz I2C-compatible interface
- Individual open and short error detect function
- 180-degree phase delay operation to reduce power noise
- Spread spectrum
- QFN-20 (3mm×3mm) package
- RoHS & Halogen-Free Compliance
- TSCA Compliance

APPLICATIONS

- Hand-held devices for LED display
- Gaming device (Mouse, Mouse MAT etc.)
- IOT device (AI speaker etc.)

TYPICAL APPLICATION CIRCUIT

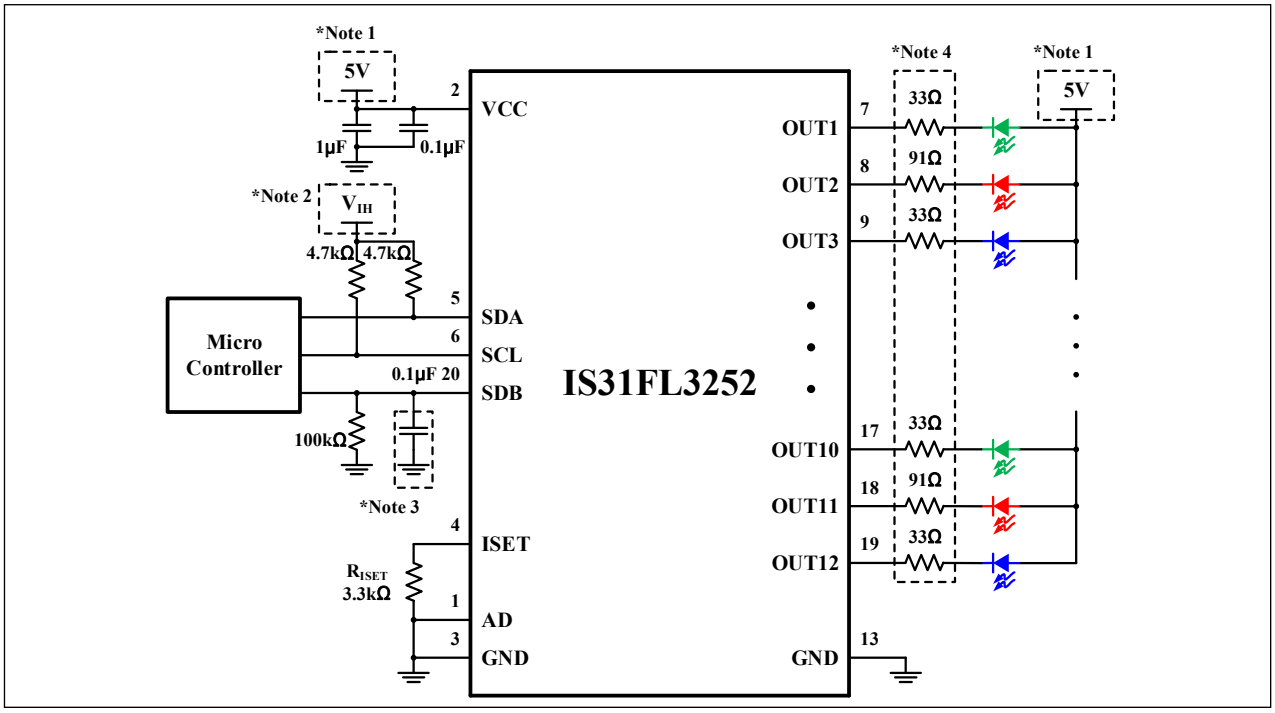


Figure 1 Typical Application Circuit: 4 RGBs

Note 1: VLED+ should be same as VCC voltage.

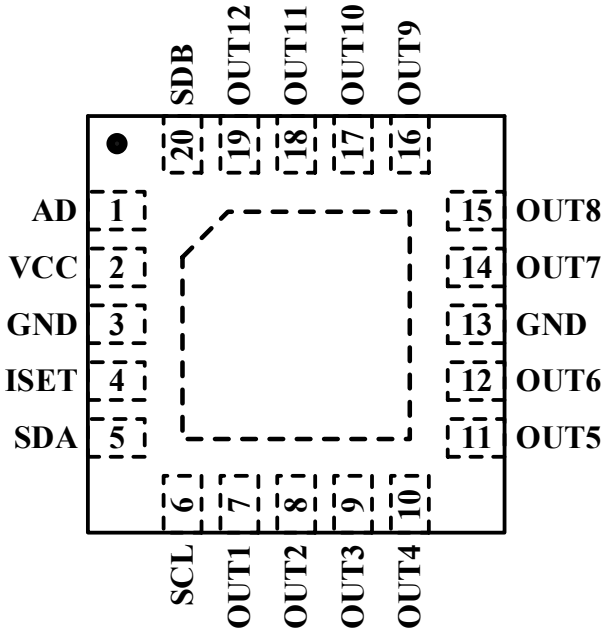
Note 2: V_{IH} is the high-level voltage for IS31FL3252, which is usually same as V_{CC} of Micro Controller, e.g. if V_{CC} of Micro Controller is 3.3V, V_{IH}= 3.3V. If V_{CC}= 5V and VIH is lower than 2.8V, recommend to add a level shift circuit for SDA and SCL.

Note 3: A 0.1μF capacitor is necessary for passing the EFT test.

Note 4: These optional resistors are for offloading the thermal dissipation (P= I^2R) away from the IS31FL3252 only (values are for V_{LED+}= 5V).

Note 5: The maximum output current is $I_{OUT(MAX)}$= 27.5mA when R_{ISET}= 3kΩ. Please refer RISET section of APPLICATION INFORMATION for setting LED current.

PIN CONFIGURATION

Package	Pin Configuration (Top View)
QFN-20	

PIN DESCRIPTION

No.	Pin	Description
1	AD	I2C address setting.
2	VCC	Power supply.
3, 13	GND	Ground.
4	ISET	Input terminal used to connect an external resistor. This regulates the global output current.
5	SDA	I2C serial data.
6	SCL	I2C serial clock.
7~12	OUT1 ~ OUT6	Output channel 1~6 for LEDs.
14~19	OUT7 ~ OUT12	Output channel 7~12 for LEDs.
20	SDB	Shutdown the chip when pulled low.
	Thermal Pad	Connect to GND.

ORDERING INFORMATION

Industrial Range: -40°C to +125°C

Order Part No.	Package	QTY/Reel
IS31FL3252-QFLS4-TR	QFN-20, Lead-free	2500

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	-0.3V ~+6.0V
Voltage at any input pin	-0.3V ~ V_{CC}+0.3V
Maximum junction temperature, T_{JMAX}	+150°C
Storage temperature range, T_{STG}	-65°C ~+150°C
Operating temperature range, T_A=T_J	-40°C ~ +125°C
Package thermal resistance, junction to ambient (4-layer standard test PCB based on JESD 51-2A), θ_{JA}	56.6°C/W
ESD (HBM) ESD (CDM)	±6kV ±750kV

Note 7: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

The following specifications apply for V_{CC}= 5V, T_A= 25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage		2.7		5.5	V
I_{CC}	Quiescent power supply current	V_{CC}= 5V, V_{SDB}= V_{CC}, all LEDs off, 8bit mode, SLM= 0, PFS= "010" (8MHz), R_{ISET}= 3.3kΩ		3.4	3.8	mA
		V_{CC}= 3.6V, V_{SDB}= V_{CC}, all LEDs off, 8bit mode, SLM=0, PFS= "010" (8MHz), R_{ISET}= 3.3kΩ		3.2	3.6	
		V_{CC}= 5V, V_{SDB}= V_{CC}, all LEDs off, 10+4bit mode, SLM=0, PFS= "010" (8MHz), R_{ISET}= 3.3kΩ		3.4	3.8	
		V_{CC}= 5V, V_{SDB}= V_{CC}, all LEDs off, 12bit mode, SLM=1, PFS= "010" (8MHz), R_{ISET}= 3.3kΩ		0.1	0.15	
I_{SD}	Shutdown current	V_{SDB}= 0V		0.5	1	μA
		V_{SDB}= V_{CC}, Configuration Register written "0000 0000"		0.5	1	
I_{OUT}	Maximum constant current of OUTx	GCC= 0xFF, V_{OUT}= 0.6V, R_{ISET}= 3kΩ (Note 7)		27.5		mA
	Constant current of OUTx	GCC= 0xFF, V_{OUT}= 0.6V, R_{ISET}= 3.3kΩ	23.25	25	26.75	mA
ΔI_{MAT}	Between channels	I_{OUT}= 25mA, V_{OUT}= 0.6V (Note 8)	-6		6	%
ΔI_{ACC}	Between device to device	I_{OUT}= 25mA, V_{OUT}= 0.6V (Note 9)	-4		4	%
V_{HR}	Current sink headroom voltage OUTx	I_{SINK}= 25mA		300	500	mV
f_{PWM}	PWM frequency	8bit mode, PFS= "010" (32kHz)	30	32	34	kHz
V_{OD}	OUTx pin open detect threshold	V_{CC}= 5V, GCC=0x0F, PWM= 0x0FFF, measured at OUTx	0.08	0.1		V
V_{SD}	LED short detect threshold	V_{CC}= 5V, GCC= 0x0F, PWM= 0x0FFF, measured at (V_{CC}-V_{OUTx})	0.8	1.0	1.2	V
T_{SD}	Thermal shutdown	(Note 10)		158		°C
T_{SD_HY}	Thermal shutdown hysteresis	(Note 10)		18		°C

ELECTRICAL CHARACTERISTICS (CONTINUED)

The following specifications apply for V_{CC}= 5V, T_A= 25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Logic Electrical Characteristics (SDA, SCL, SDB, AD)						
V_{IL}	Logic “0” input voltage	V_{CC}= 2.7V~5.5V	GND		0.4	V
V_{IH}	Logic “1” input voltage	V_{CC}= 2.7V~5.5V	1.4		V_{CC}	V
I_{IL}	Logic “0” input current	V_{INPUT}= 0V (Note 10)		5		nA
I_{IH}	Logic “1” input current	V_{INPUT}= V_{CC} (Note 10)		5		nA
V_{OL_SDA}	Low-level output voltage of SDA	I_{LOAD}= 5mA			0.4	V

DIGITAL INPUT I2C SWITCHING CHARACTERISTICS (NOTE 10)

Symbol	Parameter	Standard Mode		Fast Mode		Fast Mode Plus		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{SCL}	Serial-clock frequency	-	100	-	400	-	1000	kHz
t_{BUF}	Bus free time between a STOP and a START condition	4.7	-	1.3	-	0.5	-	µs
$t_{HD, STA}$	Hold time (repeated) START condition	4.0	-	0.6	-	0.26	-	µs
$t_{SU, STA}$	Repeated START condition setup time	4.7	-	0.6	-	0.26	-	µs
$t_{SU, STO}$	STOP condition setup time	4.0	-	0.6	-	0.26	-	µs
$t_{HD, DAT}$	Data hold time	5.0	-	-	-	-	-	µs
$t_{SU, DAT}$	Data setup time	250	-	100	-	50	-	ns
t_{LOW}	SCL clock low period	4.7	-	1.3	-	0.5	-	µs
t_{HIGH}	SCL clock high period	4.0	-	0.7	-	0.26	-	µs
t_R	Rise time of both SDA and SCL signals, receiving	-	1000	-	300	-	120	ns
t_F	Fall time of both SDA and SCL signals, receiving	-	300	-	300	-	120	ns

Note 7: The recommended minimum value of R_{ISET} is 3kΩ.

Note 8: I_{OUT} mismatch (bit to bit) $\triangle I_{MAT}$ is calculated:

$$\Delta I_{MAT} = \left(\frac{I_{OUTn}(n = 1 \sim 12)}{\left(\frac{I_{OUT1}+I_{OUT2}+I_{OUT3}+ \ldots\ldots+I_{OUT12}}{12} \right)} - 1 \right) \times 100\%$$

Note 9: I_{OUT} accuracy (device to device) $\triangle I_{ACC}$ is calculated:

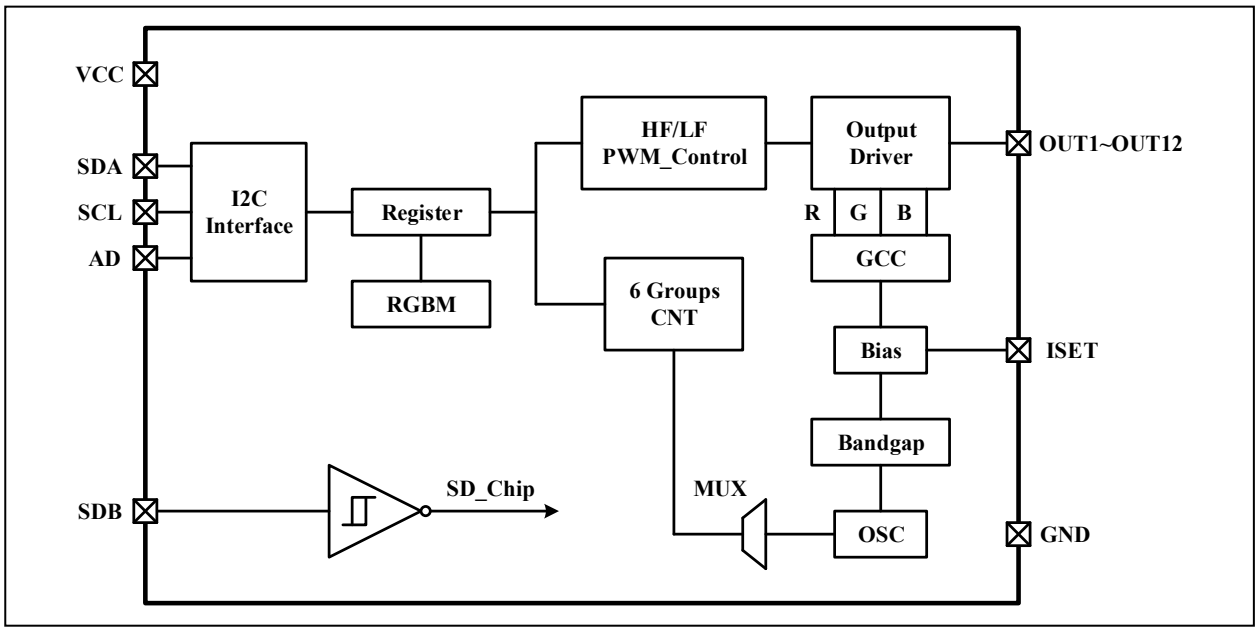
$$\Delta I_{ACC} = \left(\frac{\left(\frac{I_{OUT1}+I_{OUT2}+I_{OUT3}+ \ldots\ldots+I_{OUT12}}{12} - I_{OUT(IDEAL)} \right)}{I_{OUT(IDEAL)}} \right) \times 100\%$$

Where $I_{OUT(IDEAL)}$= 25mA when R_{ISET}= 3.3kΩ.

Note 10: Guaranteed by design.

Note 11: C_b = total capacitance of one bus line in pF. $I_{SINK} \leq$ 6mA. T_R and t_F measured between 0.3×V_{CC} and 0.7×V_{CC}.

FUNCTION BLOCK DIAGRAM



DETAILED DESCRIPTION

I2C INTERFACE

IS31FL3252 uses a serial bus, which conforms to the I2C protocol, to control the chip's functions with two wires: SCL and SDA. The IS31FL3252 has a 7-bit slave address (A7:A1), followed by the R/W bit, A0. Set A0 to "0" for a write command and set A0 to "1" for a read command. The value of bits A1 and A2 are decided by the connection of the AD pin.

Table 1 Slave Address

AD	A7:A3	A2:A1	A0
GND	01101	00	0/1
SCL		01	
SDA		10	
VCC		11	

AD connected to GND, A2:A1=00;

AD connected to VCC, A2:A1=11;

AD connected to SCL, A2:A1=01;

AD connected to SDA, A2:A1=10;

The SCL line is uni-directional. The SDA line is bi-directional (open-drain) with a pull-up resistor (typically 2kΩ). The maximum clock frequency specified by the I2C standard is 1MHz. In this discussion, the master is the microcontroller and the slave is the IS31FL3252.

The timing diagram for the I2C is shown in Figure 2. The SDA is latched in on the stable high level of the SCL. When there is no interface activity, the SDA line should be held high.

The "START" signal is generated by lowering the SDA signal while the SCL signal is high. The start signal will alert all devices attached to the I2C bus to check the incoming address against their own chip address.

The 8-bit chip address is sent next, most significant bit first. Each address bit must be stable while the SCL level is high.

After the last bit of the chip address is sent, the master checks for the IS31FL3252's acknowledge. The master releases the SDA line high (through a pull-up resistor). Then the master sends an SCL pulse. If the IS31FL3252 has received the address correctly, then it holds the SDA line low during the SCL pulse. If the SDA line is not low, then the master should send a "STOP" signal (discussed later) and abort the transfer.

Following acknowledge of IS31FL3252, the register address byte is sent, most significant bit first. IS31FL3252 must generate another acknowledge indicating that the register address has been received.

Then 8-bit of data byte are sent next, most significant bit first. Each data bit should be valid while the SCL level is stable high. After the data byte is sent, the IS31FL3252 must generate another acknowledge to indicate that the data was received.

The "STOP" signal ends the transfer. To signal "STOP", the SDA signal goes high while the SCL signal is high.

ADDRESS AUTO INCREMENT

To write multiple bytes of data into IS31FL3252, load the address of the data register that the first data byte is intended for. During the IS31FL3252 acknowledge of receiving the data byte, the internal address pointer will increment by one. The next data byte sent to IS31FL3252 will be placed in the new address, and so on. The auto increment of the address will continue as long as data continues to be written to IS31FL3252 (Figure 5).

READING OPERATION

Most of the registers can be read.

To read the register, after I2C start condition, the bus master must send the IS31FL3252 device address with the R/$\overline{W}$ bit set to "0", followed by the register address which determines which register is accessed. Then restart I2C, the bus master should send the IS31FL3252 device address with the R/$\overline{W}$ bit set to "1". Data from the register defined by the command byte is then sent from the IS31FL3252 to the master (Figure 6).

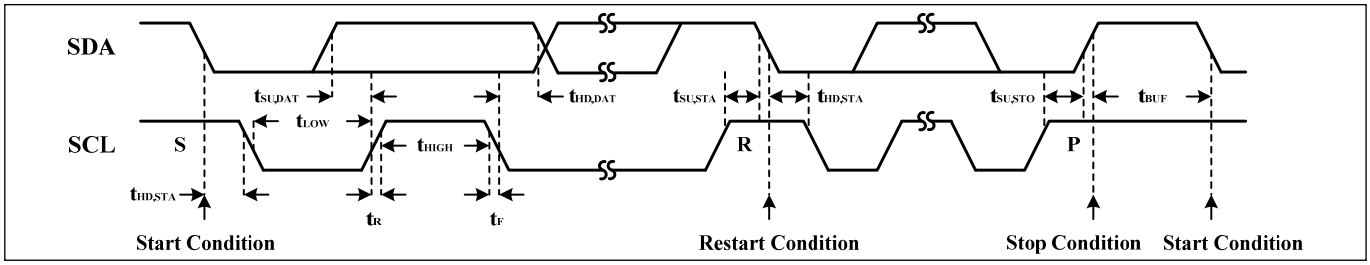


Figure 2 I2C Interface Timing

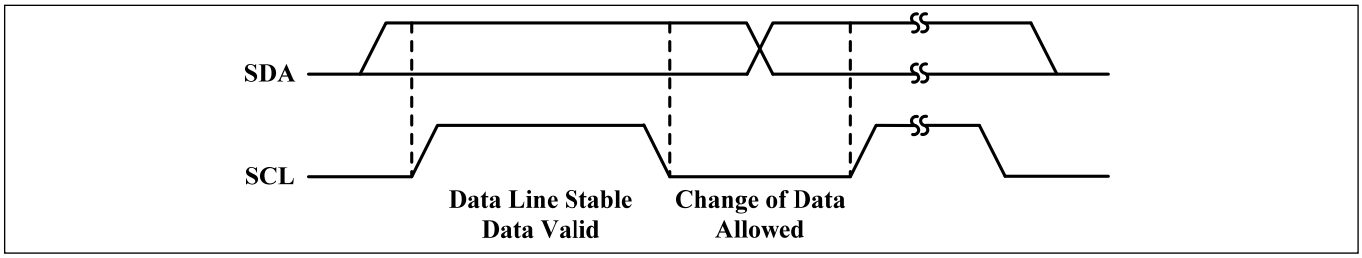


Figure 3 I2C Bit Transfer

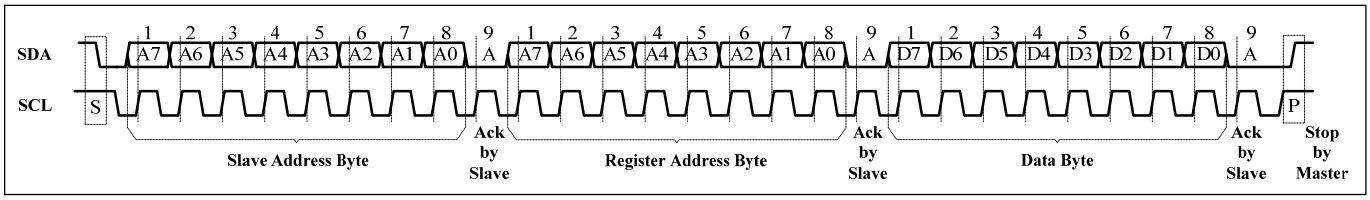


Figure 4 I2C Writing to IS31FL3252 (Typical)

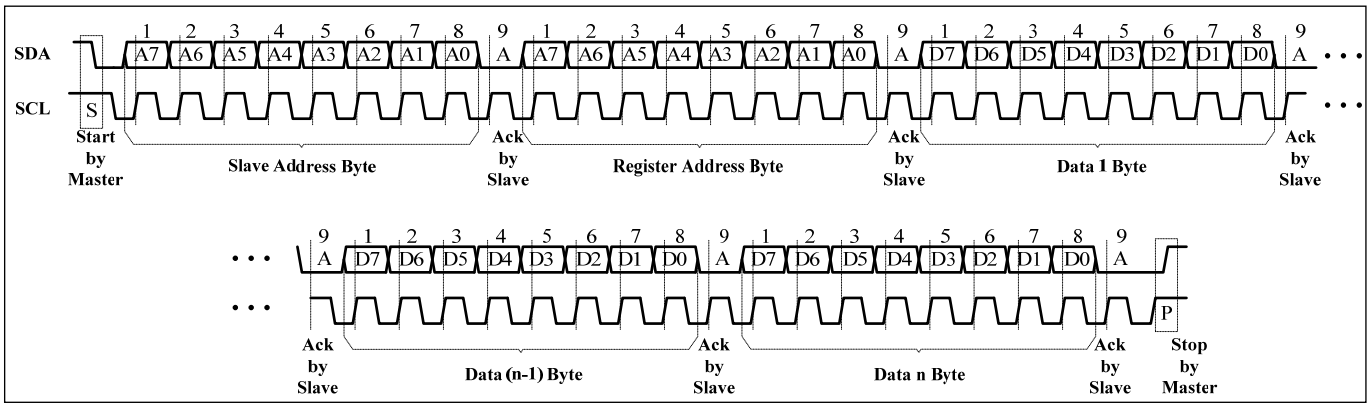


Figure 5 I2C Writing to IS31FL3252 (Automatic Address Increment)

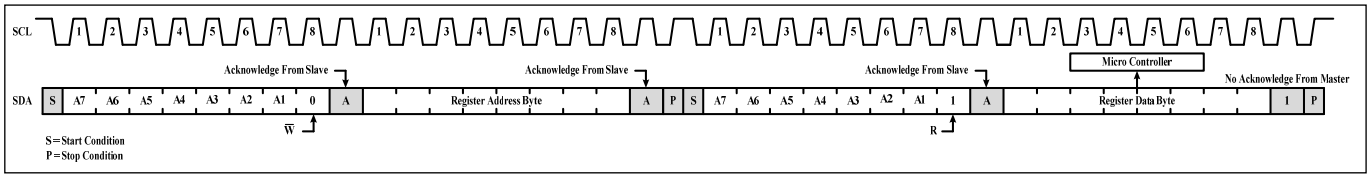


Figure 6 I2C Reading from IS31FL3252

Table 2 Register Definition

Address	Name	Function	Table	R/W	Default
00h	Configuration Register	Configure the operation mode	3	R/W	0000 0000
07h~1Eh	PWM Registers	PWM data of each dot	4	R/W	0000 0000
25h	PWM Update Register	Update the PWM Register data	-	R/W	0000 0000
26h	Global Current Control Register-G	Set the global current for R channels	5	R/W	0000 0000
27h	Global Current Control Register-R	Set the global current for R channels		R/W	0000 0000
28h	Global Current Control Register-B	Set the global current for R channels		R/W	0000 0000
29h	FPS and Open Short Enable Register	PWM frequency setting and Open Short Enable	6	R/W	0000 0000
2Ah~2Ch	DC mode Register	Set DC mode for each channel	7	R/W	0000 0000
2Dh	Spread Spectrum Register	Spread spectrum function enable	8	R/W	0000 0000
2Eh~30h	Open/short Register	Open/short information	9	R	0000 0000
3Fh	Reset Register	Reset all register to POR state	-	W	0000 0000

Table 3 00h Configuration Register

Bit	D7	D6	D5	D4	D3	D2:D1	D0
Name	-	PDE	SLM	OPC	-	PMS	SSD
Default	0	0	0	0	0	00	0

The Configuration Register sets operating mode of IS31FL3252.

When PDS is “1”, Phase Delay Enable, it makes OUT2x-1 less 180 degree than OUT2x (Where x = 1,2…9).

When SLM is “1”, Sleep Mode is Enable, IS31FL3252 enter Ultra-low operational current after all channels PWM off TIME>100ms.

When OPC is “1”, shutdown OP when PWM off, if OPC is “0”, will use OP when PWM off (when PWM off, shutdown OP will make the static current smaller).

When PMS is “00”, PWM Mode is 10+4-bit mode (default PWM mode), if PMS is “01”, PWM Mode is 8-bit mode and PMS is “10”, PWM Mode is 12-bit mode and PMS is “11”, PWM Mode is 16-bit mode. PMS default mode is 10+4-bit mode, when change the PWM mode, a writing of “0000 0000” to 25h is need to update the PMS bits (00h) value.

When SSD is “0”, IS31FL3252 works in software shutdown mode and to normal operate the SSD bit should set to “1”.

SSD Software Shutdown Control
0 Software shutdown
1 Normal operation

PMS PWM Mode Select
00 10+4bit mode (default)
01 8-bit mode
10 12-bit mode
11 16-bit mode

PMS default mode is 10+4-bit mode, when change the PWM mode, a writing of “0000 0000” to 25h is need to update the PMS bits (00h) value. After writing the 00h, delay one PWM cycle time (select by PFS bits in 29h) to write 25h.

OPC Shutdown Output Control
0 Do not shutdown channel output
1 Shutdown channel output when PWM off

SLM Sleep Mode enable
0 Sleep mode disable
1 Sleep mode enable

PDE Phase Delay Enable
0 All channels 0 degree phase delay
1 OUT1, OUT3, OUT5… OUT17 0 degree phase delay,
OUT2, OUT4, OUT6…OUT18 180 degree phase delay

Table 4 07h~1Eh PWM Register

Reg	08h (0Ah, 0Ch…)	07h (09h, 0Bh…)
Bit	D7:D0	D7:D0
Name	PWM_H	PWM_L
Default	0000 0000	0000 0000

Each output has10+4 bits (N=16384)/ 8 bits (N=256)/12 bits (N=4096)/ 16 bits (N=65536) to modulate the PWM duty in 16384/256/4096/65536 steps.

PWM_H PWM High Byte Duty Value (0x00~0xFF)

PWM_L PWM Low Byte Duty Value (0x00~0xFF)

I_{OUT} and the value of the PWM Registers decide the average current of each LED noted I_{LED}.
I_{OUT} is computed by Formula (1):

$$I_{OUTx} = I_{OUT\ (MAX)} \times \frac{GCCx}{256} \quad (1)$$

Where x = R, G or B, $I_{OUT(MAX)}$ is the maximum output current decided by R_{ISET} (Check R_{ISET} section for more information), GCCx if the GCCG (26h), GCCR (27h) and GCCB (28h), (26h is for G-group channels (OUT1, OUT4…OUT10). 27h is for R-group channels (OUT2, OUT5…OUT11). 28h is for B-group channels (OUT3, OUT6…OUT12)). Please refer to the detail information in Table 10.

$$GCCG\,(26h) = \sum_{n=0}^{7} D[n] \cdot 2^n \quad (2)$$

$$GCCR(27h) = \sum_{n=0}^{7} D[n] \cdot 2^n \quad (3)$$

$$GCCB(28h) = \sum_{n=0}^{7} D[n] \cdot 2^n \quad (4)$$

I_{LED} computed by Formula (5):

$$I_{LED} = \frac{PWM}{N} \times I_{OUT} \quad (5)$$

N=16384: $PWM = \sum_{n=0}^{13} D[n] \cdot 2^n$ (6)

N=256: $PWM = \sum_{n=0}^{7} D[n] \cdot 2^n$ (7)

N=4096: $PWM = \sum_{n=0}^{11} D[n] \cdot 2^n$ (8)

N=65536: $PWM = \sum_{n=0}^{15} D[n] \cdot 2^n$ (9)

Where PWM is the PWM Duty of each output (01h~24h), N=16384 (10+4-bit PWM resolution).
For example: R_{ISET}=3.3kΩ, GCCG=0xFF, GCCR=0x80, GCCB=0x40, PWM_H=0x3F, PWM_L=0xFF, $I_{OUT(MAX)}$= 23.18mA

$$I_{OUTG} = I_{OUT\ (MAX)} \times \frac{255}{256} = 23\,mA \quad (1)$$

$$I_{OUTR} = I_{OUT\ (MAX)} \times \frac{128}{256} = 11.5\,mA \quad (1)$$

$$I_{OUTB} = I_{OUT\ (MAX)} \times \frac{64}{256} = 5.76\,mA \quad (1)$$

$$PWM = \sum_{n=0}^{13} D[n] \cdot 2^n = 16383 \quad (6)$$

N= 16384

$$I_{LEDG} = \frac{16393}{16384} \times 23\,mA = 23\,mA$$

$$I_{LEDR} = \frac{16393}{16384} \times 11.5\,mA = 11.5\,mA$$

$$I_{LEDB} = \frac{16393}{16384} \times 5.76\,mA = 5.76\,mA \quad (5)$$

Where PWM is the PWM Duty of each output (01h~24h), N=4096 (12bit PWM resolution).
For example: R_{ISET}=3.3kΩ, GCCG=0xFF, GCCR=0x80, GCCB=0x40, PWM_H=0x0F, PWM_L=0xFF, $I_{OUT(MAX)}$= 23.18mA

$$I_{OUTG} = I_{OUT\ (MAX)} \times \frac{255}{256} = 23\,mA \quad (1)$$

$$I_{OUTR} = I_{OUT\ (MAX)} \times \frac{128}{256} = 11.5\,mA \quad (1)$$

$$I_{OUTB} = I_{OUT\ (MAX)} \times \frac{64}{256} = 5.76\,mA \quad (1)$$

$$PWM = \sum_{n=0}^{13} D[n] \cdot 2^n = 16383 \quad (6)$$

N= 4096

$$I_{LEDG} = \frac{4095}{4096} \times 23\,mA = 23\,mA$$

$$I_{LEDR} = \frac{4095}{4096} \times 11.5\,mA = 11.5\,mA$$

$$I_{LEDB} = \frac{4095}{4096} \times 5.76\,mA = 5.76\,mA \quad (5)$$

25h Update Register

When SDB= “H” and SSD= “1”, a writing of “0000 0000” to 25h is to update the PMS bits (00h) and PWM register (01h~24h) values, and it takes effect after one PWM cycle time. After writing the 00h (change the PWM mode), it is recommended to delay one PWM cycle time (select by PFS bits in 29h) before write 25h.

Table 5-1 26h Global Current Control Register-G

Bit	D7:D0
Name	GCCG
Default	0000 0000

Table 5-2 27h Global Current Control Register-R

Bit	D7:D0
Name	GCCR
Default	0000 0000

Table 5-3 28h Global Current Control Register-B

Bit	D7:D0
Name	GCCB
Default	0000 0000

The Global Current Control Register modulates all channels DC current which is noted as IOUT in 256 steps.

26h (GCCG) is for G-group channels (OUT1, OUT4…OUT10). 27h (GCCR) is for R-group channels (OUT2, OUT5…OUT11). 28h (GCCB) is for B-group channels (OUT3, OUT6…OUT12).
GCCx control the I_{OUT} as shown in Formula (1).

$$GCCx = \sum_{n=0}^{7} D[n] \cdot 2^n \qquad (2)$$

If GCCx=0xFF,

$$I_{OUTx} = I_{OUT\ (MAX)} \times \frac{255}{256}$$

If GCCx=0x01,

$$I_{OUTx} = I_{OUT\ (MAX)} \times \frac{1}{256}$$

Where x = R, G or B, $I_{OUT(MAX)}$ is the maximum output current decided by R_{ISET} (Check R_{ISET} section for more information).

Table 6 29h FPS/Open Short Enable Register

Bit	D7	D6:D4	D3:D2	D1:D0
Name	-	PFS	-	OSEN
Default	0	000	-	00

The internal oscillator clock frequency and the PWM resolution will decide the output PWM frequency.

When OSEN is “01” or “1x”, the Open short detect enable. If OSEN is “01”, Open detect enable and if OSEN is “10” or “11”, Short detect enable, and the result stored in 2Eh~30h, note either open or short information is saved not both.

The PFS is PWM frequency setting, it has five PWM frequency can setting, for example setting PFS = “000”, the PWM frequency is 128kHz for 8-bit mode, 32kHz for 8kHz for 10+4-bit mode,8kHz for 12-bit mode,500kHz for 16-bit mode.

OSEN Open short detect enable
00 Detect disable
01 Open detect enable
1x Short detect enable

PFS PWM frequency setting
000 128kHz for 8-bit mode, 32MHz OSC
32kHz for 10+4-bit mode, 32MHz OSC
8kHz for 12-bit mode, 32MHz OSC
500Hz for 16-bit mode, 32MHz OSC
001 64kHz for 8-bit mode, 16MHz OSC
16kHz for 10+4-bit mode, 16MHz OSC
4kHz for 12-bit mode, 16MHz OSC
250Hz for 16-bit mode, 16MHz OSC
010 32kHz for 8-bit mode, 8MHz OSC
8kHz for 10+4-bit mode, 8MHz OSC
2kHz for 12-bit mode, 8MHz OSC
125Hz for 16-bit mode, 8MHz OSC
011 16kHz for 8-bit mode, 4MHz OSC
4kHz for 10+4-bit mode, 4MHz OSC
1kHz for 12-bit mode, 4MHz OSC
60Hz for 16-bit mode, 4MHz OSC (LED will flicker)
100 8kHz for 8-bit mode, 2MHz OSC
2kHz for 10+4-bit mode, 2MHz OSC
500Hz for 12-bit mode, 2MHz OSC
30Hz for 16-bit mode, 2MHz OSC (LED will flicker)

Table 7-1 2Ah DC Mode Register 1 (OUT1~OUT6)

Bit	D7:D6	D5:D3	D2:D0
Name	-	DCM [OUT3:OUT1]	-
Default	00	00 0	000

Table 7-2 2Bh DC Mode Register 2 (OUT7~OUT12)

Bit	D7:D6	D5:D0
Name	-	DCM [OUT9:OUT4]
Default	00	00 0000

Table 7-3 2Ch DC Mode Register 3 (OUT13~OUT18)

Bit	D7:D3	D2:D0
Name	-	DCM [OUT12:OUT10]
Default	0000 0	000

The DC Mode Registers control the current mode of each channel. When DCMx is "0", OUTx work in DC mode, when DCMx is "1", OUTx work in PWM mode.

DCMx DC Mode Select
0 PWM Mode
1 DC Mode

Table 8 2Dh Spread Spectrum Register

Bit	D7:D6	D5	D4	D3:D2	D1:D0
Name	-	SSY	SSP	RNG	CLT
Default	00	0	0	00	00

When SSP enable, the spread spectrum function will be enabled and the RNG & CLT bits will adjust the range and cycle time of spread spectrum function. In some specific conditions, turning on the spread spectrum function will cause the LEDs to flicker. Spread spectrum synch function can eliminate flickering on the LED.

SSY Spread Spectrum Synch Enable
0 Disable
1 Enable

SSP Spread spectrum function enable
0 Disable
1 Enable

RNG Spread spectrum range
00 ±5%
01 ±15%
10 ±24%
11 ±34%

CLT Spread spectrum cycle time
00 500ms
01 125ms
10 1.4ms
11 0.35ms

Table 9-1 2Eh Open/Short Register (Read Only)

Bit	D7:D6	D5:D3	D2:D0
Name	-	OP/ST[3:1]	-
Default	00	00 0	000

Table 9-2 2Fh Open/Short Register (Read Only)

Bit	D7:D6	D5:D0
Name	-	OP/ST[9:4]
Default	00	00 0000

Table 9-3 30h Open/Short Register (Read Only)

Bit	D7:D3	D2:D0
Name	-	OP/ST[12:10]
Default	0000 0	000

When OSEN (29h) is set to "01", open detection will be trigger once, and the open information will be stored at 2Eh~30h.

When OSEN (29h) is set to "1x", short detection will be trigger once, and the short information will be stored at 2Eh~30h.

It should be noted that it will not store both open/short detect information at the same time, either it will store open or it will store short information. Open/short information can be read by the 2Eh~30h registers

To get the correct open/short information, several configurations are recommended to set before setting the OSEN bits (D1:D0 of 29h);

1. GCC ≥ 0x0F
2. PWM value ≥ 0x0FFF

OP[12:1] Open Information of OUT12:OUT1
0 Open not detected
1 Open detected

ST[12:1] Short Information of OUT12:OUT1
0 Short not detected
1 Short detected

3Fh Reset Register

Once user writes the Reset Register with 0xAE, IS31FL3252 will reset all the IS31FL3252 registers to their default value. On initial power-up, the IS31FL3252 registers are reset to their default values for a blank display

Table 10-1 PWM & GCCx Register Map-24 Channel Mode (18 CH-LED)

OUT	PWM_H	PWM_L	GCCx
1	08h	07h	26h
2	0Ah	09h	27h
3	0Ch	0Bh	28h
4	0Eh	0Dh	26h
5	10h	0Fh	27h
6	12h	11h	28h
7	14h	13h	26h
8	16h	15h	27h
9	18h	17h	28h
10	1Ah	19h	26h
11	1Ch	1Bh	27h
12	1Eh	1Dh	28h

Table 10-2 PWM & GCCx Register Map-24 Channel (6-RGB)

RGB Group	OUT	PWM_H	PWM_L	GCCx
RGB Group 1	4	08h	07h	26h
	5	0Ah	09h	27h
	6	0Ch	0Bh	28h
RGB Group 2	7	0Eh	0Dh	26h
	8	10h	0Fh	27h
	9	12h	11h	28h
RGB Group 3	10	14h	13h	26h
	11	16h	15h	27h
	12	18h	17h	28h
RGB Group 4	13	1Ah	19h	26h
	14	1Ch	1Bh	27h
	15	1Eh	1Dh	28h

APPLICATION INFORMATION

RISET

The maximum output current $I_{OUT(MAX)}$ of OUT1~OUT18 can be adjusted by the external resistor, R_{ISET}, as described in Formula (8).

$$I_{OUT\,(MAX\,)} = x \cdot \frac{V_{ISET}}{R_{ISET}} \qquad (8)$$

x= 85.05, V_{ISET}= 0.97V.

The recommended minimum value of R_{ISET} is 3kΩ.

When R_{ISET}= 3.3kΩ, $I_{OUT(MAX)}$= 25mA

When R_{ISET}= 3kΩ, $I_{OUT(MAX)}$= 27.5mA

R_{ISET} should be close to the chip and the ground side should well connect to the GND plane.

CURRENT SETTING

The maximum output current is set by the external resistor R_{ISET}. The Global Current Control register GCCX can be used to set a lower current than set by R_{ISET}.

The IS31FL3252 provides independent gradation control for each of the red, green and blue colors. The Global Current Control Register modulates all channels DC current which is noted as IOUT in 256 steps.

26h is for G-group channels. 27h is for R-group channels. 28h is for B-group channels.

SPREAD SPECTRUM

PWM current switching of LED outputs can be particularly troublesome when the EMI is concerned. To optimize the EMI performance, the IS31FL3252 includes a spread spectrum function. By setting the RNG bit of Spread Spectrum Register (2Dh), Spread Spectrum range can be chosen from ±5% /±15% /±24% /±34%. The spread spectrum function will lower the total electromagnetic emitting energy by spreading the energy into a wider range to significantly degrades the peak energy of EMI. With spread spectrum, the EMI test is easier to pass with a smaller size and lower cost filter circuit.

PWM FREQUENCY SELECT

The IS31FL3252 output channels operate with a default 10+4-bit PWM resolution mode and the PWM frequency at 32kHz (the oscillator frequency is 32MHz). Because all the OUTx channels are synchronized, the DC power supply will experience large instantaneous current surges when the OUTx channels turn ON.

These current surges will generate an AC ripple on the power supply which cause stress to the decoupling capacitors. When the AC ripple is applied to a monolithic ceramic capacitor chip (MLCC) it will expand and contract causing the PCB to flex and generate audible hum in the range of between 200Hz to 18kHz, to avoid this hum, there are many countermeasures, such as selecting the capacitor type and value which will not cause the PCB to flex and contract.

An additional option for avoiding audible hum is to set the IS31FL3252's output PWM frequency above/below the audible range. The FPS/Open Short Enable Register (29h) can be used to set the switching frequency to 2kHz~32kHz as shown in Table 6, the frequency PWM is higher than 20kHz, to reduce the audible hum.

PWM CONTROL

The PWM Registers (07h~1Eh) can modulate LED brightness of each channel. There are four PWM mode with 10+4-bit, 8-bit,12-bit and 16-bit can choose. For example, if there choose 12-bit mode and the data in PWM_H Register is "0000 0000" and in PWM_L Register is "0000 0100", then the PWM is 4/4096.

Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve a breathing effect.

PHASE DELAY

To reduce audible noise due to PWM switching, the IS31FL3252 features Phase Delay. When Phase Delay disable (default)all of the outputs turn on simultaneously causing large current draw from the ceramic capacitors and produces audible noise.

The PDE bit of register 00h will enable the Phase Delay function so at power-on the OUTx channel will not all turn on at the same time to minimize peak load current, resulting in reduced voltage ripple on the LED power supply rail. Phase Delay separates the 12 outputs as 2 groups, OUT1, OUT3... OUT11 as group 1, OUT2, OUTT4... OUT12 as group 2, when Phase Delay is enabled, group 2 will have 180-degree time delay than group 1.

OPEN AND SHORT DETECT

IS31FL3252 has open and short detect bit for each LED.

By the OSEN bits of FPS/Open Short Enable Register (29h) from "00" to "01" or "1x", the LED Open/short Register will start to store the open/short information and after at least 2 scanning cycles and the MCU can get the open/short information by reading the 2Eh~30h.

It should be noted that it will not store both open/short detect information at the same time, either it will store open or it will store short information. Open/short information can be read by the 2Eh~30h registers.

To get the correct open/short information, several configurations are recommended to set before setting the OSEN bits (D1:D0 of 29h);

1. GCC ≥ 0x0F
2. PWM value ≥ 0x0FFF

OPERATING MODE

IS31FL3252 can operate in PWM Mode or DC Mode. The brightness of each LED can be modulated with 65535 steps by PWM registers. In DC Mode, there is no PWM and I_{OUT}=$I_{OUT(MAX)}$ always.

Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve a breathing effect.

SHUTDOWN MODE

Shutdown mode can be used as a means of reducing power consumption. During shutdown mode all registers retain their data.

Software Shutdown

By setting the SSD bit of the Control Register (00h) to "0", the IS31FL3252 will operate in software shutdown mode. When the IS31FL3252 is in software shutdown, all current sources are switched off, so the LEDs are OFF but all registers accessible. Typical current consume is 0.5μA (V_{CC}=3.6V).

Hardware Shutdown

The chip enters hardware shutdown when the SDB pin is pulled low. All analog circuits are disabled during hardware shutdown, typical the current consumption is 0.5μA (V_{CC}=3.6V).

The chip releases hardware shutdown when the SDB pin is pulled high. The rising edge of SDB pin will reset the I2C module, but the register information is retained. During hardware shutdown the registers are accessible.

If the VCC supply drops below 1.75V but remains above 0.1V during SDB pulled low, please re-initialize all Function Registers before SDB pulled high.

LAYOUT

The IS31FL3252 consumes lots of power so good PCB layout will help improve the reliability of the chip. Please consider below factors when layout the PCB.

Power Supply Lines

When designing the PCB layout, the first PCB trace to consider is the power supply trace and GND connections, especially those traces with high current. Also the digital and analog blocks' supply line and GND should be separated to avoid noise from digital block affecting the analog block.

At least one 0.1μF capacitor, if possible with a 1μF capacitor is recommended to connected to the ground at power supply pin of the chip, and it needs to close to the chip and the ground net of the capacitor should be well connected to the GND plane.

Thermal Consideration

The over temperature of the chip may result in deterioration of the properties of the chip. The thermal pad of IS31FL3252 should connect to GND net and need to use 9 or 16 vias connect to GND copper area, the GND area should be as large area as possible to help radiate the heat from the IS31FL3252.

Current Rating Example

For a R_{ISET}=3.3kΩ application, the current rating for each net is as follows:

• VCC pin maximum current is lower than 10mA when V_{CC}=5V, but the VLED+ net is provide total current of all outputs, its current can as much as 25mA×12=300mA, recommend trace width for VCC pin: 0.20mm~0.3mm, recommend trace width for VLED+ net: 0.30mm~0.5mm

• Output pins=25mA, recommend trace width is 0.2mm~0.254mm

• All other pins<3mA, recommend trace width is 0.15mm~0.254mm

10+4-bit Function

When PMS of the Control Register (address 00h) is 00, 10+4-bit function is enabled. Then the final output PWM frequency is 10 bits, resolution is 14 bits. This is achieved through 10-bit PWM modulation and 4-bit dither control. For 4-bit dither, according to the 16 dither timing, each of the 16 PWM groups can add one PWM_H or PWM_L.

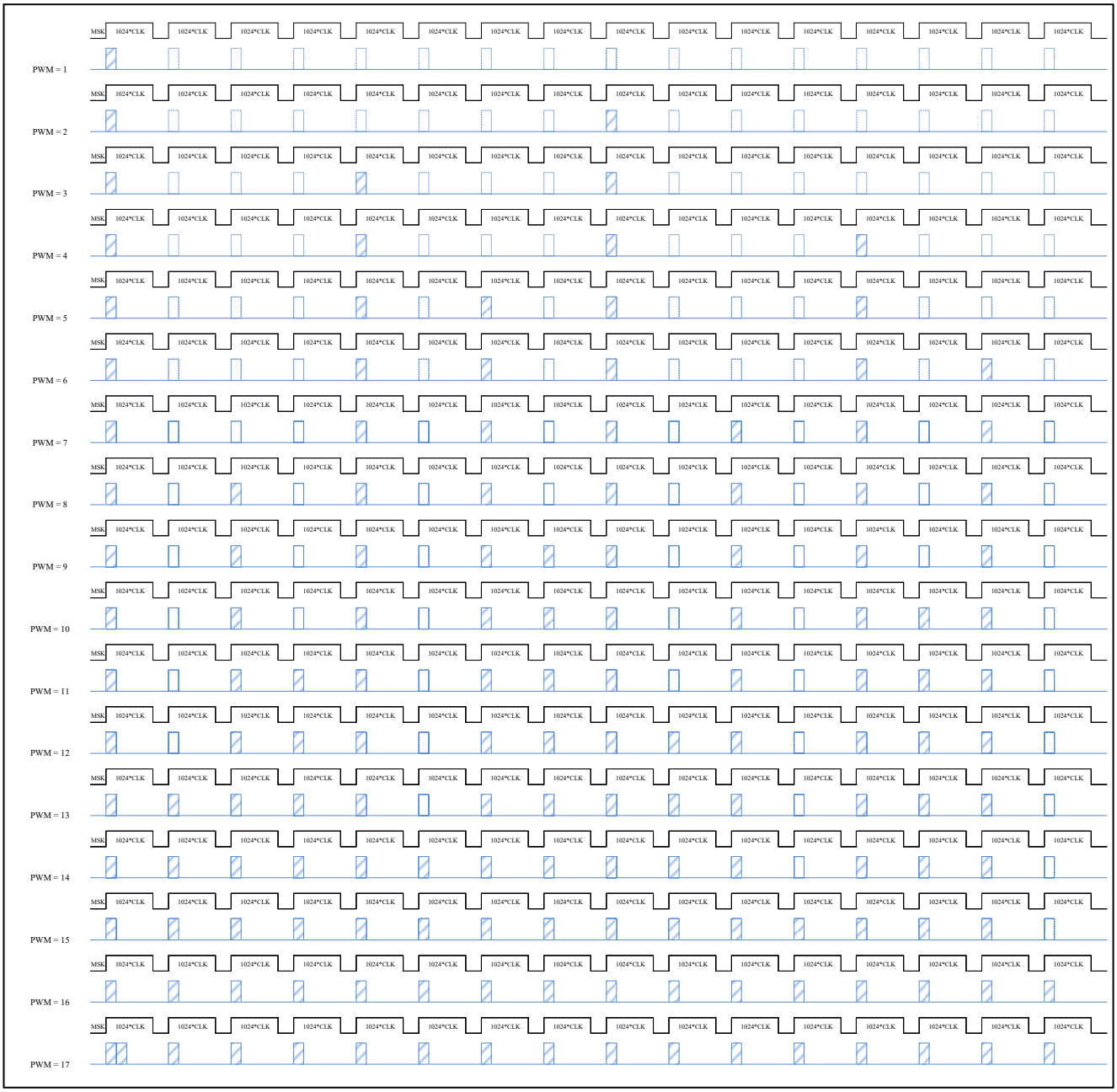


Figure 7 10+4-bit Mode Enable

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

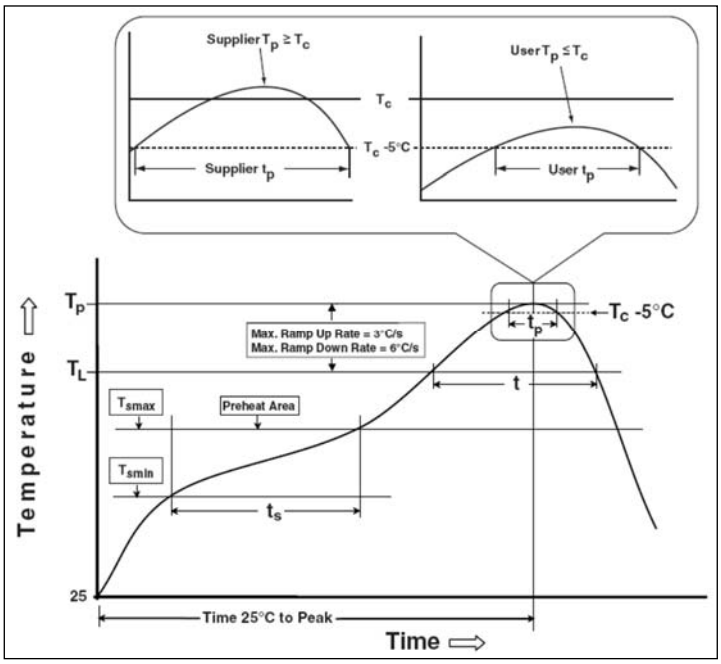
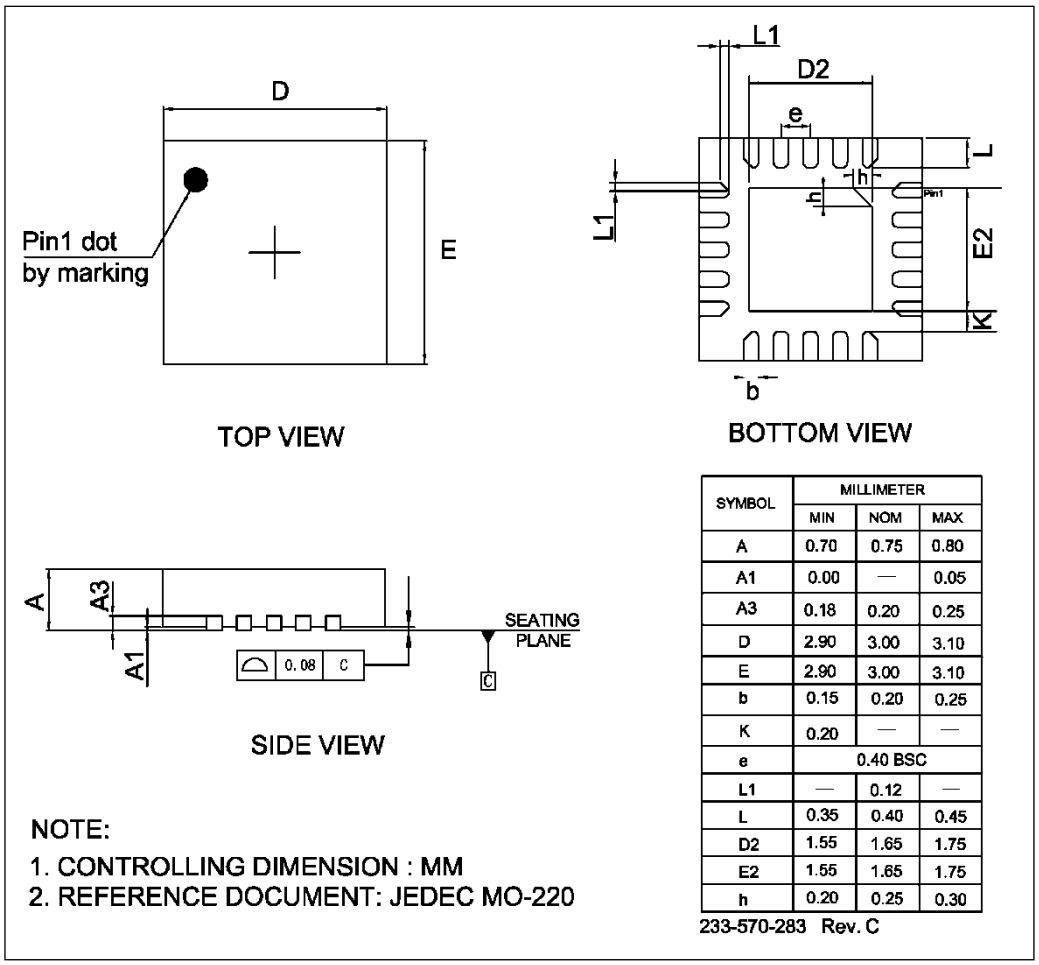


Figure 8 Classification Profile

PACKAGE INFORMATION

QFN-20



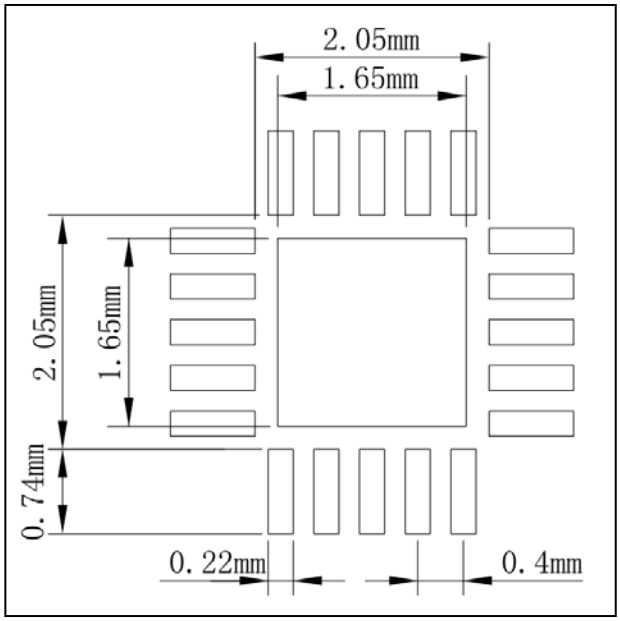
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	—	0.05
A3	0.18	0.20	0.25
D	2.90	3.00	3.10
E	2.90	3.00	3.10
b	0.15	0.20	0.25
K	0.20	—	—
e	0.40 BSC		
L1	—	0.12	—
L	0.35	0.40	0.45
D2	1.55	1.65	1.75
E2	1.55	1.65	1.75
h	0.20	0.25	0.30

NOTE:
1. CONTROLLING DIMENSION : MM
2. REFERENCE DOCUMENT: JEDEC MO-220

233-570-283 Rev. C

RECOMMENDED LAND PATTERN

QFN-20



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. User's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
A	Initial release	2023.09.06
B	1. Update the condition for VHR value 2. Update to new Lumissil logo	2024.10.10