IS31AP2010B

3W@5.0V MONO FILTER-LESS CLASS-D AUDIO POWER AMPLIFIER

March 2024

GENERAL DESCRIPTION

The IS31AP2010B is a high efficiency, 3W@5.0V mono filter-less Class-D audio power amplifier. A low noise, filter-less PWM architecture eliminates the output filter, reduces external component count, system cost, and simplifying design.

Operating in a single 5.0V supply, IS31AP2010B is capable of driving 4Ω speaker load at a continuous average output of 3W@10% THD+N. The IS31AP2010B has high efficiency with speaker load compared to a typical Class-AB amplifier.

In cellular handsets, the earpiece, speaker phone, and melody ringer speaker can each be driven by the IS31AP2010B. The gain of IS31AP2010B is externally configurable which allows independent gain control from multiple sources by summing signals from each function.

IS31AP2010B is available in UTQFN-9 package. It operates from 2.7V to 5.5V over the temperature range of -40°C to +85°C.

FEATURES

- 5.0V supply at THD+N= 10%
  - 3W into 4Ω (Typ.)
  - 1.68W into 8Ω (Typ.)
- Efficiency at 5.0V
  - 85% at 400mW with a 4Ω speaker
  - 88% at 400mW with an 8Ω speaker
- Less than 1μA shutdown current
- Optimized PWM output stage eliminates LC output filter
- Fully differential design reduces RF rectification and eliminates bypass capacitor
- Improved CMRR eliminates two input coupling capacitors
- Integrated click-and-pop suppression circuitry
- UTQFN-9 package
- RoHS & Halogen-Free Compliance
- TSCA Compliance

APPLICATIONS

- Wireless or cellular handsets and PDAs
- Portable DVD player
- Notebook PC
- Portable radio
- Educational toys
- Portable gaming

TYPICAL APPLICATION CIRCUIT

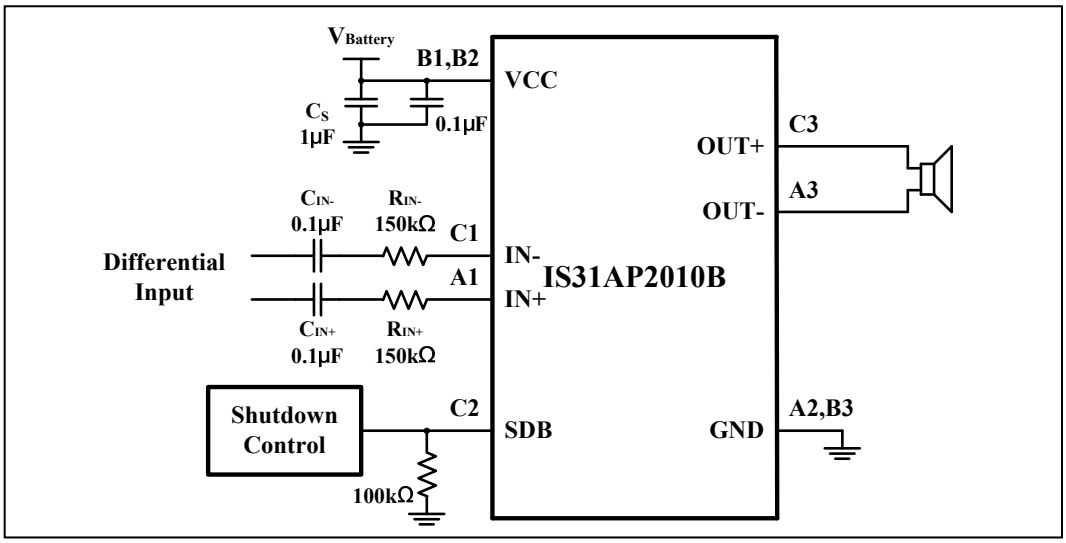
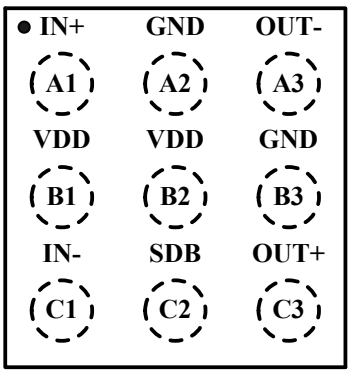


Figure 1 Typical Application Circuit

PIN CONFIGURATION

Package	Pin Configuration (Top View)
UTQFN-9	

PIN DESCRIPTION

No.	Pin	Description
A1	IN+	Positive audio input.
A2, B3	GND	Connect to ground.
A3	OUT-	Negative audio output.
B1, B2	VCC	Power supply.
C1	IN-	Negative audio input.
C2	SDB	Enter in shutdown mode when active low.
C3	OUT+	Positive audio output.

ORDERING INFORMATION

Industrial Range: -40°C to +85°C

Order Part No.	Package	QTY/Reel
IS31AP2010B-UTLS2-TR	UTQFN-9, Lead-free	3000

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	-0.3V ~ +6.0V
Voltage at any input pin	-0.3V ~ V_{CC}+0.3V
Junction temperature, T_{JMAX}	+150°C
Storage temperature range, T_{STG}	-65°C ~ +150°C
Operating temperature range, T_A	-40°C ~ +85°C

Note 1: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

V_{CC} = 2.7V ~ 5.5V, T_A = 25°C, unless otherwise noted. (Note 2)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage		2.7		5.5	V
$\|V_{OS}\|$	Output offset voltage (measured differentially)	V_{SDB} = 0V, A_V = 2V/V		10		mV
I_{DD}	Quiescent current	V_{CC} = 5.5V, no load		2.6		mA
		V_{CC} = 2.7V, no load		1.2		
I_{SDB}	Shutdown current	V_{SDB} = 0.4V			1	μA
f_{sw}	Switching frequency			250		kHz
R_{IN}	Input resistor	Gain ≤ 20V/V	15			kΩ
Gain		R_{IN} = 150kΩ		2		V/V
V_{IH}	High-level input voltage		1.4			V
V_{IL}	Low-level input voltage				0.4	V

ELECTRICAL CHARACTERISTICS

T_A = 25°C, Gain = 2V/V, C_{IN} = 2µF, unless otherwise noted. (Note 3)

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
P_O	Output power	THD+N = 10% f = 1kHz, R_L = 8Ω	V_{CC} = 5.0V		1.68		W
			V_{CC} = 4.2V		1.2		
			V_{CC} = 3.6V		0.88		
		THD+N = 10% f = 1kHz, R_L = 4Ω	V_{CC} = 5.0V		3.0		W
			V_{CC} = 4.2V		2.0		
			V_{CC} = 3.6V		1.5		
		THD+N = 1% f = 1kHz, R_L = 8Ω	V_{CC} = 5.0V		1.4		W
			V_{CC} = 4.2V		1.0		
			V_{CC} = 3.6V		0.7		
		THD+N = 1% f = 1kHz, R_L = 4Ω	V_{CC} = 5.0V		2.4		W
			V_{CC} = 4.2V		1.68		
			V_{CC} = 3.6V		1.2		
THD+N	Total harmonic distortion plus noise	V_{CC} = 4.2V, P_O = 0.6W, R_L = 8Ω, f = 1kHz			0.18		%
		V_{CC} = 4.2V, P_O = 1.1W, R_L = 4Ω, f = 1kHz			0.22		
V_{NO}	Output voltage noise	V_{CC} = 4.2V, f = 20Hz to 20kHz Inputs AC-grounded			80		µVrms
T_{WU}	Wake-up time from shutdown	V_{CC} = 3.6V			32		ms
SNR	Signal-to-noise ratio	P_O = 1.0W, R_L = 8Ω, V_{CC} = 4.2V			91		dB
PSRR	Power supply rejection ratio	f = 217Hz， R_L = 8Ω Input grounded	V_{CC} = 5.0V		-75		dB
			V_{CC} = 4.2V		-70		
			V_{CC} = 3.6V		-66		

Note 2: All parts are production tested at T_A = 25°C. Other temperature limits are guaranteed by design.

Note 3: Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTIC

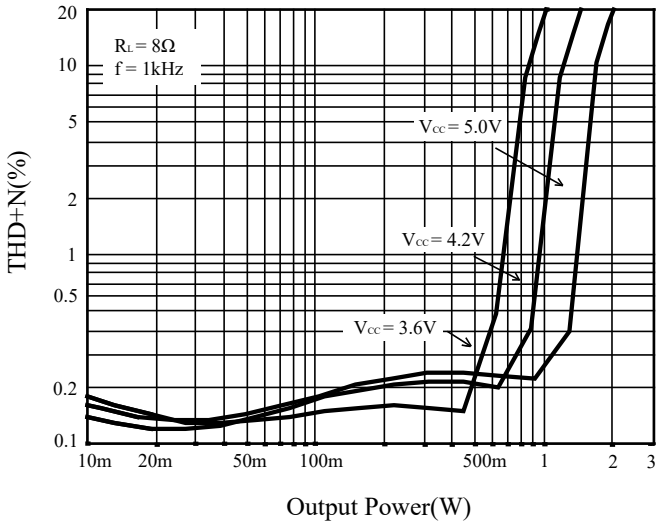


Figure 2 THD+N vs. Output Power

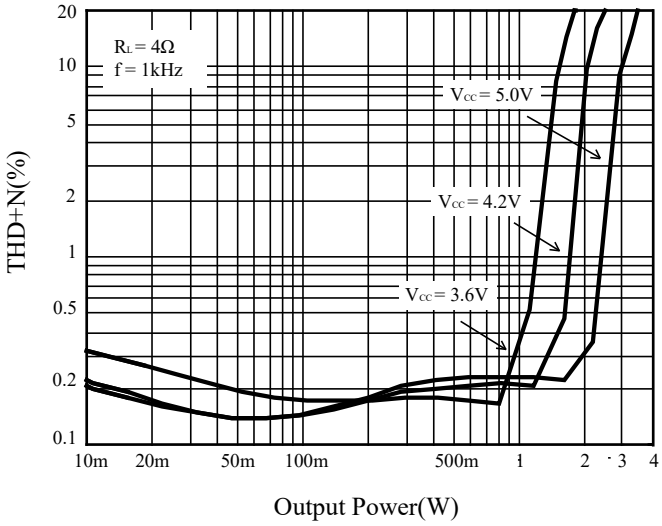


Figure 3 THD+N vs. Output Power

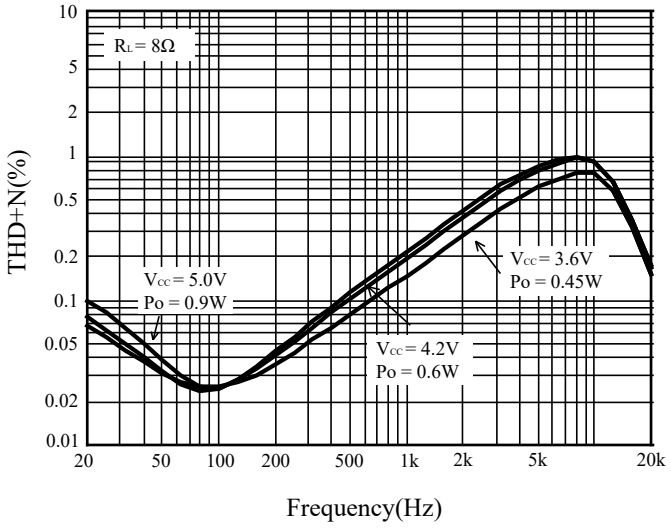


Figure 4 THD+N vs. Frequency

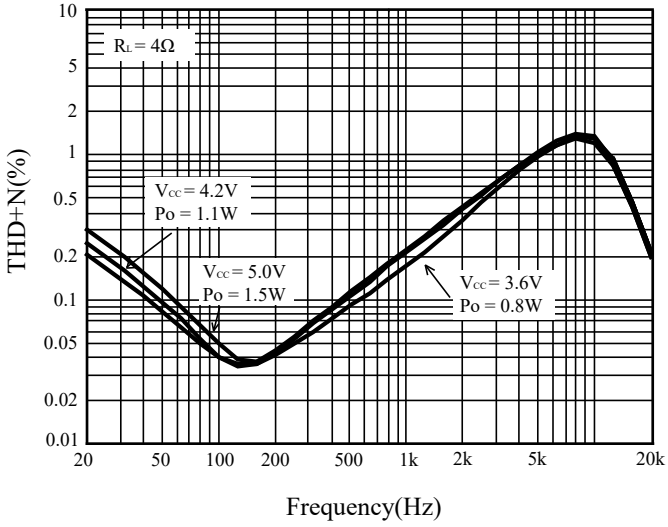


Figure 5 THD+N vs. Frequency

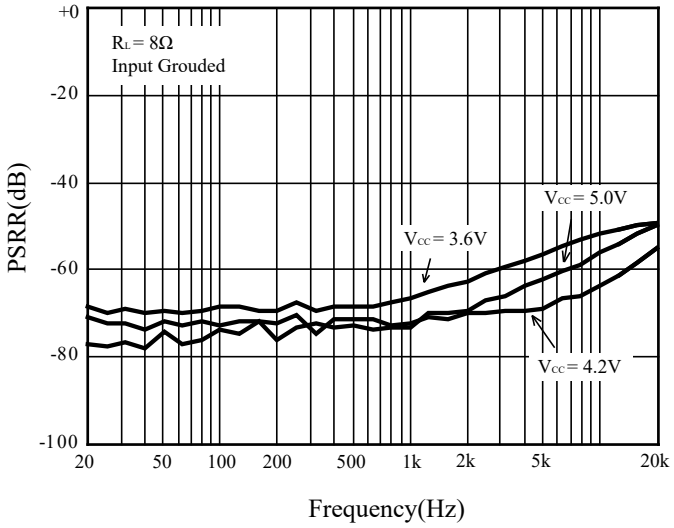


Figure 6 PSRR vs. Frequency

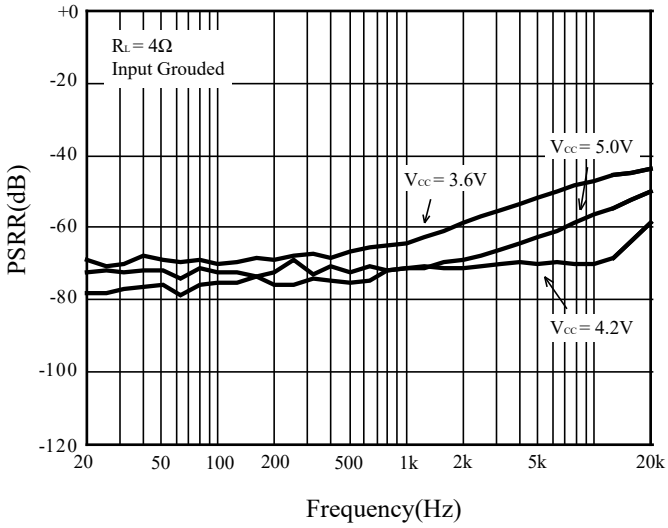


Figure 7 PSRR vs. Frequency

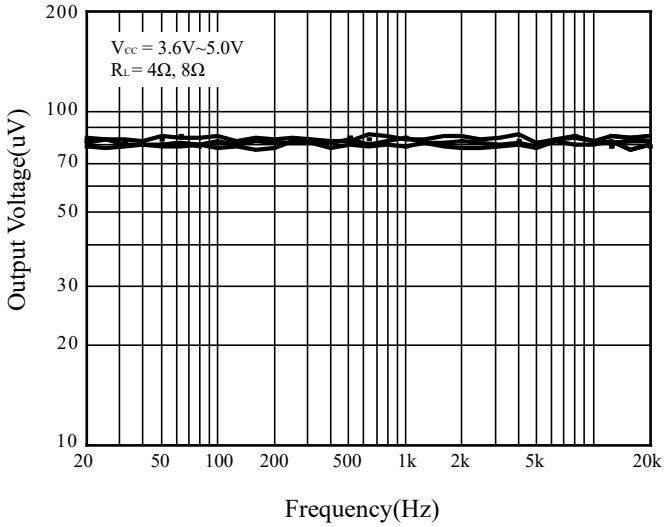


Figure 8 Noise

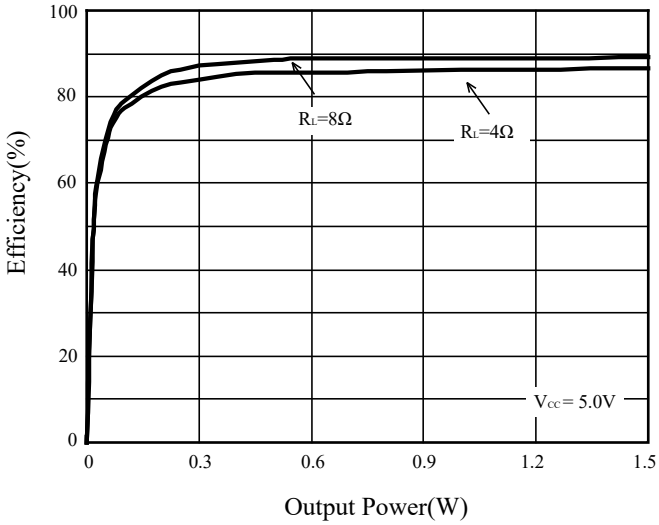
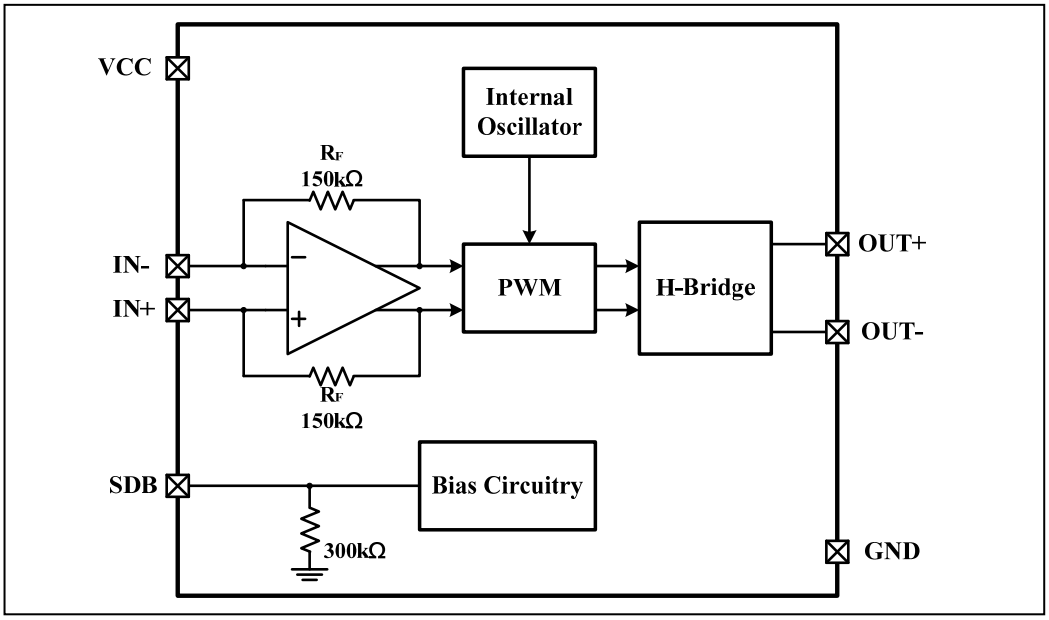


Figure 9 Efficiency

FUNCTIONAL BLOCK DIAGRAM



APPLICATION INFORMATION

FULLY DIFFERENTIAL AMPLIFIER

The IS31AP2010B is a fully differential amplifier with differential inputs and outputs. The fully differential amplifier consists of a differential amplifier and a common mode amplifier. The differential amplifier ensures that the amplifier outputs a differential voltage on the output that is equal to the differential input times the gain. The common-mode feedback ensures that the common-mode voltage at the output is biased around $V_{CC}/2$ regardless of the common-mode voltage at the input. The fully differential IS31AP2010B can still be used with a single-ended input; however, the IS31AP2010B should be used with differential inputs when in a noisy environment, like a wireless handset, to ensure maximum noise rejection.

ADVANTAGES OF FULLY DIFFERENTIAL AMPLIFIERS

The fully differential amplifier does not require a bypass capacitor. This is because any shift in the mid-supply affects both positive and negative channels equally and cancels at the differential output.

GSM handsets save power by turning on and shutting off the RF transmitter at a rate of 217Hz. The transmitted signal is picked-up on input and output traces. The fully differential amplifier cancels the signal much better than the typical audio amplifier.

COMPONENT SELECTION

Figure 10 shows the IS31AP2010B with differential inputs and input capacitors, and Figure 11 shows the IS31AP2010B with single-ended inputs. Differential inputs should be used whenever possible because the single-ended inputs are much more susceptible to noise.

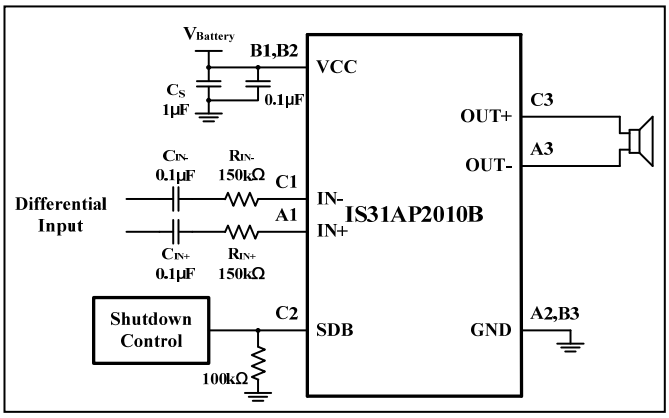


Figure 10 Differential Input

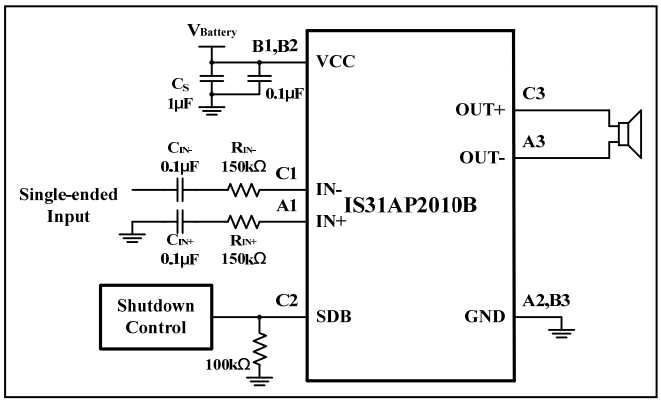


Figure 11 Single-Ended Input

INPUT RESISTORS (R_{IN})

The input resistors (R_{IN}) set the gain of the amplifier according to Equation (1).

$$Gain = \frac{2 \times R_F}{R_{IN}} \left(\frac{V}{V} \right) \qquad (1)$$

Resistor matching is very important in fully differential amplifiers. The balance of the output on the reference voltage depends on matched ratios of the resistors. CMRR, PSRR, and cancellation of the second harmonic distortion diminish if resistor mismatch occurs. Therefore, it is recommended to use 1% tolerance resistors or better to keep the performance optimized. Matching is more important than overall tolerance. Resistor arrays with 1% matching can be used with a tolerance greater than 1%.

Place the input resistors very close to the IS31AP2010B to limit noise injection on the high-impedance nodes.

For optimal performance the gain should be set to 2V/V or lower. Lower gain allows the IS31AP2010B to operate at its best, and keeps a high voltage at the input making the inputs less susceptible to noise.

DECOUPLING CAPACITOR (C_S)

The IS31AP2010B is a high performance Class-D audio amplifier that requires adequate power supply decoupling to ensure the efficiency is high and total harmonic distortion (THD) is low. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1μF, placed as close as possible to the device VCC lead works best. Placing this decoupling capacitor close to the IS31AP2010B is very important for the efficiency of the Class-D amplifier, because any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency. For filtering lower frequency noise signals, a 10μF or greater capacitor placed near the audio power amplifier would also help, but it is not required in most applications because of the high PSRR of this device.

INPUT CAPACITORS (C_{IN})

The input capacitors and input resistors form a high pass filter with the corner frequency, f_C, determined in Equation (2).

$$f_c = \frac{1}{2\pi R_{IN} C_{IN}} \qquad (2)$$

The value of the input capacitor is important to consider as it directly affects the bass (low frequency) performance of the circuit. Speakers in wireless phones cannot usually respond well to low frequencies, so the corner frequency can be set to block low frequencies in this application.

Equation (3) is reconfigured to solve for the input coupling capacitance.

$$C_{IN} = \frac{1}{2\pi R_{IN} f_c} \qquad (3)$$

If the corner frequency is within the audio band, the capacitors should have a tolerance of ±10% or better, because any mismatch in capacitance causes an impedance mismatch at the corner frequency and below.

For a flat low frequency response, use large input coupling capacitors (1μF). However, in a GSM phone the ground signal is fluctuating at 217Hz, but the signal from the codec does not have the same 217Hz fluctuation. The difference between the two signals is amplified, sent to the speaker, and heard as a 217Hz hum.

SUMMING INPUT SIGNALS

Most wireless phones or PDAs need to sum signals at the audio power amplifier or just have two signal sources that need separate gain. The IS31AP2010B makes it easy to sum signals or use separate signal sources with different gains. Many phones now use the same speaker for the earpiece and ringer, where the wireless phone would require a much lower gain for the phone earpiece than for the ringer. PDAs and phones that have stereo headphones require summing of the right and left channels to output the stereo signal to the mono speaker.

SUMMING TWO DIFFERENTIAL INPUT SIGNALS

Two extra resistors are needed for summing differential signals (a total of 5 components). The gain for each input source can be set independently (see Equations (4) and (5) and Figure 12).

$$Gain1 = \frac{V_O}{V_{I1}} = \frac{2\times 150k\Omega}{R_{IN1}} \left(\frac{V}{V}\right) \qquad (4)$$

$$Gain2 = \frac{V_O}{V_{I2}} = \frac{2\times 150k\Omega}{R_{IN2}} \left(\frac{V}{V}\right) \qquad (5)$$

If summing left and right inputs with a gain of 1V/V, use $R_{IN1} = R_{IN2} = 300k\Omega$.

If summing a ring tone and a phone signal, set the ring-tone gain to Gain1 = 2V/V, and the phone gain to Gain2 = 0.1V/V. The resistor values would be

$R_{IN1} = 150k\Omega$, $R_{IN2} = 3M\Omega$

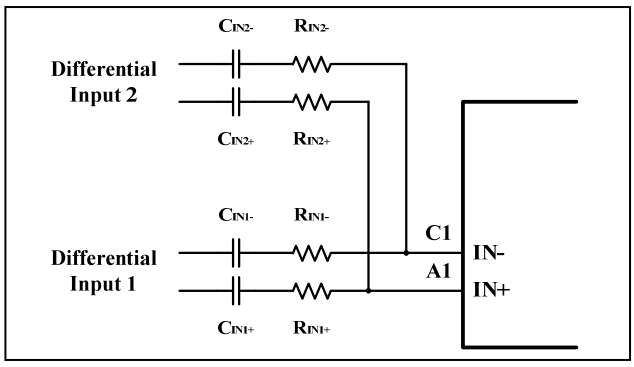


Figure 12 Summing Two Differential Inputs

SUMMING A DIFFERENTIAL INPUT SIGNAL AND A SINGLE-ENDED INPUT SIGNAL

Figure 13 shows how to sum a differential input signal and a single-ended input signal. Ground noise may couple in through IN- with this method. It is better to use differential inputs. The corner frequency of the single-ended input is set by C_{IN2}, shown in Equation (8). To assure that each input is balanced, the single-ended input must be driven by a low-impedance source even if the input is not in use.

$$C_{IN2} = \frac{1}{2\pi R_{IN2} f_{c2}} \qquad (6)$$

To assure that each input is balanced, the single-ended input must be driven by a low-impedance source even if the input is not in use. If summing a ring tone and a phone signal, the phone signal should use a differential input signal while the ring tone might be limited to a single-ended signal. Phone gain is set at Gain1 = 2V/V, and the ring-tone gain is set to Gain2 = 0.1V/V, the resistor values would be R_{IN1} =150kΩ, R_{IN2} =3MΩ.
The high pass corner frequency of the single-ended input is set by C_{IN2}. If the desired corner frequency is less than 20Hz.

So, $C_{IN2} > \frac{1}{2\pi 150k\Omega \times 20Hz}$

and $C_{IN2} > 53\,pF$

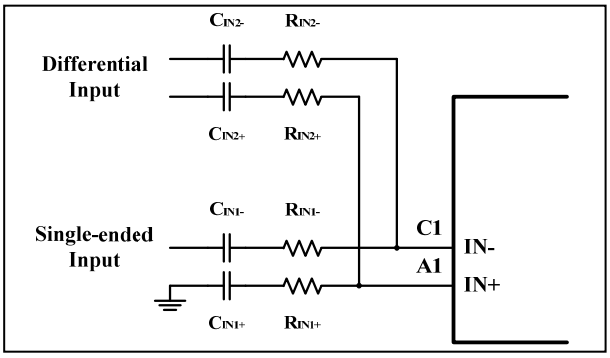


Figure 13 Summing Differential Input and Single-Ended Input Signals

SUMMING TWO SINGLE-ENDED INPUT SIGNALS

The gain and corner frequencies (f_{C1} and f_{C2}) for each input source can be set independently by Equations (4) and (5). Resistor, R_P, and capacitor, C_P, are needed on the IN+ terminal to match the impedance on the IN- terminal. The single-ended inputs must be driven by low impedance sources even if one of the inputs is not outputting an ac signal.

$$C_{IN1} = \frac{1}{2\pi R_{IN1} f_{c1}} \quad (7)$$

$$C_{IN2} = \frac{1}{2\pi R_{IN2} f_{c2}} \quad (8)$$

$$C_p = C_{IN1} + C_{IN2} \quad (9)$$

$$R_P = \frac{R_{IN1} \times R_{IN2}}{(R_{IN1} + R_{IN2})} \quad (10)$$

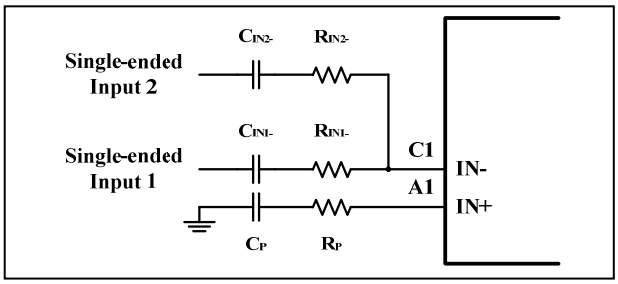


Figure 14 Summing Two Single-Ended Inputs

EMI EVALUATION RESULT

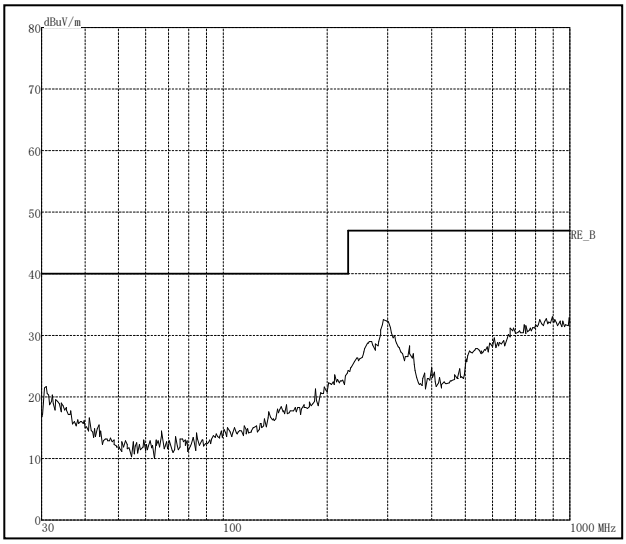


Figure 15 EMI Evaluation Result

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

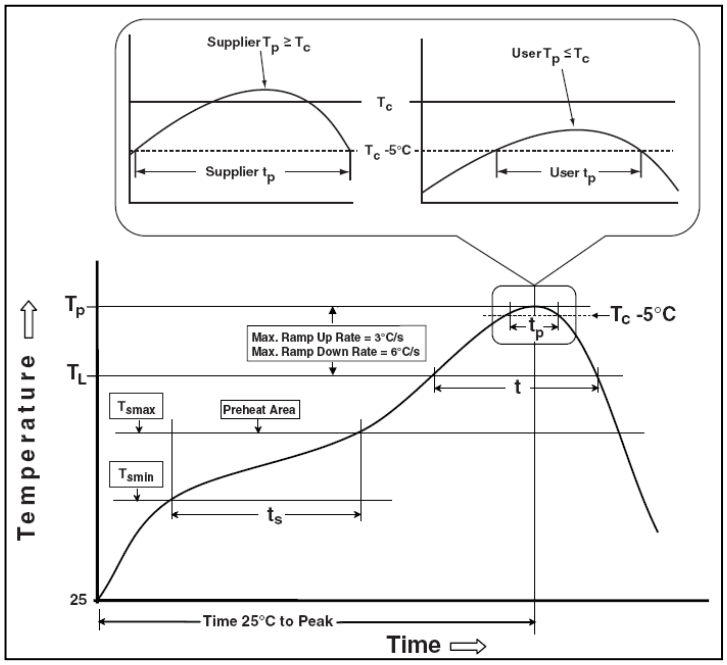
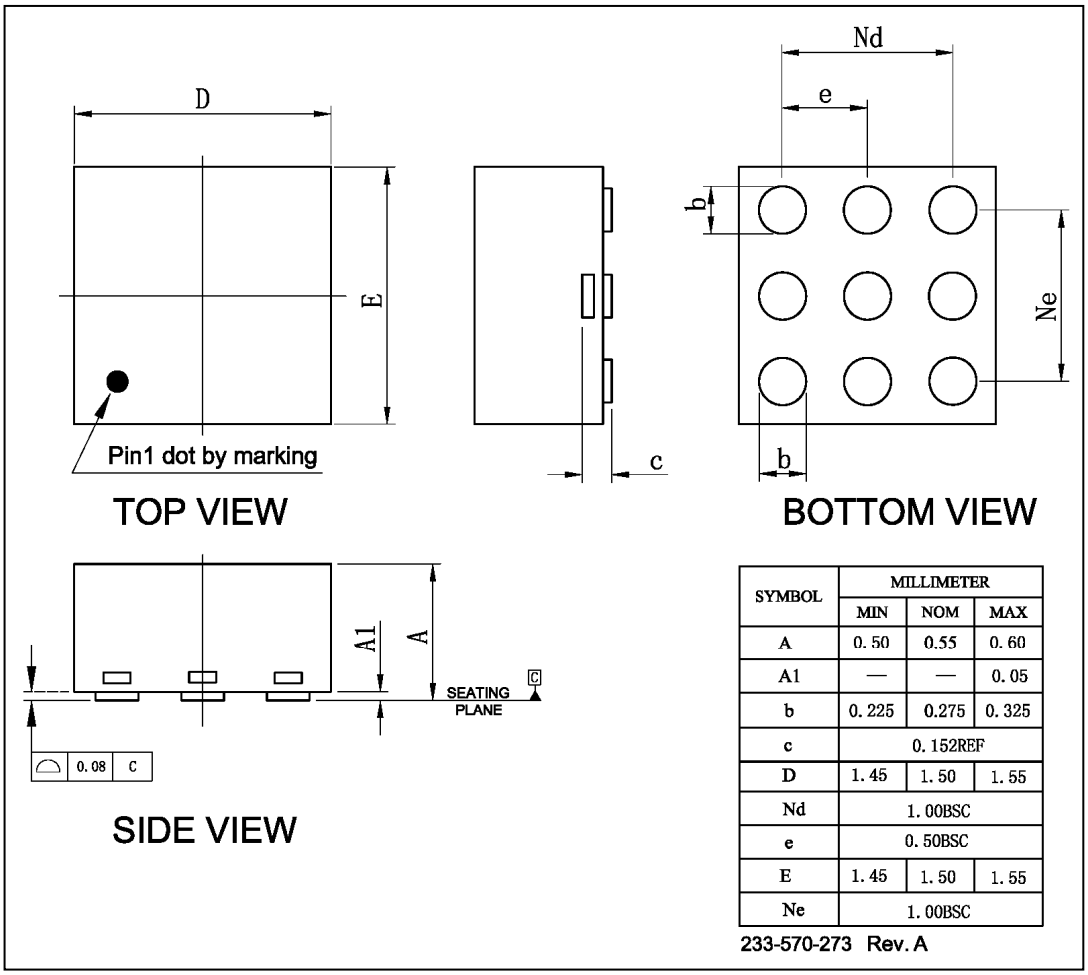


Figure 16 Classification Profile

PACKAGING INFORMATION

UTQFN-9

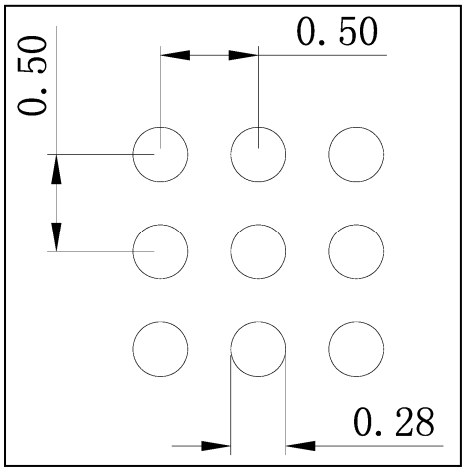


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	—	—	0.05
b	0.225	0.275	0.325
c	0.152REF		
D	1.45	1.50	1.55
Nd	1.00BSC		
e	0.50BSC		
E	1.45	1.50	1.55
Ne	1.00BSC		

233-570-273 Rev. A

RECOMMENDED LAND PATTERN

UTQFN-9



Note:
1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. user's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
A	Initial release	2011.08.03
B	Update UTQFN-9 POD	2013.04.10
C	1. Update new Lumissil logo 2. Update POD and add LP	2024.03.07